

# Rockchip Linux USB Developer Guide

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## Preface

## Overview

The purpose of this manual is to show you the hardware circuits of USB, how to configure the USB in Kernel, and help you to develop and debug the driver of USB PHYs and Controllers quickly.

## Product version

Chipset name	Kernel version
RK3399Pro、RK3399、RK3368、RK3366、RK3328、RK3288、RK3228、RK312X、RK3188、RK30XX、RK3308、RK3326、RK1808、RK1108、PX30	Linux-4.4、Linux-4.19

## Intended Audience

This document (this guide) is mainly intended for:

Technical support engineers Software development engineers Hardware development engineers

## Revision history

Date	Version	Author	Revision description
2017-12-22	v1.0	william.wu, frank.wang	The initial version
2018-06-08	v1.1	william.wu	Support RK3308、RK3326、PX30 Correct formats and errors
2019-03-11	v1.2	william.wu	Fix style issues by markdownlint
2019-11-12	v1.2.1	william.wu	Modify document name, support Linux-4.19
2020-02-19	v1.2.2	william.wu	Add DISCLAIMER, Trademark Statement, etc.
2020-05-13	v1.4.0	jianing.ren	Correct the content of most chapters to improve readability Add new chapters "5.1 Linux USB Driver Framework" and "7 USB Common Debug Methods And Commands" Add analysis of common problems

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# 1 Overview

## 1.1 RK USB Controllers Solution

Rockchip SoC usually has several USB controllers built in, and different controllers are independent of each other. Please get detailed information in the chip TRM. Because some USB controllers have limitations on usage, it is important to clarify the requirements of the scheme and the limitations of the controller before determining the design scheme of USB. The built-in USB controllers of each chip are shown in Table 1-1.

Table 1 - 1 USB Controllers List

Chip	USB 2.0 HOST (EHCI&OHCI)	USB HSIC (EHCI)	USB 2.0/3.0 OTG (DWC3/xHCI)	USB 2.0 OTG (DWC2)
RK3399Pro	2	1	2	0
RK3399	2	1	2	0
RK3368	1	1	0	1
RK3366	1	0	1	1
RK3328	1	0	1	1
RK3288	0	1	0	2 (HOST+OTG)
RK3228	3	0	0	1
RK312X	1	0	0	1
RK3188	1	1	0	1
RK30XX	1	0	0	1
RK3308	1	0	0	1
RK3326	0	0	0	1
RK1808	1	0	1	0
RK1108	1	0	0	1
PX30	1	0	0	1

### Note:

1. In the table, the number N indicates that it supports N independent USB controllers.
2. In the table, "EHCI/OHCI" indicates that the USB controller integrates the EHCI controller and OHCI controller. "DWC3/xHCI" indicates that the USB controller integrates the DWC3 controller and xHCI controller.
3. RK3288 supports two independent DWC2 controllers. One DWC2 supports OTG function and the other DWC2 only supports Host function.

## 1.2 USB 2.0 Host

### Compatible Specification

- Universal Serial Bus Specification, Revision 2.0
- Enhanced Host Controller Interface Specification(EHCI), Revision 1.0
- Open Host Controller Interface Specification(OHCI), Revision 1.0a

### Features

- Support high-speed(480Mbps), full-speed(12Mbps) and low-speed(1.5Mbps). The block diagram of the USB 2.0 Host controller is shown in Figure 1-1.

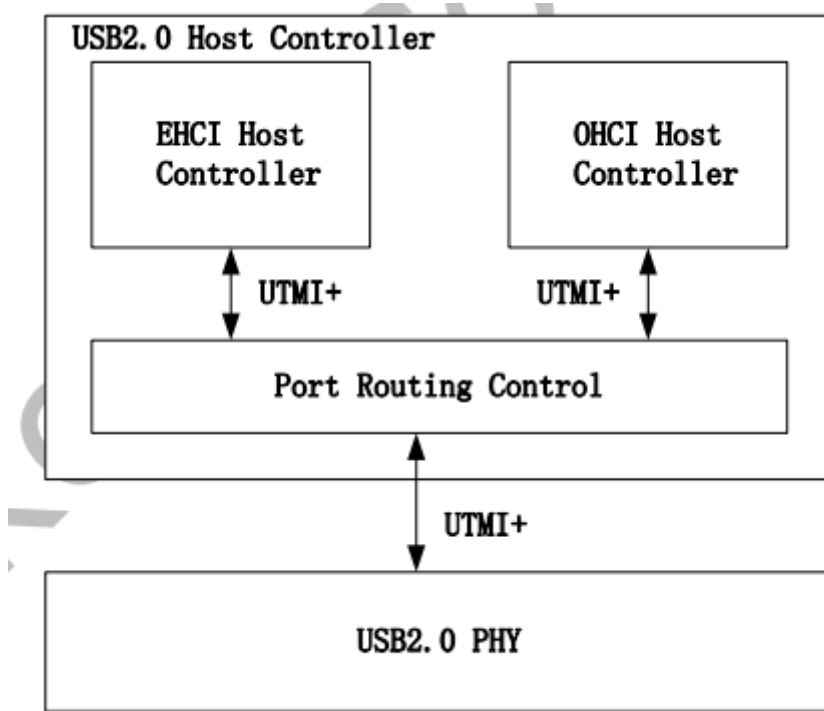


Figure 1-1 USB 2.0 Host Controller Block Diagram

## 1.3 USB 2.0 OTG

### Compatible Specification

- Universal Serial Bus Specification, Revision 2.0

### Features

- Supports Host mode and Device mode
- Support OTG ID detection, and automatically switch between Host mode and Device mode by ID status
- Does not support ADP/SRP/HNP protocols
- Supports high speed, full speed, and low speed in Host mode, and only supports high speed and full speed in Device mode
- Support 9 channels in host mode
- 9 Device mode endpoints in addition to control endpoint 0, 4 in, 3 out and 2 IN/OUT
- Built-in one 1024x35 bits FIFO
- Internal DMA with scatter/gather function
- Supports packet-based, dynamic FIFO memory allocation for endpoints for flexible, efficient use of RAM
- Support dynamic FIFO sizing
- Support Battery Charge in device role
- Support Uart Bypass Mode

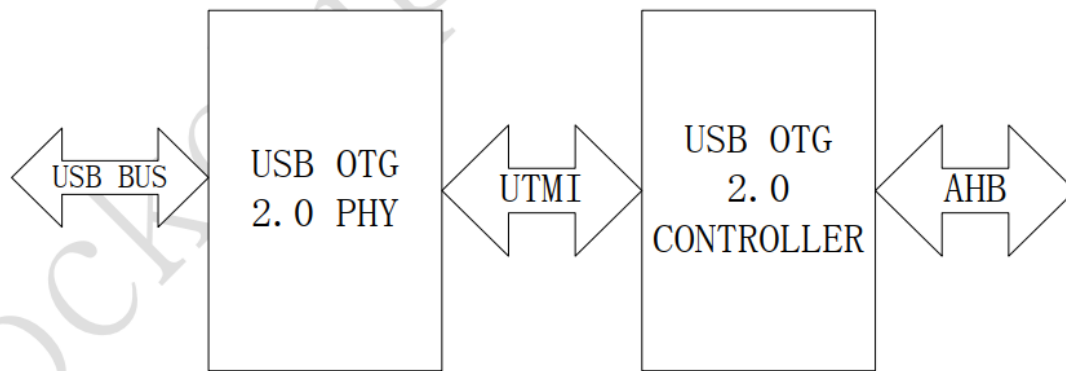


Figure 1 - 2 USB 2.0 OTG Block Diagram

## 1.4 USB 3.0 OTG

### Compatible Specification

- Universal Serial Bus 3.0 Specification, Revision 1.0
- Universal Serial Bus Specification, Revision 2.0
- eXtensible Host Controller Interface for Universal Serial Bus(xHCI), Revision 1.1

### DWC3 Features

- Support Control/Bulk(including stream)/Interrupt/Isochronous Transfer
- Simultaneous IN and OUT transfer for USB 3.0, up to 8Gbps bandwidth
- Descriptor Caching and Data Pre-fetching
- USB 3.0 Device Features
- Up to 7 IN endpoints, including control endpoint 0
- Up to 6 OUT endpoints, including control endpoint 0
- Up to 13 endpoint transfer resources, each one for each endpoint
- Flexible endpoint configuration for multiple applications/USBset-configuration modes
- Hardware handles ERDY and burst
- Stream-based bulk endpoints with controller automatically initiating data movement
- Isochronous endpoints with isochronous data in data buffers
- Flexible Descriptor with rich set of features to support buffer interrupt moderation, multiple transfers, isochronous, control, and scattered buffering support
- USB 3.0 Dual-Role Device(DRD) Features
- Static Device operation
- Static Host operation
- USB 3.0/USB 2.0 OTG A device and B device basing on ID
- UFP/DFP and Data Role Swap Defined in USB TypeC Specification
- Not support USB 3.0/USB 2.0 OTG session request protocol(SRP), host negotiation protocol(HNP) and Role Swap Protocol(RSP)

### USB 3.0 xHCI Host Features

- Support up to 64 devices
- Support 1 interrupter
- Support 1 USB 2.0 port and 1 Super-Speed port
- Concurrent USB 3.0/USB 2.0 traffic, up to 8.48Gbps bandwidth
- Support standard or open-source xHCI and class driver
- Support xHCI Debug Capability

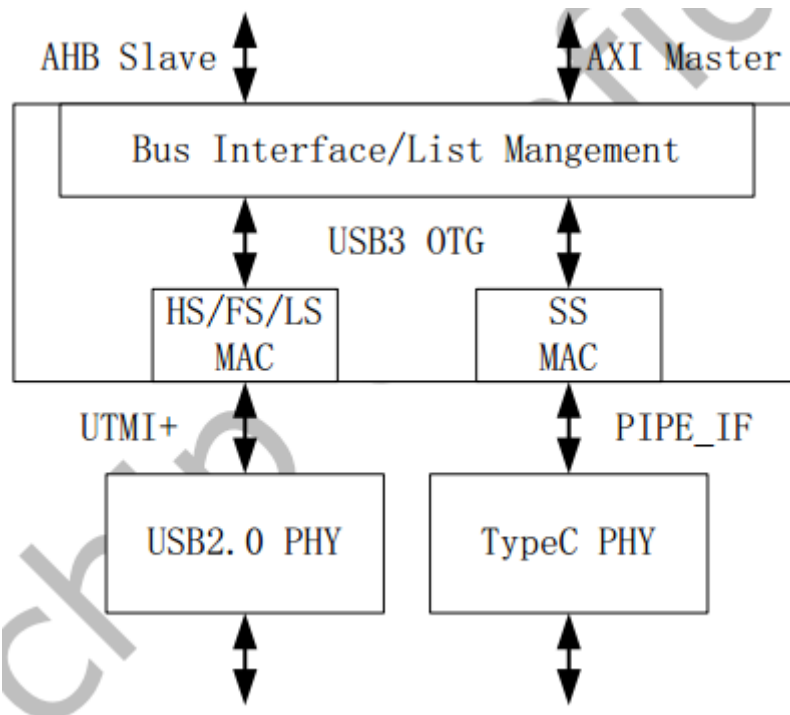


Figure 1 - 3 USB 3.0 OTG Block Diagram

## 1.5 USB 2.0 PHY

The USB 2.0 PHY supports two designs, one port and two ports. Figure 1-4 below is a block diagram that supports two ports.

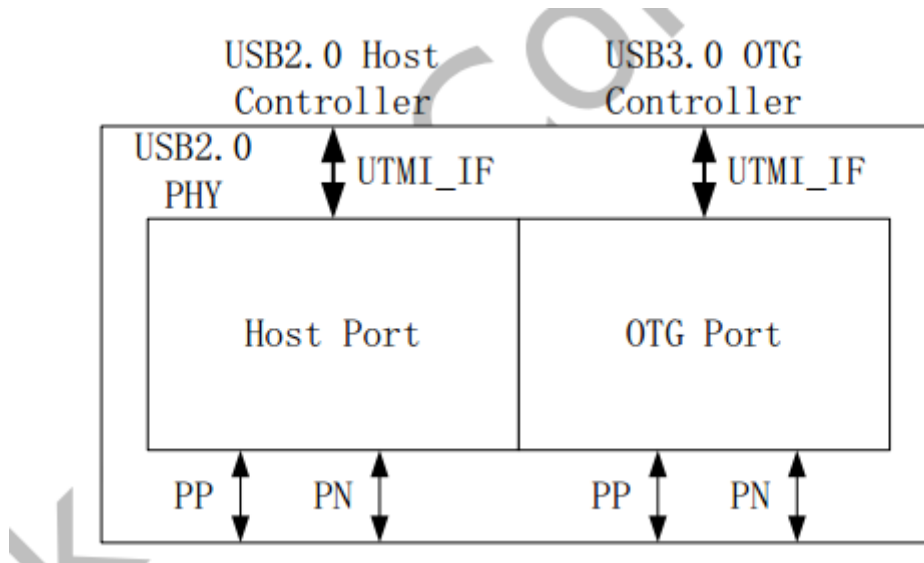


Figure 1 - 4 USB 2.0 PHY Block Diagram

- Host Port: connect to USB 2.0 Host controller via UTMI+
- OTG Port: connect to USB 3.0 OTG controller or USB 2.0 logic module of USB 2.0 OTG controller via UTMI+

## 1.6 Type-C USB 3.0 PHY

- Support USB 3.0 (SuperSpeed only)
- Support DisplayPort 1.3 (RBR, HBR and HBR2 data rates only)
- Support DisplayPort AUX channel
- Support USB TypeC and DisplayPort Alt Mode
- Support DisplayPort Alt Mode on TypeC A, B, C, D, E and F pinassignments
- Support Normal and Flipped orientation



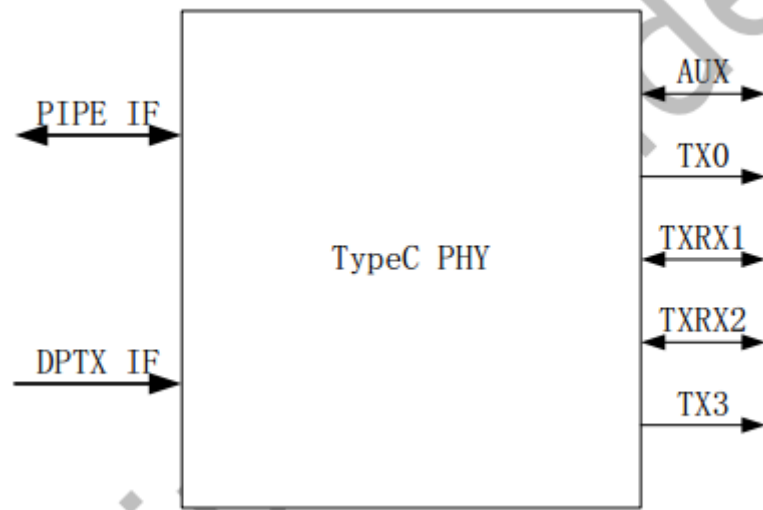


Figure 1 - 5 TypeC PHY Block Diagram

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## 2 Hardware Circuits and Signals

### 2.1 USB 2.0 Host Hardware Circuits

This chapter introduces the hardware circuit design and signal of USB 2.0 HOST. According to the type of USB 2.0 PHY used, it can be divided into common USB 2.0 HOST hardware circuit and USB 2.0 HSIC hardware circuit.

#### 2.1.1 Common USB 2.0 Host Hardware Circuit

USB 2.0 works at 480MHz clock, it is suggested that the width of USB 2.0 DP/DM lines should be 7-8 MIL and 90  $\Omega$  impedance differential. It is better to layout on the surface layer and cover the ground, and no interference source on the edge and no other signal line on the right upper and lower layers.

Example (USB 2.0 HOST hardware circuit design of RK3399 SoC).

- The SoC pins of the USB 2.0 Host controller are shown in Figure 2-1

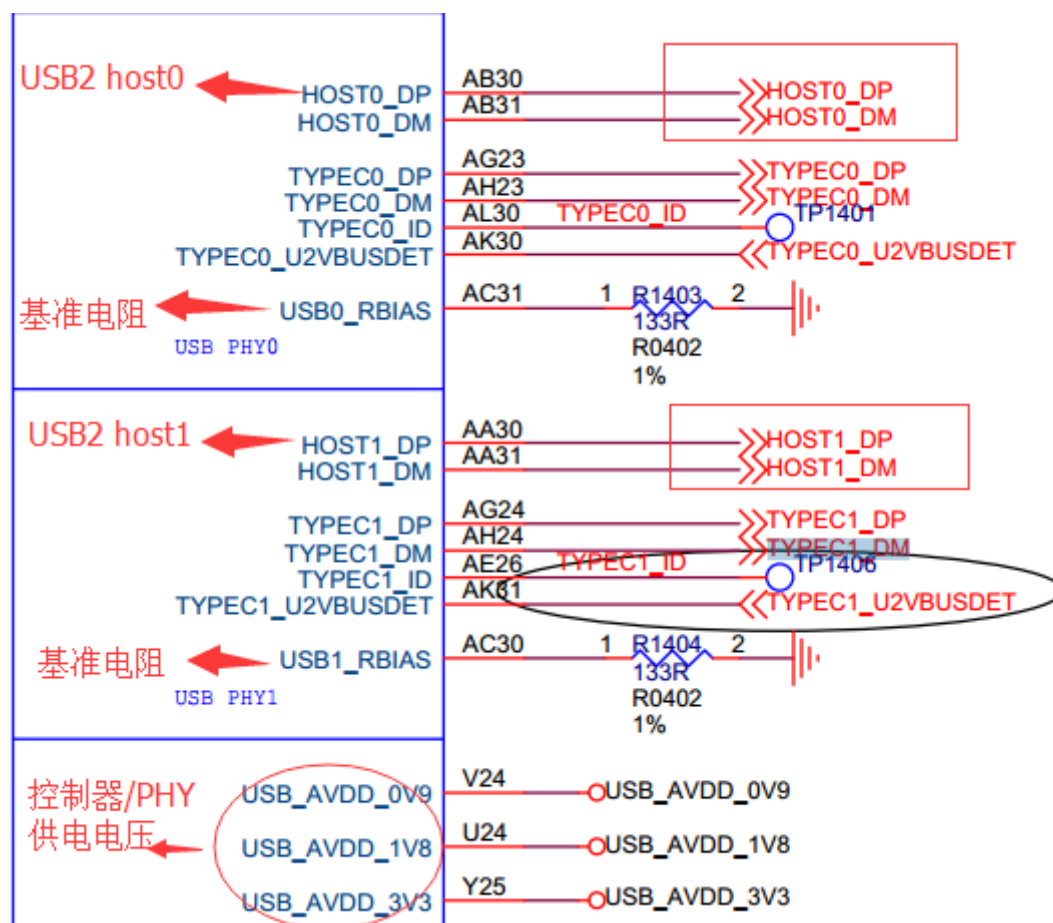


Figure 2 - 1 USB 2.0 HOST pin in SoC

- The control circuit and interface circuit of USB 2.0 Host VBUS are shown in Figure 2-2 and Figure 2-3

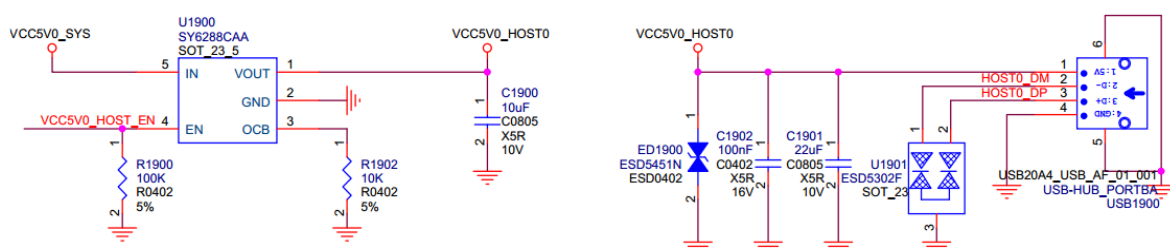


Figure 2-2 USB 2.0 Host VBUS control circuit and interface circuit

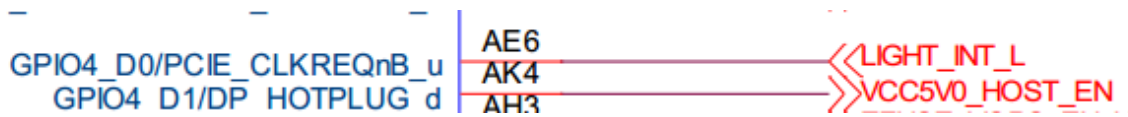


Figure 2 - 3 USB 2.0 Host VBUS GPIO controller pin

## 2.1.2 USB 2.0 HSIC Hardware Circuit

HSIC (High Speed Inter Chip) uses 240 MHz DDR signal, so the transmission rate is 480 Mbps, the same as USB 2.0, and the typical line impedance is 50  $\Omega$ . It is suggested that the maximum length of the line should not exceed 10 cm on the PCB.

As shown in Figure 2-4, USIC\_STROBE is 240MHz DDR signal line, USIC\_DATA is data line. The power supply voltage is only 0.9V and 1.2V, and standard voltage of signal transmission is 1.2V, which has lower power consumption than USB 2.0 PHY.

Example (USB 2.0 HSIC hardware circuit design of RK3399 SoC)

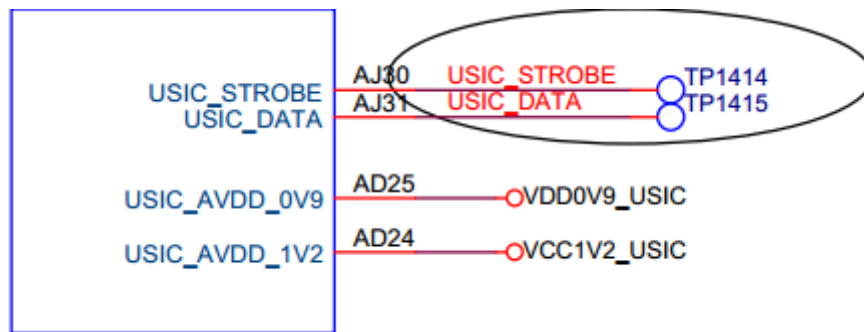


Figure 2 - 4 USB 2.0 HSIC pin in SoC

## 2.2 USB OTG Hardware Circuits

### 2.2.1 USB 2.0 OTG Hardware Circuit

USB 2.0 OTG related hardware signals:

- OTG\_DP/OTG\_DM: USB differential signal D+/D-, need to place 2.2 $\Omega$  series resistance on each signal line.
- USB\_DET: Input signal, used for OTG Peripheral mode to determine whether to connect to Host or USB charger. Default is low level 0V. If connect to Host or USB charger, the high level is 3.0~3.2 V.
- USB\_ID: Input signal, used to determine whether to switch to Host mode or Peripheral mode. Default is high level 1.8V (pull-up inside chip), and OTG works as Peripheral mode. The USB\_ID will be pull-down to the ground if connect with OTG-Host cable, and the USB driver will switch OTG to Host mode if the USB\_ID level changes from high to low voltage.
- USB\_RBIAS: Base resistance of USB 2.0 PHY. Because the resistance of the resistor will affect the amplitude of the USB signal, so please strictly follow the resistance design of the SDK reference schematic diagram.
- VCC5V0\_OTG: When OTG work as Peripheral mode, it's the input origin signal of USB\_DET. When OTG work as Host mode, it's supply VBUS 5V for USB Devices.
- USB\_AVDD\_1V0/USB\_AVDD\_1V8/USB\_AVDD\_3V3: Power supply for USB 2.0 PHY.

USB 2.0 OTG PHY power supply: **USB\_AVDD\_1V0**, **USB\_AVDD\_1V8**, **USB\_AVDD\_3V3**

The complete USB 2.0 OTG reference circuit is shown in Figures 2-5 ~ 2-8 (Reference to PX30 EVB) .



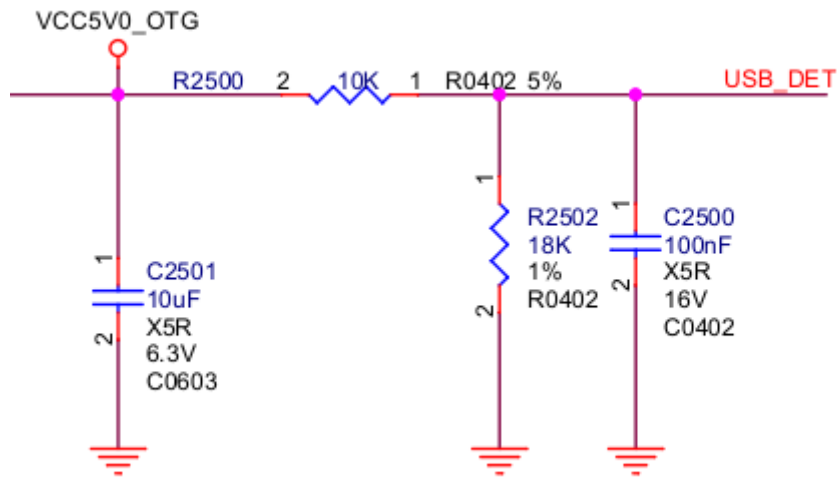


Figure 2-7 USB 2.0 OTG\_DET circuit

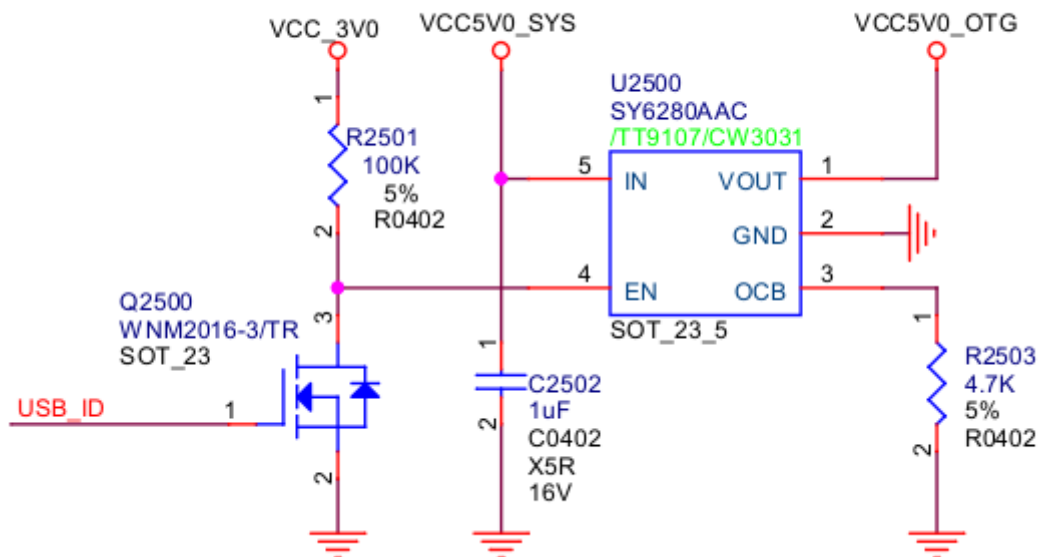


Figure 2-8 USB 2.0 OTG\_DRV circuit

## 2.2.2 USB 3.0 OTG Hardware Circuit

The maximum transmission rate of USB 3.0 OTG is 5Gbps, which is downward compatible with USB 2.0 OTG function. The physical interface is Type-C or Type-A. The USB 3.0 OTG supports 4-wire differential signal lines up to 3 meters and 11-inch PCB. In order to avoid interference and reduce electromagnetic interference, the 5Gbps signal is transmitted by differential signal on long cable.

Figure 2-9 ~ 2-14 is the Type-C USB 3.0 related circuit design of RK3399 platform.

A1	A2	A3	A4	A5	A6	A7	A8	A9	A10	A11	A12
GND	TX1+	TX1-	VBUS	CC1	D+	D-	SBU1	VBUS	RX2-	RX2+	GND
B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1
GND	RX1+	RX1-	VBUS	SBU2	D-	D+	CC2	VBUS	TX2-	TX2+	GND

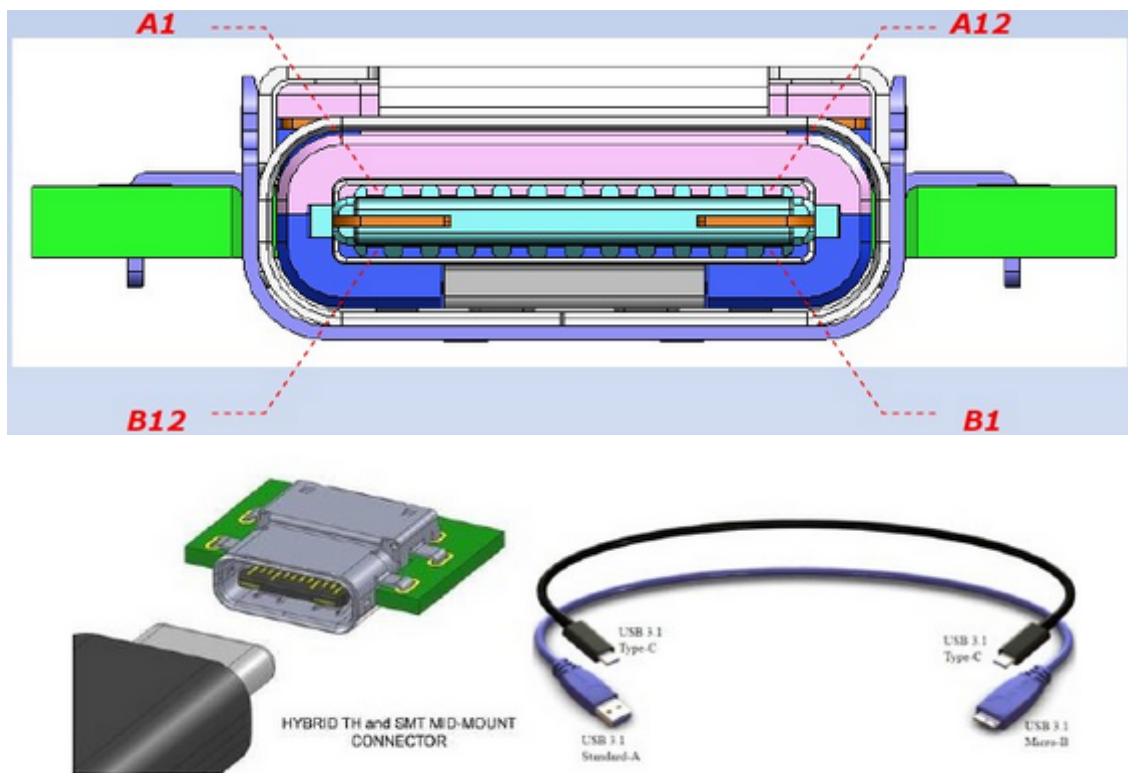


Figure 2 - 9 Type-C interface definition

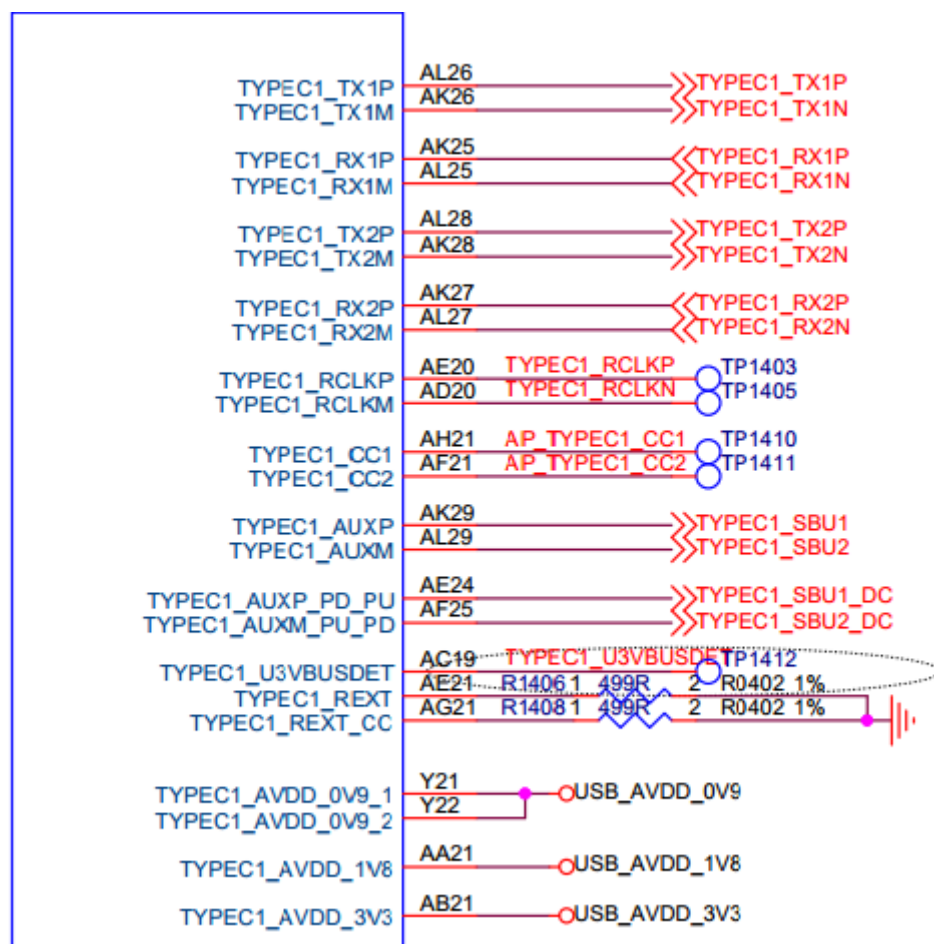


Figure 2 - 10 USB 3.0 OTG pin in SoC



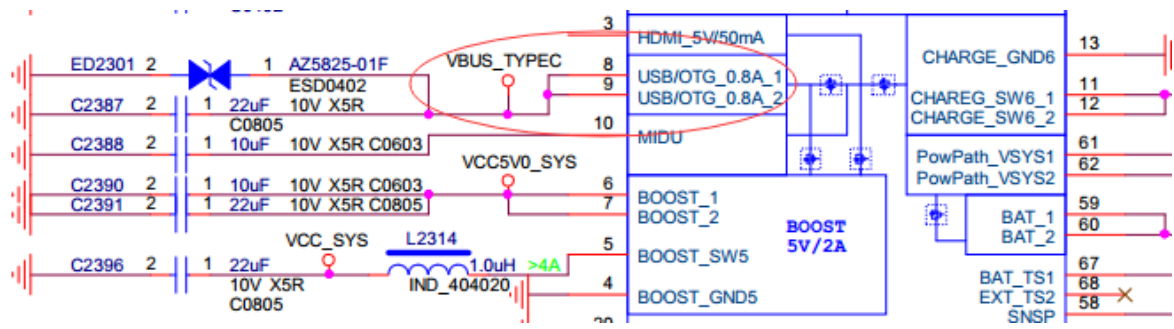


Figure 2 - 14 USB 3.0 VBUS Control-2 (Control by RK818)



## 3 Kernel USB CONFIG

The configuration and saving of the USB module is the same as the other kernel modules.

Import the default configuration:

```
1 | make ARCH=arm64 rockchip_defconfig
```

Select kernel configuration:

```
1 | make ARCH=arm64 menuconfig
```

Save the configuration:

```
1 | make ARCH=arm64 savedefconfig
```

Use the defconfig instead of the rockchip\_defconfig

### 3.1 USB PHY CONFIG

```
1 |
2 | Device Drivers --->
3 |     PHY Subsystem --->
4 |         ...
5 |         <*> Rockchip INNO USB2PHY Driver
6 |         ...
7 |         <*> Rockchip TYPEC PHY Driver
8 |         ...
9 |         <*> Rockchip INNO USB 3.0 PHY Driver
10 |
```

"Rockchip INNO USB2PHY Driver" is used for USB 2.0 PHY with Innosilicon IP block;

"Rockchip TYPEC PHY Driver" is used for USB 3.0 PHY IP block, e.g. RK3399;

"Rockchip INNO USB 3.0 PHY Driver" is used for USB 3.0 PHY with Innosilicon IP block, e.g. RK3328;

### 3.2 USB Host CONFIG

The configuration of the USB Host module is located at

```
1 |
2 | Device Drivers --->
3 |     [*] USB support --->
4 |         *- Support for Host-side USB
5 |         ...
6 |         <*> xHCI HCD (USB 3.0) support
7 |         *- Generic xHCI driver for a platform device
8 |         ...
9 |         <*> EHCI HCD (USB 2.0) support
10 |     [ ] Root Hub Transaction Translators
11 |     [*] Improved Transaction Translator scheduling
12 |     <*> Generic EHCI driver for a platform device
13 |     ...
```

```

14      <*> OHCI HCD (USB 1.1) support
15      < >      OHCI support for PCI-bus USB controllers
16      <*>      Generic OHCI driver for a platform device
17

```

Select the "USB support" first to add core support for USB.

Select the "Supportfor Host-side USB" to add core support for USB HOST.

Select the OHCI configurations to support USB 1.1 HOST.

Select the EHCI configurations to support USB 2.0 HOST.

Select the xHCI configurations to support USB 3.0 HOST.

Note: In order to cut the Kernel core, the rk3308\_linux\_defconfig used for RK3308 doesn't support USB HOST. But actually, RK3308 SoC integrates one USB 2.0 Host controller (EHCI&OHCI). Select the OHCI/EHCI configurations and the related device class drivers if you want to use USB 2.0 HOST interface on RK3308 Board.

### 3.3 USB OTG CONFIG

Select the “DesignWare USB2 DRD Core Support” and the mode for USB 2.0 OTG controller driver.

Select the “DesignWare USB3 DRD Core Support“ and the mode for USB 3.0 OTG Controller driver.

```

1
2 Device Drivers --->
3     *- Support for Host-side USB
4     [*] USB support --->
5         ...
6         <*> DesignWare USB2 DRD Core Support
7             DWC2 Mode Selection (Dual Role mode)
8         ...
9         <*> DesignWare USB3 DRD Core Support
10             DWC3 Mode Selection (Dual Role mode)
11

```

### 3.4 USB Gadget CONFIG

Rockchip platforms support the USB Gadget ACM、RNDIS、MSC、MTP、PTP、Accessory、ADB、MIDI、Audio function by default. Developers can enable more USB Gadget functions according to actual product requirements, but at the same time, init files in Android system need to be modified.

(init.rk30board.usb.rc and init.usb.configfs.rc) 。

```

1
2 DeviceDrivers --->
3     [*]USB support --->
4         [*] USB Gadget Support --->
5             ...
6             USBGadget Drivers (USB functions configurable through configfs)
7         --->
8             [ ]      Generic serial bulk in/out
9             [*]      Abstract Control Model (CDC ACM)
10            [ ]      Object Exchange Model (CDC OBEX)
11            [ ]      Network Control Model (CDC NCM)
12            [ ]      Ethernet Control Model (CDC ECM)

```

```

12      [ ]      Ethernet Control Model (CDC ECM) subset
13      [*]      RNDIS
14      [ ]      Ethernet Emulation Model (EEM)
15      [*]      Mass storage
16      [ ]      Loopback and sourcesink function (for testing)
17      [*]      Function filesystem (FunctionFS)
18      [*]      MTP gadget
19      [*]      PTP gadget
20      [*]      Accessory gadget
21      [*]      Audio Source gadget
22      [*]      Uevent notification of Gadget state
23      [ ]      Audio Class 1.0
24      [ ]      Audio Class 2.0
25      [*]      MIDI function
26      [ ]      HID function
27      [ ]      USB Webcam function
28      [ ]      Printer function
29

```

## 3.5 USB Device Class Driver CONFIG

### 3.5.1 Mass Storage Class CONFIG

The U disk belongs to SCSI device, so the SCSI options need to be configured before enable the USB Mass Storage configuration.

```

1
2 Device Drivers --->
3     SCSI device support --->
4         <*> SCSI device support
5         [ ] SCSI: use blk-mq I/O path by default
6         [*] legacy /proc/scsi/ support
7             *** SCSI support type (disk, tape, CD-ROM) ***
8         <*> SCSI disk support
9         < > SCSI tape support
10        < > SCSI OnStream SC-x0 tape support
11        < > SCSI CDROM support
12        <*> SCSI generic support
13        <*> SCSI media changer support
14        [*] Verbose SCSI error reporting (kernel size +=75K)
15        [*] SCSI logging facility
16        [*] Asynchronous SCSI scanning
17            SCSI Transports --->
18        [*] SCSI low-level drivers --->
19        [ ] PCMCIA SCSI adapter support ----
20        [ ] SCSI Device Handlers ----
21

```

After add SCSI Device Support, you can enable the "USB Mass Storage support" in "USB Support".

```

1
2 Device Driver --->
3     [*] USB support --->
4         <*> USB Mass Storage support
5

```

### 3.5.2 USB Serial Converter CONFIG

- Support USB 3G Modem

```
1
2 Device Driver --->
3     [*] USB support --->
4         <*> USB Serial Converter support --->
5             <*> USB driver for GSM and CDMA modems
6
```

```
1
2 Device Driver --->
3     [*] Network device support --->
4         <*> PPP (point-to-point protocol) support
5             <*> PPP BSD-Compress compression
6             <*> PPP Deflate compression
7             [*] PPP filtering
8             <*> PPP MPPE compression (encryption)
9             [*] PPP multilink support
10            <*> PPP over Ethernet
11            <*> PPP over L2TP
12            <*> PPP on L2TP Access Concentrator
13            <*> PPP on PPTP Network Server
14            <*> PPP support for async serial ports
15            <*> PPP support for sync tty ports
16
```

- Support PL2303

Select the following configuration for PL203, and disable the "USB driver for GSM and CDMA modems" configuration at the same time. Otherwise, PL2303 may be misidentified as USB 3G modem.

```
1
2 Device Driver --->
3     [*] USB support --->
4         <*> USB Serial Converter support --->
5             <*> USB Prolific 2303 Single Port Serial Driver
6
```

- Support USB GPS (e.g. u-blox 6 - GPS Receiver)

```
1
2 Device Drivers --->
3     [*] USB support --->
4         [*] USB Modem (CDC ACM) support
5
```

### 3.5.3 USB HID CONFIG

Select the following HID configuration to support generic USB Mouse and Keyboard.

```

1
2 Device Drivers --->
3     [*] HID support
4         [*] USB HID transport layer
5         [ ] PID device support
6         [*] /dev/hiddev raw HID device support
7

```

### 3.5.4 USB Net CONFIG

- USB Bluetooth CONFIG

```

1
2 [*] Networking support --->
3     ...
4     <*> Bluetooth subsystem support --->
5         Bluetooth device drivers --->
6             ...
7             <*> HCI USB driver
8             [*]   Broadcom protocol support (NEW)
9             [*]   Realtek protocol support (NEW)
10            ...
11

```

- USB WIFI CONFIG

Need to add WIFI Vendor special driver.

- USB Ethernet CONFIG

```

1
2 Device Driver --->
3     [*] Network device support --->
4         <*> USB Network Adapters --->
5             <*> USB CATC NetMate-based Ethernet device support
6             <*> USB KLSI KL5USB101-based ethernet device support
7             <*> USB Pegasus/Pegasus-II based ethernet device support
8             <*> USB RTL8150 based ethernet device support
9             <*> Realtek RTL8152/RTL8153 Based USB Ethernet Adapters
10            < > Microchip LAN78XX Based USB Ethernet Adapters
11            <*> Multi-purpose USB Networking Framework
12            <*>   ASIX AX88xxx Based USB 2.0 Ethernet Adapters
13            <*>   ASIX AX88179/178A USB 3.0/2.0 to Gigabit Ethernet
14            -* CDC Ethernet support (smart devices such as cable modems)
15            <*> CDC EEM support
16            -* CDC NCM support
17            < > Huawei NCM embedded AT channel support
18            <*> CDC MBIM support
19            <*> Davicom DM96xx based USB 10/100 ethernet devices
20            < > CoreChip-sz SR9700 based USB 1.1 10/100 ethernet devices
21            < > CoreChip-sz SR9800 based USB 2.0 10/100 ethernet devices
22            <*> SMSC LAN75XX based USB 2.0 gigabit ethernet devices
23            <*> SMSC LAN95XX based USB 2.0 10/100 ethernet devices
24            <*> GeneSys GL620USB-A based cables
25            <*> NetChip 1080 based cables (Laplink, ...)
26            <*> Prolific PL-2301/2302/25A1/27A1 based cables

```

```

27      <*> MosChip MCS7830 based Ethernet adapters
28      <*> Host for RNDIS and ActiveSync devices
29      <*> Simple USB Network Links (CDC Ethernet subset)
30      [*]     ALi M5632 based 'USB 2.0 Data Link' cables
31      [*]     AnchorChips 2720 based cables (Xircom PGUNET, ...)
32      [*]     eTEK based host-to-host cables (Advance, Belkin, ...)
33      [*]     Embedded ARM Linux links (iPaq, ...)
34      [*]     Epson 2888 based firmware (DEVELOPMENT)
35      [*]     KT Technology KC2190 based cables (InstaNet)
36      <*> Sharp Zaurus (stock ROMs) and compatible
37      <*> Conexant CX82310 USB ethernet port
38      <*> Samsung Kalmia based LTE USB modem
39      <*> QMI WWAN driver for Qualcomm MSM based 3G and LTE modems
40      <*> Option USB High Speed Mobile Devices
41      <*> Intellon PLC based usb adapter
42      <*> Apple iPhone USB Ethernet driver
43      <*> USB-to-WWAN Driver for Sierra Wireless modems
44      < > LG VL600 modem dongle
45      < > QingHeng CH9200 USB ethernet support
46

```

### 3.5.5 USB Camera CONFIG

```

1
2 Device Driver --->
3     <*> Multimedia support --->
4         [*] Media USB Adapters --->
5             *** Webcam devices ***
6         <*> USB Video Class (UVC)
7         [*] UVC input events device support
8

```

### 3.5.6 USB Audio CONFIG

```

1
2 Device Driver --->
3     <*> Sound card support --->
4         <*> Advanced Linux Sound Architecture --->
5             ...
6         [*] USB sound devices --->
7             [*] USB Audio /MIDI driver
8

```

### 3.5.7 USB HUB CONFIG

Disable the configuration “Disable external HUBs” to support the external USB HUB.

```

1
2 Device Drivers --->
3     [*] USB support --->
4         *- Support for Host-side USB
5         ...
6         [ ] Disable external hubs
7

```

There are many other USB devices that may be used, such as GPS, Printer, etc. It may need Vendor customized driver or standard Class driver. If you need to support these USB devices, you can search methods via internet to support them. Rockchip platforms have no special requirements, you can directly refer to those methods.

---

## 4 USB DTS Configuration

### 4.1 USB 2.0/3.0 PHY DTS

USB PHY is divided into USB 2.0 PHY and USB 3.0 PHY. These two PHYs are independent of each other, and their characteristics are quite different, so you need to configure DTS separately.

**Note:** The USB PHY DTS configuration of the RK3399 SoC is more flexible and complicated, please refer to the document:

Rockchip\_RK3399\_Developer\_Guide\_USB\_DTS\_CN

#### 4.1.1 USB 2.0 PHY DTS

Rockchip series SoCs mainly use two USB 2.0 PHY IPs: Innosilicon IP and Synopsis IP. The hardware design of these two IPs is different, so the corresponding PHY DTS configuration is also different. Most of the Rockchip series USB 2.0 PHYs use Innosilicon IP.

##### 1. USB 2.0 PHY DTS Configuration Document

Innosilicon USB 2.0 PHY DTS configuration document (for SoCs other than RK3188/RK3288)

Documentation/devicetree/bindings/phy/phy-rockchip-inno-usb2.txt

Synopsis USB 2.0 PHY DTS Configuration document (for RK3188/RK3288 SoC)

Documentation/devicetree/bindings/phy/rockchip-usb-phy.txt

##### 2. USB 2.0 PHY DTS Example

Example (RK3399 USB 2.0 PHY0 DTS)

- USB 2.0 PHY parent node: RK3399 USB 2.0 PHY registers are in GRF, so use GRF node as the parent of USB 2.0 PHY, and use the base address of GRF.
- USB 2.0 PHY node: RK3399 USB 2.0 PHY is a combphy, it comprises with a Host port and a OTG port. And both of these two port use the same reference input clock and the same 480MHz out clock. And also use the same address offset of GRF for USB PHY configuration.
- USB 2.0 PHY sub-nodes: A sub-node is required for each port the phy provides. The sub-node name is used to identify Host or OTG port, "otg-port" is the name of otg port, "host-port" is the name of host port. These two port has different interrupts.

```
1
2 grf: syscon@ff770000 {
3     compatible = "rockchip,rk3399-grf", "syscon", "simple-mfd";
4     reg = <0x0 0xff770000 0x0 0x10000>;
5     #address-cells = <1>;
6     #size-cells = <1>;
7
8     u2phy0: usb2-phy@e450 {
9         compatible = "rockchip,rk3399-usb2phy";
10        reg = <0xe450 0x10>;
11        clocks = <&cru SCLK_USB2PHY0_REF>;
12        clock-names = "phyclk";
13        #clock-cells = <0>;
14        clock-output-names = "clk_usbphy0_480m";
15        status = "disabled";
16
17        u2phy0_host: host-port {
```



```

18         #phy-cells = <0>;
19         interrupts = <GIC_SPI 27 IRQ_TYPE_LEVEL_HIGH 0>;
20         interrupt-names = "linestate";
21         status = "disabled";
22     };
23
24     u2phy0_otg: otg-port {
25         #phy-cells = <0>;
26         interrupts = <GIC_SPI 103 IRQ_TYPE_LEVEL_HIGH 0>,
27                     <GIC_SPI 104 IRQ_TYPE_LEVEL_HIGH 0>,
28                     <GIC_SPI 106 IRQ_TYPE_LEVEL_HIGH 0>;
29         interrupt-names = "otg-bvalid", "otg-id",
30                         "linestate";
31         status = "disabled";
32     };
33 };
34 };
35

```

For Host port and OTG port host mode, we may need to config regulator for USB VBUS 5V in board DTS, it's an optional property.

Example (RK3399 USB 2.0 Host VBUS regulator property in DTS)

The control method of RK3399 USB 2.0 Host VBUS is: if GPIO is pulled high, the VBUS 5V output is enabled; when GPIO is pulled low, the VBUS 5V output is closed. In DTS, regulator is used to configure GPIO. Among them, the attribute "regulator-always-on" indicates that after the system is started, the GPIO is pulled up to enable the VBUS 5V output until the system is shut down.

```

1
2     vcc5v0_host: vcc5v0-host-regulator {
3         compatible = "regulator-fixed";
4         enable-active-high;
5         gpio = <&gpio4 25 GPIO_ACTIVE_HIGH>;
6         pinctrl-names = "default";
7         pinctrl-0 = <&host_vbus_drv>;
8         regulator-name = "vcc5v0_host";
9         regulator-always-on;
10    };
11
12    usb2 {
13        host_vbus_drv: host-vbus-drv {
14            rockchip,pins =
15                <4 25 RK_FUNC_GPIO &pcfg_pull_none>;
16        };
17    };
18

```

Set the "phy-supply" property to the regulator "vcc5v0\_host" that provides power to VBUS 5V. In this way, the core code of the PHY framework will automatically parse the attribute and control the GPIO corresponding to the USB VBUS.

```

1     u2phy0_host: host-port {
2         phy-supply = <&vcc5v0_host>;
3         status = "okay";
4     };

```

## 4.1.2 USB 3.0 PHY DTS

Rockchip series SoCs mainly use three types of USB 3.0 PHY IP: Type-C PHY IP, Innosilicon USB 3.0 PHY IP and Innosilicon USB 3.0 CombPhy IP. These three IPs have different hardware designs, so their corresponding PHY DTS configurations are also different.

### 1. USB 3.0 PHY DTS Configuration Document

Type-C PHY DTS configuration document(for RK3399/RK3399Pro SoC)

```
Documentation/devicetree/bindings/phy/phy-rockchip-typec.txt
```

Innosilicon USB 3.0 PHY DTS configuration document(for RK3228H/RK3228 Soc)

```
Documentation/devicetree/bindings/phy/phy-rockchip-inno-usb3.txt
```

Innosilicon USB 3.0 Combphy configuration document(for RK1808 SoC, USB 3.0 & PCIe Combphy)

```
Documentation/devicetree/bindings/phy/phy-rockchip-inno-combophy.txt
```

### 2. USB 3.0 PHY DTS Example

Example (RK3399 Type-C0 USB 3.0 PHY)

Type-C PHY is a combination of USB 3.0 SuperSpeed PHY and DisplayPort Transmit PHY. So the tcphy0 has two sub-nodes "tcphy0\_dp" and "tcphy0\_usb3".

main DTS attribute description:

- rockchip,grf : phandle to the syscon managing the "general register files" .
- rockchip,typec-conn-dir : the register of type-c connector direction.
- rockchip,usb3tousb2-en : the register of type-c force usb3 to usb2 enable.
- rockchip,external-psm : the register of type-c phy external psm clock.
- rockchip,pipe-status : the register of type-c phy pipe status.
- rockchip,uphy-dp-sel : the register of type-c phy selection for DP.

```
1  tcphy0: phy@ff7c0000 {
2      compatible = "rockchip,rk3399-typec-phy";
3      reg = <0x0 0xff7c0000 0x0 0x40000>;
4      rockchip,grf = <&grf>;
5      #phy-cells = <1>;
6      clocks = <&cru SCLK_UPHY0_TCPDCORE>,
7              <&cru SCLK_UPHY0_TCPDPHY_REF>;
8      clock-names = "tcpdcore", "tcpdphy-ref";
9      assigned-clocks = <&cru SCLK_UPHY0_TCPDCORE>;
10     assigned-clock-rates = <50000000>;
11     power-domains = <&power RK3399_PD_TCPD0>;
12     resets = <&cru SRST_UPHY0>,
13            <&cru SRST_UPHY0_PIPE_L00>,
14            <&cru SRST_P_UPHY0_TCPHY>;
15     reset-names = "uphy", "uphy-pipe", "uphy-tcphy";
16     rockchip,typec-conn-dir = <0xe580 0 16>;
17     rockchip,usb3tousb2-en = <0xe580 3 19>;
18     rockchip,usb3-host-disable = <0x2434 0 16>;
19     rockchip,usb3-host-port = <0x2434 12 28>;
20     rockchip,external-psm = <0xe588 14 30>;
21     rockchip,pipe-status = <0xe5c0 0 0>;
22     rockchip,uphy-dp-sel = <0x6268 19 19>;
23     status = "disabled";
24 }
```

```

25
26     tcphy0_dp: dp-port {
27         #phy-cells = <0>;
28     };
29
30     tcphy0_usb3: usb3-port {
31         #phy-cells = <0>;
32     };
33 };
34

```

#### Note:

*There are 2 type-c phys for RK3399, and they are almost identical.*

*This document only describes the configuration of RK3399 USB 3.0 Type-C PHY in DTSI. In fact, there are some related configurations in DTS such as the extcon attribute and the hardware attributes of CC chip (FUSB302).*

*For details, please refer to the document:*

Rockchip\_RK3399\_Developer\_Guide\_USB\_DTS\_CN

## 4.2 USB 2.0 Controller DTS

There are two different architectures controllers:

- EHCI (Enhanced Host Controller Interfac, only support USB 2.0) and OHCI (Open Host Controller Interface, support USB 1.1 & 1.0)
- DWC2 (DesignWare Cores USB 2.0 Hi-Speed On-The-Go (OTG), support USB 2.0 & 1.1 & & 1.0)

The following describes the two different architectures of the USB 2.0 controller DTS.

### 4.2.1 USB 2.0 Host Controller DTS

#### 1. USB 2.0 Host Controller DTS configuration document

Documentation/devicetree/bindings/usb/usb-ehci.txt

Documentation/devicetree/bindings/usb/usb-ohci.txt

#### 2. USB 2.0 Host Controller DTS example

Example (DTS of RK3399 USB 2.0 Host0 EHCI & OHCI Controller)

The compatible of the EHCI controller is fixed as “generic-ehci”, and the compatible of the OHCI controller is fixed as “generic-ohci”. In addition, EHCI and OHCI multiplex the same clocks and phys.

Attribute "power-domains" needs to be configured only when the SoC's USB 2.0 Host controller supports the power-domains function.

```

1
2 usb_host0_ehci: usb@fe380000 {
3     compatible = "generic-ehci";
4     reg = <0x0 0xfe380000 0x0 0x20000>;
5     interrupts = <GIC_SPI 26 IRQ_TYPE_LEVEL_HIGH 0>;
6     clocks = <&cru HCLK_HOST0>, <&cru HCLK_HOST0_ARB>,
7           <&cru SCLK_USBPHY0_480M_SRC>;
8     clock-names = "hclk_host0", "hclk_host0_arb", "usbphy0_480m";
9     phys = <&u2phy0_host>;
10    phy-names = "usb";
11    power-domains = <&power RK3399_PD_PERIHP>;
12    status = "disabled";

```

```

13 };
14
15 usb_host0_ohci: usb@fe3a0000 {
16     compatible = "generic-ohci";
17     reg = <0x0 0xfe3a0000 0x0 0x20000>;
18     interrupts = <GIC_SPI 28 IRQ_TYPE_LEVEL_HIGH 0>;
19     clocks = <&cru HCLK_HOST0>, <&cru HCLK_HOST0_ARB>,
20             <&cru SCLK_USBPHY0_480M_SRC>;
21     clock-names = "hclk_host0", "hclk_host0_arb", "usbphy0_480m";
22     phys = <&u2phy0_host>;
23     phy-names = "usb";
24     power-domains = <&power RK3399_PD_PERIHP>;
25     status = "disabled";
26 };
27

```

## 4.2.2 USB 2.0 OTG Controller DTS

### 1. USB 2.0 OTG Controller DTS configuration document

The USB 2.0 OTG uses a DWC2 controller. In the Linux-4.4 kernel, the DWC2 controller driver has two versions (dwc2 driver and dwc\_otg\_310 driver). Among them, the dwc\_otg\_310 driver is an older version of the driver only used for RK3288/RK3368 SoC. In the Linux-4.19 kernel, DWC2 controller use the dwc2 driver version for all SoCs and is no longer compatible with the old dwc\_otg\_310 driver.

DTS configuration file for dwc2 driver (for Linux-4.4 and newer kernels)

Documentation/devicetree/bindings/usb/dwc2.txt

Documentation/devicetree/bindings/usb/generic.txt

DTS configuration document for dwc\_otg\_310 driver (only for Linux-4.4, RK3288/RK3368 SoC)

Documentation/devicetree/bindings/usb/rockchip-usb.txt

### 2. USB 2.0 OTG Controller example

Example (DTS of RK3328 USB 2.0 OTG)

Main attribute as follows:

- dr\_mode: shall be one of "host", "peripheral" and "otg" ( Refer to usb/generic.txt).
- g-rx-fifo-size: size of rx fifo size in gadget mode.
- g-np-tx-fifo-size: size of non-periodic tx fifo size in gadget mode.
- g-tx-fifo-size: size of tx fifo per endpoint (except ep0) in gadget mode.
- g-use-dma: enable dma usage in gadget driver.
- phys: phy provider specifier.
- phy-names: shall be "usb2-phy".

Among them, "g-np-tx-fifo-size", "g-rx-fifo-size" and "g-tx-fifo-size" are used for fifo configuration in device mode, which can be configured according to the actual USB device application of the product. The requirements are described as follows:

1. "g-np-tx-fifo-size" configure the endpoint 0 fifo of the device. It is recommended to fix it to 16 (unit: 4Bytes);
2. "g-rx-fifo-size" configure the receiving fifo of the device OUT Endpoint. All OUT Endpoints share one receiving fifo. It is recommended to fix it to 275 (unit: 4Bytes);

3. "g-tx-fifo-size" configure the sending fifo of the device IN Endpoint, each IN Endpoint has a dedicated sending fifo. The corresponding tx-fifo can be configured according to the number of IN Endpoints actually used. When configuring tx-fifo, there are two principles:

- 1) tx-fifo cannot be smaller than EP max-packet;
- 2) The larger the tx-fifo, the better the transmission performance, so if the tx-fifo is large enough, it is recommended to configure it to be 2 times or larger than the EP max-packet;

```
1
2 usb20_otg: usb@ff580000 {
3     compatible = "rockchip,rk3328-usb", "rockchip,rk3066-usb",
4                 "snps,dwc2";
5     reg = <0x0 0xff580000 0x0 0x40000>;
6     interrupts = <GIC_SPI 23 IRQ_TYPE_LEVEL_HIGH>;
7     clocks = <&cru HCLK_OTG>, <&cru HCLK_OTG_PMU>;
8     clock-names = "otg", "otg_pmu";
9     dr_mode = "otg";
10    g-np-tx-fifo-size = <16>;
11    g-rx-fifo-size = <275>;
12    g-tx-fifo-size = <256 128 128 64 64 32>;
13    g-use-dma;
14    phys = <&u2phy_otg>;
15    phy-names = "usb2-phy";
16    status = "disabled";
17 };
18
```

## 4.3 USB 3.0 Controller DTS

### 4.3.1 USB 3.0 Host Controller DTS

USB 3.0 Host controller is xHCI, integrated in DWC3 OTG IP, so it is not necessary to configure DTS separately for xHCI. We only need to configure DWC3 DTS, and set the "dr\_mode" attribute of DWC3 to "otg" or "host".

### 4.3.2 USB 3.0 OTG Controller DTS

#### 1. USB 3.0 OTG Controller DTS Configuration Document

The USB 3.0 OTG uses a DWC3 controller. Linux-4.4 and Linux-4.19 or later kernel versions have different USB 3.0 OTG DTS configurations because Linux-4.19 USB DWC3 controller driver has been upgraded significantly compared to Linux-4.4 (for specific differences, please refer to [5.3.1 USB 3.0 OTG Controller Driver Development](#))

Linux-4.4 USB 3.0 OTG controller DTS configuration document

Documentation/devicetree/bindings/usb/dwc3.txt (DWC3 Controller common attribute configuration description) Documentation/devicetree/bindings/usb/generic.txt (USB Controller common attribute configuration description)

Documentation/devicetree/bindings/usb/rockchip,dwc3.txt (for RK3399/RK1808 SoC)

Documentation/devicetree/bindings/usb/rockchip-inno,dwc3.txt (for RK3328/RK3228H SoC)

Linux-4.19 and newer kernel USB 3.0 OTG Controller DTS configuration document

[Documentation/devicetree/bindings/usb/dwc3.txt](#) (DWC3 Controller common attribute configuration description) [Documentation/devicetree/bindings/usb/generic.txt](#) (USB Controller common attribute configuration description) [Documentation/devicetree/bindings/usb/rockchip-inno,dwc3.txt](#) (for RK3328/RK3228H SoC)

## Differences in DTS configuration between Linux-4.4 and 4.19 USB 3.0 controllers

- DWC3's power-domains, resets and extcon attribute have different reference locations. In Linux-4.4 kernel, these three attributes are placed on the parent node (usbdrd3) of the DWC3 controller, while in Linux-4.19 kernel, these three attributes are moved to the child nodes (usbdrd\_dwc3) of the DWC3 controller;
- When configuring Type-C to Type-A USB 2.0/3.0 OTG DTS, it is necessary to add the configuration of the extcon attribute in the USB controller sub-node (usbdrd\_dwc3) to support software switching OTG mode in Linux-4.19 kernel, but not in Linux-4.4 kernel.

## 2. USB 3.0 OTG Controller DTS Example

Example (RK3399 USB 3.0 OTG DTS in Linux-4.4 kernel)

The USB 3.0 OTG DTS includes a parent node "usbdrd3\_0" and a child node "usbdrd\_dwc3\_0". For all SoCs except for RK3328/RK3228H supporting DWC3 controller, compatible attribute in the parent node must add "rockchip, rk3399-dwc3". The child nodes of all SoCs are configured as "snps, dwc3". The role of the parent node is to configure chip-level related attributes, such as clocks, power-domains, and reset. The role of the child node is to configure the controller-related attributes in which the quirk attribute is applicable to the DWC3 controllers of all SoCs.

```
1  usbdrd3_0: usb0 {
2      compatible = "rockchip,rk3399-dwc3";
3      clocks = <&cru SCLK_USB3OTG0_REF>, <&cru SCLK_USB3OTG0_SUSPEND>,
4              <&cru ACLK_USB3OTG0>, <&cru ACLK_USB3_GRF>;
5      clock-names = "ref_clk", "suspend_clk",
6                  "bus_clk", "grf_clk";
7      power-domains = <&power RK3399_PD_USB3>;
8      resets = <&cru SRST_A_USB3_OTG0>;
9      reset-names = "usb3-otg";
10     #address-cells = <2>;
11     #size-cells = <2>;
12     ranges;
13     status = "disabled";
14
15     usbdrd_dwc3_0: dwc3@fe800000 {
16         compatible = "snps,dwc3";
17         reg = <0x0 0xfe800000 0x0 0x100000>;
18         interrupts = <GIC_SPI 105 IRQ_TYPE_LEVEL_HIGH 0>;
19         dr_mode = "otg";
20         phys = <&u2phy0_otg>, <&tcphy0_usb3>;
21         phy-names = "usb2-phy", "usb3-phy";
22         phy_type = "utmi_wide";
23         snps,dis_enblslpm_quirk;
24         snps,dis-u2-freeclk-exists-quirk;
25         snps,dis_u2_susphy_quirk;
26         snps,dis-del-phy-power-chg-quirk;
27         snps,tx-ipgap-linecheck-dis-quirk;
28         snps,xhci-slow-suspend-quirk;
29         snps,xhci-trb-ent-quirk;
30         snps,usb3-warm-reset-on-resume-quirk;
31         status = "disabled";
```



# 5 USB Driver Development

## 5.1 Linux USB Driver Framework

The Linux USB protocol stack is a layered architecture, as shown in Figure 5-1 below. The left is the USB device driver, the right is the USB host driver, and the bottom layer is the driver for the different USB controllers and PHYs of the Rockchip SoCs.

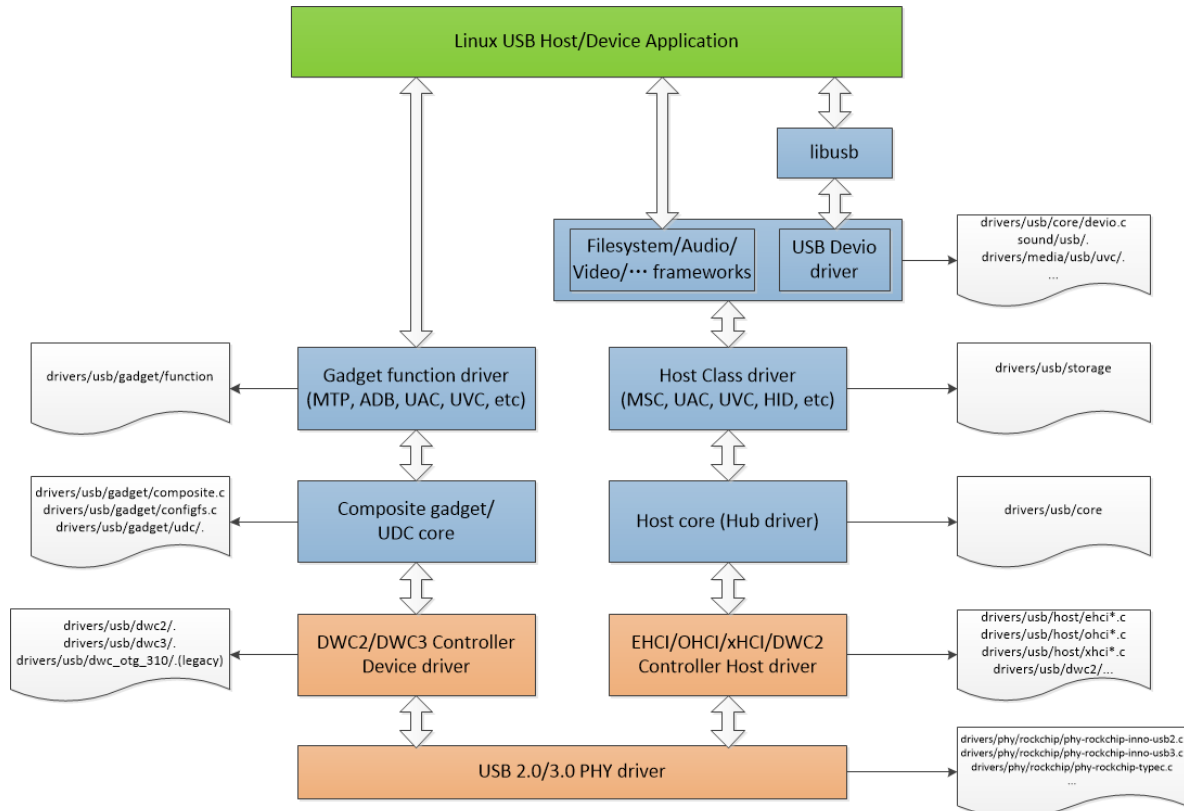


Figure 5-1 Linux USB driver framework

## 5.2 USB PHY Drivers

This chapter mainly introduces the driver code of PHY briefly. If you want to know more about the hardware framework, register description, signal adjustment of PHY, please refer to the document

`Rockchip_Developer_Guide_Linux_USB_PHY_CN`

### 5.2.1 USB 2.0 PHY Driver

Rockchip SoCs mainly use two USB 2.0 PHY IPs: Innosilicon IP and Synopsis IP. The hardware design of these two IPs is different, so a separate USB PHY driver is required. At the same time, SoCs with the same USB 2.0 PHY IP use the same driver, instead of each SoC having a dedicated driver.

#### 1. USB 2.0 PHT driver code

- Innosilicon USB 2.0 PHY Driver code

`drivers/phy/phy-rockchip-inno-usb2.c`

- Synopsis USB 2.0 PHY Driver code (only used for RK3188/RK3288):

`drivers/phy/rockchip/phy-rockchip-usb.c`

For the time being, most of SoCs except RK3188/RK3288 use Innosilicon IP, so this chapter mainly introduces Innosilicon IP.



## 2. Innosilicon USB 2.0 PHY IP feature

- Fully compliant with USB specification Rev 2.0
- Support 480Mbps/12Mbps/1.5Mbps serial data transmission
- Support all test modes defined in USB2.0 Specification
- Support one port of one PHY, or two ports of one PHY (Comprises with one OTG port and one Host port)
- OTG Port support dual-role device
- fully support Battery Charge 1.2 Specification

## 3. USB 2.0 PHY driver's important structure

In the USB 2.0 PHY driver, there is an important structure `rockchip_usb2phy_cfg`, which is mainly used to operate the USB PHY related registers. When adding a new SoC support for Innosilicon USB 2.0 PHY, the main job is to add the corresponding `rkxxxx_phy_cfgs` structure.

```
1 struct rockchip_usb2phy_cfg {
2     unsigned int    reg;
3     unsigned int    num_ports;
4     int (*phy_tuning)(struct rockchip_usb2phy *);
5     struct usb2phy_reg    clkout_ctl;
6     const struct rockchip_usb2phy_port_cfg    port_cfgs[USB2PHY_NUM_PORTS];
7     const struct rockchip_chg_det_reg    chg_det;
8 };
```

The members of the `rockchip_usb2phy_cfg` structure are described as follows:

- `reg`: the offset address of the USB PHY in the GRF module. This address should be the same as the corresponding `reg` attribute of the DTS USB 2.0 PHY. The purpose is to match the configuration of the DTS PHY and the PHY in the driver.
- `num_ports`: defines the number of ports supported by the USB PHY. For example, if OTG port and Host port are supported, `num_ports` is 2.
- `phy_tuning`: used for USB PHY signal adjustment, such as increasing pre-emphasis and increasing signal amplitude.
- `clkout_ctl`: controls the USB PHY's 480MHz output clock.
- `port_cfgs`: register configuration of USB PHY port.
- `chg_det`: register configuration related to charge detection.

## 4. USB 2.0 PHY state machine

The USB 2.0 PHY driver has three works that are used to handle different state machines:

- `rockchip_chg_detect_work`: charge detection function for OTG port device mode;
- `rockchip_usb2phy_otg_sm_work`: detect the connection status of the OTG port and control the PHY to enter/exit suspend;
- `rockchip_usb2phy_sm_work`: detect the connection status of the host port and control the PHY to enter/exit suspend;

In the driver, `dev_dbg` log has been added in key places, which makes it easy to view the state machine rotation during device connection and disconnection.

## 5. USB 2.0 PHY Driver Development Example

Example (RK3399 USB 3.0 PHY driver)

RK3399 supports two independent USB 2.0 PHYs. Each PHY comprises with one OTG port and one Host port. OTG port is used for USB3.0 OTG controller with Type-C USB 3.0 PHY to comprise as fully feature Type-C. Host port is used for USB2.0 host controller. The detailed `rk3399_phy_cfgs` structure code is as follows:

The registers in port\_cfgs is mainly used for PHY suspend mode control, VBUS level status detection, OTG ID level status detection, DP/DM line level status detection, etc. For the specific function description of each member, please refer to the notes of the structure members in the driver.

```

1  static const struct rockchip_usb2phy_cfg rk3399_phy_cfgs[] = {
2      {
3          .reg                = 0xe450,
4          .num_ports          = 2,
5          .phy_tuning          = rk3399_usb2phy_tuning,
6          .clkout_ctl          = { 0xe450, 4, 4, 1, 0 },
7          .port_cfgs           = {
8              [USB2PHY_PORT_OTG] = {
9                  .phy_sus = { 0xe454, 8, 0, 0x052, 0x1d1 },
10                 .bvalid_det_en = { 0xe3c0, 3, 3, 0, 1 },
11                 .bvalid_det_st = { 0xe3e0, 3, 3, 0, 1 },
12                 .bvalid_det_clr = { 0xe3d0, 3, 3, 0, 1 },
13                 .bypass_dm_en = { 0xe450, 2, 2, 0, 1 },
14                 .bypass_sel = { 0xe450, 3, 3, 0, 1 },
15                 .idfall_det_en = { 0xe3c0, 5, 5, 0, 1 },
16                 .idfall_det_st = { 0xe3e0, 5, 5, 0, 1 },
17                 .idfall_det_clr = { 0xe3d0, 5, 5, 0, 1 },
18                 .idrise_det_en = { 0xe3c0, 4, 4, 0, 1 },
19                 .idrise_det_st = { 0xe3e0, 4, 4, 0, 1 },
20                 .idrise_det_clr = { 0xe3d0, 4, 4, 0, 1 },
21                 .ls_det_en = { 0xe3c0, 2, 2, 0, 1 },
22                 .ls_det_st = { 0xe3e0, 2, 2, 0, 1 },
23                 .ls_det_clr = { 0xe3d0, 2, 2, 0, 1 },
24                 .utmi_avalid = { 0xe2ac, 7, 7, 0, 1 },
25                 .utmi_bvalid = { 0xe2ac, 12, 12, 0, 1 },
26             },
27             .utmi_iddig = { 0xe2ac, 8, 8, 0, 1 },
28             .utmi_ls = { 0xe2ac, 14, 13, 0, 1 },
29         },
30         .vbus_det_en = { 0x449c, 15, 15, 1, 0 },
31     },
32     [USB2PHY_PORT_HOST] = {
33         .phy_sus = { 0xe458, 1, 0, 0x2, 0x1 },
34         .ls_det_en = { 0xe3c0, 6, 6, 0, 1 },
35         .ls_det_st = { 0xe3e0, 6, 6, 0, 1 },
36         .ls_det_clr = { 0xe3d0, 6, 6, 0, 1 },
37         .utmi_ls = { 0xe2ac, 22, 21, 0, 1 },
38         .utmi_hstdet = { 0xe2ac, 23, 23, 0, 1 },
39     },
40     .chg_det = {
41         .opmode = { 0xe454, 3, 0, 5, 1 },
42         .cp_det = { 0xe2ac, 2, 2, 0, 1 },
43         .dcp_det = { 0xe2ac, 1, 1, 0, 1 },
44         .dp_det = { 0xe2ac, 0, 0, 0, 1 },
45         .idm_sink_en = { 0xe450, 8, 8, 0, 1 },
46         .idp_sink_en = { 0xe450, 7, 7, 0, 1 },
47         .idp_src_en = { 0xe450, 9, 9, 0, 1 },
48         .rdm_pdwn_en = { 0xe450, 10, 10, 0, 1 },
49         .vdm_src_en = { 0xe450, 12, 12, 0, 1 },
50     },
51 }

```

```

49         .vdp_src_en      = { 0xe450, 11, 11, 0, 1 },
50     },
51 },
52 {
53     .reg                  = 0xe460,
54     .num_ports            = 2,
55     .phy_tuning            = rk3399_usb2phy_tuning,
56     .clkout_ctl           = { 0xe460, 4, 4, 1, 0 },
57     .port_cfgs            = {
58         [USB2PHY_PORT_OTG] = {
59             .phy_sus = { 0xe464, 8, 0, 0x052, 0x1d1 },
60             .bvalid_det_en = { 0xe3c0, 8, 8, 0, 1 },
61             .bvalid_det_st = { 0xe3e0, 8, 8, 0, 1 },
62             .bvalid_det_clr = { 0xe3d0, 8, 8, 0, 1 },
63             .idfall_det_en = { 0xe3c0, 10, 10, 0, 1
64 },
65             .idfall_det_st = { 0xe3e0, 10, 10, 0, 1
66 },
67             .idfall_det_clr = { 0xe3d0, 10, 10, 0, 1
68 },
69             .idrise_det_en = { 0xe3c0, 9, 9, 0, 1 },
70             .idrise_det_st = { 0xe3e0, 9, 9, 0, 1 },
71             .idrise_det_clr = { 0xe3d0, 9, 9, 0, 1 },
72             .ls_det_en = { 0xe3c0, 7, 7, 0, 1 },
73             .ls_det_st = { 0xe3e0, 7, 7, 0, 1 },
74             .ls_det_clr = { 0xe3d0, 7, 7, 0, 1 },
75             .utmi_avalid = { 0xe2ac, 10, 10, 0, 1
76 },
77             .utmi_bvalid = { 0xe2ac, 16, 16, 0, 1
78 },
79             .utmi_iddig = { 0xe2ac, 11, 11, 0, 1
80 },
81             .utmi_ls = { 0xe2ac, 18, 17, 0, 1
82 },
83             .vbus_det_en = { 0x451c, 15, 15, 1, 0
84 },
85             },
86         [USB2PHY_PORT_HOST] = {
87             .phy_sus = { 0xe468, 1, 0, 0x2, 0x1
88 },
89             .ls_det_en = { 0xe3c0, 11, 11, 0, 1
90 },
91             .ls_det_st = { 0xe3e0, 11, 11, 0, 1
92 },
93             .ls_det_clr = { 0xe3d0, 11, 11, 0, 1
94 },
95             .utmi_ls = { 0xe2ac, 26, 25, 0, 1
96 },
97             .utmi_hstdet = { 0xe2ac, 27, 27, 0, 1 }
98         }
99     },
100     .chg_det = {
101         .opmode = { 0xe464, 3, 0, 5, 1 },
102         .cp_det = { 0xe2ac, 5, 5, 0, 1 },
103         .dcp_det = { 0xe2ac, 4, 4, 0, 1 },
104         .dp_det = { 0xe2ac, 3, 3, 0, 1 },
105         .idm_sink_en = { 0xe460, 8, 8, 0, 1 },
106         .idp_sink_en = { 0xe460, 7, 7, 0, 1 },

```

```

94 |             .idp_src_en      = { 0xe460, 9, 9, 0, 1 },
95 |             .rdm_pdown_en    = { 0xe460, 10, 10, 0, 1 },
96 |             .vdm_src_en      = { 0xe460, 12, 12, 0, 1 },
97 |             .vdp_src_en      = { 0xe460, 11, 11, 0, 1 },
98 |             },
99 |     },
100 |     { /* sentinel */ }
101 | };
102 |

```

## 6. USB 2.0 PHY Debug Interface

```

1 | /sys/devices/platform/[u2phy dev name] # ls
2 | driver          extcon  of_node  phy      subsystem
3 | driver_override modalias otg_mode  power    uevent
4 |

```

Note: [U2phy dev name] in the USB 2.0 PHY full path needs to be modified to the specific PHY node name corresponding to the SoC.

The "**otg\_mode**" node is used to switch the OTG Device/Host mode by software, and it is not affected by the OTG ID level status.

For example:

- Force host mode

```
echo host > /sys/devices/platform/[u2phy dev name]/otg_mode
```

- Force device mode

```
echo peripheral > /sys/devices/platform/[u2phy dev name]/otg_mode
```

- Force otg mode

```
echo otg > /sys/devices/platform/[u2phy dev name]/otg_mode
```

At the same time, the node is still compatible with the old order of Linux-3.10 and earlier, namely:

- Force host mode

```
echo 1 > /sys/devices/platform/[u2phy dev name]/otg_mode
```

- Force device mode

```
echo 2 > /sys/devices/platform/[u2phy dev name]/otg_mode
```

- Force otg mode

```
echo 0 > /sys/devices/platform/[u2phy dev name]/otg_mode
```

## 5.2.2 USB 3.0 PHY Drivers

Rockchip SoCs mainly use three types of USB 3.0 PHY IP: Type-C PHY IP, Innosilicon USB 3.0 PHY IP and Innosilicon USB 3.0 CombPhy IP. These three IPs have different hardware designs, so they need separate USB PHY drivers.

Note that all three USB 3.0 PHY IPs only support SuperSpeed, so they must be used together with USB 2.0 PHY to fully support the USB 3.0 protocol(supporting HighSpeed/FullSpeed/LowSpeed).

The three different USB 3.0 PHY IP drivers are briefly described below.

### 1. Type-C PHY Driver

- **Type-C USB 3.0 PHY driver code**

```
drivers/phy/rockchip/phy-rockchip-typec.c
```

- **Type-C USB 3.0 PHY driver example**

Example (RK3399 Type-C PHY)

Type-C PHY is a combination of USB 3.0 SuperSpeed PHY and DisplayPort Transmit PHY. Please refer to [1.6 USB 3.0 Type-C PHY](#) to learn about Type-C PHY's features.

In the probe function of Type-C PHY driver, rockchip\_dp\_phy\_ops of "dp-port" and rockchip\_usb3\_phy\_ops of "usb3-port" are created respectively, that is, the operation functions of USB 3.0 PHY and DP PHY such as power\_on and power\_off are independent and do not affect each other.

The Type-C PHY driver can support the following 4 working modes:

- USB 3.0 only: only works in USB 3.0 mode, such as a Type-C to Type-A USB 3.0 adapter cable;
- DP only: only works in DP mode, such as connecting a DP cable;
- USB 3.0 + DP 2 lanes: support USB 3.0 and DP 2 lanes work at the same time, such as connecting Type-C dongle;
- USB 2.0 + DP 4 lanes: support USB 2.0 and DP 4 lanes work at the same time, such as connecting Type-C VR headset;

In order to support the above four working modes, the Type-C PHY needs to be combined with a CC chip (FUSB302 chip is recommended) to detect the type of the inserted Type-C cable. The CC chip sends a message to the Type-C PHY using the extcon notification mechanism.

Important USB 3.0 phy\_ops:

- rockchip\_usb3\_phy\_power\_on: used for USB 3.0 Controller to power on Type-C USB 3.0 PHY.
- rockchip\_usb3\_phy\_power\_off: used for USB 3.0 Controller to power off Type-C USB 3.0 PHY.

Other important functions for USB 3.0:

- tphy\_cfg\_usb3\_to\_usb2\_only: used to force USB 3.0 works on USB 2.0 only.
- tphy\_cfg\_usb3\_pll: config PHY PLL for USB 3.0.

## 2. Innosilicon USB 3.0 PHY Driver

- **Innosilicon USB 3.0 PHY driver code**

```
drivers/phy/rockchip/phy-rockchip-inno-usb3.c
```

- **Innosilicon USB 3.0 PHY driver example**

Example (RK3328 USB 3.0 PHY).

RK3328 USB 3.0 PHY is combination of USB 3.0 PHY and USB 2.0 PHY. Some key features of the USB3.0 PHY are:

- Supports 5.0Gb/s serial data transmission rate
- Utilizes 8-bit, 16-bit or 32-bit parallel interface to transmit and receive USB SuperSpeed data
- Allows integration of high speed components into a single functional block as seen by the device designer
- Data and clock recovery from serial stream on the USB SuperSpeed bus
- Holding registers to stage transmit and receive data
- Supports direct disparity control for use in transmitting compliance pattern
- 8b/10b encode/decode and error indication
- Can not detect peripheral disconnection

The Innosilicon USB 3.0 PHY driver has two special features:

- The USB 2.0 PHY and USB 3.0 PHY operation functions are implemented at the same time (although the two PHYs are independent from the hardware), which is different from other USB 3.0 PHYs. In the driver, “U3PHY\_TYPE\_UTMI” and “U3PHY\_TYPE\_PIPE” are used as the indexes of USB 2.0 PHY and USB 3.0 PHY respectively. For details, please refer to the following functions in the driver code:

rockchip\_u3phy\_port\_init(): Initializes the USB 2.0 port and USB 3.0 port of USB 3.0.

rockchip\_u3phy\_power\_on(): Turn on the clock, and configure the USB 2.0 PHY to Normal mode, and configure the USB 3.0 PHY to enter the P0 state.

rockchip\_u3phy\_power\_off(): Configure the USB 2.0 PHY to suspend mode, configure the USB 3.0 PHY to enter P3 state, and turn off the clock to save the overall power consumption of the PHY.

- In order to solve the USB 3.0 PHY cannot detect the disconnection status of the peripheral, a special function has been added, which is different from other USB 3.0 PHYs. For details, please refer to the following functions in the driver:

rockchip\_u3phy\_on\_disconnect(): When the USB HUB core driver determines that the peripheral has been disconnected by detecting changes in the state of the linkstate, it will call the disconnect function through the notifier registered by the PHY to complete a series of soft disconnect operations.

rockchip\_u3phy\_on\_shutdown(): This function is provided to the DWC3 controller driver call, and its role is to reset the USB3 PHY during the soft disconnect process.

rockchip\_u3phy\_on\_init(): This function is provided to the DWC3 controller driver call. Its role is to release the reset signal of the USB 3.0 PHY at the end of the soft disconnect process;

The Innosilicon USB 3.0 PHY supports software commands to force the PHY to work only in USB 2.0 only mode:

- Command to configure USB 3.0 PHY to USB 2.0 only mode

```
echo u2> /sys/kernel/debug/[phy_name]/u3phy_mode
```

- Command to configure USB 3.0 PHY to support both USB 3.0 and USB 2.0 mode (default after driver initialization)

```
echo u3> /sys/kernel/debug/[phy_name]/u3phy_mode
```

Note: [phy name] needs to be modified to the specific PHY node name corresponding to the SoC.

### 3. Innosilicom USB 3.0 CombPhy Driver

- **Innosilicon USB 3.0 CombPhy driver code**

```
drivers/phy/rockchip/phy-rockchip-inno-combphy.c
```

- **Innosilicon USB 3.0 CombPhy driver example**

Example (RK1808 USB 3.0 combphy)

RK1808 USB 3.0 combphy is a combination of USB 3.0 SuperSpeed PHY and PCIe PHY, and the USB 3.0 PHY and PCIe PHY can't work at the same time. In the driver, PHY interface function rockchip\_combphy\_xlate() is registered and provided to USB 3.0 controller driver and PCIe driver to configure the USB 3.0 CombPHY to work at the type required by the controller.

If you are using USB 3.0, configure the USB 3.0 controller DTS's phys attribute to

```
1 phys = <&u2phy_otg>, <&combphy PHY_TYPE_USB3>;
2 phy-names = "usb2-phy", "usb3-phy";
3
```

If you are using PCIe, configure the PCIe controller DTS's phys attribute to

```

1 | phys = <&combphy PHY_TYPE_PCIE>;
2 | phy-names = "pcie-phy";
3 |

```

For USB 3.0 PHY, it only supports SuperSpeed, and it works with USB 2.0 PHY OTG port to comprise as fully feature USB 3.0/2.0/1.1/1.0.

Some key features of the USB3.0 CombPhy are:

- Supports 5.0Gb/s serial data transmission rate
- Utilizes 8-bit, 16-bit or 32-bit parallel interface to transmit and receive USB SuperSpeed data
- Allows integration of high speed components into a single functional block as seen by the device designer
- Data and clock recovery from serial stream on the USB SuperSpeed bus
- Holding registers to stage transmit and receive data
- Supports direct disparity control for use in transmitting compliance pattern
- 8b/10b encode/decode and error indication

Important USB 3.0 PHY and PCIe PHY multiplex phy\_ops:

- rockchip\_combphy\_init: prepare PHY reference clock, set PHY type and init PHY registers
- rockchip\_combphy\_exit: unprepare PHY reference clock
- rockchip\_combphy\_power\_on: used for USB 3.0 controller to power on USB 3.0 PHY block
- rockchip\_combphy\_power\_off: used for USB 3.0 controller to power off USB 3.0 PHY block to save power

Other important functions for USB 3.0:

- rk1808\_combphy\_low\_power\_control: used for lower power control for USB 3.0 PHY when system enter deepsleep
- u3phy\_mode\_store/u3phy\_mode\_show: used to force USB 3.0 to works on USB 2.0 only via **"u3phy\_mode"** in sysfs.

It needs to reinit the xHCI when switch between USB 2.0 only and USB 2.0/3.0 mode dynamically. In order to reinit the xHCI, we use the **"otg\_mode"** node in sysfs to remove/add xHCI HCD.

```

1 | 1. Default is USB 3.0 OTG mode, config to USB 2.0 only mode
2 |   echo u2 > /sys/devices/platform/[u3phy dev name]/u3phy_mode
3 |   echo host > /sys/devices/platform/[u2phy dev name]/otg_mode
4 |
5 | 2. Default is USB 3.0 Host mode, config to USB 2.0 only mode
6 |   echo otg > /sys/devices/platform/[u2phy dev name]/otg_mode
7 |   echo u2 > /sys/devices/platform/[u3phy dev name]/u3phy_mode
8 |   echo host > /sys/devices/platform/[u2phy dev name]/otg_mode
9 |
10 | 3. Default is USB 2.0 only Host mode, config to USB 3.0 mode
11 |   echo otg > /sys/devices/platform/[u2phy dev name]/otg_mode
12 |   echo u3 > /sys/devices/platform/[u3phy dev name]/u3phy_mode
13 |   echo host > /sys/devices/platform/[u2phy dev name]/otg_mode

```

Note:

- [u3phy dev name] and [u2phy dev name] need to be modified to the specific PHY node names corresponding to the SoC;
- USB's default mode, which is determined by the attribute "dr\_mode" in the DTS of the DWC3 controller;

## 5.3 USB Controller Drivers

## 5.3.1 USB 2.0 OTG Driver

### 5.3.1.1 USB 2.0 OTG Driver Framework

The USB 2.0 OTG uses a DWC2 controller. The system-level block diagram is shown in Figure 5-2 below. The DWC2 controller has both AHB master interface and AHB slave interface. This is because that the DWC2 controller has internal DMA to move data between USB FIFO and Memory via the AHB bus. At the same time, please note that the green box in the figure is hardware IP optional function. The DWC2 controller of the Rockchip SoC does not support external DMA function and endp\_multi\_proc\_interrupt. The interface protocol for communication with the USB PHY is UTMI+.

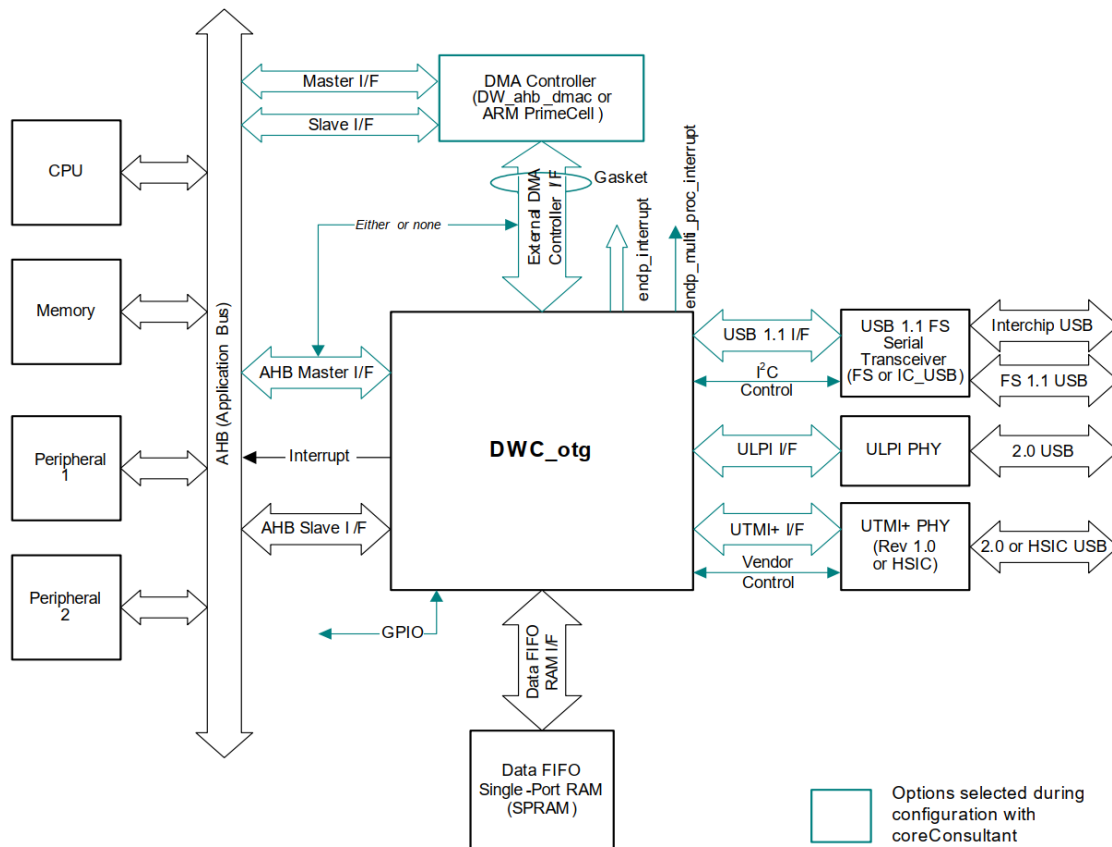


Figure 5-2 DWC2 controller system-level block diagram

Figure 5-3 below illustrates the interrupt handling hierarchy of the DWC2 controller. From the figure, it can be seen that DWC2 supports device interrupt/host interrupt/OTG interrupt. These three types of interrupts also include sub-interrupts. All interrupts are connected to the chip's interrupt processing module through a total interrupt signal.



[illegible]

```

4 | └─ core_intr.c (dwc2 general interrupt events, including otg intr, id intr,
   | wakeup intr, etc.)
5 | └─ debugfs.c (dwc2 debug interface, such as printing register information)
6 | └─ debug.h
7 | └─ gadget.c (all tasks related to dwc2 gadget mode, such as gadget
   | initialization, gadget interrupt event)
8 | └─ hcd.c (dwc2 host mode related tasks and core init, phy init, device/host
   | mode switching)
9 | └─ hcd_ddma.c (dwc2 descriptor DMA related tasks)
10 | └─ hcd.h
11 | └─ hcd_intr.c (handling of all interrupt events in dwc2 host mode)
12 | └─ hcd_queue.c (dwc2 host mode transmission queue processing)
13 | └─ hw.h
14 | └─ Kconfig
15 | └─ Makefile
16 | └─ pci.c (initialization of pci bus interface, Rockchip dwc2 uses AHB bus)
17 | └─ platform.c (implement dwc2 probe, initialize dwc2 lowlevel hw resources
   | according to core_params configuration of different chips)

```

### 5.3.1.3 USB 2.0 OTG Debug Interface

- DWC2 Driver Debug Interface

Example (RK3328 SoC):

```

1 | rk3328_box:/sys/kernel/debug/ff580000.usb # ls
2 | ep0    ep2out ep4out ep6out ep8in  ep9in  fifo    state
3 | eplin  ep3in  ep5in  ep7in  ep8out ep9out regdump testmode
4 |

```

**ep\*in/out:** Shows the state of the given endpoint (one is registered for each available).

**fifo:** Show the FIFO information for the overall fifo and all the periodic transmission FIFOs.

**state:** shows the overall state of the hardware and some general information about each of the endpoints available to the system.

**regdump:** Gets register values of core.

**testmode:** Modify the current usb test mode.

- DWC\_OTG\_310 Driver Debug Interface

Example (RK3288 SoC):

```

1 | rk3288:/sys/devices/platform/ff580000.usb # ls
2 | busconnected  fr_interval gsnpsid  modalias      regoffset     uevent
3 | buspower      gadget      guid      mode          regvalue      usb5
4 | bussuspend    ggpio      gusbcfg   mode_ch_tim_en remote_wakeup wr_reg_test
5 | devspeed      gnptxfsiz  hcd_frrem pools         spramdum
6 | disconnect_us gotgctl    hcddump   power         subsystem
7 | driver        gpvndctl   hp0       rd_reg_test   test_sq
8 | enumspeed     grxfsize   hptxfsize regdump       udc
9 |
10 | rk3328_box:/sys/devices/platform/ff580000.usb/driver # ls
11 | bind          dwc_otg_conn_en force_usb_mode uevent vbus_status
12 | debuglevel    ff580000.usb op_state      unbind versio
13 |

```

**busconnected:** Gets or sets the Core Control Status Register.

**fr\_interval:** On read, shows the value of HFIR Frame Interval. On write, dynamically reload HFIR register during runtime. The application can write a value to this register only after the Port Enable bit of the Host Port Control and Status register (HPRT.PrtEnaPort) has been set.

**gsnpsid:** Gets the value of the Synopsys ID Register.

**regoffset:** Sets the register offset for the next Register Access.

**buspower:** Gets or sets the Power State of the bus (0 - Off or 1 - On).

**guid:** Gets or sets the value of the User ID Register.

**regvalue:** Gets or sets the value of the register at the offset in the regoffset attribute.

**bussuspend:** Suspends the USB bus.

**ggpio:** Gets the value in the lower 16-bits of the General Purpose IO Register or sets the upper 16 bits.

**gusbcfg:** Gets or sets the Core USB Configuration Register.

**mode\_ch\_tim\_en:** This bit is used to enable or disable the host core to wait for 200 PHY clock cycles at the end of Resume to change the opmode signal to the PHY to 00 after Suspend or LPM.

**remote\_wakeup:** On read, shows the status of Remote Wakeup. On write, initiates a remote wakeup of the host. When bit 0 is 1 and Remote Wakeup is enabled, the Remote Wakeup signalling bit in the Device Control Register is set for 1 milli-second.

**wr\_reg\_test:** Displays the time required to write the GNPTXFSIZ register many times (the output shows the number of times the register is written).

**devspeed:** Gets or sets the device speed setting in the DCFG register.

**gnptxsiz:** Gets or sets the non-periodic Transmit Size Register.

**spramdmp:** Dumps the contents of core registers.

**disconnect\_us:** On read, shows the status of disconnect\_device\_us. On write, sets disconnect\_us which causes soft disconnect for 100us. Applicable only for device mode of operation.

**gotgctl:** Gets or sets the Core Control Status Register.

**hcddmp:** Dumps the current HCD state.

**gpvndctl:** Gets or sets the PHY Vendor Control Register.

**hprt0:** Gets or sets the value in the Host Port Control and Status Register.

**rd\_reg\_test:** Displays the time required to read the GNPTXFSIZ register many times (the output shows the number of times the register is read).

**test\_sq:** Gets or sets the usage of usb controller test\_sq attribute.

**enumspeed:** Gets the device enumeration Speed.

**grxsiz:** Gets or sets the Receive FIFO Size Register.

**hptxsiz:** Gets the value of the Host Periodic Transmit FIFO.

**regdmp:** Dumps the contents of core registers.

**dwc\_otg\_conn\_en:** Enable or disable connect to PC in device mode.

**force\_usb\_mode:** Force work mode of core (0 - Normal, 1 - Host, 2 - Device).

**vbus\_status:** Gets the Voltage of VBUS.

**debuglevel:** Gets or sets the driver Debug Level.

**op\_state:** Gets or sets the operational State, during transactions (a\_host>>a\_peripheral and b\_device=>b\_host) this may not match the core but allows the software to determine transitions.

**version:** Gets the Driver Version.

## 5.3.2 USB 2.0 Host Driver

### 5.3.2.1 USB 2.0 Host Controller framework

The USB 2.0 Host controller is composed of a USB 2.0 EHCI controller and a USB 1.1 OHCI controller. The green box in Figure 5-4 is the hardware IP optional function. The USB 2.0 Host controller of the Rockchip SoC is configured as an EHCI controller and an OHCI controller, and communicate with the USB PHY by UTMI + interface. Both EHCI and OHCI use internal DMA to access system memory via the AHB bus. EHCI is responsible for handling HighSpeed transmission transactions, and OHCI is responsible for handling FullSpeed and LowSpeed transmission transactions.

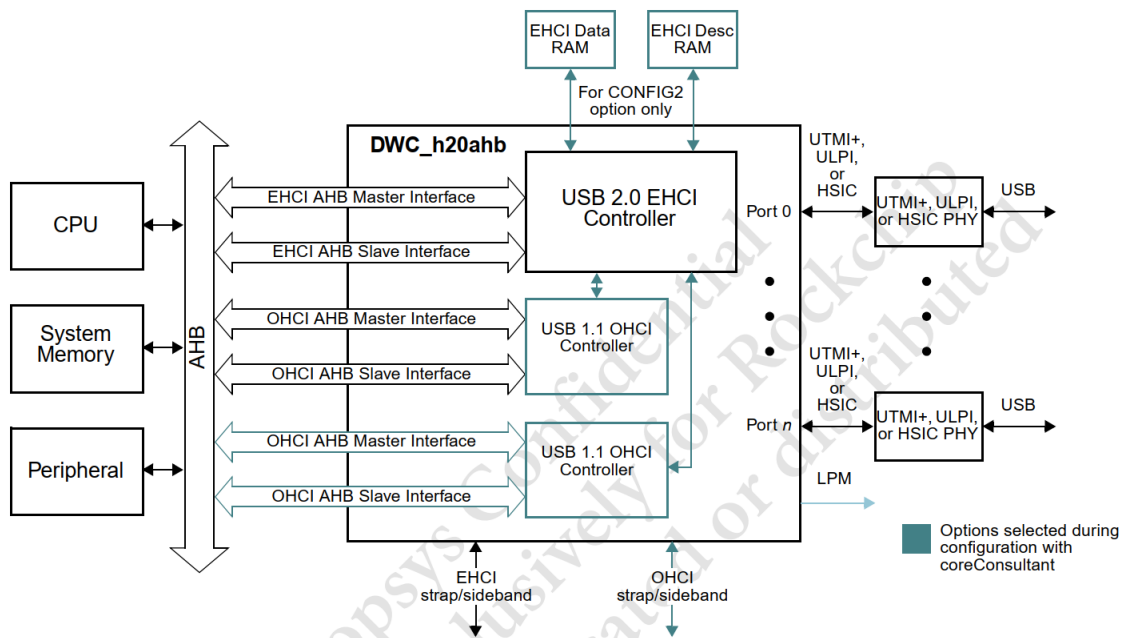


Figure 5-4 EHCI & OHCI controller system-level block diagram

### 5.3.2.2 USB 2.0 Host Driver Overview

#### 1. USB 2.0 Host driver code

`drivers/usb/host/ehci*` (USB 2.0 Host Driver)

`drivers/usb/host/ohci*` (USB 1.1/1.0 Host Driver)

#### 2. USB 2.0 Host driver code structure description

The ehci driver code structure is as follows:

Other ehci driver files not listed are platform ehci drivers implemented by different Vendors, such as ehci-exynos.c. Rockchip's EHCI controller design conforms to the standard EHCI controller specifications, so the general platform ehci driver "ehci-platform.c" is used.

```

1  ~/src/android_Q/kernel/drivers/usb/host$ tree
2  └─ ehci-dbg.c (ehci debugfs debugging interface, such as printing ehci
   register information)
3  └─ ehci.h
4  └─ ehci-hcd.c (Initialization of ehci controller, interrupt event
   processing, urb queue management, etc.)
5  └─ ehci-hub.c (control and status query of ehci root hub, bus
   suspend/resume)
6  └─ ehci-mem.c (allocation and initialization of ehci mem, allocation and
   initialization of qtd/qh resources)
7  └─ ehci-pci.c (Initialization of pci bus interface, Rockchip ehci uses AHB
   bus, does not use this driver)
8  └─ ehci-platform.c (ehci universal platform driver, implement ehci probe,
   register ehci hcd with usb bus, enable ehci controller)
9  └─ ehci-q.c (processing of ehci qtd/qh transmission queue)
10 └─ ehci-sched.c (cyclic transmission scheduling processing of ehci
   interrupt, iso, split iso)
11 └─ ehci-sysfs.c (ehci sysfs debugging interface, display companion
   controller, display uframe_periodic_max)
12 └─ ehci-timer.c (task processing related to ehci timer)

```

#### Important EHCI Structure:

```

1  static const struct hc_driver ehci_hc_driver = {
2      .description =      hcd_name,
3      .product_desc =     "EHCI Host Controller",
4      .hcd_priv_size =    sizeof(struct ehci_hcd),
5      /*
6       * generic hardware linkage
7       */
8      .irq =              ehci_irq,
9      .flags =             HCD_MEMORY | HCD_USB2 | HCD_BH,
10     /*
11      * basic lifecycle operations
12      */
13     .reset =              ehci_setup,
14     .start =              ehci_run,
15     .stop =               ehci_stop,
16     .shutdown =           ehci_shutdown,
17     /*
18      * managing i/o requests and associated device resources
19      */
20     .urb_enqueue =        ehci_urb_enqueue,
21     .urb_dequeue =        ehci_urb_dequeue,
22     .endpoint_disable =   ehci_endpoint_disable,
23     .endpoint_reset =     ehci_endpoint_reset,
24     .clear_tt_buffer_complete = ehci_clear_tt_buffer_complete,
25     /*
26      * scheduling support
27      */
28     .get_frame_number =   ehci_get_frame,
29     /*
30      * root hub support
31      */
32     .hub_status_data =    ehci_hub_status_data,
33     .hub_control =        ehci_hub_control,

```

```

34     .bus_suspend =      ehci_bus_suspend,
35     .bus_resume =      ehci_bus_resume,
36     .relinquish_port = ehci_relinquish_port,
37     .port_handed_over = ehci_port_handed_over,
38     /*
39      * device support
40      */
41     .free_dev =      ehci_remove_device,
42 };
43

```

The structure of ohci driver code is as follows:

Other ohci driver files not listed are platform ohci drivers implemented by different Vendors, such as ohci-exynos.c. The OHCI controller design of the Rockchip chip conforms to the standard OHCI controller specifications, so the general platform ohci driver "ohci-platform.c" is used.

```

1  ~/src/android_Q/kernel/drivers/usb/host$ tree
2  └─ ohci-dbg.c (ohci debugfs debugging interface, such as printing ohci
   register information)
3  └─ ohci.h
4  └─ ohci-hcd.c (initialization of ohci controller, interrupt event
   processing, urb queue management, etc.)
5  └─ ohci-hub.c (control and status query of ohci root hub, bus
   suspend/resume)
6  └─ ohci-mem.c (allocation and initialization of ohci mem, allocation and
   initialization of td/ed resources)
7  └─ ohci-pci.c (Initialization of pci bus interface, Rockchip ohci uses AHB
   bus, does not use this driver file)
8  └─ ohci-platform.c (ohci universal platform driver, implement ohci probe,
   register ohci hcd with usb bus, enable ohci controller)
9  └─ ohci-q.c (handling of ohci td/ed transmission queue)

```

Important OHCI Structures:

```

1  static const struct hc_driver ohci_hc_driver = {
2      .description =      hcd_name,
3      .product_desc =      "OHCI Host Controller",
4      .hcd_priv_size =      sizeof(struct ohci_hcd),
5      /*
6       * generic hardware linkage
7       */
8      .irq =      ohci_irq,
9      .flags =      HCD_MEMORY | HCD_USB11,
10     /*
11     * basic lifecycle operations
12     */
13     .reset =      ohci_setup,
14     .start =      ohci_start,
15     .stop =      ohci_stop,
16     .shutdown =      ohci_shutdown,
17     /*
18     * managing i/o requests and associated device resources
19     */
20     .urb_enqueue =      ohci_urb_enqueue,
21     .urb_dequeue =      ohci_urb_dequeue,

```

```

22     .endpoint_disable =      ohci_endpoint_disable,
23     /*
24     * scheduling support
25     */
26     .get_frame_number =      ohci_get_frame,
27     /*
28     * root hub support
29     */
30     .hub_status_data =       ohci_hub_status_data,
31     .hub_control =           ohci_hub_control,
32 #ifdef CONFIG_PM
33     .bus_suspend =           ohci_bus_suspend,
34     .bus_resume =            ohci_bus_resume,
35 #endif
36     .start_port_reset = ohci_start_port_reset,
37 };
38

```

### 5.3.2.3 USB 2.0 Host Debug Interface

Example (RK3399 USB 2.0 EHCI/OHCI)

- **EHCI Driver Debug Interface**

(Need to enable CONFIG\_DYNAMIC\_DEBUG)

```

1
2 rk3399_box:/sys/kernel/debug/usb/ehci/fe380000.usb # ls
3 async bandwidth periodic registers
4
5 rk3399:/sys/devices/platform/fe380000.usb # ls
6 companion driver_override of_node power uevent usb5
7 driver modalias pools subsystem uframe_periodic_max usbmon
8

```

**async:** Dump a snapshot of the Async Schedule.

**bandwidth:** Dump the HS Bandwidth Table.

**periodic:** Dump a snapshot of the Periodic Schedule.

**registers:** Dump Capability Registers, Interrupt Params and Operational Registers.

**companion:** Print EHCI's companion controller information

**uframe\_periodic\_max:** Displays the maximum usable microframe bandwidth for EHCI periodic transmission, the default is 100 (unit: microseconds), and the maximum can be configured to 125 microseconds

- **OHCI Driver Debug Interface**

(Need to enable CONFIG\_DYNAMIC\_DEBUG)

```

1 rk3399_box:/sys/kernel/debug/usb/ohci/fe3a0000.usb # ls
2 async periodic registers
3

```

**async:** Display Control and Bulk Lists together, for simplicity

**periodic:** Dump a snapshot of the Periodic Schedule (and load)

**registers:** Dump driver info, then registers in Spec order and other registers mostly affect Frame Timings

### 5.3.3 USB 3.0 OTG Driver

#### 5.3.3.1 USB 3.0 OTG Controller Framework

USB 3.0 OTG Controller is DWC3 Controller, as shown in Figure 5-5 below.

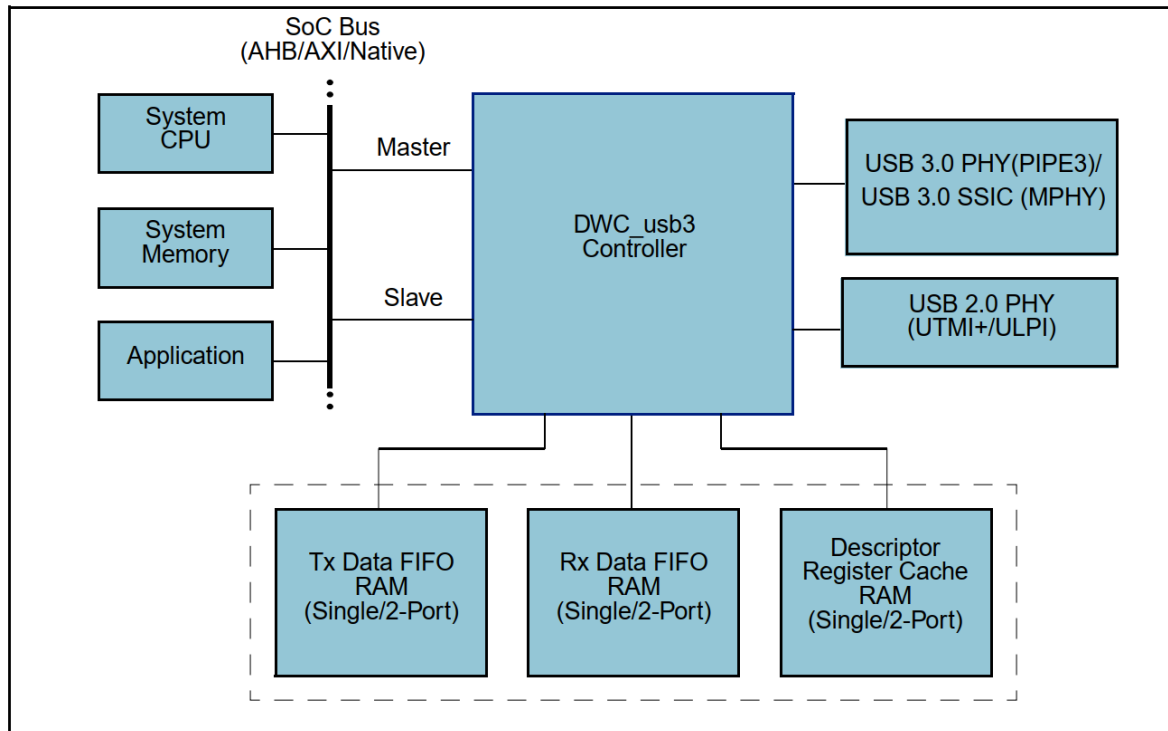


Figure 5-5 DWC3 controller system-level block diagram

USB 3.0 OTG Controller is Synopsys DesignWare Core USB 3.0 Controller integrated with xHCI USB 3.0 host controller. It can act as static host, static device, USB2.0/3.0 OTG A device or B device basing on the status of input ID from USB2.0 PHY or DFP/UFP/Data Role Swap defined in USB TypeC specification. It can perform data transmission between host and device as host or device for Super-Speed/High-Speed/Full-Speed/Low-Speed.

The characteristics of the USB3.0 controller are as follows:

- Support USB 3.0/2.0/1.1/1.0 protocol
- Integrated xHCI Host controller
- Only DRD mode (dual role) is supported, OTG mode is not supported
- Device and Host functions cannot be used at the same time
- The USB2.0 Port and USB3.0 Port of Host can be used independently at the same time
- Only DMA mode is supported, Slave mode is not supported
- Requires System Memory (Sram/Dram)
- xHCI is a standard USB3.0 Host controller, with the PC USB 3.0 interface. And, it can support Force USB2.0 only mode.

#### 5.3.3.2 USB 3.0 OTG Driver Overview

1. **USB 3.0 OTG driver code** `drivers/usb/dwc3/*` (USB 3.0 OTG Global core and Peripheral driver) `drivers/usb/host/xhci*` (USB 3.0 Host driver)
2. **USB 3.0 OTG driver code structure description**

Linux-4.19 USB DWC3 controller driver has been greatly upgraded compared to Linux-4.4, but the code file structure remains basically the same. The differences are mainly reflected in:

- Linux-4.19 added `drd.c` driver file for dynamic switching of dual role mode;



- Linux-4.19 deletes the **dwc3-rockchip.c** file and uses the generic driver **dwc3-of-simple.c** instead;
- Linux-4.19 still retains **dwc3-rockchip-inno.c**, which is dedicated to RK3328/RK3228H chip;

Linux-4.19 DWC3 and xHCI driver code structure is as follows:

```

1  ~/src/kernel-4.19/drivers/usb/dwc3$ tree .
2  ├── core.c (implementation of dwc3 core probe, allocate various resources,
   │  initialize controller, PM runtime management)
3  ├── core.h
4  ├── debugfs.c (implementation of dwc3 debugfs debug interface)
5  ├── debug.h
6  ├── drd.c (dwc3 drd/otg mode dynamic switching processing)
7  ├── dwc3-of-simple.c (dwc3 universal platform driver, realize the first
   │  level dwc3_of_simple_probe of dwc3, and call the second level dwc3_probe of
   │  dwc3 core through of_platform_populate)
8  ├── dwc3-pci.c (Initialization of pci bus interface, Rockchip dwc3 uses AXI
   │  bus, does not use this driver file)
9  ├── dwc3-rockchip-inno.c (glue layer for RK3328/RK3228H, increase the
   │  realization of disconnect work)
10 ├── ep0.c (task processing of dwc3 gadget ep0)
11 ├── gadget.c (dwc3 gadget endpoint task processing except ep0, interrupt
   │  entry function implementation)
12 ├── gadget.h
13 ├── host.c (dwc3 host resource allocation, and call xhci_plat_probe of xHCI
   │  through platform_device_add)
14 ├── io.h
15 ├── Kconfig
16 ├── Makefile
17 ├── trace.c (Dwc3 trace implementation, Linux-based trace interface)
18 ├── trace.h
19 └── ulpi.c (code implementation of ulpi phy interface, Rockchip dwc3 does
   │  not use ulpi)
20
21 ~/src/kernel-4.19/drivers/usb/host$ tree
22 ├── xhci.c (initialize xhci_hc_driver, start xHCI controller, manage urb
   │  queue, etc.)
23 ├── xhci-dbg.c (realize debug function for printing log)
24 ├── xhci-dbgcap.c (xHCI hardware module debug capability function is not
   │  supported by Rockchip)
25 ├── xhci-dbgcap.h
26 ├── xhci-debugfs.c (xHCI debugfs debugging interface)
27 ├── xhci-debugfs.h
28 ├── xhci-ext-caps.c (xHCI extended capability function implementation, not
   │  supported by Rockchip)
29 ├── xhci-ext-caps.h
30 ├── xhci.h
31 ├── xhci-hub.c (xHCI root hub control and status query, bus suspend/resume)
32 ├── xhci-mem.c (xHCI mem management, including allocation, initialization,
   │  release and other operations)
33 ├── xhci-pci.c (Initialization of pci bus interface, Rockchip xHCI uses AXI
   │  bus, does not use this driver file)
34 ├── xhci-plat.c (xHCI universal platform driver, implement xhci_plat_probe,
   │  Rockchip uses this driver)
35 ├── xhci-plat.h
36 ├── xhci-ring.c (management of xHCI transfer/command/event ring)
37 ├── xhci-trace.c (xHCI trace implementation, Linux-based trace interface)
38 └── xhci-trace.h

```

### Important Gadget Structure:

```
1
2 static const struct usb_gadget_ops dwc3_gadget_ops = {
3     .get_frame      = dwc3_gadget_get_frame,
4     .wakeup         = dwc3_gadget_wakeup,
5     .set_selfpowered = dwc3_gadget_set_selfpowered,
6     .pullup         = dwc3_gadget_pullup,
7     .udc_start      = dwc3_gadget_start,
8     .udc_stop       = dwc3_gadget_stop,
9 };
10
```

### Important Host Structure:

```
1
2 static const struct hc_driver xhci_hc_driver = {
3     .description = "xhci-hcd",
4     .product_desc = "xHCI Host Controller",
5     .hcd_priv_size = sizeof(struct xhci_hcd *),
6     /*
7      * generic hardware linkage
8      */
9     .irq = xhci_irq,
10    .flags = HCD_MEMORY | HCD_USB3 | HCD_SHARED,
11    /*
12     * basic lifecycle operations
13     */
14    .reset = NULL, /* set in xhci_init_driver() */
15    .start = xhci_run,
16    .stop = xhci_stop,
17    .shutdown = xhci_shutdown,
18    /*
19     * managing i/o requests and associated device resources
20     */
21    .urb_enqueue = xhci_urb_enqueue,
22    .urb_dequeue = xhci_urb_dequeue,
23    .alloc_dev = xhci_alloc_dev,
24    .free_dev = xhci_free_dev,
25    .alloc_streams = xhci_alloc_streams,
26    .free_streams = xhci_free_streams,
27    .add_endpoint = xhci_add_endpoint,
28    .drop_endpoint = xhci_drop_endpoint,
29    .endpoint_reset = xhci_endpoint_reset,
30    .check_bandwidth = xhci_check_bandwidth,
31    .reset_bandwidth = xhci_reset_bandwidth,
32    .address_device = xhci_address_device,
33    .enable_device = xhci_enable_device,
34    .update_hub_device = xhci_update_hub_device,
35    .reset_device = xhci_discover_or_reset_device,
36    /*
37     * scheduling support
38     */
39    .get_frame_number = xhci_get_frame,
40    /*
41     * root hub support
42     */
43 }
```

```

43     .hub_control =      xhci_hub_control,
44     .hub_status_data = xhci_hub_status_data,
45     .bus_suspend =     xhci_bus_suspend,
46     .bus_resume =      xhci_bus_resume,
47     /*
48      * call back when device connected and addressed
49      */
50     .update_device =    xhci_update_device,
51     .set_usb2_hw_lpm =  xhci_set_usb2_hardware_lpm,
52     .enable_usb3_lpm_timeout = xhci_enable_usb3_lpm_timeout,
53     .disable_usb3_lpm_timeout = xhci_disable_usb3_lpm_timeout,
54     .find_raw_port_number = xhci_find_raw_port_number,
55 };
56

```

### 5.3.3.3 USB 3.0 OTG Debug Interface

Example (Linux-4.19 RK3399 USB 3.0 OTG0)

```

1
2 console:/sys/kernel/debug/fe800000.dwc3 # ls
3 ep0in ep1in ep2in ep3in ep4in ep5in ep6out lsp_dump regdump
4 ep0out ep1out ep2out ep3out ep4out ep5out link_state mode testmode
5
6 console:/sys/kernel/debug/fe800000.dwc3/ep0in # ls
7 descriptor_fetch_queue rx_info_queue trb_ring
8 event_queue rx_request_queue tx_fifo_queue
9 rx_fifo_queue transfer_type tx_request_queue
10
11 console:/sys/kernel/debug/usb/xhci/xhci-hcd.0.auto # ls
12 command-ring ports reg-ext-legsup:00 reg-op
13 devices reg-cap reg-ext-protocol:00 reg-runtime
14 event-ring reg-ext-dbc:00 reg-ext-protocol:01
15

```

Common debugging nodes:

**mode:** dr\_mode read or store

**testmode:** Set DWC3 to enter HighSpeed test mode for eye diagram test

**link\_state:** Link state read or store

**regdump:** Dump registers of DWC3

**ep\*in/out:** Directory of EP debug files

**descriptor\_fetch\_queue:** Dump the available DescFetchQ space of EP

**rx\_info\_queue:** Dump the available RXInfoQ space of EP

**trb\_ring:** Dump the TRB pool of EP

**event\_queue:** Dump the available EventQ space of EP

**rx\_request\_queue:** Dump the available RxReqQ space of EP

**tx\_fifo\_queue:** Dump the available TxFIFO space of EP

**rx\_fifo\_queue:** Dump the available RxFIFO space of EP

**transfer\_type:** Print the Transfer Type of EP

**tx\_request\_queue:** Dump the available TxReqQ space of EP

**command-ring:** Print the status information of xHCI command ring

**event-ring:** Print the status information of xHCI event ring

**reg-op:** Print xHCI register status information

- **USB 3.0 OTG tracepoint**

```
sys/kernel/debug/tracing/events/xhci-hcd sys/kernel/debug/tracing/events/dwc3
```

For more details, please refer to:

```
sys/kernel/debug/tracing/README
```

- **USB 3.0 OTG switch command**

Function: Through software method, force OTG to work in Host mode or Device mode without being affected by USB hardware circuit.

#### **Linux-4.4 USB 3.0 OTG switch command**

Linux-4.4 old command (only used for RK3399):

```
1 RK3399 Type-C0 USB OTG switch command
2 1.Force host mode
3   echo host > sys/kernel/debug/usb@fe800000/rk_usb_force_mode
4 2.Force peripheral mode
5   echo peripheral > sys/kernel/debug/usb@fe800000/rk_usb_force_mode
6
```

Linux-4.4 new command (only used for RK3399/RK1808):

```
1 RK3399 Type-C0 USB OTG switch command
2 1.Force host mode
3   echo host > sys/devices/platform/usb0/dwc3_mode
4 2.Force peripheral mode
5   echo peripheral > sys/devices/platform/usb0/dwc3_mode
6
7 RK1808 USB OTG switch command
8 1.Force host mode
9   echo host > sys/devices/platform/usb/dwc3_mode
10 2.Force peripheral mode
11   echo peripheral > sys/devices/platform/usb/dwc3_mode
12
```

#### **Linux-4.19 USB 3.0 OTG switch command** (used for all SoCs with DWC3 Controller)

```
1 RK3399 Type-C0 USB OTG switch command
2 1.Force host mode
3     echo host > sys/devices/platform/ff770000.syscon/ff770000.syscon:usb2-
phy@e450/otg_mode
4 2.Force peripheral mode
5     echo peripheral >
sys/devices/platform/ff770000.syscon/ff770000.syscon:usb2-phy@e450/otg_mode
6
7 For other SoCs, the method is similar, just search for the otg_mode node
under the sys/devices/platform path, and then set the node.
8
```

---

# 6 Android USB Gadget Configuration

## 6.1 USB Gadget Configfs Framework

Since Linux-3.11, USB Gadgets have been configured in the framework of Configfs, and the android.c file in the Gadget directory has been deleted from the kernel. Device class drivers that support the Configfs framework are moved to the directory `drivers/usb/gadget/function`.

For instructions on how to use Android ConfigFS Gadgets, please refer to:

```
1 | Documentation/ABI/testing/configfs-usb-gadget-xxxx.txt
2 | Documentation/filesystems/configfs/configfs.txt
3 | Documentation/usb/gadget_configfs.txt
4 | Documentation/usb/gadget-testing.txt
```

[Kernel USB Gadget Configfs Interface](#)

[TIZEN USB](#)

<https://wiki.linaro.org/LMG/Kernel/AndroidConfigFSGadgets>

## 6.2 USB Gadget Configuration File

USB-related scripts in Android include:

```
1 |
2 | init.usb.rc
3 | init.usb.configfs.rc
4 | init.rk30board.usb.rc
5 | fstab.rk30board.bootmode.emmc
6 |
```

1. init.usb.rc: Android standard RC files, no need change.
2. fstab.rk30board.bootmode.emmc: Android fstab file, it can be used to configure the mount paths of sdcard and usb storage. On Rockchip platform, the Vold can use wildcard to search and match USB mount paths automatically.

```
1 |
2 | # for USB 2.0
3 | /devices/platform/*.usb*          auto vfat defaults      voldmanaged=usb:auto
4 | # for USB 3.0
5 | /devices/platform/usb@*/*.dwc3*   auto vfat defaults
6 | voldmanaged=usb:auto
7 |
```

3. init.rk30board.usb.rc and init.usb.configfs.rc: used for usb functions configuration.

```
1 |
2 | on boot
3 |     mkdir /dev/usb-ffs 0770 shell shell
4 |     mkdir /dev/usb-ffs/adb 0770 shell shell
5 |     mount configfs none /config
6 |     mkdir /config/usb_gadget/g1 0770 shell shell
7 |     write /config/usb_gadget/g1/idVendor 0x2207
```

```

8     write /config/usb_gadget/g1/bcdDevice 0x0310
9     write /config/usb_gadget/g1/bcdUSB 0x0200
10    mkdir /config/usb_gadget/g1/strings/0x409 0770
11    write /config/usb_gadget/g1/strings/0x409/serialnumber ${ro.serialno}
12    write /config/usb_gadget/g1/strings/0x409/manufacturer
    ${ro.product.manufacturer}
13    write /config/usb_gadget/g1/strings/0x409/product ${ro.product.model}
14    mkdir /config/usb_gadget/g1/functions/accessory.gs2
15    mkdir /config/usb_gadget/g1/functions/audio_source.gs3
16    mkdir /config/usb_gadget/g1/functions/ffs.adb
17    mkdir /config/usb_gadget/g1/functions/mtp.gs0
18    mkdir /config/usb_gadget/g1/functions/ptp.gs1
19    mkdir /config/usb_gadget/g1/functions/rndis.gs4
20    write /config/usb_gadget/g1/functions/rndis.gs4/wceis 1
21    mkdir /config/usb_gadget/g1/functions/midi.gs5
22    mkdir /config/usb_gadget/g1/configs/b.1 0770 shell shell
23    mkdir /config/usb_gadget/g1/configs/b.1/strings/0x409 0770 shell shell
24    write /config/usb_gadget/g1/os_desc/b_vendor_code 0x1
25    write /config/usb_gadget/g1/os_desc/qw_sign "MSFT100"
26    write /config/usb_gadget/g1/configs/b.1/MaxPower 500
27    symlink /config/usb_gadget/g1/configs/b.1
    /config/usb_gadget/g1/os_desc/b.1
28    mount functionfs adb /dev/usb-ffs/adb uid=2000,gid=2000
29    setprop sys.usb.configfs 1
30    setprop sys.usb.controller "fe800000.dwc3"
31
32    on property:sys.usb.config=none && property:sys.usb.configfs=1
33        write /config/usb_gadget/g1/os_desc/use 0
34        setprop sys.usb.ffmpeg.ready 0
35
36    on property:init.svc.adbd=stopped
37        setprop sys.usb.ffmpeg.ready 0
38
39    on property:sys.usb.config=mtp && property:sys.usb.configfs=1
40        write
    /config/usb_gadget/g1/functions/mtp.gs0/os_desc/interface.MTP/compatible_id
    "MTP"
41        write /config/usb_gadget/g1/os_desc/use 1
42        write /config/usb_gadget/g1/idProduct 0x0001
43
44    on property:sys.usb.config=mtp,adb && property:sys.usb.configfs=1
45        write
    /config/usb_gadget/g1/functions/mtp.gs0/os_desc/interface.MTP/compatible_id
    "MTP"
46        write /config/usb_gadget/g1/os_desc/use 1
47        write /config/usb_gadget/g1/idProduct 0x0011
48

```

The three attributes of **serialnumber**, **manufacturer** and **product** are dynamically configured by the Android application layer. If the serialnumber is not configured successfully, it may cause ADB to be unusable.

"setprop sys.usb.controller" is used to enable the corresponding USB controller of Gadget. For RK3399, it has two OTG controllers, both of them can support the function of USB Gadget. But because the current architecture of USB Gadget Driver only supports one USB controller, it is necessary to configure the corresponding USB controller according to the actual product requirements, such as RK3399 Android SDK, which configures the Type-C0 as the USB Gadget function by default.

```
1 | setprop sys.usb.controller "fe800000.usb"
```

**Note:**

The Kernel USB Gadget Framework only supports one USB Gadget at the same time. And RK3399 supports two Type-C USB 3.0 OTG controllers (Type-C0 and Type-C1). If you want to use Type-C1 USB 3.0 as USB Gadget instead of Type-C0, simply change two configurations:

1. Use Type-C1 controller name "fe900000.usb" instead of "fe800000.usb" in init.rk30board.usb.rc.

```
1 | setprop sys.usb.controller "fe900000.usb"
```

2. set dr\_mode = "otg" in usbdrd\_dwc3\_1 node in DTS.

```
1 | &usbdrd_dwc3_1 {  
2 |     status = "okay";  
3 |     dr_mode = "otg"; /* Configure Type-C1 USB Controller to OTG mode  
4 |     */  
5 |     extcon = <&fusbl>; /* Note: extcon should be configured according  
6 |     to actual hardware */  
7 | };
```

## 6.3 USB VID And PID Configuration

USB VID and PID configuration need to follow the following principles:

- VID is fixed at 0x2207 (authorized by USB-IF)
- PID can be defined according to product requirements, but the upper 8 bits must be 0 to avoid conflicts with Maskrom/Loader USB PID
- VID and PID of accessory need to be configured as defined by Google
- USB-IF stipulates that VID is unique to each Vendor, and the same VID cannot be authorized for different Vendors

VID and PID commonly used in the Android platform are defined as follows:



USB Function	VID	PID
MTP	0x2207	0x0001
PTP	0x2207	0x0002
RNDIS	0x2207	0x0003
MIDI	0x2207	0x0004
UVC	0x2207	0x0005
ADB	0x2207	0x0006
MTP,ADB	0x2207	0x0011
PTP,ADB	0x2207	0x0012
RNDIS,ADB	0x2207	0x0013
MIDI,ADB	0x2207	0x0014
UVC,ADB	0x2207	0x0015
ACCESSORY	0x18d1	0x18d1
ACCESSORY,ADB	0x18d1	0x2d01

## 6.4 USB Gadget Debug Interface

- **Configfs Configure Interface**

The kernel provides device nodes to view key configuration information for USB Gadgets, as follows:

```

1 |
2 | root@rk3399:/config/usb_gadget/g1 # ls
3 | UDC          bDeviceProtocol bMaxPacketSize0 bcdUSB  functions idVendor
   | strings
4 | bDeviceClass bDeviceSubClass bcdDevice      configs idProduct os_desc
5 |
```

Refer to

```

1 | Documentation/usb/gadget_configfs.txt
```

In order to enable the gadget it must be bound to a UDC (USB Device Controller).

```

1 | echo <udc name> > UDC
2 | #where <udc name> is one of those found in /sys/class/udc/*
```

Example:

Bind Type-C0 USB Device Controller in RK3399 to UDC

```

1 | echo fe800000.dwc3 > config/usb_gadget/g1/UDC
```

Unbind USB Device Controller

```
1 | echo none > config/usb_gadget/g1/UDC
```

- **View USB Device Connection Status**

```
1 rk3399:/sys/class/udc/fe800000.dwc3 # ls
2 a_alt_hnp_support device is_selfpowered srp
3 a_hnp_support function maximum_speed state
4 b_hnp_enable is_a_peripheral power subsystem
5 current_speed is_otg soft_connect uevent
6
7 rk3399:/sys/class/android_usb/android0 # ls
8 f_audio_source f_midi power state subsystem uevent
```

---

# 7 USB Common Debug Methods And Commands

## 7.1 USB Common Debug Methods

### 1. Common USB Debug Instruments And Software Tools

- Multimeter: for simple voltage test, such as: USB VBUS, OTG\_ID and USB PHY power supply.
- High-bandwidth oscilloscope: used to measure the signal quality of the USB eye diagram, USB charging detection and handshake signals, USB VBUS voltage collapse, etc.
- USB protocol analyzer: Analyze the USB communication protocol flow, and locate whether it is a host problem or a device problem.
- Windows tools: BusHound software is used to grab USB bus packets; Usbview software is used to view detailed descriptor information of USB devices.
- Linux tools: usbmon is a tool for grabbing USB bus packets; vusb-analyzer graphical tool is used to parse the data captured by usbmon; lsusb command is used to view detailed descriptor information of USB devices.

For more information, please refer to the documentation:

`Documentation/usb/usbmon.txt`

[《USB Debugging and Profiling Techniques》](#)

### 2. Common USB Debug Interface

- Sysfs entry in host: `/sys/bus/usb/*` (view USB devices and drivers supported by the system)
- Debugfs entry in host:
  - `/sys/kernel/debug/usb/devices` (view all USB device information on the USB bus)
  - `/sys/kernel/debug/*.*dwc3` (DWC3 controller debug interface)
  - `/sys/kernel/debug/usb/usbmon` (USBMon packet capture tool)
  - `/sys/kernel/debug/usb/xhci` (xHCI controller debug interface)
  - `/sys/kernel/debug/usb/uvcdvideo` (UVC device debug interface)
- Debugfs for controllers: refer to [5.2.1.3 USB 2.0 OTG Debug Interface](#), [5.2.2.3 USB 2.0 Host Debug Interface](#), [5.3.1.3 USB 3.0 OTG Debug Interface](#)
- trace for usb gadget/dwc3/xHCI:
  - `/sys/kernel/debug/tracing/events/gadget` (trace Gadget Driver interacting with Device Controller Driver)
  - `/sys/kernel/debug/tracing/events/dwc3` (trace DWC3 controller transmission process)
  - `/sys/kernel/debug/tracing/events/xhci-hcd` (trace xHCI controller transmission process)
- Print usb host uvc log: `echo 0xffff>/sys/module/uvcdvideo/parameters/trace`
- Print usb devio driver log: `echo 1>/sys/module/usbcore/parameters/usbfs_snoop`

## 7.2 USB Common Commands

This chapter mainly describes the specific commands for Rockchip USB driver USB, including 2.0 OTG switch command, USB 3.0 OTG switch command, USB 3.0 force USB 2.0 only command and USB eye diagram test command.

- USB 2.0 OTG switch command

Function: Through software method, force USB 2.0 OTG to Host mode or Device mode without being affected by OTG ID level.

For the USB 2.0 OTG switch command, please refer to the description of the USB 2.0 PHY debug interface in [5.1.1 USB 2.0 PHY Driver Development](#).

- USB 3.0 OTG switch command

Function: Through software method, force USB 3.0 OTG to Host mode or Device mode without being affected by OTG ID level or Type-C interface.

For the USB 3.0 OTG switch command, please refer to the USB 3.0 OTG switch command description in [5.3.1.3 USB 3.0 OTG Debug Interface](#).

- USB 3.0 force USB 2.0 only command

Function: Force USB 3.0 Host controller and PHY to work in USB 2.0 only mode.

For USB 3.0 force USB 2.0 only command, please refer to [5.1.2 USB 3.0 PHY driver development](#)

- USB eye diagram test command

Function: Set the USB 3.0/2.0 controller to test mode.

For the USB eye diagram test command, please refer to the document

Rockchip\_Developer\_Guide\_USB\_SQ\_Test\_CN

---

## 8 Analysis of Common USB Questions

### 8.1 Device Enumeration Log

#### 8.1.1 USB 2.0 OTG Normal Boot Log

Default mode is device when booting without USB cable.

```
1
2 [ 8.764441]otg id chg last id -1 currentid 67108864
3 [ 8.764925] PortPower off
4 [ 8.866923] Using Buffer DMA mode
5 [ 8.867280] Periodic Transfer Interrupt Enhancement- disabled
6 [ 8.867787] Multiprocessor InterruptEnhancement - disabled
7 [ 8.868294] OTG VER PARAM: 0, OTG VER FLAG: 0
8 [ 8.868700] ^^^^^^^^^^^^^^^^^Device Mode
9
```

#### 8.1.2 USB 2.0 Device Normal Connection Log

```
1
2 [ 133.368479] ***vbusdetect*
3 [ 133.500590] Using Buffer DMA mode
4 [ 133.500886] Periodic Transfer InterruptEnhancement - disabled
5 [ 133.501391] Multiprocessor InterruptEnhancement - disabled
6 [ 133.501875] OTG VER PARAM: 0, OTG VER FLAG: 0
7 [ 133.502255] ^^^^^^^^^^^^^^^^^Device Mode
8 [ 133.502630] *****softconnect!!!*****
9 [ 133.618581] USB RESET
10 [ 133.710877] android_work: sent ueventUSB_STATE=CONNECTED
11 [ 133.714269] USB RESET
12 [ 133.947001] configfs-gadget gadget: high-speed config #1: b
13 [ 133.947649] android_work: sent ueventUSB_STATE=CONFIGURED
14 [ 133.995447] mtp_open
15
```

#### 8.1.3 USB 2.0 Device Disconnect Log

```
1
2 [ 187.085682] *****session end ,softdisconnect*****
3 [ 187.086486] android_work: sent ueventUSB_STATE=DISCONNECTED
4 [ 187.087217] mtp_release
5
```

#### 8.1.4 USB 2.0 Host Enumerate LS Device Log

```

1
2 [ 325.412454] usb 2-1: new low-speed USB device number 2 using ohci-platform
3 [ 325.619507] usb 2-1: New USB device found,idVendor=046d, idProduct=c077
4 [ 325.620116] usb 2-1: New USB device strings:Mfr=1, Product=2,
   SerialNumber=0
5 [ 325.620809] usb 2-1: Product: USB OpticalMouse
6 [ 325.621222] usb 2-1: Manufacturer: Logitech
7

```

### 8.1.5 USB 2.0 Host Enumerate FS Device Log

```

1
2 [ 370.896519] usb 2-1: new full-speed USB device number 3 using ohci-
platform
3 [ 371.109574] usb 2-1: New USB device found,idVendor=1915, idProduct=0199
4 [ 371.110183] usb 2-1: New USB device strings:Mfr=1, Product=2,
   SerialNumber=0
5 [ 371.110832] usb 2-1: Product: Memsartcontroller
6 [ 371.111251] usb 2-1: Manufacturer: Memsart
7 [ 371.123172] input: Memsart Memsart controlleras /
8

```

### 8.1.6 USB 2.0 Host Enumerate HS Device Log

```

1
2 [ 405.400521] usb 1-1: new high-speed USB device number 5 using ehci-
platform
3 [ 405.536569] usb 1-1: New USB device found,idVendor=0951, idProduct=1687
4 [ 405.537178] usb 1-1: New USB device strings:Mfr=1, Product=2,
   SerialNumber=3
5 [ 405.537815] usb 1-1: Product: DT R400
6 [ 405.538151] usb 1-1: Manufacturer: Kingston
7 [ 405.538533] usb 1-1: SerialNumber:0018F3D97D02BB91517E017D
8 [ 405.541111] usb-storage 1-1:1.0: USB MassStorage device detected
9 [ 405.542472] scsi host1: usb-storage 1-1:1.0
10 [ 406.584573] scsi 1:0:0:0: Direct-AccessKingston DT R400 PMAP PQ: 0 ANSI:
   0 CCS
11 [ 406.586425] sd 1:0:0:0: Attached scsi genericsg0 type 0
12 [ 408.171256] sd 1:0:0:0: [sda] 15646720512-byte logical blocks: (8.01
   GB/7.46 GiB)
13 [ 408.172788] sd 1:0:0:0: [sda] Write Protectis off
14 [ 408.173970] sd 1:0:0:0: [sda] No Caching modepage found
15 [ 408.174453] sd 1:0:0:0: [sda] Assuming drivecache: write through
16 [ 408.223001] sda: sda1
17 [ 408.229280] sd 1:0:0:0: [sda] Attached SCSIremovable disk
18

```

### 8.1.7 USB 2.0 Host-LS/FS/HS Device Disconnect Log

```

1 [ 443.151067] usb 1-1: USB disconnect, devicenumber 3

```

### 7.1.8 USB 3.0 Device Normal Connection Log

```

1
2 [ 72.310531] android_work: sent ueventUSB_STATE=CONNECTED
3 [ 72.689120] configfs-gadget gadget: super-speed config #1: b
4 [ 72.690110] android_work: sent ueventUSB_STATE=CONFIGURED
5 [ 72.767950] mtp_open
6

```

## 8.1.9 USB 3.0 Host Enumerate SS Device Log

```

1
2 [ 26.715320] usb 8-1: new SuperSpeed USB device number 2 using xhci-hcd
3 [ 26.732190] usb 8-1: New USB device found,idVendor=0bc2, idProduct=2320
4 [ 26.732812] usb 8-1: New USB device strings:Mfr=2, Product=3,
  SerialNumber=1
5 [ 26.733515] usb 8-1: Product: Expansion
6 [ 26.733885] usb 8-1: Manufacturer: Seagate
7 [ 26.734263] usb 8-1: SerialNumber: NA45HT1K
8 [ 26.738410] usb-storage 8-1:1.0: USB MassStorage device detected
9 [ 26.740446] scsi host0: usb-storage 8-1:1.0
10 [ 27.745028] scsi 0:0:0:0: Direct-Access      Seagate Expansion      0608
  PQ: 0 ANSI:6
11 [ 27.753066] sd 0:0:0:0: [sda] 1953525167512-byte logical blocks: (1.00
  TB/932 GiB)
12 [ 27.754245] sd 0:0:0:0: [sda] Write Protectis off
13 [ 27.754982] sd 0:0:0:0: Attached scsi genericsg0 type 0
14 [ 27.755281] sd 0:0:0:0: [sda] Write cache:enabled, read cache: enabled,
  doesn't support DPO or FUA
15 [ 27.783395] sda: sda1
16 [ 27.791561] sd 0:0:0:0: [sda] Attached SCSIdisk
17

```

## 8.2 Analysis of Common Questions

### 8.2.1 USB Hardware Circuit Problem

1. Use multimeter to measure the voltage of PHY power supply, VCC5V0\_OTG, USB\_DET, USB\_ID.
2. Measuring voltage ripple of PHY power supply with oscilloscope.
3. Test USB eye diagram with oscilloscope.

### 8.2.2 USB Device Problem

The phenomenon that the USB Device is normally connected to the PC mainly includes:

1. The serial port output normal log, see [8.1.2 USB 2.0 Device Normal Connection Log](#);
2. The drive letter appears on the PC, but it cannot be accessed by default; (Windows 7 and MAC OS may only appear in the device manager);
3. "USB connected" logo appears in the status bar of the device UI;
4. Open the prompt window of USB connected. The default is charger only mode. After selecting "MTP" or "PTP", the PC can access the drive letter.

**Issue-1:** When the USB is plug in, the PC does not respond, and no usb enumeration log.

First, make sure you have selected "MTP", "PTP" or "ADB" on device side. Second, check if USB controller has worked as Device mode via kernel debug interface. Third, check the USB hardware circuit and the USB D+/D- signals.

**Issue-2:** PC fails to recognize USB device, and dump the following log on device side:

```
1
2 [36.682587] DWC_OTG:
   *****softconnect!!!*****
3 [36.688603] DWC_OTG: USB SUSPEND
4 [36.807373] DWC_OTG: USB RESET
5
```

Maybe it's USB signal quality problem. Please test USB eye diagram and check the USB hardware circuit.

**Issue-3:** After connecting to PC, the kernel usb enumeration log is normal, but PC cannot access the device

USB driver is OK, maybe it's Android USB server issue. Need to dump android log to analysis this issue.

**Issue-4:** When the USB cable is unplugged, the UI status bar still shows "USB Connected", and dump the following log:

```
1 [25.330017] DWC_OTG: USB SUSPEND
```

Without the following log:

```
1 [25.514407] DWC_OTG: session end intr, softdisconnect
```

This issue is always caused by USB\_DET voltage abnormality. Use multimeter to measure the voltage of USB\_DET. Normally, the voltage is low (0V) when USB cable is unplugged. If the voltage is still high (~3V) after USB cable is unplugged, it will cause the disconnection issue.

### 8.2.3 USB Host Problem

**Issue-1:** No USB enumeration log when USB device plug into the USB Host port.

First, use multimeter to measure the voltage of VBUS, normally, the voltage of VBUS must be 5V. Second, check if the Kernel USB driver has support USB Host driver and the USB Class driver. Refer to [3 Kernel USB CONFIG](#)

**Issue-2:** USB Disk cannot be mounted

First, check if the Kernel has identified the partition information of the U disk. Second, check whether the mount patch in the fstab script is correct.

**Issue-3:** urb transfer\_buffer address not align

```
1
2 DWC_OTG:dwc_otg_hcd_urb_enqueue urb->transfer_buffer address not align to 4-
  byte0xd6eab00a
3 DWC_OTG:dwc_otg_hcd_urb_enqueue urb->transfer_buffer address not align to 4-
  byte0xccf6140a
4
```

The dwc2 otg driver requires the transfer buffer address of urb must be 4 bytes aligned. Generally, the buffer address of urb is allocated in USB class drivers, so try to fix this issue in corresponding USB class driver.

### 8.2.4 USB Camera Problem

1. USB camera cannot be turned on



First, check whether there is a camera device node video0 or Video1 in the /dev directory. If not, check whether the kernel is configured correctly. If there are nodes, make sure that USB camera is inserted before the system boots, because Rockchip SDK doesn't support USB camera hot-plug by default. If you want to support USB Camera hot plug-in, please contact the Engineer in charge of Camera to support you. The USB driver doesn't need to be modified.

## 2. Image jitter, no image and abnormal exit of camera application

It may be caused by frame loss of USB driver. You need to use USB analyzer to analyze the actual USB communication data.

## 8.2.5 USB Charge Detection

USB 2.0 PHY supports charging detection of BC1.2 standard. It can detect four charging types: SDP/CDP/standard DCP (D+/D-short connection) and non-standard DCP (D+/D-not short connection).

Refer to `drivers/phy/rockchip/phy-rockchip-inno-usb2.c`

SDP: Standard Downstream Port

According to the USB 2.0 specification, when a USB peripheral is in an un-connected or suspend state, a Standard Downstream Port can provide an average current of no more than 2.5mA to the peripheral; when the peripheral is connected and not sleeping, the current can reach a maximum of 100mA (USB 3.0 150mA); and when the peripheral is configured and not sleeping, the maximum current can be 500 mA (USB 3.0 900 mA).

CDP: Charging Downstream Port

It is compatible with the USB 2.0 specification and optimized downlink USB interface for USB charging. It provides the maximum 1.5A power supply current to meet the needs of high current fast charging.

DCP: Dedicated Charging Port (USB Charger)

BC1.2 spec requires D + and D - in USB Charger to be short connected to match the recognition action of USB peripherals, but it does not have the ability to communicate with USB devices.

The USB charging type detection process is shown in the following figure:

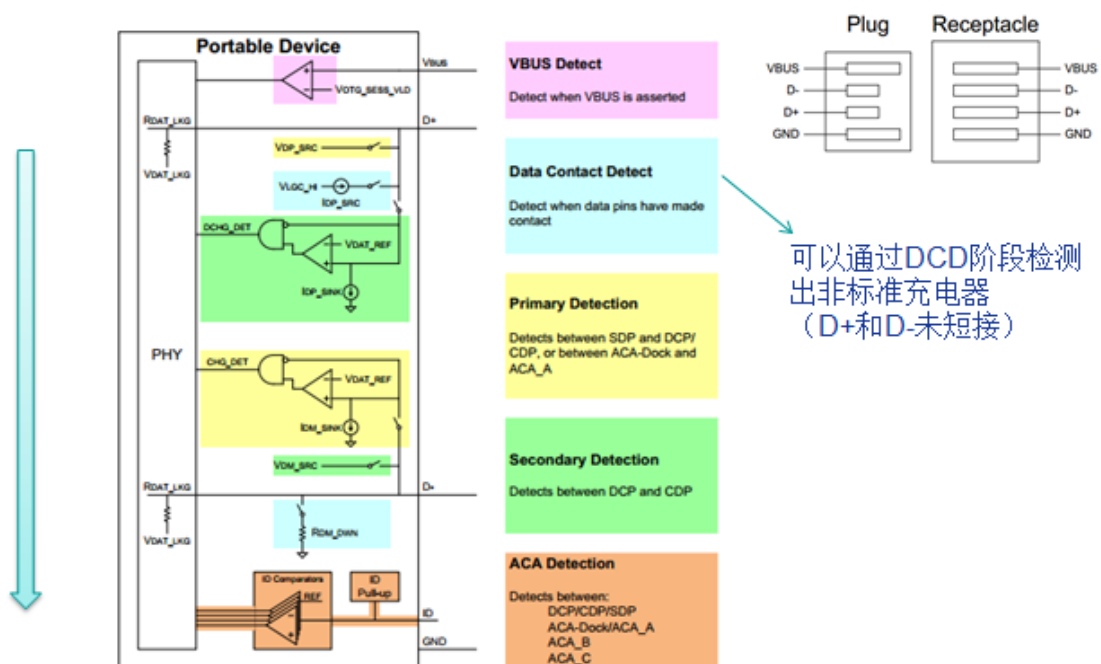


Figure 8 - 1 USB Charging Detection Process

In the typical SDP detection process, the D+/D- signals is shown as follows:

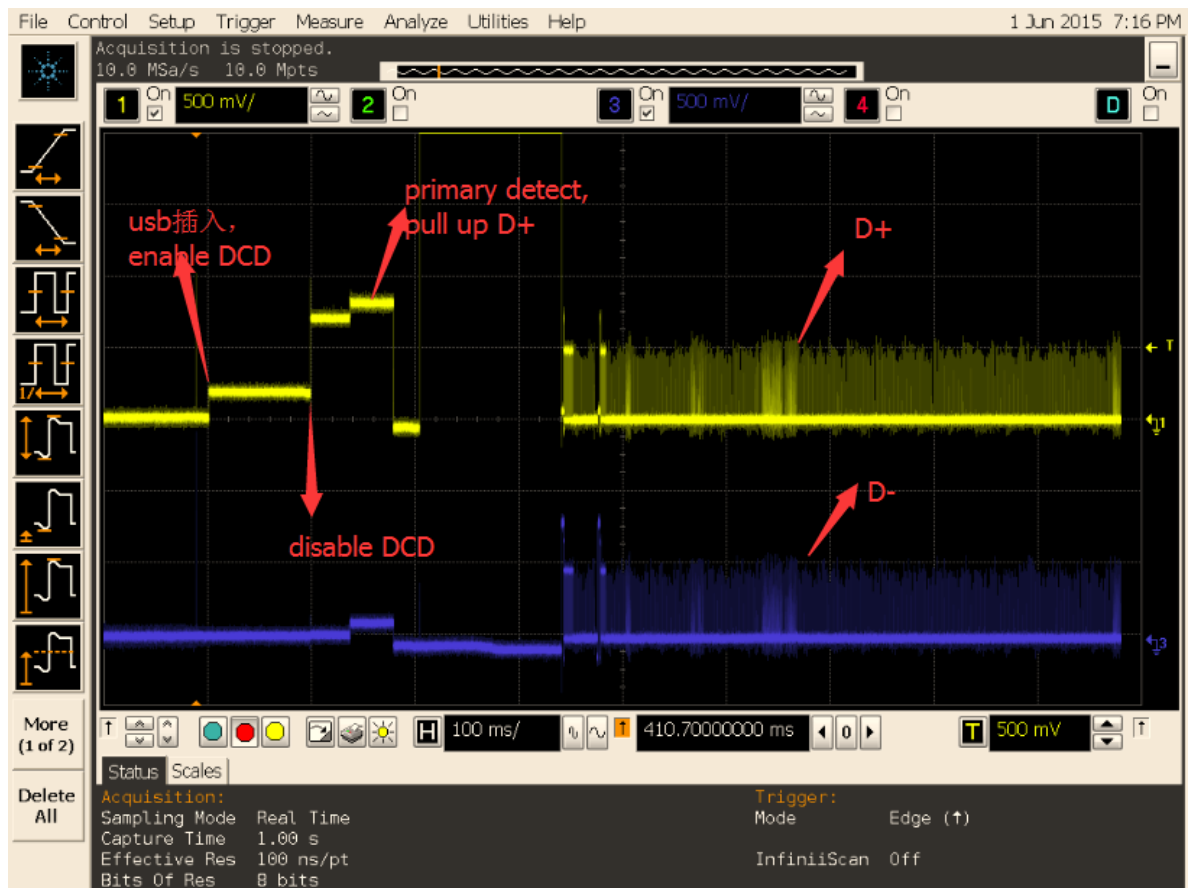


Figure 8 - 2 SDP detection signals

In the typical DCP detection process, the D+/D- signals is shown as follows:

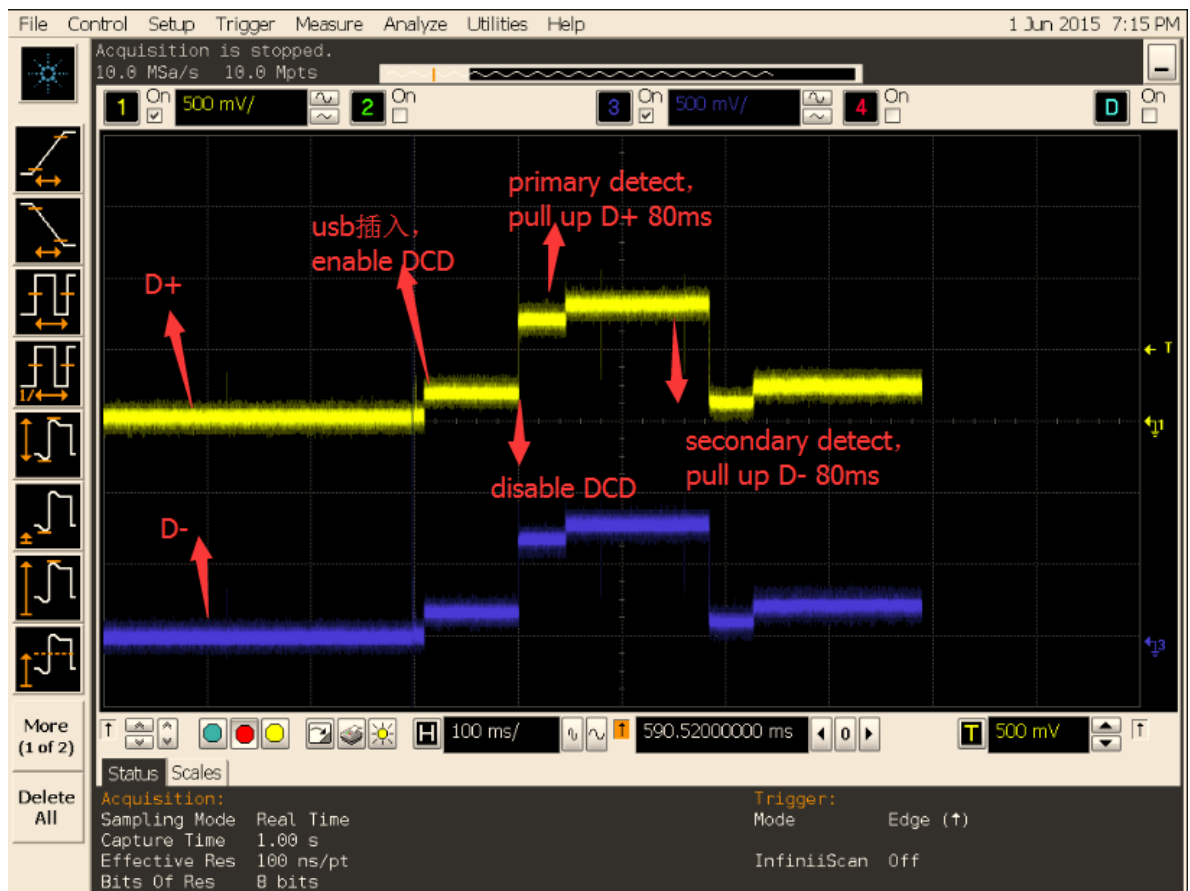


Figure 8 - 3 DCP detection signals

If connected to an USB charger, but it is found that charging is slow, may be the DCP is misdetected as SDP, resulting in charging current set to 500 mA. This problem may happens when the USB cable connection is unstable or the charging detection driver is wrong.

Try to fix it step by step:

1. Capture the uart log when connected to the USB charger and judge the charging type by the prompt of the log. The normal charging type log should be DCP.
2. If the log shows that the charge type is SDP, then an error detection has occurred. First, try to change an USB cable, and test again, if this issue still exists, please use oscilloscope to capture D+/D- signals when USB cable plug in, and send both the error kernel log and D+/D- signals to us.
3. If the connection is a USB charger and the logs show it's DCP, it indicates that the software detects normally, but if the charging is still slow, it may be a problem of charging IC or battery.

## 8.2.6 USB Transfer Rate Problem

The main factors affecting the transmission rate:

- USB signal quality
- USB controller bus frequency
- CPU/DDR operating frequency
- Read and write performance of storage media
- File system format of storage device
- USB device class driver

Reference:

`Rockchip_Developer_Guide_Linux_USB_Performance_Analysis_CN`

## 8.2.7 USB Enumeration Rate

Pay attention to the printed log of the USB enumeration. "high-speed" means recognized as USB 2.0, and "super-speed" means recognized as USB 3.0.

## 8.2.8 USB3.0 Recognized Problem

After the USB3.0 device is plugged in, nothing happens, how to troubleshoot?

According to the definition of USB3.0 enumeration process, it is generally stuck at the Link Training process of USB 3.0 PHY, that is, the problem of USB PHY signal. You can use the USB3.0 analyzer to capture the Link Training process and combine it with the LTSSM state machine described in the USB 3.0 Spec for analysis.

## 8.2.9 USB 3.0 Disk Copy Problem

- Confirm whether the VBUS supply current meets the requirements
- On the PC side, perform the same operation for comparison
- Use USB 3.0 analyzer to capture communication protocol
- Reduce the size of the data block transmitted once, update the xHCI driver, and open the xHCI debug log

## 8.2.10 USB3.0 Camera Transmission Problem

It is generally related to the efficiency of USB access to the DDR bus.

Optimization means:

- ddr fixed frequency 800MHz;
- Improve USB QOS;
- Optimize the interrupt processing efficiency of uvc driver, put memcpy operation in the lower half;
- urb buffer uses kmalloc allocation instead of the default dma\_alloc\_coherent method;

- If the RK platform is for UVC Gadget, you can dynamically allocate TxFIFO to increase the size of TxFIFO;

## 8.3 About PC USB Driver

The developers often use USB download mode (rockusb) and USB debug mode (ADB) on Rockchip platforms during development stage.

### 1. PC Windows USB Driver

Need to install Rockchip vendor special USB driver in Windows. Rockchip provides a tool “DriverAssitant” for you to install Rockchip vendor special USB driver.

### 2. PC Ubuntu USB Driver

No need to install vendor special USB driver.

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## 9 USB Signal Quality Test

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Refer to the document 《Rockchip\_Developer\_Guide\_USB\_SQ\_Test\_CN》 .