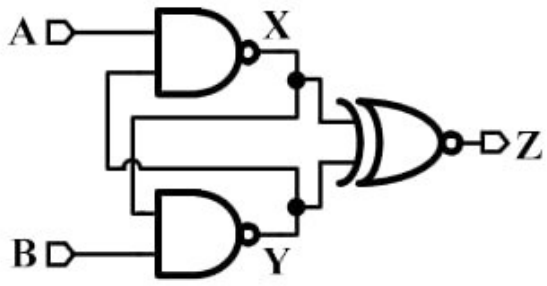
1. In the circuit diagram shown below, the logic gates operate with a supply voltage of $1V$. NAND AND XNOR have $200ps$and$400ps$ input-to-output delay, respectively.

   At time $t = T.A(t) = 0, B(t) = 1$and$Z(t) = 0$. When the inputs are changed to $A(t) = 1, B(t) = 0$at$t = 2T$, a 1 V pulse is observed at Z. the pulse width of the $1V$ pulse is ps.

   (GATE BM 2022)



   (a) $A = 100$

   (b) $A = 200$

   (c) $A = 400$

   (d) $A = 600$