Diagnostic Tests

Instruction	Use of Test
1. Hold the slam switch closed, while setting the self-test switch to the **on** position.	The monitor displays the color hue adjustment pattern of 16 rectangles, as follows. **Do not attempt any color hue or brightness adjustments unless you are a qualified color TV technician!**

Pale Yellow-Green	Orange	White	Deep Yellow
Light Green	Dark Green	Light Blue	Lime Green
Deep Rose	Red	Purple	Red
Navy Blue	Black	Royal Blue	Black

2. Activate any of the coin switches on the coin door.	A convergence pattern appears with a grid of white dots on a black screen. **Do not attempt any convergence adjustments unless you are a qualified color TV technician!**
3. Set self-test switch to the **off** position.	Check attract-mode display and readjust brightness if necessary.

Sheet 1, Side B

ATARI®

Centipede™

Synchronizer
Signature Analysis Procedure
CAT Box™ Preliminary Set-Up
Power Input
Microprocessor
Address Decoder
RAM
ROM
Memory Map

Section of 037241-01   B

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A Warner Communications Company

Power Input

+SENSE 21
+5V
+5V OUT Y

P
R9-11, 16,
32, 134
1K
PULL UP

+5V B 2   +5V

C5-25, 27-37,
40-46, 51,
54, 66, 76, 77
.1
BYPASS

+ C52
100
25V

+ C78
100
25V

R135
220

CR3
MV5053

GND A Z 1

-SENSE 22

GND

-5V D 19   -5V   -5V

+12V C 20   +12V   +12V

+22V 3 X
VR2
7815
I   O
C
+ C80
1, 50V

+15V   +15V
+ C82
1, 50V

-22V 4 W
VR1
7915
I   O
C
C79
+ 1, 50V

-15V   -15V
C81
+ 1, 50V
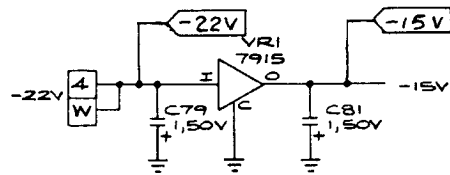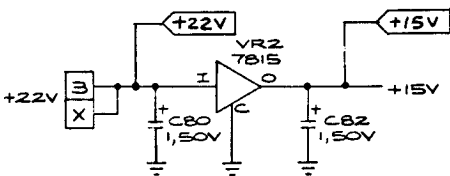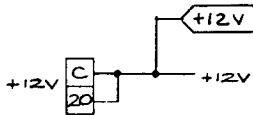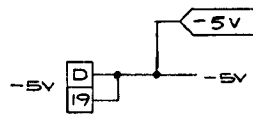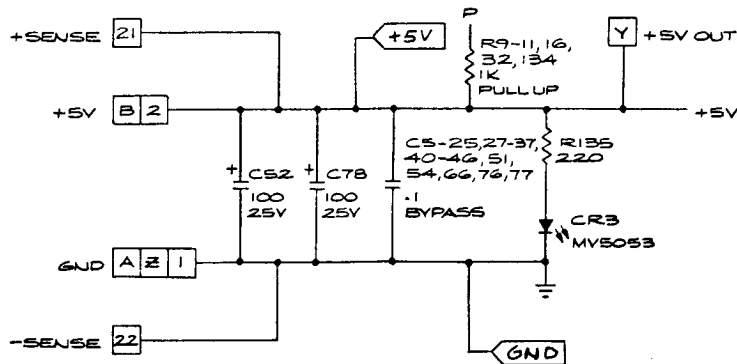
◁▭ **Denotes a test point**

Testing the

1. Perform the CA

2. Set the CAT Bo

   a. Press TEST
   b. DBUS SOUR
   c. BYTES to 10
   d. R/W MODE
   e. R/W to WRIT
   f. Key in 0000
   g. Toggle R/W
   h. R/W to REA
   i. Toggle R/W

3. If the CAT Box
   PARE ERROR
   shows the faili
   PLAY switch is

4. If the COMPAR
   peat the test w
   ensures that th
   COMPARE ERR
   is good.

-02 VERSION
64K

RAM
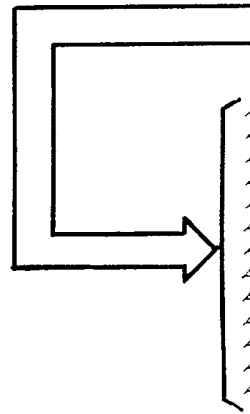
.AM

ox™ preliminary set-up.

witches as follows:

RESET
TO ADDR

OFF)

DE to SINGLE

DE to SINGLE

s an address that doesn't compare, the COM-
) lights, the ADDRESS/SIGNATURE display
address location, and the ERROR DATA DIS-
:bled.

RROR LED does not light, rekey 0000 and re-
he DBUS SOURCE switch set to ADDR. This
ata bits at address 0000 will go high. If the
LED does not light after this step, the RAM

RAM schematic (H2, F2, 90-7033, 2114)
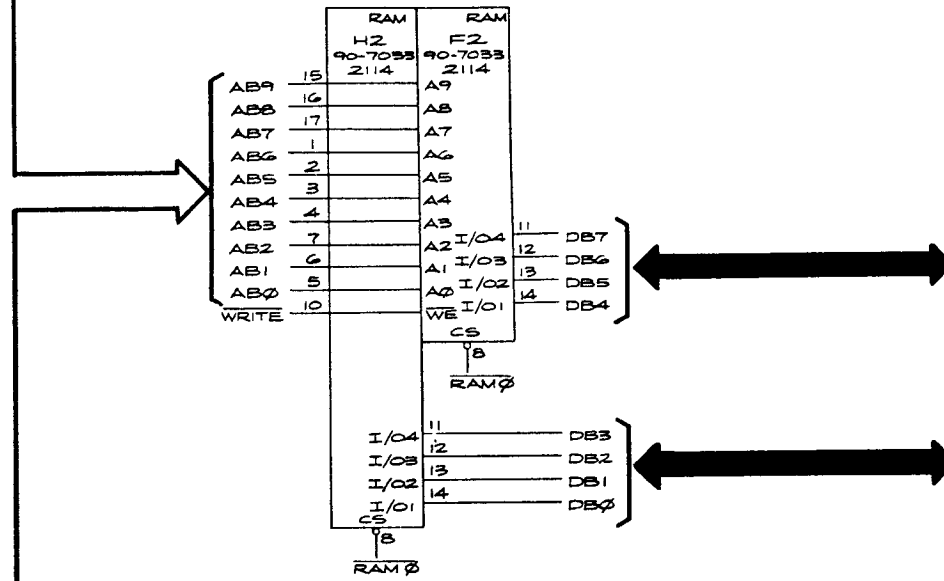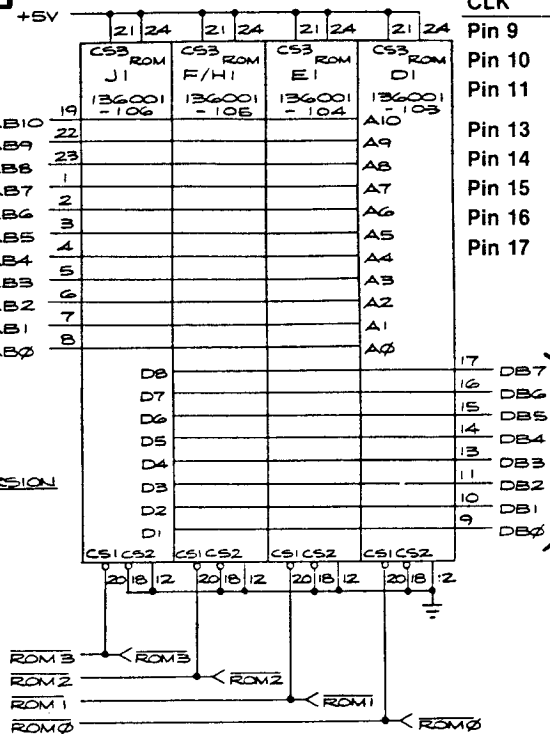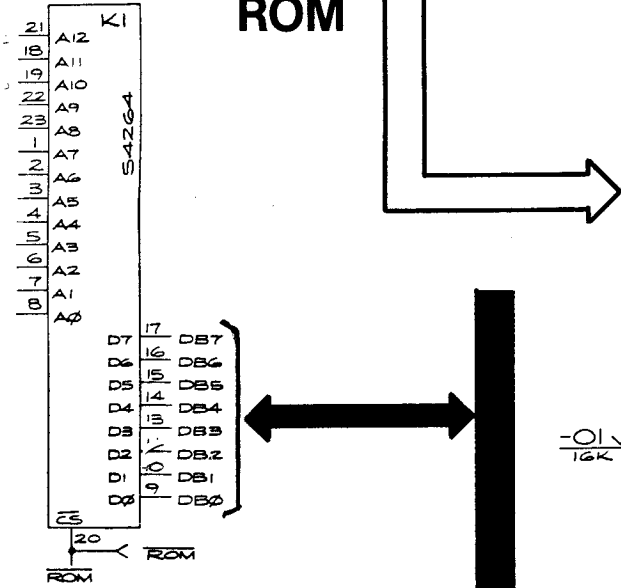
	D1	E1	F/H1	J1
START	Pin 20	Pin 20	Pin 20	Pin 20
STOP	Pin 20	Pin 20	Pin 20	Pin 20
CLK	Φ2	Φ2	Φ2	Φ2
Pin 9	OH81	13PH	CU62	476H
Pin 10	O8FC	C4P5	9553	2A2C
Pin 11	U9F7	11F3	7756	2337
Pin 13	P316	098P	A7CF	FP07
Pin 14	P8C4	5H24	6081	A9AF
Pin 15	H973	0548	5HAC	12HA
Pin 16	8F8F	33P7	6U43	2367
Pin 17	U638	80AA	F83H	8P82

ROM

ROM schematic (K1, 54264; CS3 ROM J1 136001-106, F/H1 136001-105, E1 136001-104, D1 136001-103; -01 VERSION 16K)

to obtain proper signals
from J2, ground J2 pin 1.

Memory Map

	MEMORY MAP									
HEXA-DECIMAL ADDRESS	R/W	D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
0000-03FF		D	D	D	D	D	D	D	D	RAM
0400-07BF		D	D	D	D	D	D	D	D	Playfield RAM
07C0-07CF		D	D	D	D	D	D	D	D	Motion Object Picture
07D0-07DF		D	D	D	D	D	D	D	D	Motion Object Vert.
07E0-07EF		D	D	D	D	D	D	D	D	Motion Object Horiz.
07F0-07FF			D	D	D	D	D	D	D	Motion Object Color
0800	R	D	D	D	D	D	D	D	D	Option Switch 1 (0 = On)
0801	R	D	D	D	D	D	D	D	D	Option Switch 2 (0 = On)
0C00	R	D				D	D	D	D	Horizontal Trak Ball™ Inputs
	R		D							VBLANK (1 = VBlank)
	R			D						Self-Test (0 = On)
	R				D					Cocktail Cabinet (1 = Cocktail)
0C01	R	D	D	D						R,C,L Coin Switches (0 = On)
	R				D					SLAM (0 = On)
	R					D				Player 2 Fire Switch (0 = On)
	R						D			Player 1 Fire Switch (0 = On)
	R							D		Player 2 Start Switch (0 = On)
	R								D	Player 1 Start Switch (0 = On)
0C02	R	D				D	D	D	D	Vertical Trak Ball™ Inputs
0C03	R	D	D	D	D					Player 1 Joystick (R, L, Down, Up)
	R					D	D	D	D	Player 2 Joystick (0 = On)
1000-100F	R/W	D	D	D	D	D	D	D	D	Custom Audio Chip
1404	W					D	D	D	D	Playfield Color RAM
140C	W					D	D	D	D	Motion Object Color RAM
1600	W	D	D	D	D	D	D	D	D	EA ROM Address & Data Latch
1680	W					D	D	D	D	EA ROM Control Latch
1700	R	D	D	D	D	D	D	D	D	EA ROM Read Data
1800	W									IRQ Acknowledge
1C00	W	D								Left Coin Counter (1 = On)
1C01	W	D								Center Coin Counter (1 = On)
1C02	W	D								Right Coin Counter (1 = On)
1C03	W	D								Player 1 Start LED (0 = On)
1C04	W	D								Player 2 Start LED (0 = On)
1C07	W	D								Trak Ball™ Flip Control (0 = Player 1)
2000	W									WATCHDOG
2400	W									Clear Trak Ball™ Counters
2000-3FFF	R									Program ROM

J1
Pin 20
Pin 20

φ2
476H
2A2C
2337

FP07
A9AF
12HA
2367
8P82

Synchronizer

(Schematic diagram components)

+5V
R1 10K
R2 0K
Y1 12.096 MHz
C1 100PF
C2 39PF
L1 100 uH
R3 220
Q1 2N3904
C3 .1
N1 SO4

P2	START	P2	11	⌐
	STOP	P2	11	⌐
	CLK	N1	6	⌐

N2	START	N2	11	⌐
	STOP	N2	11	⌐
	CLK	N1	6	⌐

M2	START			
	STOP			
	CLK			

LD A B C D
ET P2
EP LS163A
COUNTER
RIP
CK QA QB QC QD

K3 LS04
K4 LS08
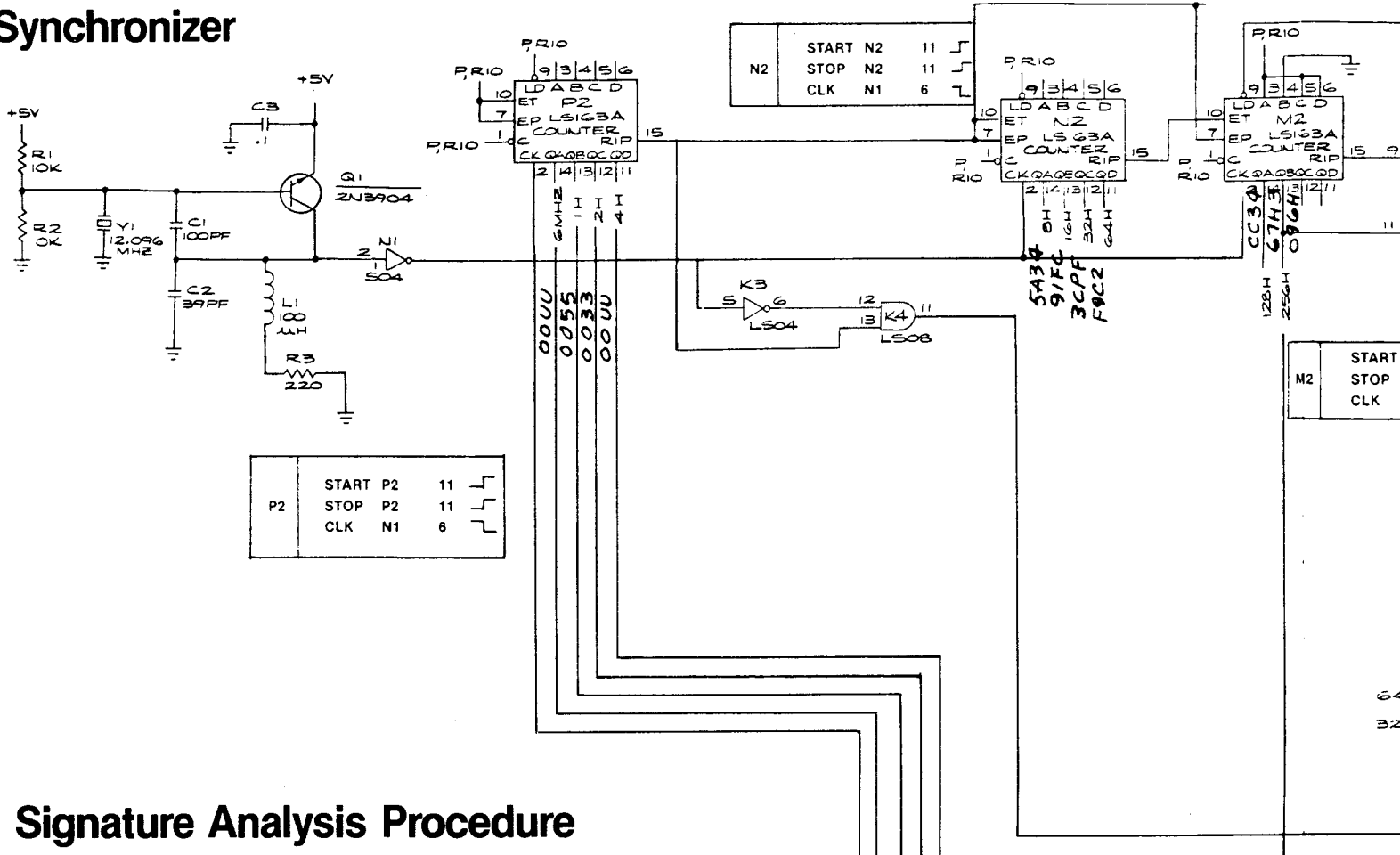
Signature Analysis Procedure

1. Perform the CAT Box™ preliminary set-up.

2. Connect the three BNC to E-Z clip cables (supplied with the CAT Box) to the SIGNATURE ANALYSIS CONTROL START, STOP, AND CLOCK jacks on the CAT Box.

3. Attach the three black E-Z clips to a ground loop on the CENTI-PEDE™ game PCB.

4. Attach the CAT Box data probe to the DATA jack on the CAT Box.

5. The red E-Z clips on the cables will be moved about for each group of signatures to be taken. The set-up for each group of signatures is located on the schematic sheet near the device to be checked. The signatures are located on or near the signal point on the schematic.

Note the example:

SET-UP — IC# PIN# — SLOPE
P2 | IC TO BE TESTED
START P2 11
STOP P2 11
CLK N1 6
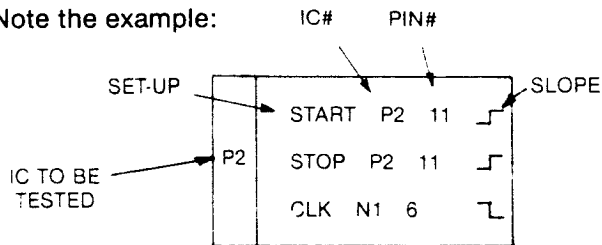
6. Set the CAT Box switches as follows:

  a. TESTER MODE: SIG
  b. TESTER SELF TEST: OFF
  c. PULSE MODE: LATCHED
  d. START:
  e. STOP:
  f. CLOCK:

CAT Box™ Prelimina

1. Remove:
  ● The electrical power from
  ● The wiring harness from
  ● The game PCB from the
  ● The MPU chip C2 from th

2. Connect:
  ● The extender cables to the
  ● Pins 37 to 39 on the MPU
  ● The CAT Box flex cable to
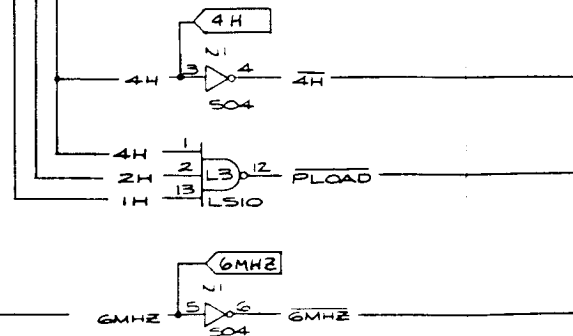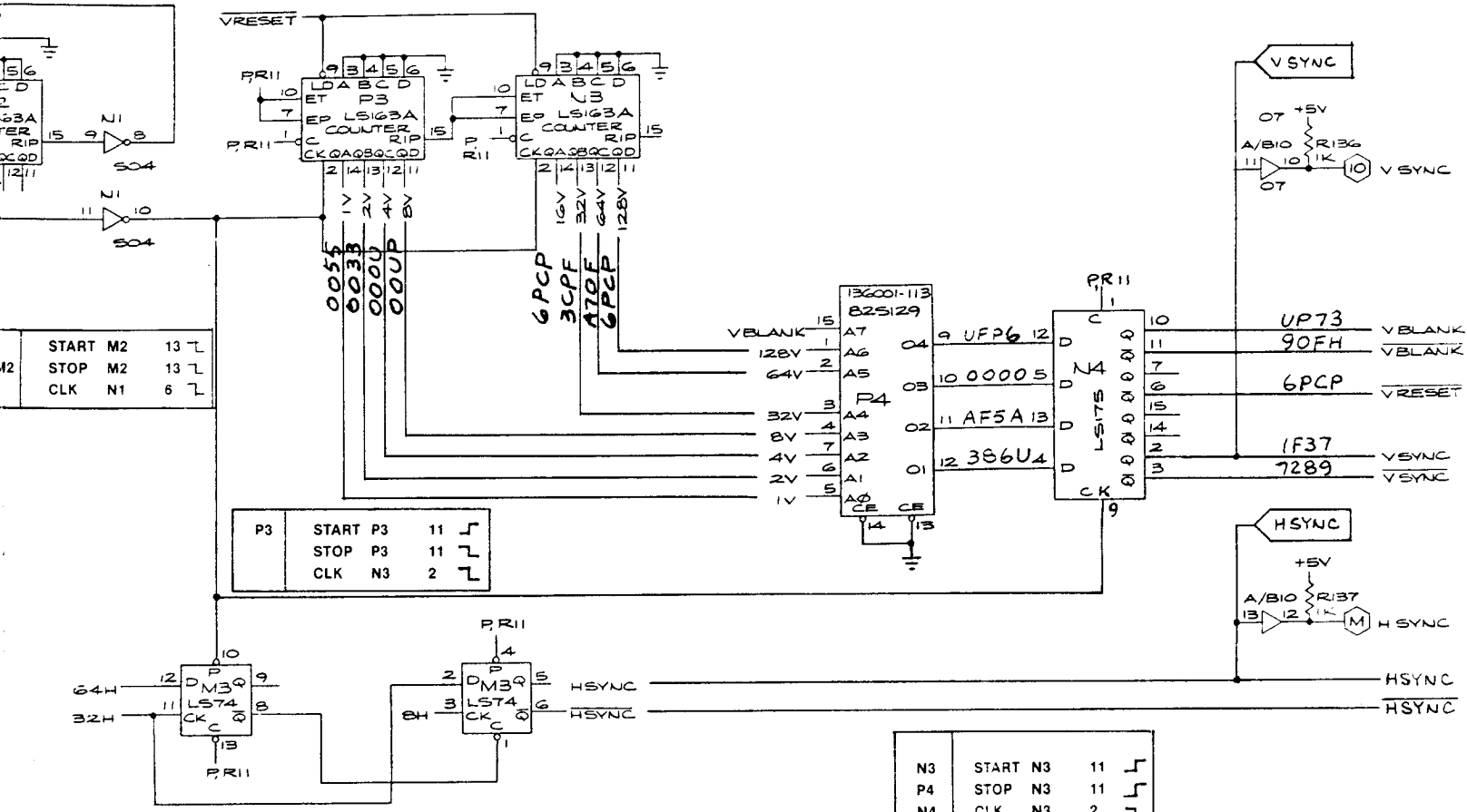
4H
4H — 4H SO4
4H
2H — L3 12 PLOAD
1H — LS10

6MHZ
6MHZ — 6MHZ SO4

liminary Set-up

wer from the game.
ess from the game PCB.
from the cabinet.
2 from the game PCB.

les to the game PCB and the wiring harness.
the MPU socket with a piece of 28 AWG wire.
cable to the game PCB test edge connector.

VRESET

P,R11
LD A B C D
ET   P3
EP LS163A
COUNTER
RIP
CK QA QB QC QD
P,R11

LD A B C D
ET   U3
EP LS163A
COUNTER
RIP
CK QA QB QC QD
P R11

504
N1
504

	START	M2	13
M2	STOP	M2	13
	CLK	N1	6

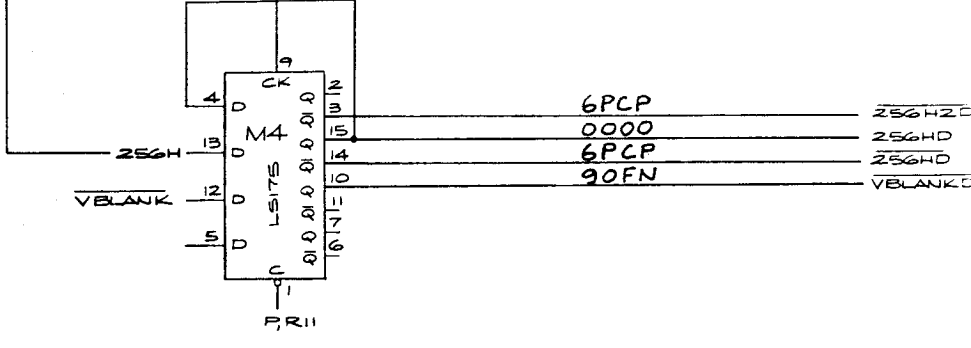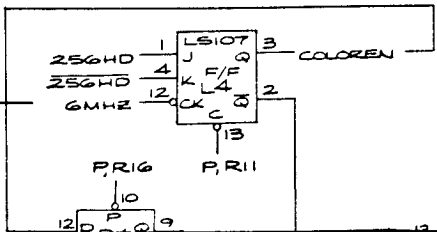| P3	START	P3	11
	STOP	P3	11
	CLK	N3	2

0055
0033
0000
0000
1V 2V 4V 8V

6PCP
3CPF
A10F
6PCP
12V 32V 64V 128V

VBLANK 15 A7   04 9 UFP6 12
128V   2 A6
64V   A5   03 10 00005
32V   3 A4
8V   4 A3   02 11 AF5A 13
4V   6 A2
2V   7 A1   01 12 386U4
1V   5 A0
136001-113
82S129
P4
CE CE
14 13

PR11
C
D   Q 10
D   Q 11
D   Q 7
D   Q 6
N4   Q 15
LS175 Q 14
D   Q 2
D   Q 3
CK
9

UP73   VBLANK
90FH   VBLANK
6PCP   VRESET
1F37   VSYNC
7289   VSYNC

V SYNC
+5V
O7   R136 1K
A/BIO
11   10
O7
V SYNC

H SYNC
+5V
A/BIO   R137 1K
13 12
H SYNC

64H   12 P M3 9
32H   11 D LS74 8
CK
13
P,R11

P,R11 4
2 P M3 5   HSYNC
8H 3 D LS74 6 HSYNC
CK   1

HSYNC
HSYNC

N3	START	N3	11
P4	STOP	N3	11
N4	CLK	N3	2
M4			

CK 2
4 D M4 Q 3
15
256H 13 D Q 14
LS175 Q 10
VBLANK 12 D Q 11
5 D Q 6
C
1
P,R11

6PCP   256H2D
0000   256HD
6PCP   256HD
90FN   VBLANK5

4H

PLOAD

6MHZ

256HD   1 J LS107 3   COLOREN
256HD   4 F/F
6MHZ   12 K L4 2
CK   Q
13
P,R16   P,R11
10

TEST CONNECTOR-FOR ATARI CAT BOX™

Microprocessor

MPU &	START	C2	25
Address	STOP	C2	25
Decoder	CLK	C2	39

To Sheet 2, Side B

To/From Sheet 2, S
Sheet 2, S

To/From Sheet 2, Side B

Address Decoder

To/From
Sheet 2, Side A
Sheet 2, Side B

+5V

25
25
39

3C97 → ROM

K3 11 10 3C97   BR/W 10 9 J3 8 15 LS139 9 5IU7 → ROM3
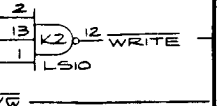LS04   LS32   G Y3 10 2960 → ROM2
            AB12 13 B Y2 11 5P33 → ROM1
            AB11 14 A Y0 12 1H32 → ROM0
                        J2

WRITE 9 8 K3   13 A7 8 WRITE 2
LS04   12
        10 LS20
6MHZ 9

WRITE

BR/W

K2 13 12 WRITE
LS10

5 4 F3 6 → STEERCLR
        LS32
9 F3 8 → WATCH DOG
10 LS32
1 F3 3 → OUT0
2 LS32
12 F3 11 → IRQRES
13 LS32

12 LS42 11 A8H2
D 13 C 10 C5P1
AB12 13 C 9 U550
AB11 14 B 7 9UC6
AB10 15 A 6 0UA5
        5

H3   5 F733 → POKEY
4 4231
3 3580 → SWRD
2 4P5C → PF
1 A00H → RAM0
0
DECODER

PAC 12 A4 11 → COLORAM
13 LS32

12 J3 11 F6HP
AB9 13 LS32

K3 10
1 2 C5 9 8
LS04 LS32

F9 7A 1 LS139 7 0099
G Y3 6 EA READ / U08A
                Y2 5 EA CONTROL / 1F7A
AB8 3 B C4 Y1 4 EA ADDR
AB7 2 A Y0

AB1 2 E3 3 0294 → IN0
1 LS32
13 K3 4 5554 6 40A4 → IN1
LS04 LS32

BR/W 9 E3 8 4P5C → PFRAMRD
10 LS32

WRITE 12 E3 11 1 LS139 7 11U6 → PFWR3
13 LS32   G Y3 6 1C3F → PFWR2
    AB5 3 B Y2 5 4FH7 → PFWR1
    AB4 2 A J2 Y0 4 461F → PFWR0

To/From
Sheet 2, Side A
Sheet 2, Side B

NOTE: