00 Video Ram Addresser - Namco Gate Array

<u>Pin #</u>	<u>Name</u>	Input/Output	EXPLANATION
1 2 3 4 5 6 7 8 9 10 11	2H 4H 8H 16H 32H 64H 128H 256H 8V 16V 32V	I I I I I I I I I I I I	SYNC INPUTS "" "" "" "" "" "" "" "" ""
12	64V	Î	
13	128V	I	
14	Gnd	POWER	
15	AB11	0	2H=Ø=High Z; 2H=1=Active; Ram Addresser
16	AB10	0	
17	AB9	0	
18	AB8	0	
19	AB7	0	
20	AB6	0	<pre>p = Normal, 1 = Reverse +5V</pre>
21	AB5	0	
22	AB4	0	
23	AB3	0	
24	AB2	0	
25	AB1	0	
26	ABØ	0	
27	FLIP	0	
28	VCC	POWER	

NOTES: Allows RAM to be addressed by CPU and Sync chain.) Requires CPU Address bus to be tri-state during 2H high.

Ø2	Unive	rsal	Shift	Registe	er

<u>Pin_</u> #	Name	I/O EXPLA	NATION - 4 Bit Mode	8 Bit Mode
1 2 3	CK FLIP DØ7	I T	<pre>Clock Imput 0 = Normal, 1 = Reverse</pre>	Clock Imput Ø = Normal, 1 = Reverse
4 5	DØ6 DØ5	i }	4 Bit Data For QØ1 —	
6	DØ4	į)	רטז עשו –	8 Bit Data for QØ1
3	DØ3 DØ2	$\frac{1}{1}$	4 Bit Data	الرب الما
9 10	DØ1 DØØ	$\frac{I}{I}$ \int	For 000	
11 12	QØØ QØ1	0 0	DØ3, DØ2, DØ1, DØØ in order DØ7, DØ6, DØ5, DØ4 in order	
13	MODE	Ī	Ø = 4 Bit Mode	1 = 8 Bit Mode

Ø2 Universal Shift Register Continued

Pin #	Name	<u>I/0</u>	EXPLANATION - 4 Bit Mode	8 Bit Mode
14	GND	POWER		
15	S/L	I	$1 = Shift, \emptyset = Load$	1 = Shift, \emptyset = Load
16	LDEN	I	Load Enable	Load Enable
17	Q11	0	D17, D16, D15, D14 in order	
18	Q1Ø	0_	D13, D12, D11, D10 in order	Not Used
19	D1Ø	I)	, , , , , , , , , , , , , , , , , , , ,	
20	D11	I	4 Bit Data	
21	D12	I (For Q1Ø	0.51.5.
22	D13	IJ	•	8 Bit Data
23	D14	I		For Q11
24	D15	I (4 Bit Data	
25	D16	I (For Q11	
26	D17	I J	•	
27	ČLR	I	CLEAR	CLEAR
28	УСС	POWER	+5V	+5V

NOTES: Can be set up for 4 4-bit parallel to serial converters or 2 8-bit parallel to serial converters. All registers use 1 set of control signals. Can shift either direction.

Ø4 Motion Object Controller

<u>Pin #</u>	Name	<u>I/0</u>	
1	1H	I	Sync Inputs
1 2 3 4 5 6 7 8	2H	I	Sync Inputs
3	HSYNC	I	Sync Inputs
4	H4	0, 1	Select which 4 of 32 motion object
5	Н8	0 >	pixels to load into video RAM
6	H16	\mathcal{L}_{0}	Piners of road most rideo will
/	RA6	\int_{0}^{0}	
8	RA5	0	Address for Motion Object RAM
	RA4	0	2H = Ø = CPU Address
10	RA3	0 >	2H = 1 = Motion Data Control
11	RA2	0	
12	RA1	0)	
13	RAØ		
14	GND	POWER	
15 16	ABØ	1)	
17	AB1 AB2	I	
18	AB2 AB3	i \	CPU Address
19	AB3 AB4	ī (Cru Address
20	AB5	I	
21	AB6	・iノ	
22	VP05	0	Strobe when vertical position is stable (1st)
23	HP05	Ŏ	Strobe when horizontel position is stabel (2nd)
24	OBJEN*	Ö	2H faster than OBJEN
25	MATCH	Ĭ	Vertical line match = Ø
26	SIZE	Ī	\emptyset = 16 x 16; 1 = 32 pixel objects
27	OBJEN	Ō	Generated if MATCH is true (low)
28	VCC	POWER	+5V

NOTE: Generates the strobes and RAM addresses for the motion objects. $(MOC\ 24\ style)$

```
EXPLANATION
Pin #
        Name
                I/0
        ER/W
  1
                 0
                         R/W Signal to Custom 50's
  2
        EDB7
                I/0-
  3
        EDB6
                I/0
  4
        EDB5
                I/0
        EDB4
  5
                I/0
                         Custom 50 Data Bus
  6
        EDB3
                I/0
  7
        EDB2
                I/0
        EDB1
                I/0
  8
  9
        EDBØ
                I/0
 10
        ECS3
                 0
        ECS2
                 0
 11
                         Custom 50 Chip Selects
        ECS1
                 0
 12
        ECSØ
                 0
 13
        GND
               POWER'
 14
        C/\overline{C}
                 I
 15
                         1 = Command, \emptyset = Data (on Data Bus)
        R/W
                 Ι
                         CPU R/W
 16
                 I
                         128H (or 64H.HSYNC) Sync input
 17
        128H
                 I
                         Chip Select-
 18
         \overline{C5}
                 0 -
                         CPU NMI -
 19
        DBØ
 20
                I/0-
        DB1
                I/0
 21
        DB2
                I/0
 22
        DB3
                I/0
 23
                         CPU Data Bus
        DB4
                I/0
 24
        DB5
 25
                I/0
        DB6
 26
                I/0
 27
        DB7
                I/0.
        VCC
               POWER
                         +51
 28
```

NOTE: Interfaces between CPU and Custom 50's. (Custom 4 bit micro-processors) Commands and data are transferred via the data bus. C/D selects Command or Data. Part of the Custom 50 Data Bus is Address and part is Data (apparently).

Ø7 SYNC GENERATOR

Pin #	Name	<u>I/0</u>	EXPLANATION
1 2 3	CK 1H	I	6MHZ Input →
3 4	2H 4H	0	
4 5	8H	0	
6	16H	0	
7	32H	0 >	Horizontal Outputs -
8 9	64H	0	·
9	128H	0	
10	256H	0	
11	HBLANK	0	
12	HSYNC	ر_0	
13	HRESET	I/0	Used to synchronize 2 chips (0.C.) →
14	GND	POWER	
15	TEST2	I	Ø = Normal ~
16	VRESET	I/0	Used to sync. two chips (open collector).
17	VSYNC	0	
18	VBLANK	0	Vertical Outputs
		•	

Ø7 SYNC GENERATOR CONTINUED

<u>Pin #</u>	Name	1/0	EXPLANATION
19 20	TEST1 128V		1 = Normal -
21	64 V	0	
22	32V	0 [
23	16V	0 (Vantiani Outsut
24	8V	0	Vertical Outputs
25	4٧	0	
26	2V	0	
27	17	2	
28	VCC	POWER	+5V ~

NOTE: Takes 6 MHZ and generates all Horizontal & Vertical timing signals. More than 1 can be used in a system using HRESET and $\overline{\text{VRESET}}$.

51 Coin I/O Controller

31 001	11/0 0	Oncion	iei
Pin #	Name	I/0	Explanation
1 2 3 4 5 6 7 8 9 10 11 12 13	EXTAL XTAL RESET IRQ SO SI SC/TO TC PØ P1 P2 P3 EDBØ	I I I I 0 ? ? I 0 0 0 0	External clock input (2H normally) (max 2Mhz) N.C. Reset signal Chip select Lockout cord signal ? Not used on D.D. ? Not used on D.D. VBLANK Lamp z output Lamp 1 output Coin Counter 2 output Coin Counter 1 output
14 15 16 17 18 19 20 21	EDB1 EDB2 EDB3 EDB4 EDB5 EDB6 EDB7 GND	I/0 I/0 I/0 I/0 I/0 I/0 I/0 POWER	Custom 50 BUS
22 23 24 25 26 27 28 29 30 31 32 33 34	RØ R1 R2 R3 R4 R5 R6 R7 R8 R9 R10 R11	I I I I I I I I I I I I I I I I I I I	Player 1 Up Right Down Left Player 2 Up Right Down Left Player 1 Shoot Player 2 Shoot Player 2 Start Coin 1

51 Coin I/O Controller Continued

<u>Explanation</u>
Coin 2
Service (Anx Coin Input) Test
Address?
R/W Input
+5V

NOTE: This custom microporcessor handles I/O (R/\overline{W})

53 Steering Controller

33 Steering Controller			
<u>Pin #</u>	<u>Name</u>	<u>I/0</u>	Explanation
1 2 3 4 5	EXTAL XTAL RESET IRQ SO	I I I	External clock input (2H normally) (max 2Mhz) N.C. Reset signal Chip select
6 7	S1 SC/T0	>	Not used on Dig Dug
8 9 10 11 12 13	TC PØ P1 P2 P3 EDBØ	0 0 0 0 1/0	• Mode determines function. Not used on Dig Dug
14 15 16 17 18 19	EDB1 EDB2 EDB3 EDB4 EDB5 EDB6	I/0 I/0 I/0 I/0 I/0 I/0	Custom 50 data Bus. 16 switches read in Dig Dug (mode 7), other things read in other modes.
20 21 22 23 24 25 26 27 28	EDB7 GND RØ R1 R2 R3 R4 R5	I I I I I I I I I I I I I I I I I I I	Reads switches, keyboards (ASCII), & different
28 29 30 31 32 33 34 35 36 37	R6 R7 R8 R9 R10 R11 R12 R13 R14		→ things for different modes.

53 Steering Controller Continued

Pin #	Name	<u>I/0</u>	Explanation
38 39	K0 K1	$\begin{bmatrix} I \end{bmatrix}$	Mode Select
40	K2	I (Mode Science
41	К3	IJ	
42	VCC	POWER	+5 V

NOTE: This custom microprocessor handles inputs (for Dig Dug). It also can apparently scan keyboards and handle steering controls. 8 different modes.