MAGICOM MAIN LOGIC SCHEMATIC REVISIONS

- A. Original release.
- B. R3: Was 1K; became 300.
 D0 on U20 incorrectly shown as Pin 8. Changed to pin 18 on 6/23/83.
- C. Addition of capacitor C63, 220pf disc between U24, Pin 3 and ground. 6/27/83.
- D. C54: Was 0.001uf disc. Became 0.1uf disc on 6/29/83.
 C63: Was 220pf disc. Became 0.001uf disc on 6/29/83.
 74LS244 inserted between 4MHz signal and U1 (280), Pin 6.
 U17, Pins 13 and 7 used these were formerly a spare gate.
 6/29/83.
- E. C40, 0.01 disc tied between U22, Pin 2 and ground is deleted. 74LS244 inserted between Ql collector and U22, Pins 1 and 2. U17, Pins 11 and 9 used these were formerly a spare gate. U1(Z80), Pin 25 cut from U7 (MC68705P5), Pin 9. U1(Z80), Pin 25 tied to R48 (new addition) 4.7K ½W 5% resistor. Other side of R48 tied to +5V.

Ul8(74LS245), Pin 19 cut from U7(68705, Pin 14. Ul8, Pin 19 tied to +5V.

Ul7(74LS244), Pin 17 cut from U7, Pin 19. Ul7, Pin 17 tied to +5V.

U23(74LS244), Pin 1 cut from U22(74LS00), Pin 11. U23, Pin 1 tied to ground.

All of "E" above were effective on 7/8/83.

- F. Deletion of the following effective 7/8/83:
 - U5 74LS244
 - U6 74LS393
 - U12 74LS244
 - U13 74LS393
 - U17 74LS244
 - U18 74LS245

Subtitute U23 for U17 (74LS244) for clock signal into Z80 (U1, Pin 6 from U23, Pin 7) and reset signal into U22, Pins 1 and 2 from U23, Pin 9 effective 7/8/83.

- G. C63: Was 0.00luf disc. Became 470pf effective 9/5/83.
- H. Reset signal sent from U23, Pin 9 to U16, Pin 1 to cure false coin count on power up.
- I. Reference letter not used.

- J. Correct pin out for inputs on U20(74LS244) effective 9/16/83.
- K. C63: Was 470pf disc; became 330pf disc.

C17: Was 330pf mica; became 330pf disc.

Addition of U31(74LS74) to divide clock.

Y1: Was 4.000MHz; became 16.000MHz.

U24: Was74LS04; became 74S04.

Addition of R29 between U29, Pin 4 and C24. Addition of R50 between U30, Pin 4 and C50.

These two additions allow option for U29 and 30 with the following components:

R49, R50 = 0 ohm jumper $\frac{\text{CA2002}}{\text{2.2 ohm, } \frac{1}{4}\text{W}}$ 5% C24, C50 = 0.2 Disc 0.1 disc

Addition of Jumper W1, when installed, allows board to be used with Pioneer 7820 disc player with proper software.

Deleted: U7 MC68705

Addition (reinstallation) U6, 74LS393

Ul3, 74LS393

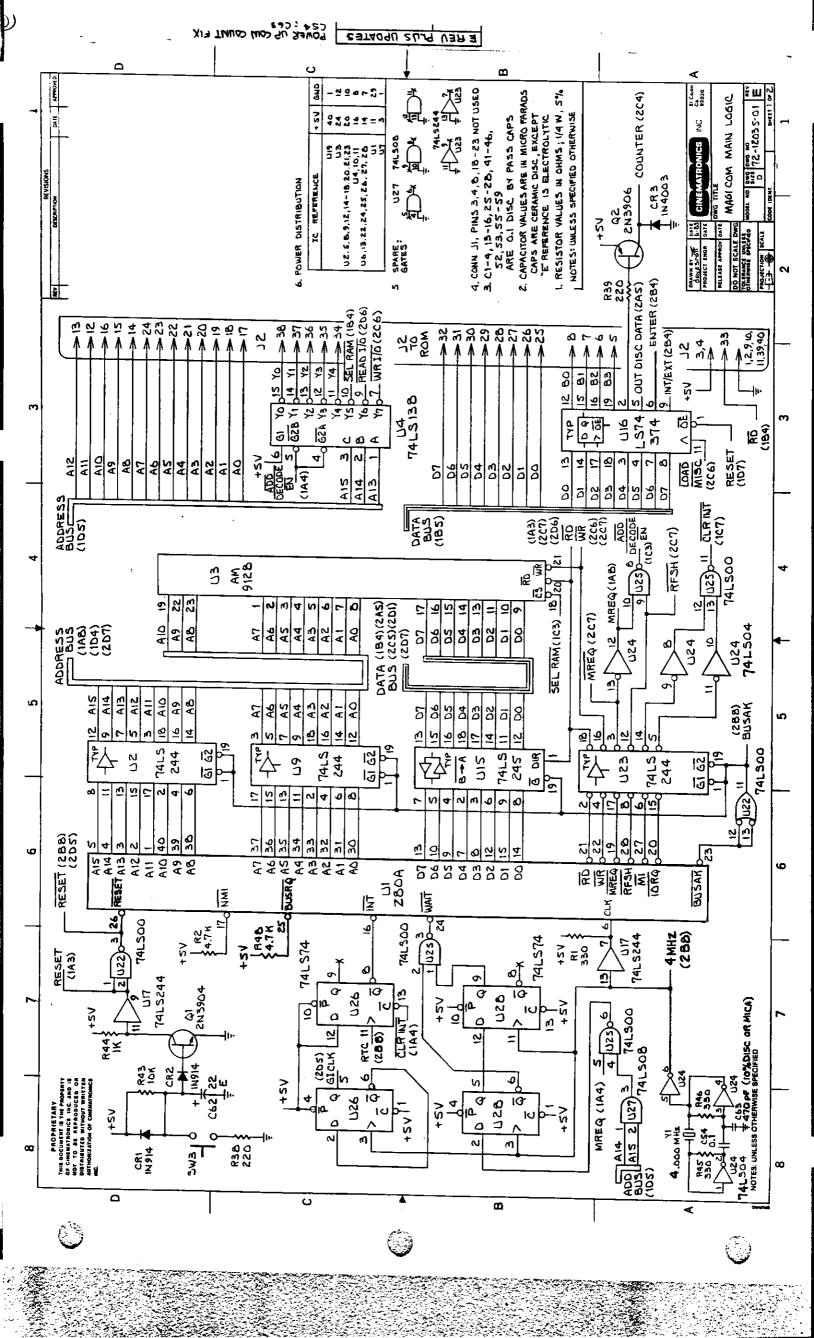
U6, Pins 2 and 12, and Ul3, Pins 2 and 12 all grounds.

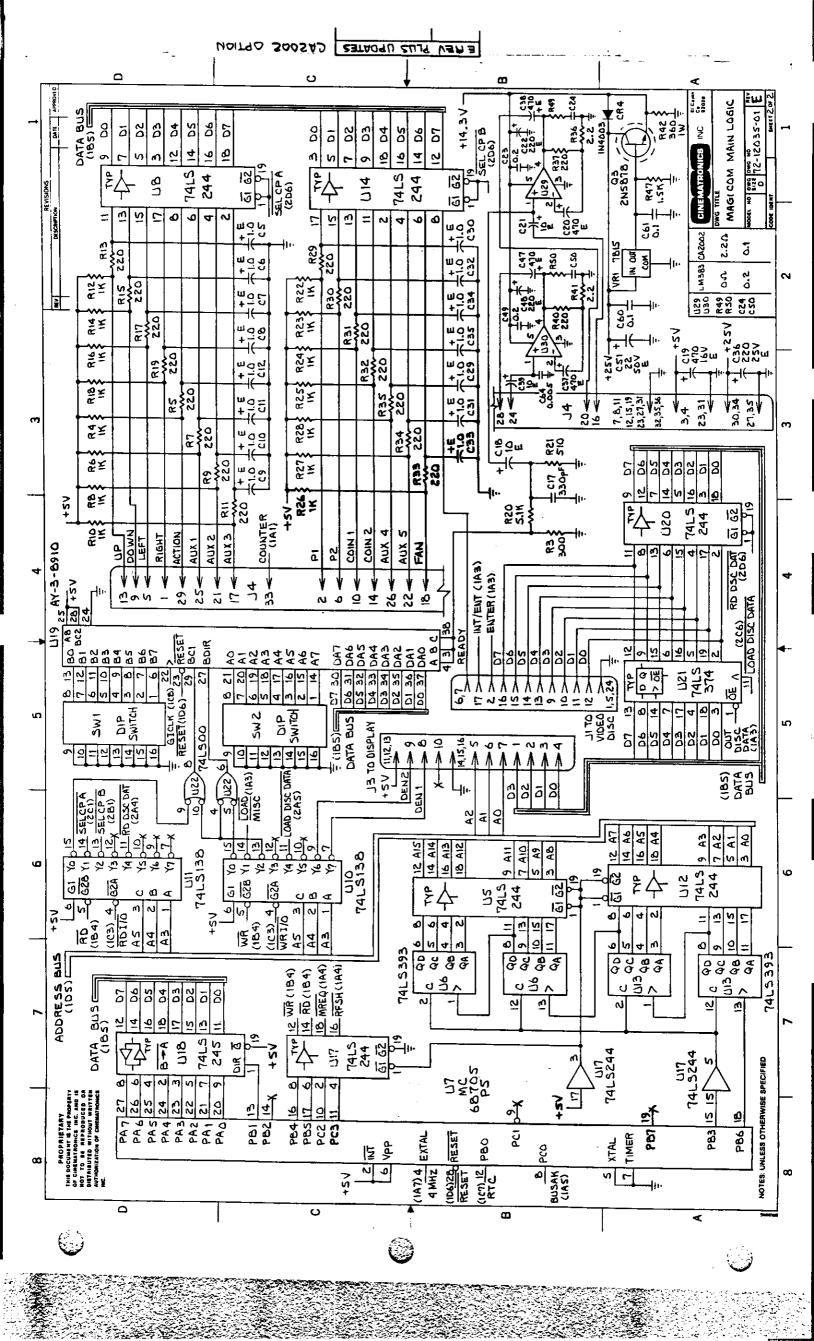
U6, Pin 6 tied to U26, Pin 11 (RTC).

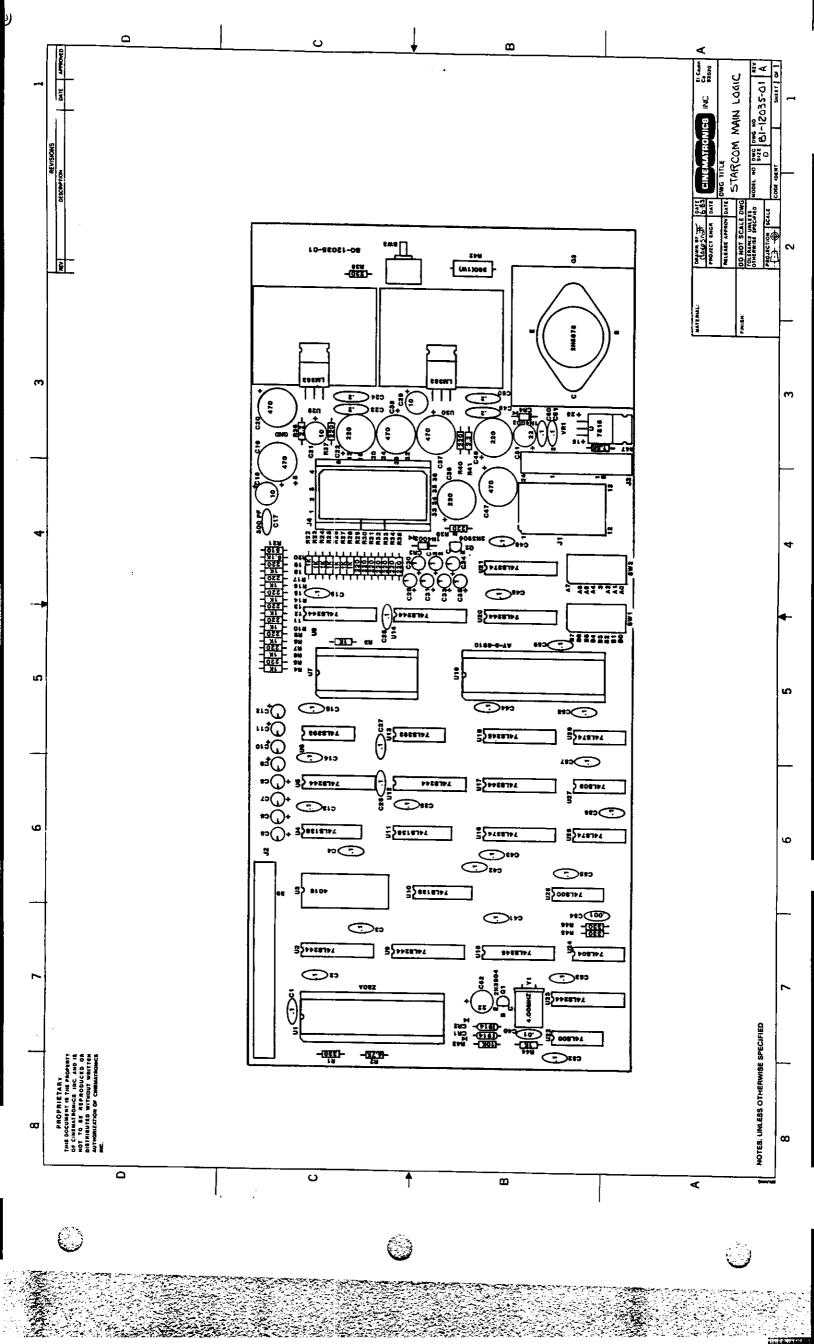
Ul3, Pin 13 tied to U26, Pin 5 (GI CLK)

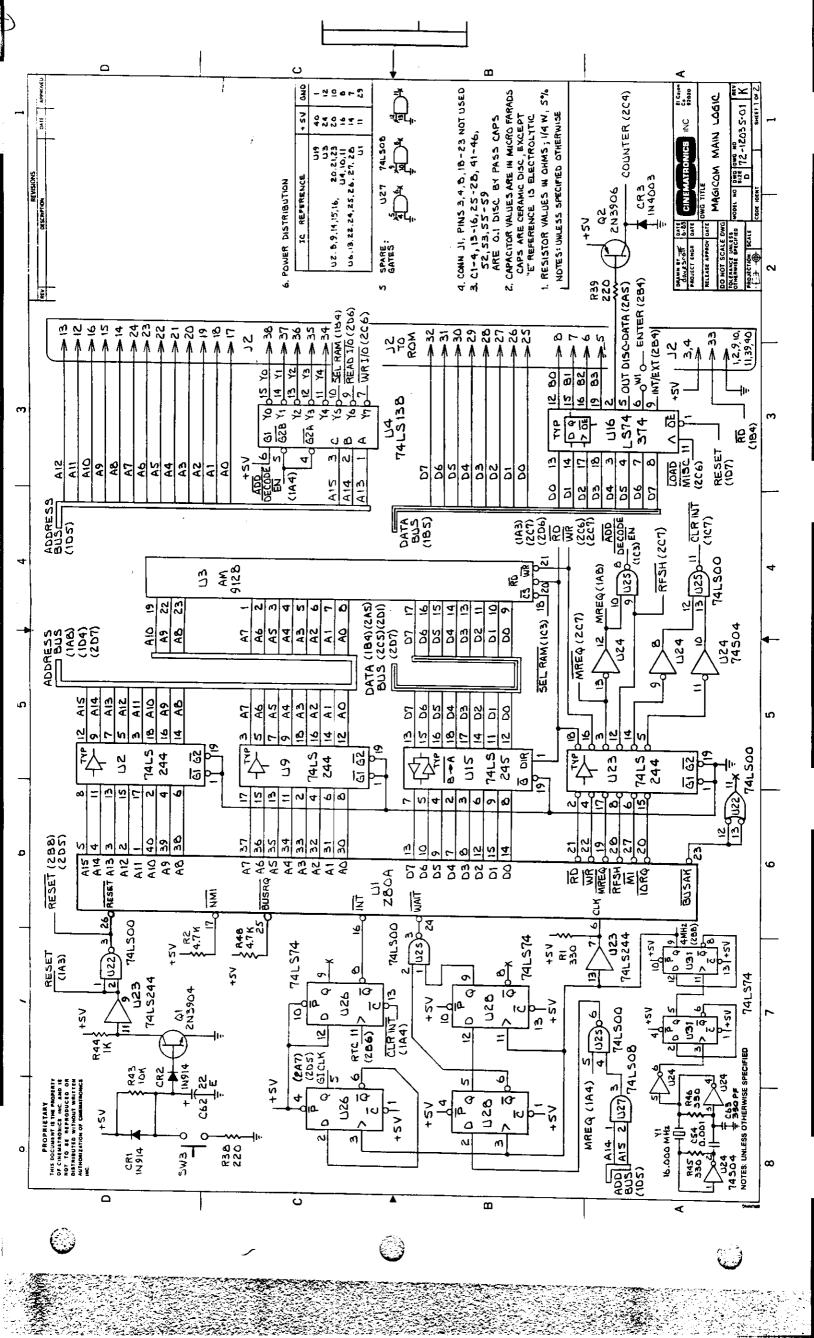
All of "K" above effective 10/10/83.

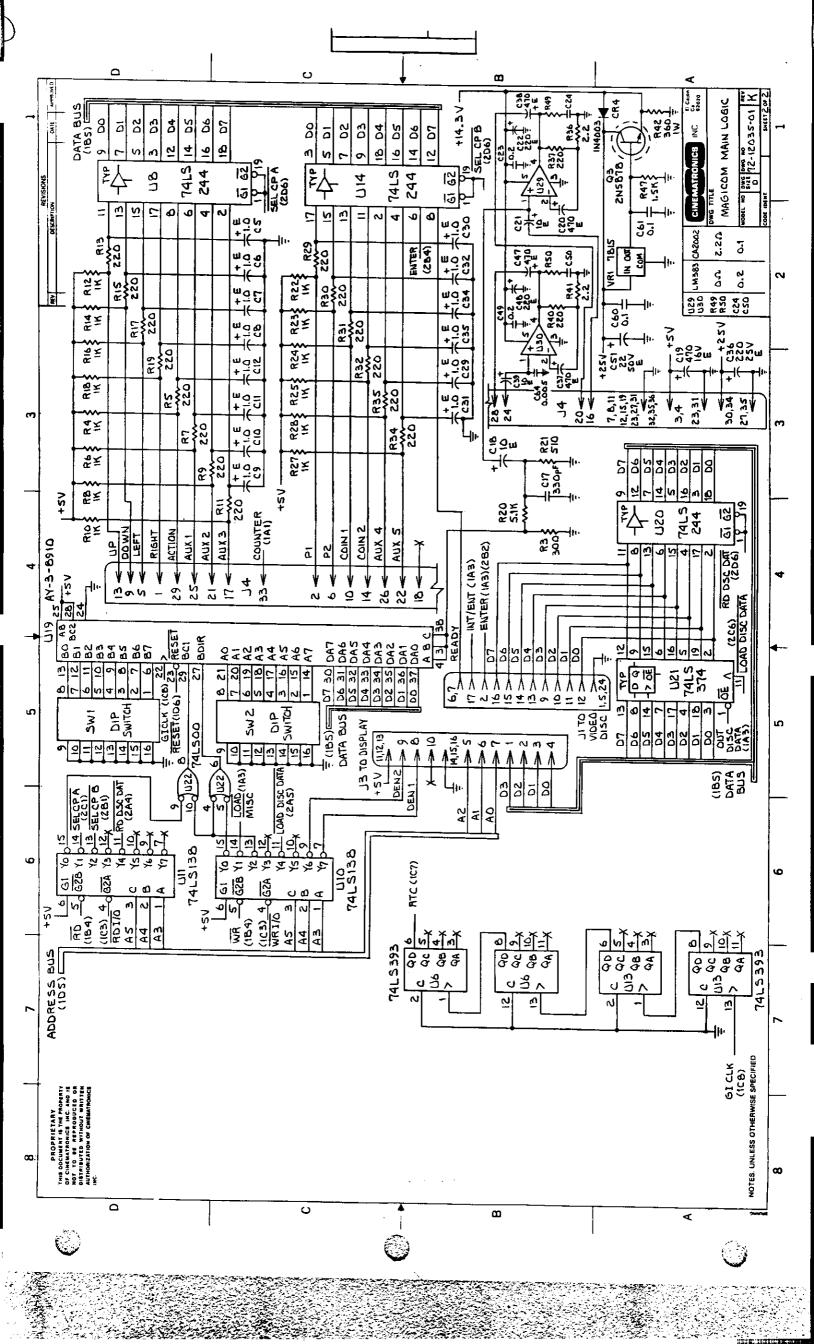
"K" revision schematic is for "C" revision printed circuit board used with LDV-1000 laser disc player.

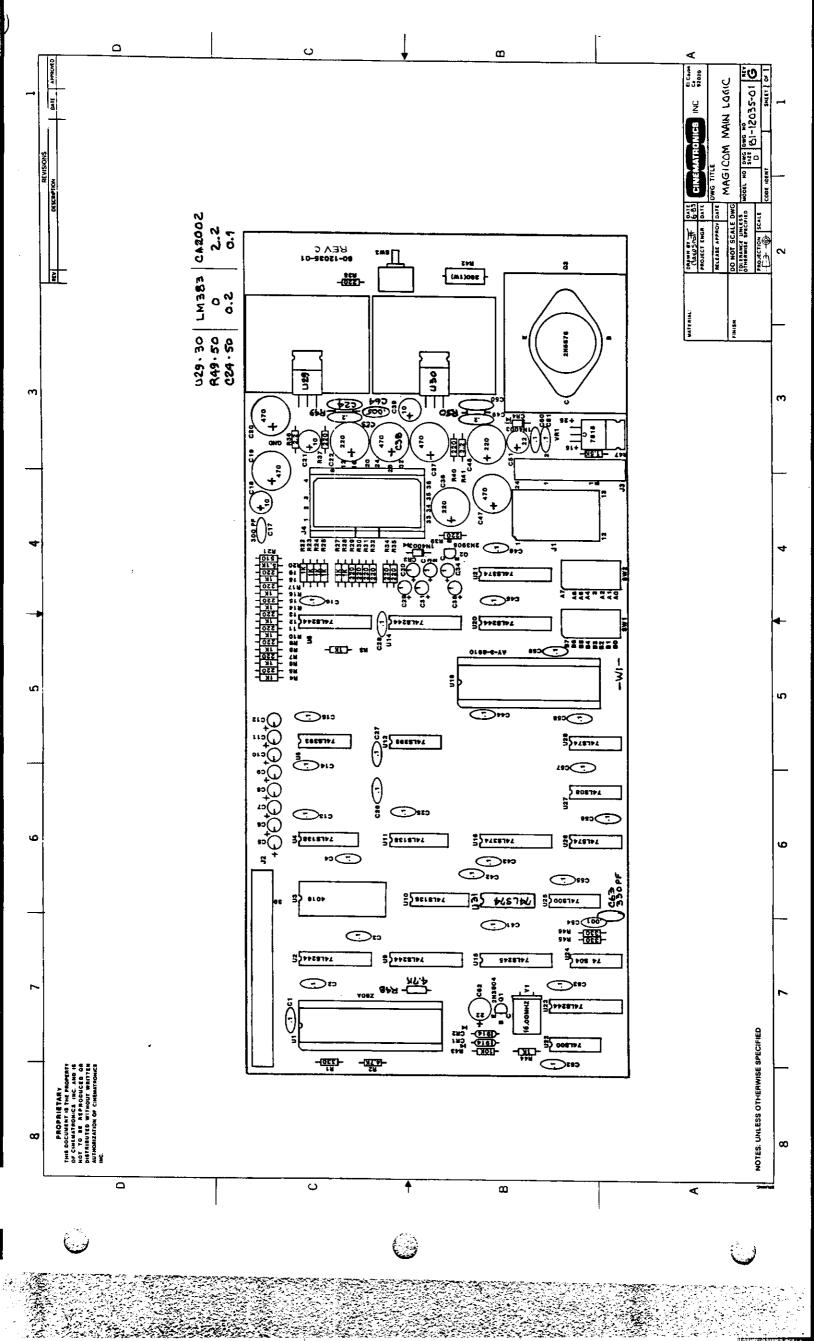


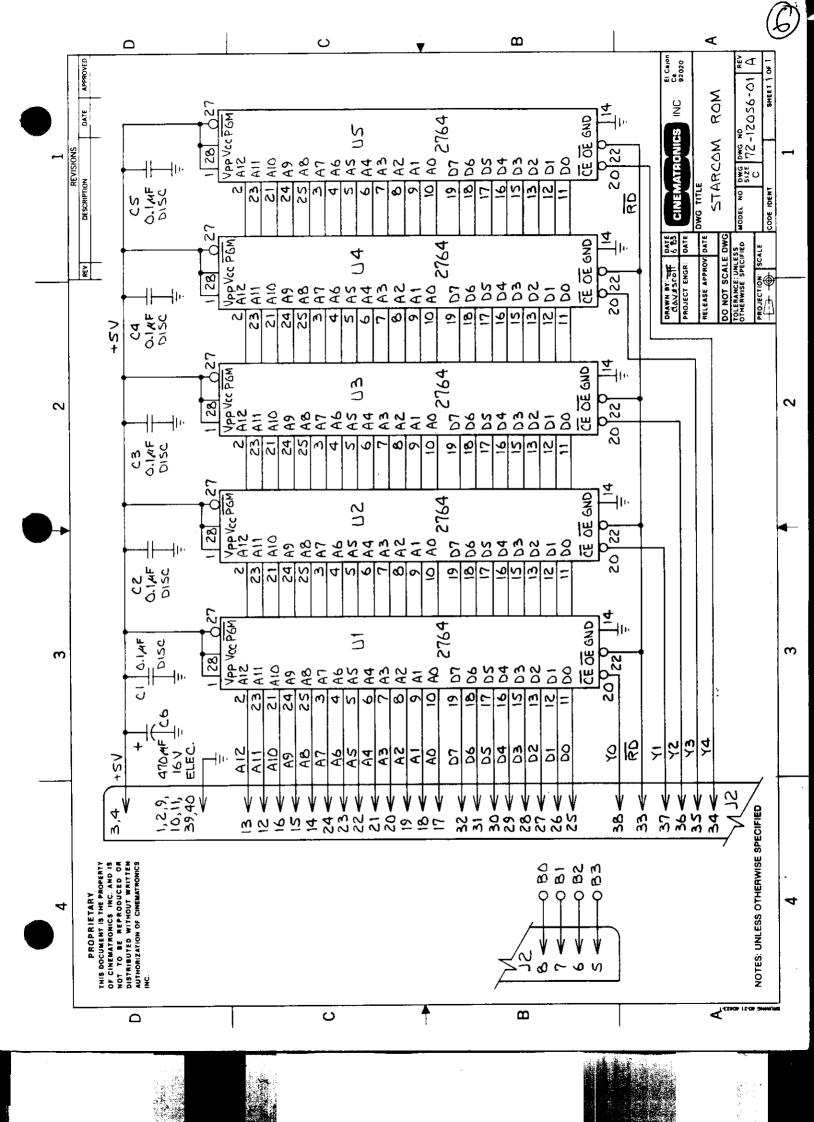


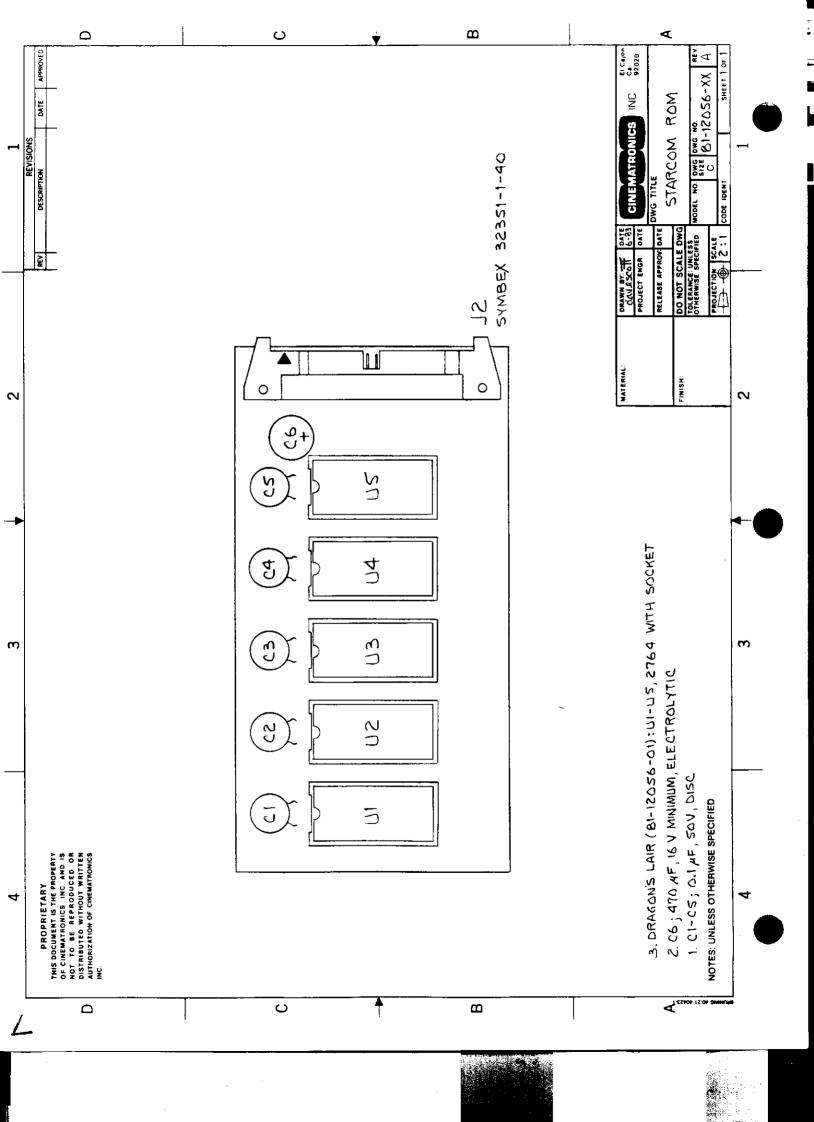


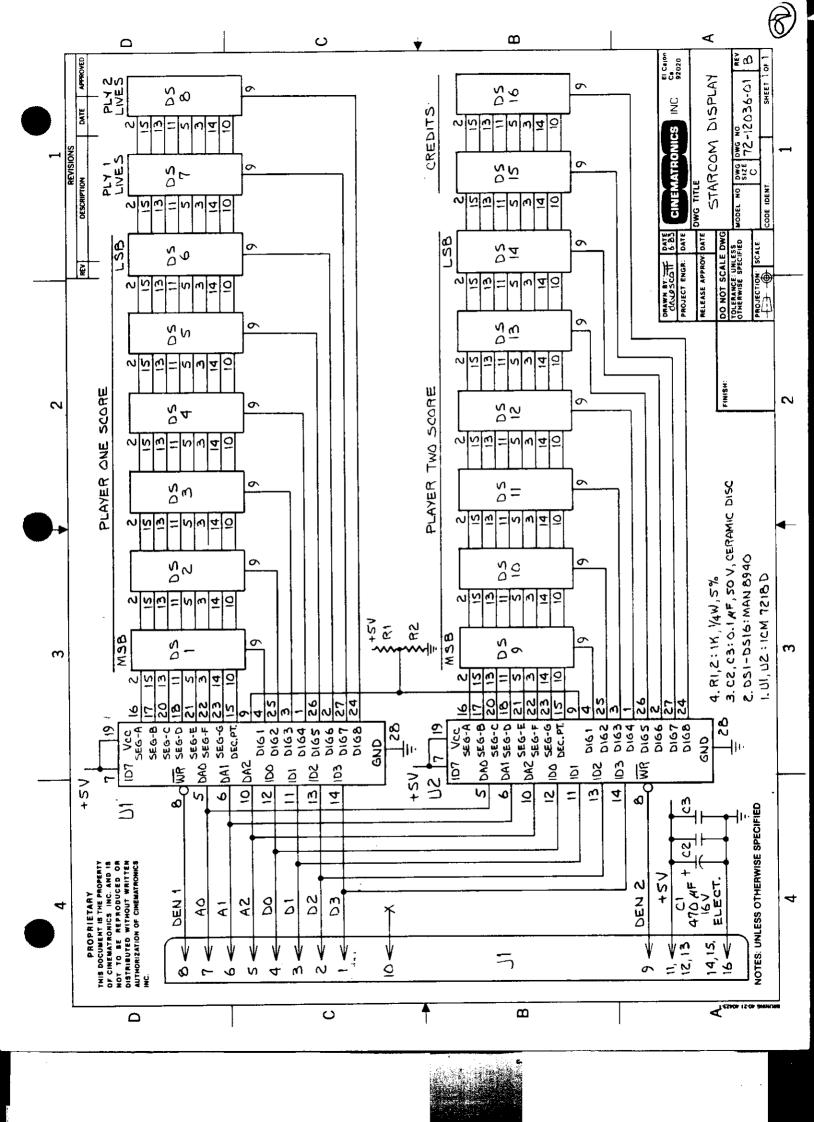


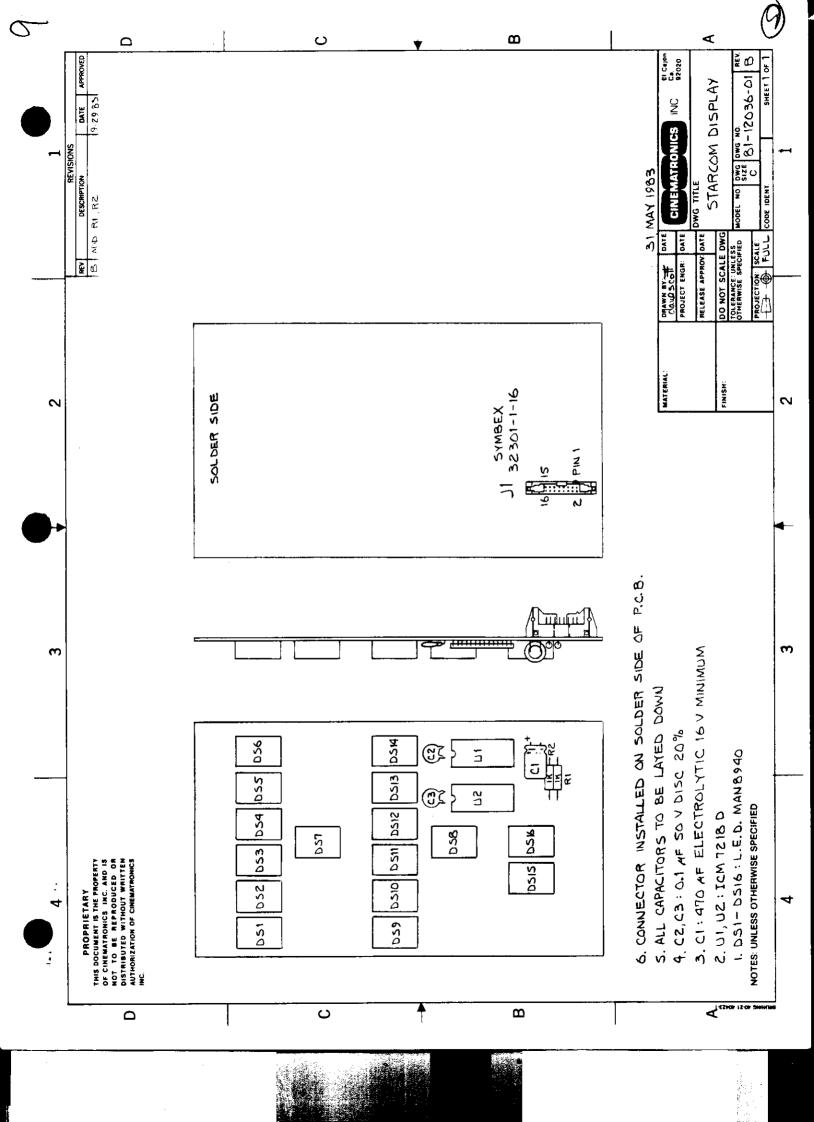


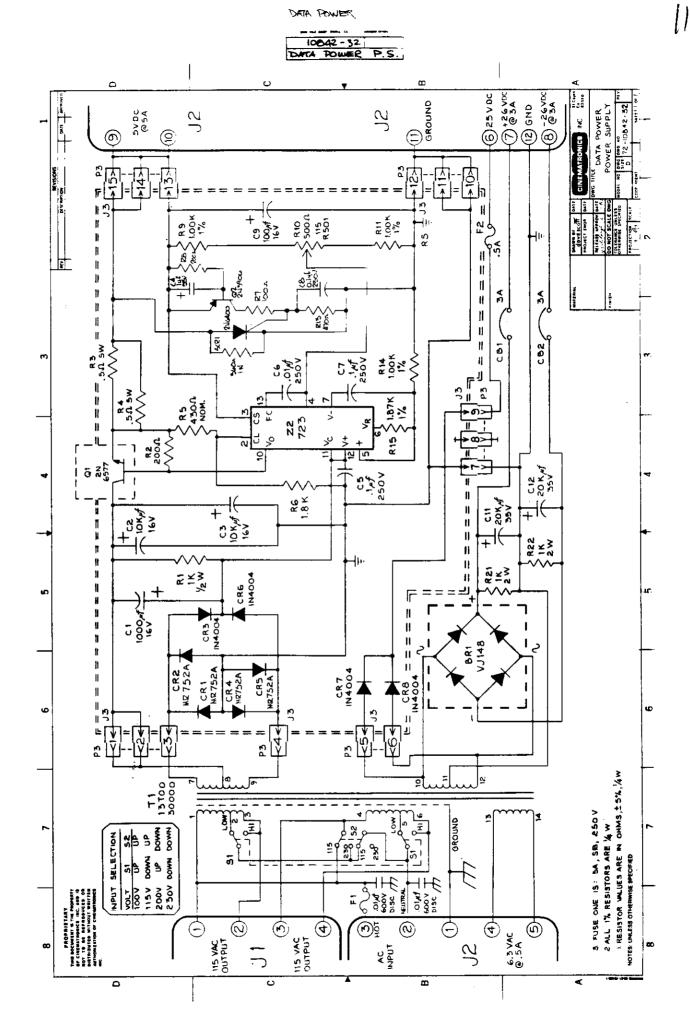


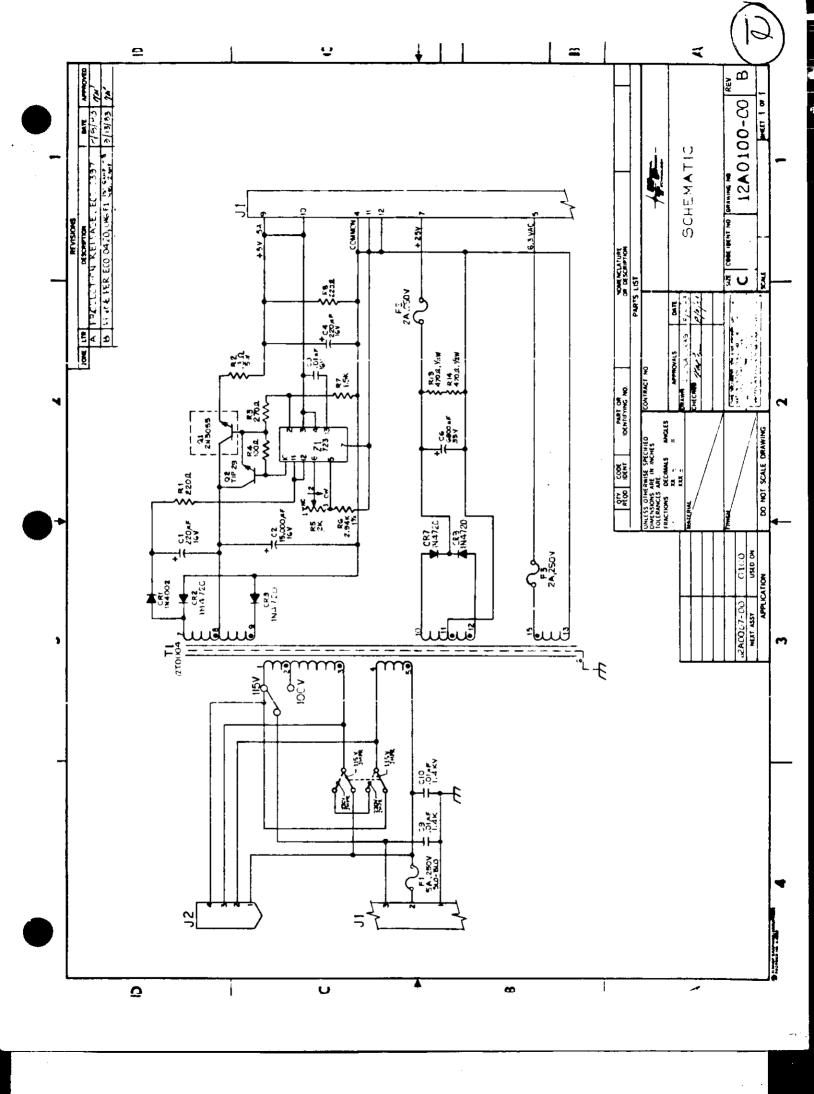


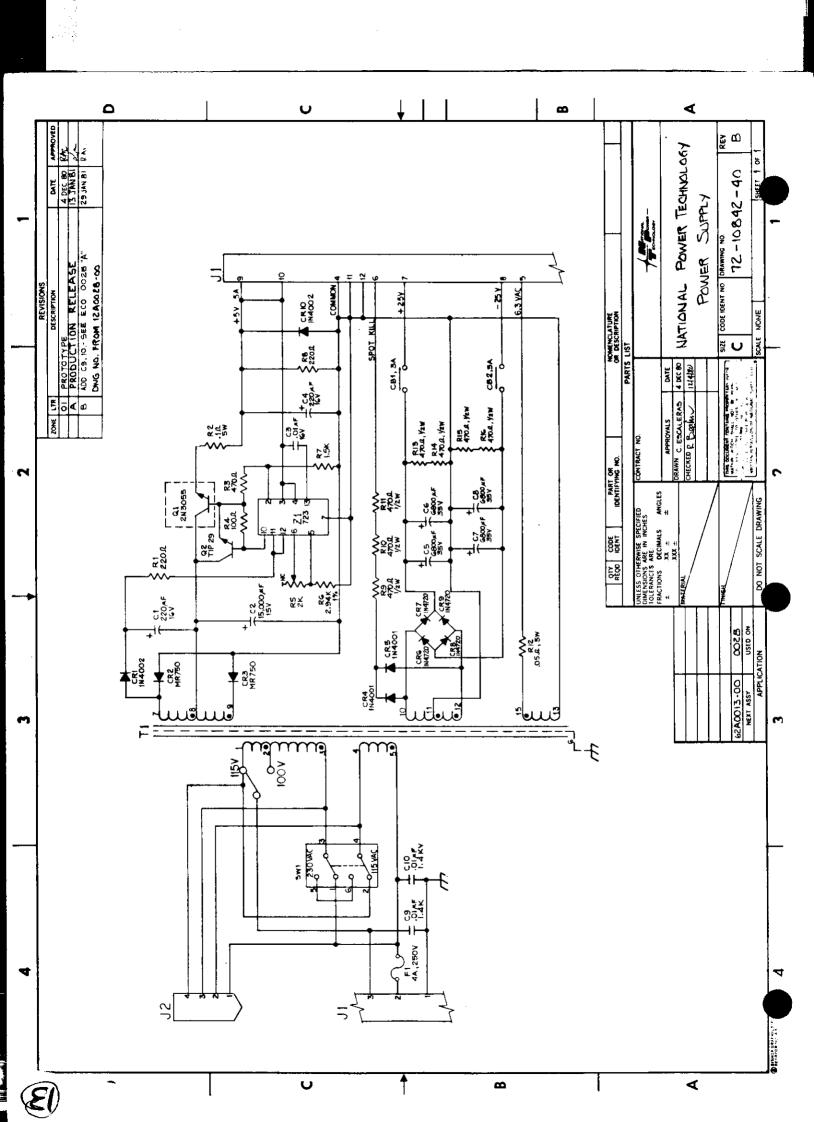


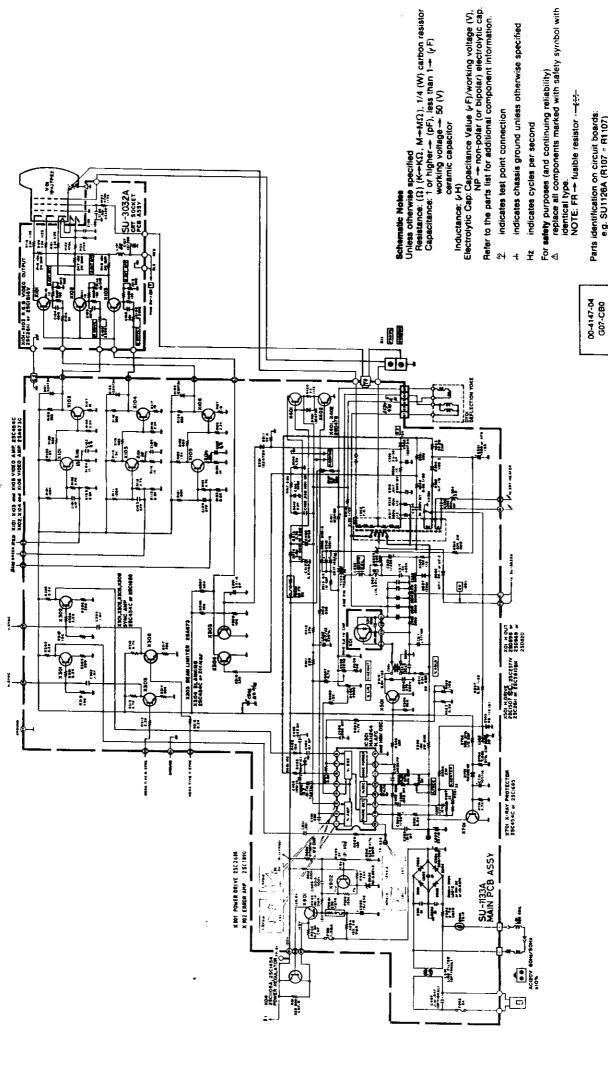




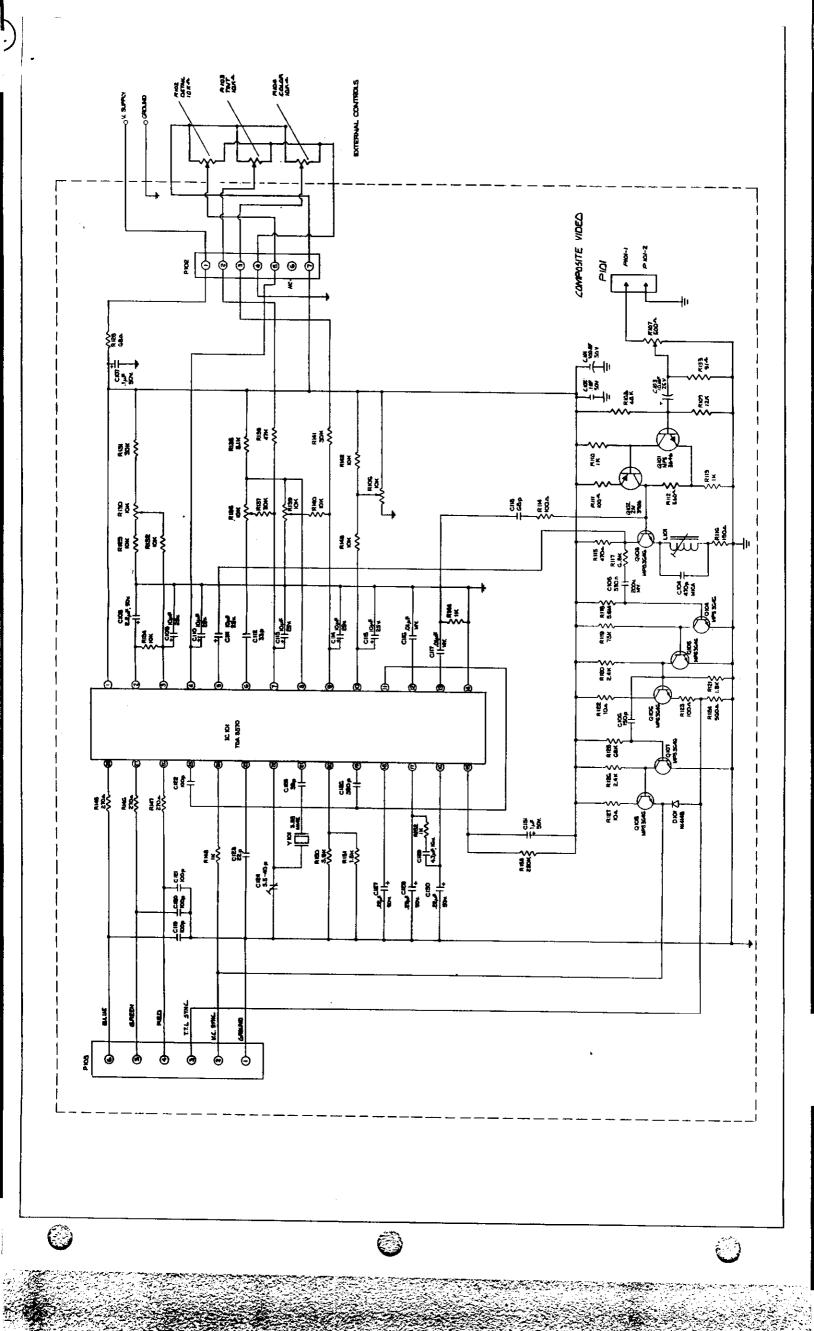






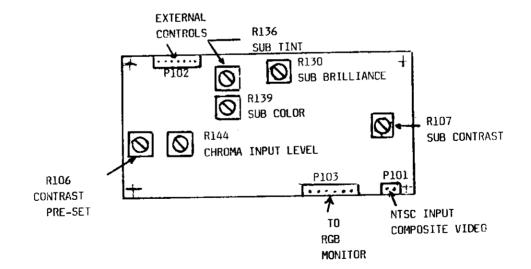


Parts identification on circuit boards: e.g. SU1126A (R107 = R1107) SU3030A (R113 = R3113)

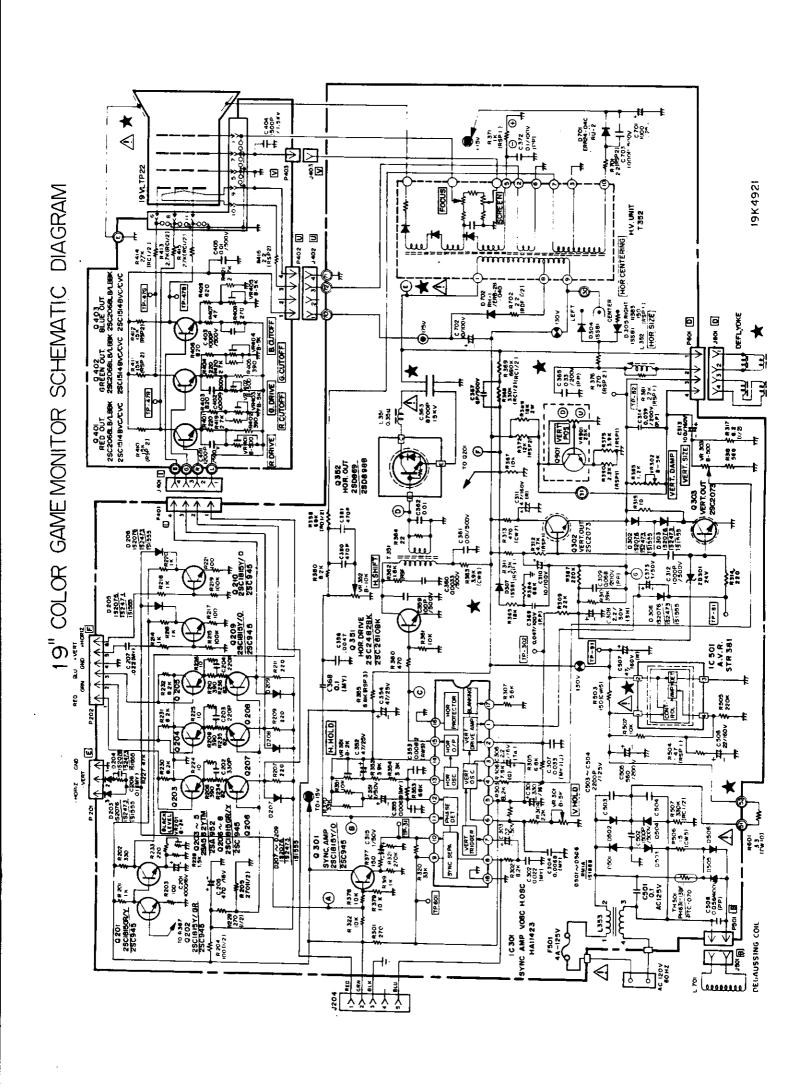


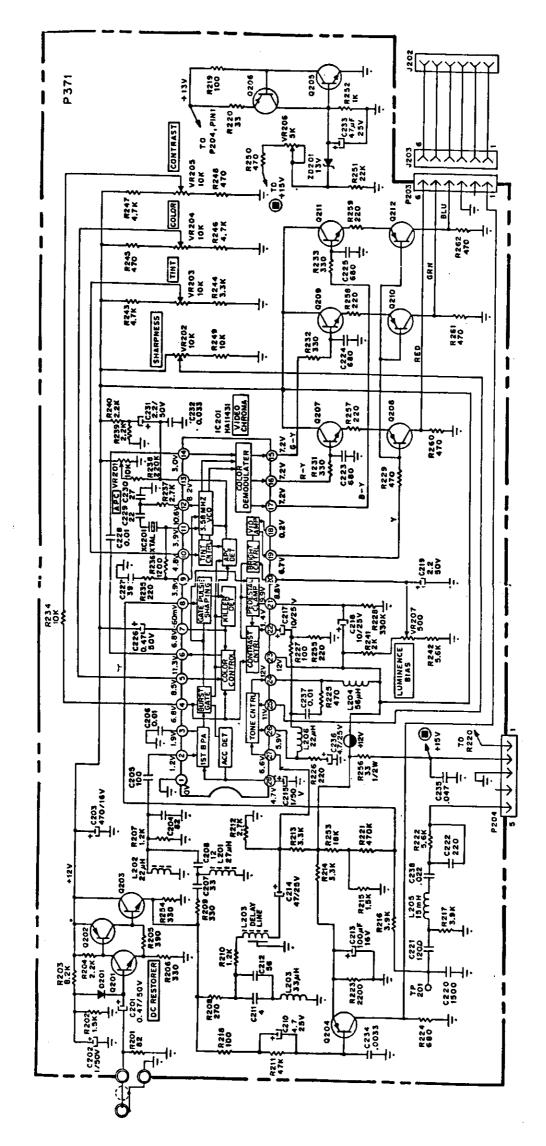
NTSC DECODER SPECIFICATIONS

Pin Outs P101-1 75 ohm Input P101-2 Ground P102-1 Vs Supply (16V) P102-2 External Tint Wiper Pl02-3 External Color Wiper Pl02-4 Grount to Control P102-5 External Detail Wiper Pl02-6 Not Used Pl02-7 Vcc to Control (12V) P103-1 Ground P103-2 Blanking Output Pl03-3 Positive Composite Sync. Pl03-4 Red Output P103-5 Green Output Pl03-6 Blue Output



c-/ 1





WELLS GARDNER NTSC DECODER SCHEMATIC

(19)

MAGICOM WIRING HARNESS

FROM	PIN	TO	PIN	SIGNAL
	HOT.	CM	COMMON	AC LINE HOT
\mathbf{LF}	HOT	SW		
SW	N/OPEN	PS1	3	AC LINE HOT
SW	N/OPEN	VDP	HOT	AC LINE HOT
\mathtt{LF}	${\tt NEUTRAL}$	PS1	2	AC LINE NEUTRAL
$_{ m LF}$	NEUTRAL	VDP	NEUTRAL	AC LINE NEUTRAL
PS2	1	ISO	PRI	115V AC #1 HOT
PS2	3	LAMP	HOT	115V AC #2 HOT
	3	FAN	НОТ	115V AC #2 HOT
PS2	3			115V AC #2 NOT 115V AC #1 NEUTRAL
PS2	2	ISO	PRI	
PS2	4	LAMP	NEUTRAL	
PS2	4	FAN	NEUTRAL	115V AC #2 NEUTRAL
MON	FRAME	LAMP	FRAME	FRAME GROUND
PS1	1	MON	FRAME	FRAME GROUND
LF	FRAME	PS1	1	FRAME GROUND
	FRAME	CPU	FRAME	FRAME GROUND
LF		COIN	3	FRAME GROUND
CPU	FRAME			FRAME GROUND
COIN	3	OCP	9 7	FRAME GROUND
OCP	9	CP	/	FRAME GROUND
PS1	9	CPU	3	+5V
PSl	10	CPU	4	+5V
PS1	11	CPU	7	+5V RETURN
PSl	7	CPU	30	+25V
PSl	12	CPU	8	+25V RETURN
PSI	12	CFO	O	
PS1	5	COIN	8	6.3V AC LAMPS
PS1	4	COIN	9	6.3V AC LAMPS RETURN
COIN	i	CPU	10	COIN SLOT O
COIN	2	CPU	14	COIN SLOT 1
	2 7	CPU	11	COIN RETURN
COIN	/	CFO	++	COIN ADIOM
CP	2	CPU	6	2 PLAYER START
CP	2 3	CPU	2	1 PLAYER START
CP	4	CPU	ī	JOYSTICK RIGHT
	5	CPU	29	SWORD/ACTION
CP	6	CPU	5	JOYSTICK LEFT
CP			9	JOYSTICK DOWN
CP	8	CPU		JOYSTICK UP
CP	9	CPU	13	
CP	1	CPU	12	CONTROL PANEL RETURN
OCP	4	CPU	33	COIN COUNTER
OCP	8	CPU	32	COIN COUNTER RETURN
OCP	3	VDP	CENTER	DISC AUDIO (LEFT)
	1	VDP	SHIELD	DISC AUDIO RETURN (LEFT)
OCP			CENTER	DISC AUDIO (RIGHT)
OCP	5	VDP	CENTER	DISC MODIO (MIGHT)

1.9.84

OCP	7	VDP	SHIELD	DISC AUDIO RETURN (RIGHT)
OCP	2	CPU	24	VOLUME OUT (LEFT)
OCP	1	CPU	23	VOLUME OUT RETURN (LEFT)
OCP	6	CPU	16	VOLUME OUT (RIGHT)
OCP	7	CPU	15	VOLUME OUT RETURN (RIGHT)
CPU	28	SPKR	L+	SPEAKER (LEFT)
CPU	27	SPKR	L-	SPEAKER RETURN (LEFT)
CPU	20	SPKR	R+	SPEAKER (RIGHT)
CPU	19	SPKR	R-	SPEAKER RETURN (RIGHT)

PS1 = POWER SUPPLY 12 PIN CONNECTOR PS2 = POWER SUPPLY 4 PIN CONNECTOR

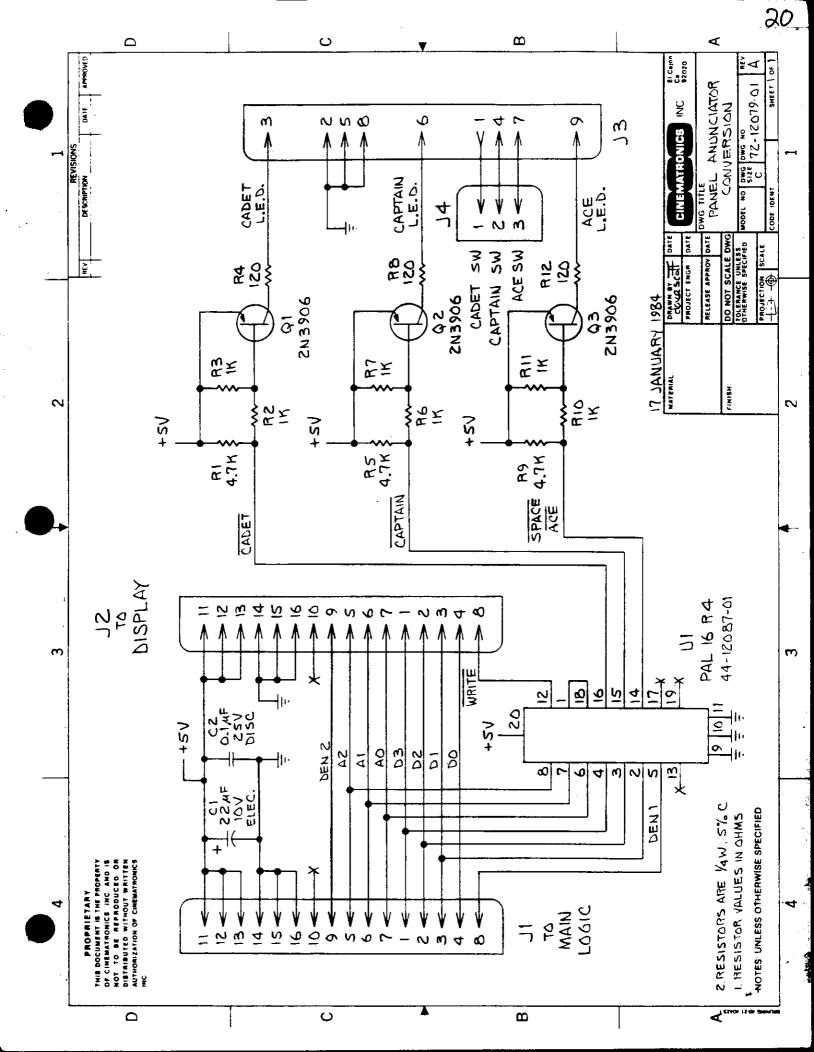
FAN = COOLING FAN
SW = POWER SWITCH
CPU = LOGIC BOARD
LAMP = FLORESCENT LAMP
CP = CONTROL PANEL

SPKR = SPEAKERS COIN = COIN DOOR MON = MONITOR

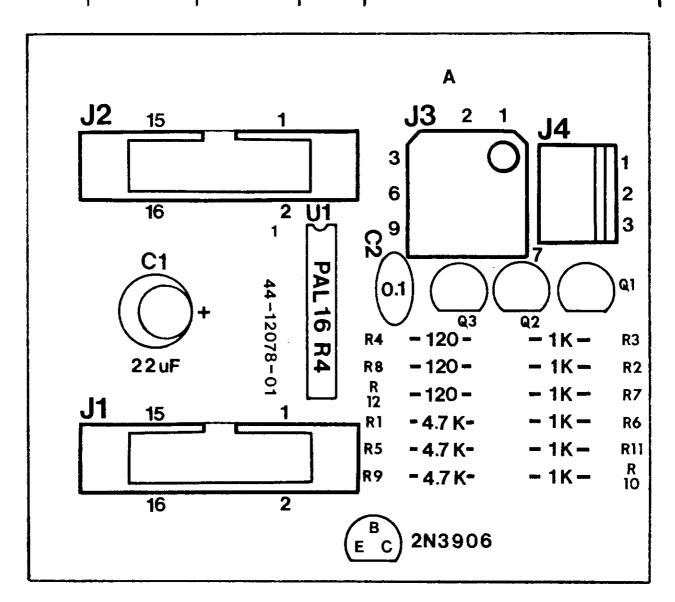
VDP = VIDEODISC PLAYER LF = AC LINE FILTER

OCP = OPERATOR CONVENIENCE PANEL ISO = MONITOR ISOLATION TRANSFORMER

NOTE: GAMES EQUIPPED WITH PR7820 DISC PLAYERS HAVE DISC PLAYER FRAME GROUND TIED TO LINE FILTER FRAME GROUND.



APPLICATION		REVISIONS				
NEXT ASSY	USED ON	APPROVED	DATE	DESCRIPTION	REV	
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UNLESS OTHERWISE	APPROVALS	DATE	CINEMATRONICS			El Cajon	
SPECFIED, DIMENSIONS ARE IN INCHES.	BY davescott	1.28.84			S INC.	Ca.	
TOLERANCES ARE:	СНК		92020				
FRAC. DEC. ANGL. + .XX± +	APPD					100	
.XXX±	APPD		PANEL ANNUNCIATOR BOARD				
MATERIAL	APPD		CONVERSION				
FINISH				WING NUMBER	R 81-120	279-01	
DO NOT SCALE DWG			SCALE 2	:1	SHEET	1 OF 1	

