

Bally Midway's MCR III

Notes from DLH on Jan 19th, 2000

Schematics scanned at 600 dpi/lineart
All other at 300 dpi/lineart

This manual had the same exact first 19 pages as the manual
for MCR II (MCR2-Part1.pdf & MCR2-Part2.pdf)

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Page 31 doesn't exist in my original copy
*if someone has it, please scan or email me

You can not imagine what a pain these yellow
Schematics were to scan ☹

Enjoy

Bally Midway's

MCR II-III Systems

General Information and Troubleshooting Procedures Micro-Processor Video Games



Bally **MIDWAY MFG. CO.**

10601 W. Belmont Avenue
Franklin Park, Illinois 60131
U.S.A.



Phone: (312) 451-9200 Cable Address: MIDCO Telex No.: 72-1596
VIDEO 800/323-7182 PINBALL 800/323-3555

July, 1983

Form No. 00381-8306

GAME VOLUME ADJUSTMENT

CONTROL. (See Figure 1)

The game volume control pot is located just inside the cabinet on the right side of the coin door frame. There is only one pot. For adjustment, it may be reached through the coin door on **ALL** models.

To make the sounds louder, turn the pot clockwise as you face it ().

To make the sounds **less** loud, turn the pot counter-clockwise as you face it ().

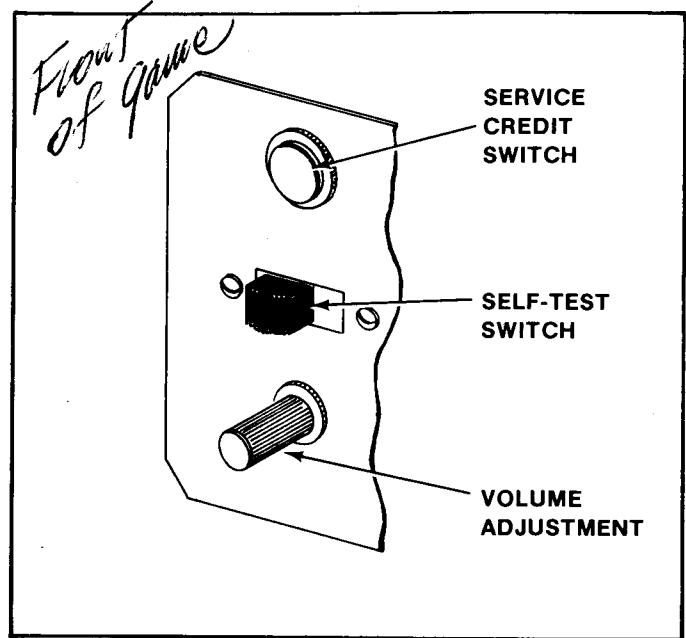


Figure 1 Game Volume Adjustment Control

OPTION SETTINGS:

To change the most common option settings, you **DO NOT** have to take the game apart or go into the cabinet and hunt for tiny switches on P.C. boards. These most common options can be changed from the main console of the game while it is in the Self-Test mode. The Self-Test switch is located just inside the cabinet on the right side of the coin door frame as you face it.

When changing any options, **ALWAYS** perform the Self-Test and play the game to be sure the ones selected are working properly. Of course, when you must change one of the switches that is located on one of the game's P.C. boards, it is also recommended that you perform the Self-Test and play the game to be sure the switches have worked properly and that no switches were accidentally moved that were not meant to be. (These switches are small and this can happen.)

The P.C. Board option switch settings, and what they will make the game do are shown in Figure 3. These switches are **MAINLY INTENDED** for use by a technician who is checking and/or performing tests on the game. See Figure 2 for option switch locations.

NOTE: In order to set the option switches located on the game's P.C. Boards, these Boards need not be removed from their card rack.

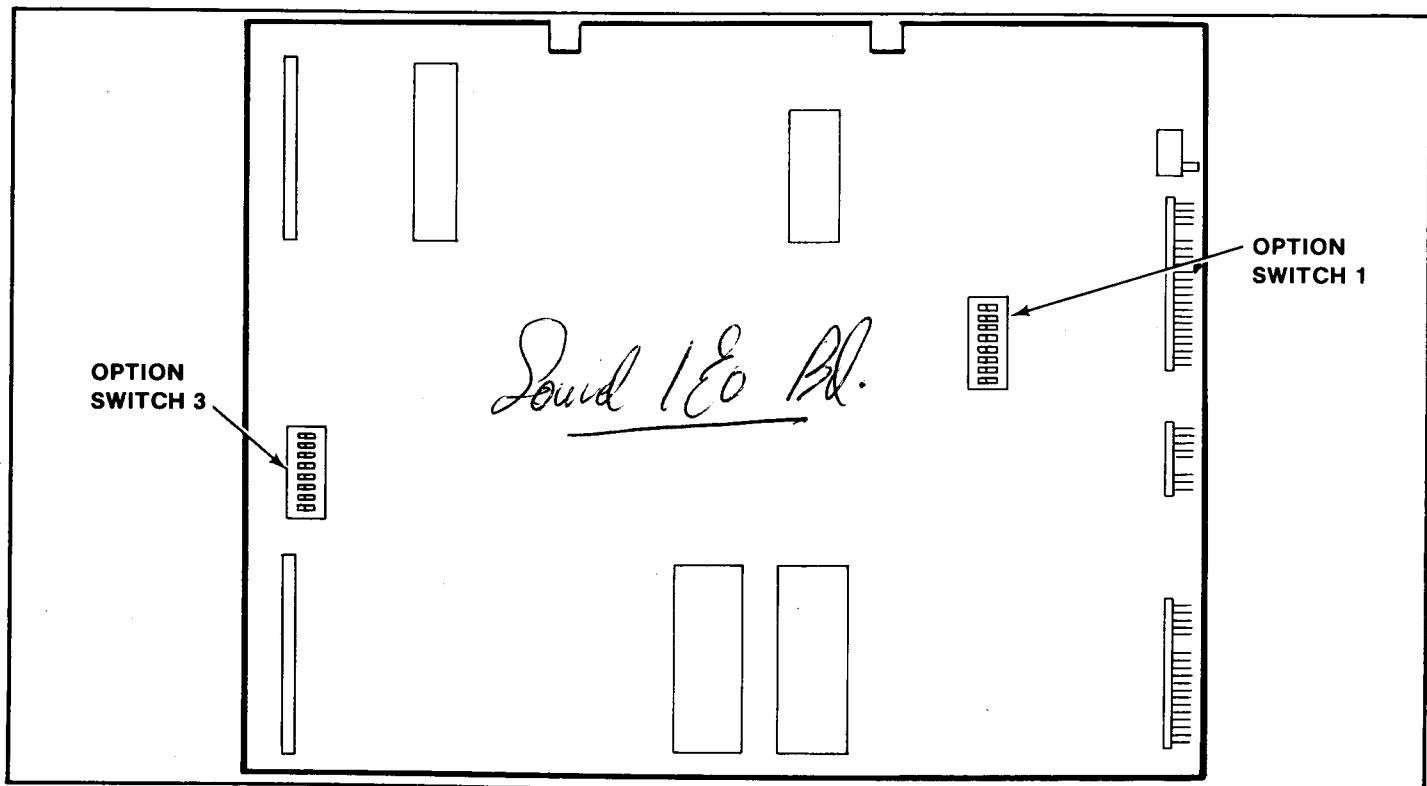


Figure 2 Option Switch Location

OPTION SWITCH SETTINGS

SWITCH NO. 1 — AT B 3 — LOCATED ON SOUND I/O P.C. BOARD

	SW#1	SW#2	SW#3	SW#4	SW#5	SW#6	SW#7	SW#8	SW#9	SW#10
2 COIN METERS	ON									NOT
1 COIN METER	OFF									USED
MINI/UPRIGHT COCKTAIL TABLE		ON								
		OFF								
BUY IN ALLOWED NO BUY IN (Explain)				ON						
				OFF						
FREEZE VIDEO NORMAL OPERATION										ON
										OFF

cause picture flip v/r

Bench Aid - must be off

SWITCH NO. 3 — AT D 14 — LOCATED ON SOUND I/O P.C. BOARD

	SW#1	**SW#2	**SW#3	**SW#4	(BENCH TESTING)
NORMAL OPERATION SOUND I/O DIAGNOSTIC MODE		OFF			
		ON			
NORMAL OPERATION RAM/ROM TEST INDICATES TEST RESULTS VIA YELLOW LED ON SOUND I/O BOARD: FAST FLASH = BAD ROM SLOW FLASH = BAD RAM		OFF	THE REMAINDER OF MOST		
		ON	COMMON OPTION SETTINGS ARE CON-		
			DUCTED DURING THE MACHINE SETUP		
			PORTION OF THE SELF-TEST MODE AND		
			WILL BE COVERED IN DETAIL IN THAT		
			SECTION OF THIS MANUAL		
NORMAL OPERATION OSCILLATOR TEST		OFF			
		ON			
NORMAL OPERATION FILTER TEST			OFF		
			ON		

**NO EFFECT IF SW#1 OF SWITCH NO. 3 IS IN THE "OFF" POSITION.

Figure 3 Option Switch Settings

SELF-TEST MODE

The Self-Test mode is a special mode for checking game play statistics as well as game switches and computer functions. It is the easiest and best way to check for proper operation of the entire game.

NOTE: Putting the game into Self-Test **WILL NOT** cause the game to erase any CREDITS it has in its memory when the Self-Test mode is entered.

You may begin a Self-Test at any time by sliding the Self-Test switch to the "ON" position after the power to the game is on (the Self-Test switch is located just inside the cabinet on the right side of the coin door frame as you face it). When this is done, the game will react as follows:

1. If the game is in the Attract mode when the Self-Test switch is moved to the "ON" position, it will finish the sequence and then go into the Self-Test mode. This is illustrated by the display of the Self-Test Mode Menue on the monitor screen.
2. If the game is in the Ready-To-Play mode or the Play mode when the Self-Test switch is slid to the "ON" position, it **WILL NOT** go into the Self-Test mode until **AFTER** the players' last TRON has been eliminated (the game **MUST** be over). At this point, the game will go into the Self-Test mode. Again, this is illustrated by the display of the Self-Test Mode Menue on the monitor screen.
3. The fastest way to enter the Self-Test mode is to slide the Self-Test switch to the "ON" position and then activate the "TILT" switch located on the back side of the coin door just below the lock mechanism. The game will then **IMMEDIATELY** go into the Self-Test mode.

The Self-Test mode has eight (8) major categories as illustrated by Figure 4.

1. It is easy to select what category you want to enter. By pushing forward or pulling backward on the controller stick, the Cursor at the left of the screen can be moved UP and DOWN, (forward=UP) and (backward=DOWN), until it is in front of the category you want to test. Release the controller stick at this time.
2. After the Cursor has been positioned, pull the trigger on the controller stick and the monitor screen will display the test category you have selected.

NOTE: There is one exception to this. If you position the Cursor in front of the "PRESET" category on the Self-Test Mode Menue, when you pull the trigger on the controller stick — **EVERYTHING**, I repeat — **EVERYTHING**; including **ALL** information in the "BOOKKEEPING" mode, and **ALL operator selected options**, will be set back to zero "0" and to the factory recommended settings — **respectively**.

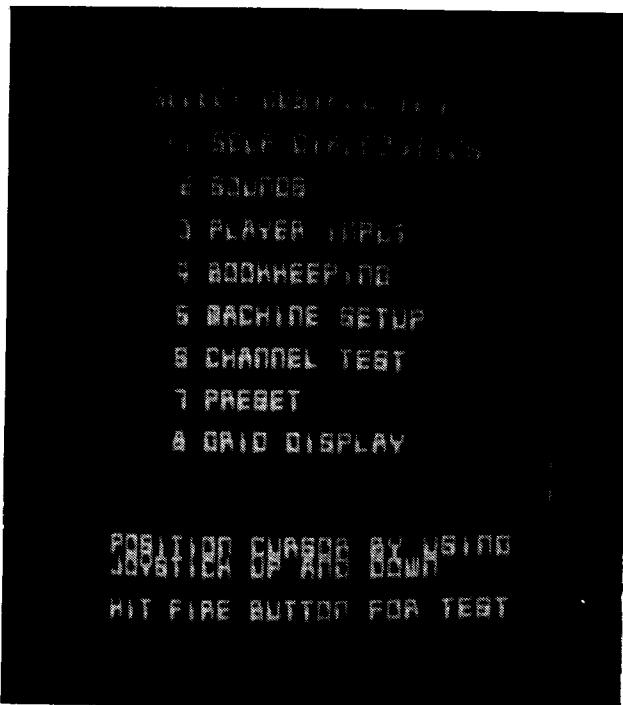


Figure 4 Self-Test—Menue

- Once you are **IN** one of the Self-Test mode categories, **FOLLOW THE ON-SCREEN INSTRUCTIONS TO COMPLETE THE TEST**.
- 3. The next group of figures shows the **CORRECT** screen presentation for **EACH** category of the Self-Test mode.

During the SELF DIAGNOSTICS section of the Self-Test mode, you will **first** see a cross hatch pattern on the screen for about 1/2 second. **Second**, you will see a lot of different colored bars shown on the monitor screen. These bars will be UNpainted one at a time from the top down. **Third**, you will see the screen painted Red, Blue, and Green in bars from the top down. **Fourth**, another group of colored bars is displayed. This sequence is repeated several times. And finally, this sequence is replaced by this message: "**HIT FIRE BUTTON TO EXIT**". If the Fire button is not hit, the test will repeat itself. This feature was designed into the game to enable over-night testing for an intermittent hardware problem.

If the SELF DIAGNOSTICS find one or more bad ROM or RAM chips: instead of going through what is described above, the game will give you a written message as to which parts are bad. This message includes their I.D.'s and their P.C. Board locations.

During the SOUNDS sections of the Self-Test mode, the game will give a display which looks like that shown in Figure 5.

- In this category, each of the game's 24 separate sounds can be checked individually in any order — or — you can tell the game to check them all in order — 3 through 26.

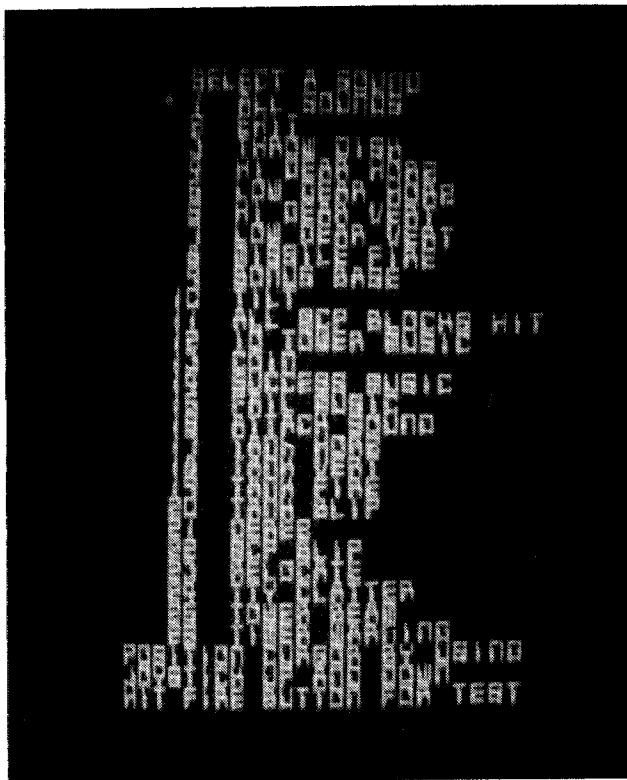


Figure 5 Self-Test—Sounds

As the Player Input Switches and Devices are activated, the Switch or Device activated is spelled out in the space indicated.

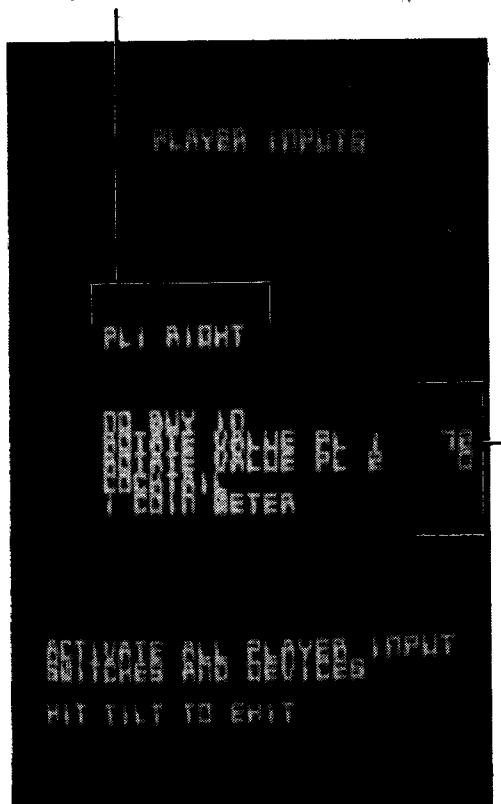


Figure 6 Self-Test—Player Input

During the PLAYER INPUT section of the Self-Test mode, the game will give a display which looks like that shown in Figure 6.

- In this category, each of the game's player operated controls — including the coin switches on the back side of the coin door — may be checked individually. A game sound will be heard as each switch/control is actuated. If no game sound is heard, that switch/control is either not working, miswired, or disconnected. Check it out thoroughly.

During the BOOKKEEPING section of the Self-Test mode, the game will give a display which looks like that shown in Figure 7.

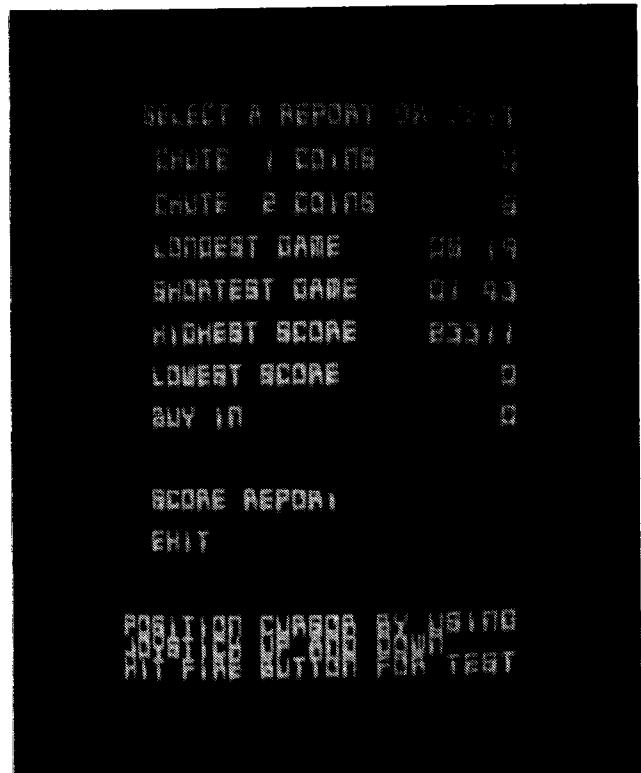


Figure 7 Self-Test—Bookkeeping

- In this category a basic bookkeeping function is performed. And with the selection of the "TIME REPORT" and the "SCORE REPORT", detailed breakdowns of game times and scores may be obtained.

In the TIME REPORT and SCORE REPORT sections of the BOOKKEEPING mode, the game will give displays which look like those shown in Figures 8 and 9 respectively.

TIME REPORT	
0 TO 10 SEC	0
10 TO 20 SEC	0
20 TO 30 SEC	0
30 TO 40 SEC	0
40 TO 100 SEC	1
100 TO 160 SEC	0
160 TO 180 SEC	0
180 TO 200 SEC	0
2 TO 4 MIN	0
4 TO 6 MIN	1
6 TO 8 MIN	1
OVER 8 MIN	0

HIT FIRE BUTTON TO EXIT

Figure 8 Self-Test—Time Report

SCORE REPORT	
0 TO 100 PTS	1
100 TO 1,000,000 PTS	0
1,000,000 TO 2,000,000 PTS	1
2,000,000 TO 3,000,000 PTS	1
3,000,000 TO 4,000,000 PTS	0
4,000,000 TO 5,000,000 PTS	0
5,000,000 TO 7,500,000 PTS	0
7,500,000 TO 10,000,000 PTS	0
10,000,000 TO 15,000,000 PTS	0
OVER 1,500,000 PTS	0

HIT FIRE BUTTON TO EXIT

Figure 9 Self-Test—Score Report

During the SETUP OPTIONS section of the Self-Test mode, the game will give a display which looks like that shown in Figure 10.

SETUP OPTIONS

- * COINS PER BASE
- * CREDITS FOR BASE
- CREDIT CRITERIA
- * CREDITS FOR PAGES
- * EXTRA PAGE AT 10000 POINTS
- * DIFFICULTY LEVEL
- EXIT

USE JOYSTICK UP AND DOWN TO POSITION CURSOR
USE D-PAD TO ALTER

* = Factory recommended settings.

Figure 10 Self-Test—Setup Options

- In this category, all common game options may be changed from the control console: coins per credit, credits per base, bonus base(s) awarded at, difficulty level --, and so on.

The Difficulty Level setting has a range of 1 to 9 with 1 representing the easiest level of play and 9 representing the most difficult level of play. One is the factory recommended setting.

During the CHANNEL TEST section of the Self-Test mode, the game will give a display which looks like that shown in Figure 11.

CHANNEL TEST

- CHANNEL 1
- CHANNEL 2
- * CHANNEL 3
- CHANNEL 4
- CHANNEL 5
- CHANNEL 6

HIT FIRE BUTTON TO EXIT

Figure 11 Self-Test—Channel Test

- In this category, the game conducts a test of its SOUND SYSTEM.

A Glossary of Microprocessor Terms

MICROPROCESSOR — one or several microcircuits that perform the function of a computer's CPU. Sections of the circuit have arithmetic and comparative functions that perform computations and executive instructions.

CPU — central-processing unit. A computing system's "brain", whose arithmetic, control and logic elements direct functions and perform computations. The microprocessor section of a microcomputer is on one chip or several chips.

PROM — programmable read-only memory. User permanently sets binary on-off bits in each cell by selectively fusing or not fusing electrical links. Non-erasable. Used for low-volume applications.

EPROM — erasable, programmable, read-only memory. Can be erased by ultraviolet light bath, then reprogrammed. Frequently used during design and

development to get programs debugged, then replaced by ROM for mass production.

ROM — read-only memory. The program, or binary on-off bit pattern, is set into ROM during manufacture, usually as part of the last metal layer put onto the chip. Nonerasable. Typical ROM's contain up to 16,000 bits of data to serve as the microprocessor's basic instructions.

RAM — random-access memory. Stores binary bits as electrical charges in transistor memory cells. Can be read or modified through the CPU. Stores input instructions and results. Erased when power is turned off.

LSI — large scale integration. Formation of hundreds or thousands of so-called gate circuits on semiconductor chips. Very large scale integration (VLS) involves microcircuits with the greatest component density.

MOS — metal-oxide semiconductor. A layered construction technique for integrated circuits that achieves high component densities. Variations in MOS chip structures create circuits with speed and low-power requirements, or other advantages (static will damage a MOS chip).

Introduction to the Z-80 CPU

The term "microcomputer" has been used to describe virtually every type of small computing device designed within the last few years. This term has been applied to everything from simple "micropogrammed" controllers constructed out of TTL MSI up to low end minicomputers with a portion of the CPU constructed out of TTL LSI "bit slices." However, the major impact of the LSI technology within the last few years has been with MOS LSI. With this technology, it is possible to fabricate complete and very powerful computer systems with only a few MOS LSI components.

The Zilog Z-80 family of components can be configured with any type of standard semiconductor memory to generate computer systems with an extremely wide range of capabilities. For example, as few as two LSI circuits and three standard TTL MSI packages can be combined to form a simple controller. With additional memory and I/O devices a computer can be constructed with capabilities that only a minicomputer could previously deliver.

New products using the MOS LSI microcomputer are being developed at an extraordinary rate. The Zilog Z-80 component set has been designed to fit into this market through the following factors:

1. The Z-80 is fully software compatible with the popular 8080A CPU.
2. Existing designs can be easily converted to include the Z-80.
3. The Z-80 component set is at present superior in both software and hardware capabilities to any other microcomputer system on the market today.
4. For increased throughput the Z80A operating at a 4 MHZ clock rate offers the user significant speed advantages.

Microcomputer systems are extremely simple to construct using Z-80 components. Any such system consists of three parts:

1. **CPU (Central Processing Unit)**
2. **Memory**
3. **Interface Circuits to peripheral devices**

The CPU is the heart of the system. Its function is to obtain instructions from the memory and perform the desired operations. The memory is used to contain instructions and in most cases data that is to be processed. For example, a typical instruction sequence may be to read data from a specific peripheral device, store it in a location in memory, check the parity and write it out to another peripheral device. Note that the Zilog component set includes the CPU and various general purpose I/O device controllers, while a wide range of memory devices may be used from any source. Thus, all required components can be connected together in a very simple manner with virtually no other external logic.

General Purpose Registers

There are two matched sets of general purpose registers, each set containing six 8-bit registers that may be used individually as 8-bit registers or as 16-bit register pairs by the programmer. One set is called BC, DE and HL while the complementary set is called BC', DE' and HL'. At any one time the programmer can select either set of registers to work with through a single exchange command for the entire set. In systems where fast interrupt response is required, one set of general purpose registers and an accumulator/flag register may be reserved for handling this very fast routine. Only a simple exchange command need be executed to go between the routines. This greatly reduces interrupt service time by eliminating the requirement for saving and retrieving register contents in the external stack during interrupt or subroutine processing. These general purpose registers are used for a wide range of applications by the programmer. They also simplify programming, especially in ROM based systems where little external read/write memory is available.

Arithmetic & Logic Unit (ALU)

The 8-bit arithmetic and logical instructions of the CPU are executed in the ALU. Internally the ALU communicates with the registers and the external

data bus on the internal data bus. The type of functions performed by the ALU include:

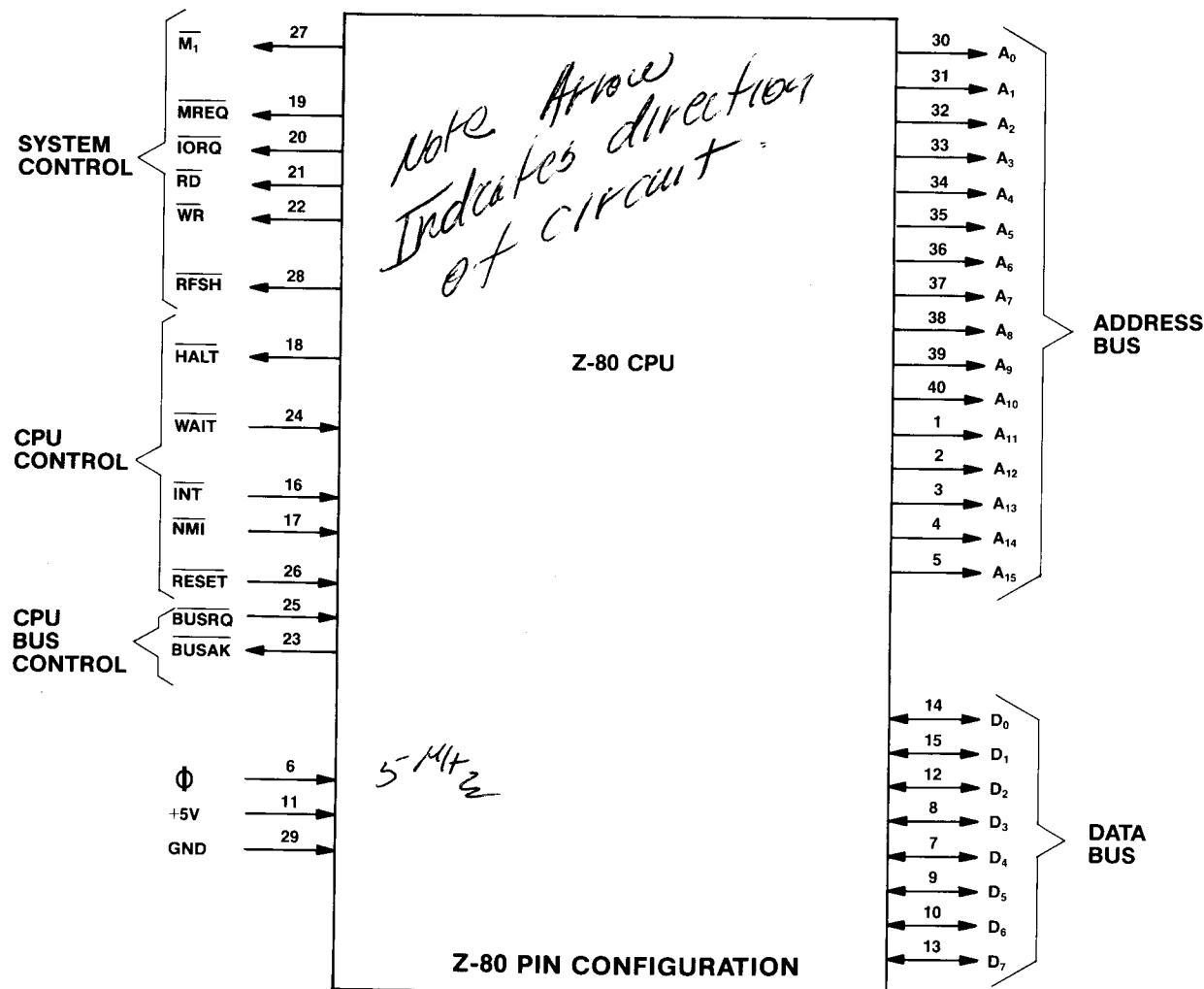
Add	Left or right shifts or rotates (arithmetic and logical)
Subtract	Increment
Logical AND	Decrement
Logical OR	Set bit
Logical Exclusive OR	Reset bit
Compare	Test bit

Instruction Register and CPU Control

As each instruction is fetched from memory, it is placed in the instruction register and decoded. The control sections performs this function and then generates and supplies all of the control signals necessary to read or write data from or to the registers, control the ALU and provide all required external control signals.

Z-80 CPU Pin Description

The Z-80 CPU is packaged in an industry standard 40 pin Dual In-Line Package. The I/O pins are shown in the below figure and the function of each is described.



A₀-A₁₅ **(Address Bus)**

Tri-state output, active high. A₀-A₁₅ constitute a 16-bit address bus. The address bus provides the address for memory (up to 64K bytes) data exchanges and for I/O device data exchanges. I/O addressing uses the 8 lower address bits to allow the user to directly select up to 256 input or 256 output ports. A₀ is the least significant address bit. During refresh time, the lower 7 bits contain a valid refresh address.

D₀-D₇ **(Data Bus)**

Tri-state input/output, active high. D₀-D₇ constitute an 8-bit bidirectional data bus. The data bus is used for data exchanges with memory and I/O devices.

M₁ **(Machine Cycle one)**

Output, active low. M₁ indicates that the current machine cycle is the OP code fetch cycle of an instruction execution. Note that during execution of 2-byte op-codes, M₁ is generated as each op code byte is fetched. These two byte op-codes always begin with CBH, DDH, EDH or FDH. M₁ also occurs with IORQ to indicate an interrupt acknowledge cycle.

MREQ **(Memory Request)**

Tri-state output, active low. The memory request signal indicates that the address bus holds a valid address for a memory read or memory write operation.

IORQ **(Input/Output Request)**

Tri-state output, active low. The IORQ signal indicates that the lower half of the address bus holds a valid I/O address for a I/O read or write operation. An IORQ signal is also generated with an M₁ signal when an interrupt is being acknowledged to indicate that an interrupt response vector can be placed on the data bus. Interrupt Acknowledge operations occur during M₁ time while I/O operations never occur during M₁ time.

RD **(Memory Read)**

Tri-state output, active low. RD indicates that the CPU wants to read data from memory or an I/O device. The addressed I/O device or memory should use this signal to gate data onto the CPU data bus.

WR **(Memory Write)**

Tri-state output, active low. WR indicates that the CPU data bus holds valid data to be stored in the addressed memory or I/O device.

RFSH **(Refresh)**

Output, active low. RFSH indicates that the lower 7 bits of the address bus contain a refresh address for dynamic memories and the current MREQ signal should be used to do a refresh read to all dynamic memories.

HALT **(Halt state)**

Output, active low. HALT indicates that the CPU has executed a HALT software instruction and is awaiting either a non maskable or a maskable interrupt (with the mask enabled) before operation can resume. While halted, the CPU executes NOP's to maintain memory refresh activity.

WAIT **(Wait)**

Input, active low. WAIT indicates to the Z-80 CPU that the addressed memory or I/O devices are not ready for a data transfer. The CPU continues to enter wait states for as long as this signal is active. This signal allows memory or I/O devices of any speed to be synchronized to the CPU.

INT **(Interrupt Request)**

Input, active low. The Interrupt Request signal is generated by I/O devices. A request will be honored at the end of the current instruction if the internal software controlled interrupt enable flip-flop (IFF) is enabled and if the BUSRQ signal is not active. When the CPU accepts the interrupt, an acknowledge signal (IORQ during M₁ time) is sent out at the beginning of the next instruction cycle. The CPU can respond to an interrupt in three different modes that are described in detail in section 5.4 (CPU Control Instructions).

NMI **(Non-Maskable Interrupt)**

Input, negative edge triggered. The non maskable interrupt request line has a higher priority than INT and is always recognized at the end of the current instruction, independent of the status of the interrupt enable flip-flop. NMI automatically forces the Z-80 CPU to restart to location 0066H. The program counter is automatically saved in the external stack so that the user can return to the program that was interrupted. Note that continuous WAIT cycles can prevent the current instruction from ending, and that a BUSRQ will override a NMI.

RESET

Input, active low. RESET forces the program counter to zero and initializes the CPU. The CPU initialization includes:

- 1) Disable the interrupt enable flip-flop

- 2) Set Register I = 00H
- 3) Set Register R = 00H
- 4) Set Interrupt Mode 0

During reset time, the address bus and data bus go to a high impedance state and all control output signals go to the inactive state.

BUSRQ

(Bus Request)

Input, active low. The bus request signal is used to request the CPU address bus, data bus and tri-state output control signals to go to a high impedance state so that other devices can control these buses. When BUSRQ is activated, the CPU will set these

buses to a high impedance state as soon as the current CPU machine cycle is terminated.

BUSAK

(Bus Acknowledge)

Output, active low. Bus acknowledge is used to indicate to the requesting device that the CPU address bus, data bus and tri-state control bus signals have been set to their high impedance state and the external device can now control these signals.

CLK

(Clock)

Single phase TTL level clock which requires only a 330 ohm pull-up resistor to +5 volts to meet all clock requirements.

MCR II SYSTEM
P.C. BOARD JUMPER OPTIONS

VIDEO GENERATOR P.C. BOARD

MANUFACTURER	EPROM NO.	JW#1	JW#2	JW#3	JW#4	JW#5	JW#6	JW#7	JW#8
MOTOROLA	68764	#	*	*	#	*	*	*	*
	68766	#	*	*	#	*	*	*	*
INTEL	2764	*	#	#	*	#	*	*	#
T. I.	2564	#	*	*	#	*	#	#	*

SUPER C.P.U. P.C. BOARD

JUMPER OPTIONS FOR PROGRAM ROMS ONLY

MANUFACTURER	EPROM NO.	JW#2	JW#4	JW#5	JW#6	JW#7	JW#18	JW#19	
MOTOROLA	68764	#	#	*	#	*	*	#	
	68766	#	#	*	#	*	*	#	
T. I.	2564	#	#	*	#	*	*	#	
INTEL	2764	*	*	#	*	#	#	*	

JUMPER OPTIONS FOR BACKGROUND ROMS ONLY

MANUFACTURER	EPROM NO.	JW#10	JW#11	JW#12	JW#13	JW#14	JW#15	JW#16	JW#17
MOTOROLA	68764	*	#	*	#	*	#	#	*
	68766	*	#	*	#	*	#	#	*
T. I.	2564	*	#	*	#	*	#	#	*
INTEL	2764	#	*	#	*	#	*	*	#

SOUND I/O P. C. BOARD

MANUFACTURER	EPROM NO.	JW#1	JW#2						
NUMEROUS MFR'S	2532	*	#						
NUMEROUS MFR'S	2732	#	*						

* = CUT JUMPER WIRES WHERE THIS SYMBOL "*" APPEARS.

= LEAVE JUMPER WIRES IN WHERE THIS SYMBOL "#" APPEARS.

The above table illustrates the fact that the Video Generator P.C. Board used in the MCR II System has 8 jumper wires, the SUPER C.P.U. P.C. Board used in the MCR II System has 19 jumper wires, and the Sound I/O P.C. Board used in the MCR II System has 2 jumper wires.

All of the above Boards can be used with a variety of different **SETS** of EPROM chips. However, these EPROMS are not all made by the same manufacturer

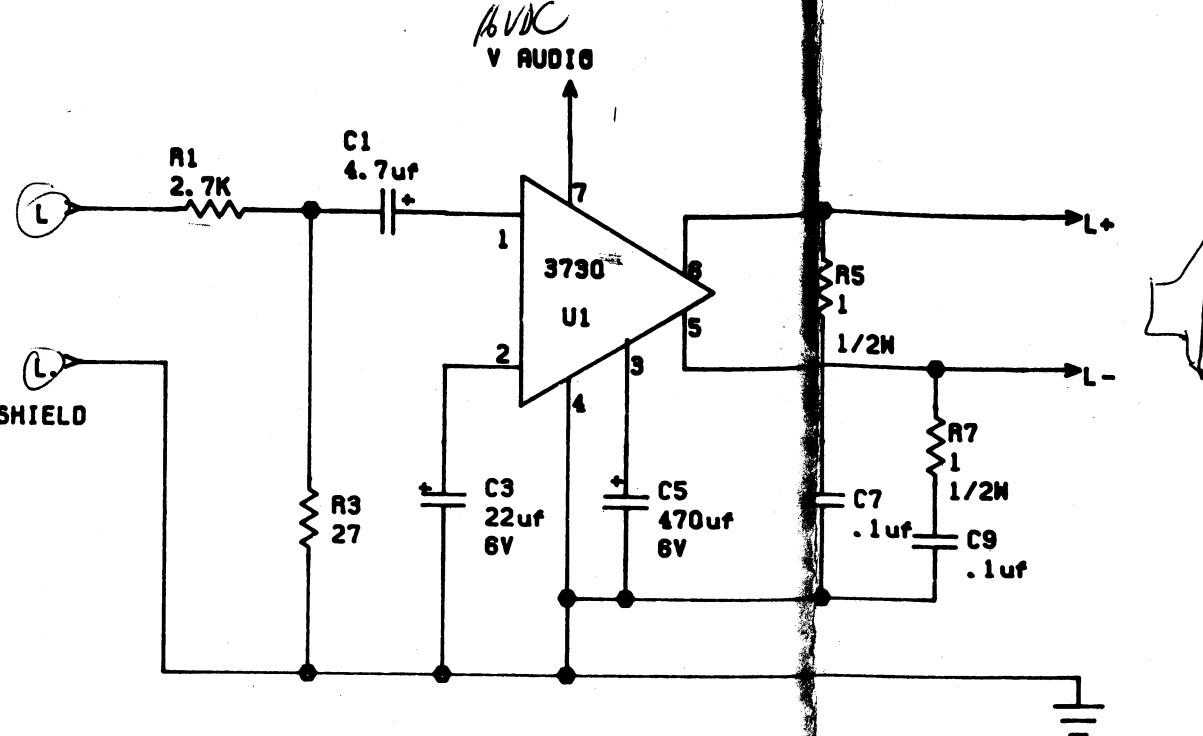
and do have some internal differences. So, in order to make them function properly in their respective P.C. Boards, certain jumper wires on these Boards have to be cut.

The above table tells you which jumpers to cut (depending on which EPROM set you're going to use) by showing a "*" under that jumper wire's number. If there is **NO** "*" under a jumper wire's number, THAT PARTICULAR JUMPER WIRE IS NOT TO BE CUT.

J1

PIN 1	N.C.
2	L. AUDIO
3	L. SHIELD
4	KEY
5	V AUDIO RETURN
6	R. AUDIO
7	R. SHIELD
8	V AUDIO

16VDC

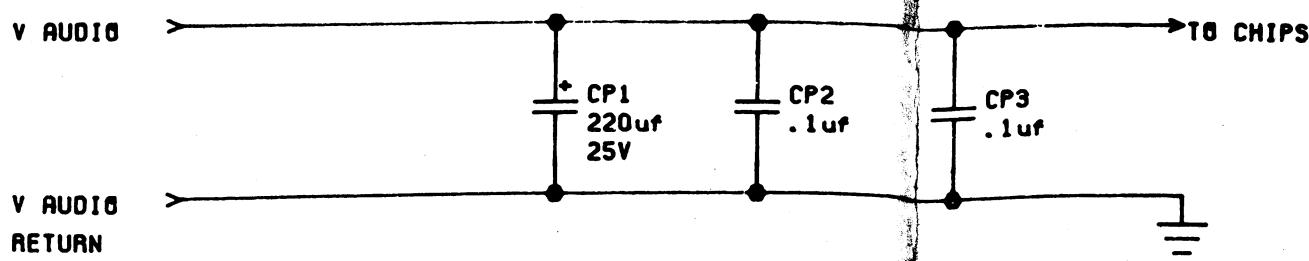
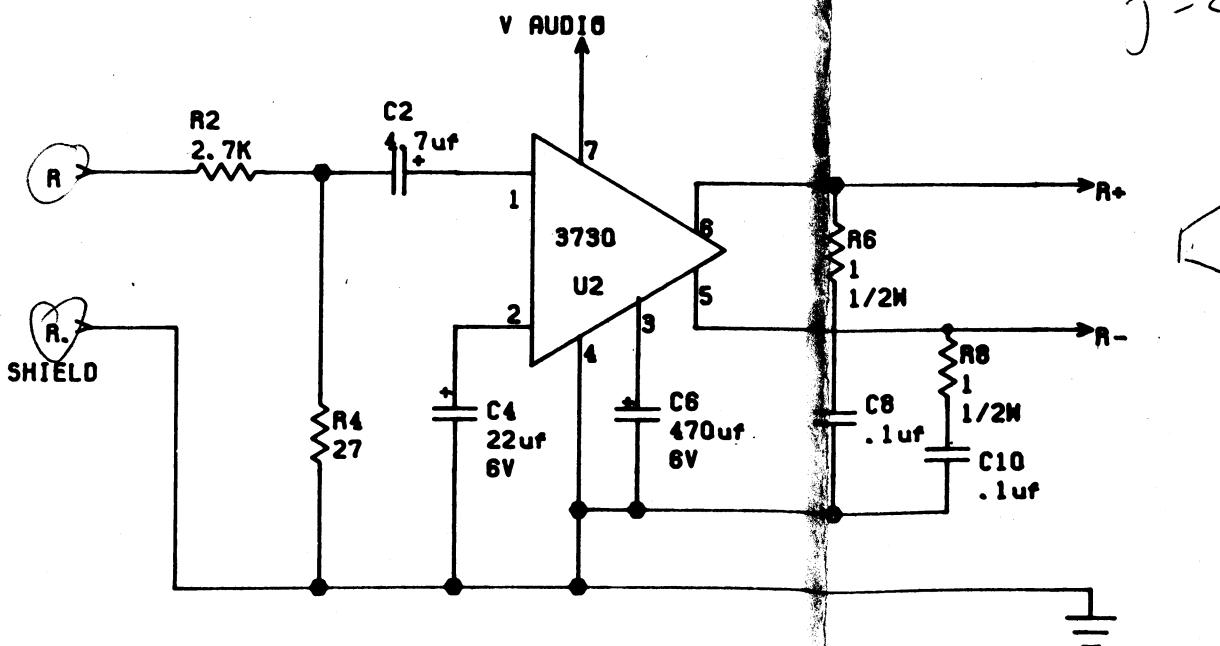


J2

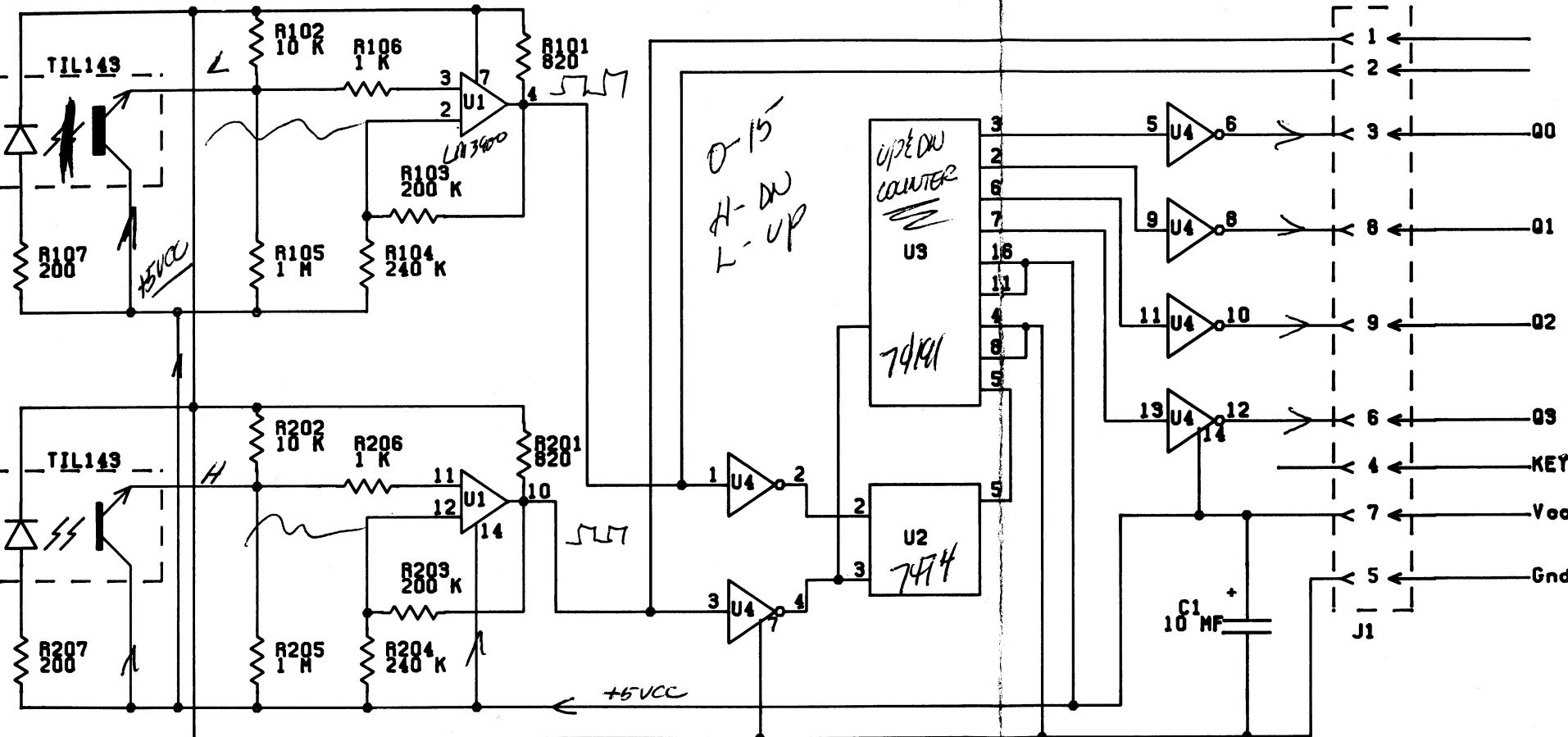
PIN 1	R+
2	R-
3	KEY
4	L+
5	N.C.
6	L-

16VDC

R. SHIELD



REVISIONS		MIDWAY MFG. CO.	
		FRANKLIN PK. ILL.	PART NO.
		MO5 1 - 00 986 - EO II	A082 - 90910 - E000
USED ON TRON		NO. REQ'D IPER.	SCALE
		NONE	
DO NOT SCALE DWG.		HEAT TREAT	MATL.
		DRN. 508	FINISH
DIM. TOLERANCES UNLESS SPECIFIED		CKD.	
CONCENTRICITY TIR .003		.005	
FRACTIONAL .1/64		.005	
DECIMAL .002		.002	
HOLE DIA. +.002-.000		.000	
DATE 5/17/82			



NOTES
 U1-LM3900
 U2-7474
 U3-74191
 U4-7414

PROJECT ENG: C.MEDNICK

CKD.	DO NOT SCALE DWG.			REVISIONS
DRN. TJK	DATE 8/26/81	USED ON		
heat treat	scale FULL	NO. REQ'D	1 PER	
mat'l.				MIDWAY MFG. CO.
finish				FRANKLIN PK. ILL.
				PART NO.
				M05I-00968-C004
BINARY ANGLE DECODER SCHEMATIC A082-91391-C000				

Chip Number

Chip Number	Function
MB8416	Ram 2K x 8
6116LP-4	Ram 2K x 8
9860-07AXN-AXHD	PROM 82S123 (SB2-A)
Z-80 CTC	Counter timer circuit
0066-313BX-XXQX (MMC01)	H-T generator - custom
0066-314BX-XXQX (MMC02)	V-T generator - custom
0066-315BX-XXQX (MMC03)	Misc. V & H circuits - custom
0066-316BX-XXQX (MMC06)	Misc. TTL circuits - custom
0066-322BX-XXQX (MMC04)	NVR controller - custom
AY-3-8910 (8910)	Sound generator
LM3900	Quad operational amplifier
MC3403	Quad operational amplifier

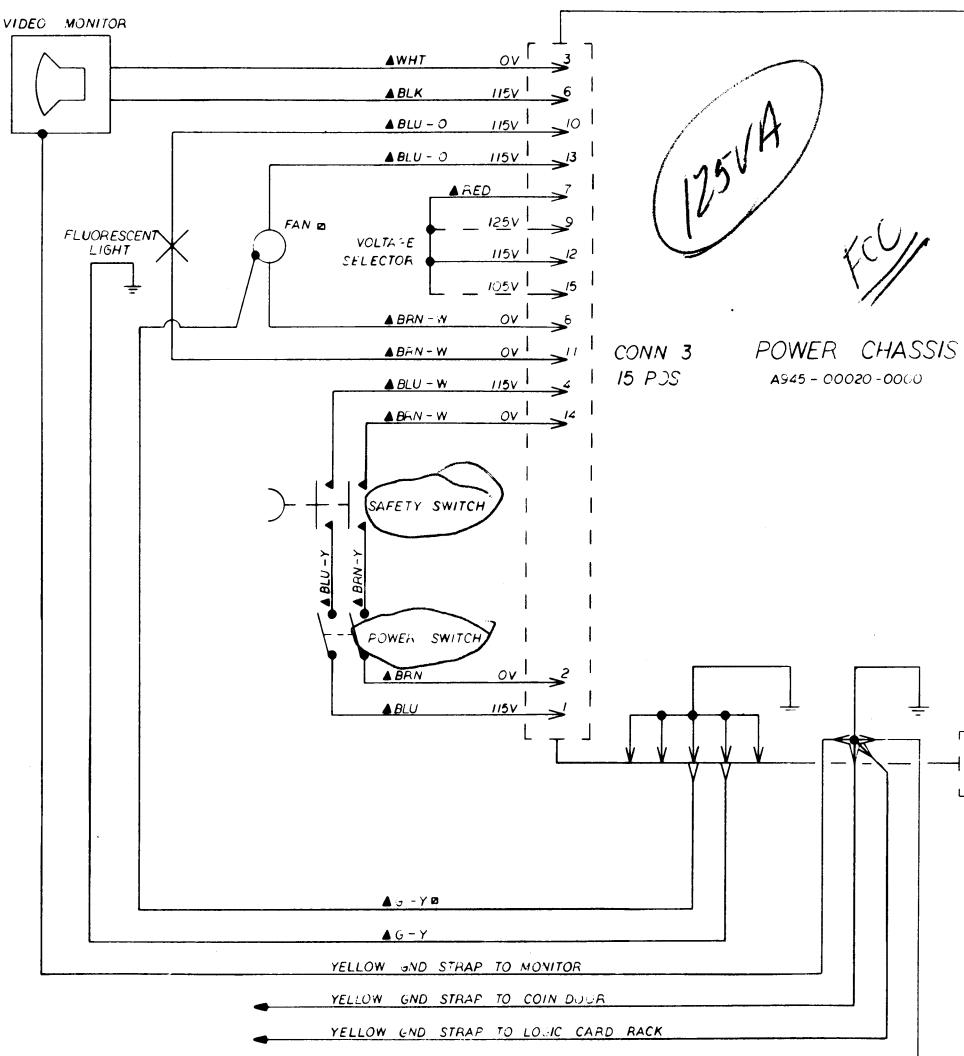
Misc. Components

16.00 & 19.9 MHZ	Z-TAL
2N4123	Transistor NPN
2N4403	Transistor PNP
MPSA70	Transistor PNP
TIP110	Transistor NPN

Logic Boards Integrated Circuits

Chip Number	Function
7400	Quad 2 input Nand
74LS02	Quad 2 input Nor
74LS04	Hex inverter
7406	Hex inverter open collector
7407	Hex buffer open collector
74LS08	Quad 2 input And
74LS20	Dual 4 input Nand
7427	Triple 3 input Nor
74LS30	8 input Nand
74LS32	Quad 2 input Or
74LS74	Dual "D" Flip-Flop
74LS86	Quad 2 input exclusive Or
7489	64 bit ram 16 x 4
74126	Quad buffer tri-state
74LS138	3 to 8 line decoder
74LS153	Dual 4 to 1 line multiplexer
74LS155	Dual 2 to 4 line decoder
74LS157	Quad 2 to 1 line multiplexer
74160	4 bit decade counter
74161	4 bit binary counter
74166	8 bit shift register
74LS174	Hex "D" Flip-Flop
74175	Quad "D" Flip-Flop
74LS191	Up/down binary counter
74LS194	8 bit shift register
74LS244	Octal buffer tri-state
74LS245	Octal buss transceiver
74LS273	Octal "D" Flip-Flop
74LS283	4 bit full adder
74LS367	Hex buss driver
74LS374	Octal "D" Flip-Flop tri-state
74LS670	4 x 4 register files
4017	Decade counter/divider
14016	Quad analog switch
14024	7 stage ripple counter
14053	Triple 2 channel analog multiplexer
Z80	CPU 2.5 MHz
Z80A	CPU 4 MHz
D780C	CPU 2.5 MHz
D780C-1	CPU 4 MHz
TMS2564	8K x 8 EPROM
MBM2732	4K x 8 EPROM
HN462532	4K x 8 EPROM
2114	Ram 1K x 4
93422	Ram 256 x 4
M58725	Ram 2K x 8
4801AN-90	Ram 1K x 8
4118A-4	Ram 1K x 8
93419 or 82S09	64 X 9 Color Ram
74LS133	13 input Nand Gate

VIDEO MONITOR



125VA

FCU

CONN 1
9 POS

6	15V UNREG	* RED
9	12V COM	* R-W
5	12V COM	* B-W
7	5V COM	* B-W
3	5V COM	* B-W
2	8V COM	* B-W
4	8V UNREG	* BLK
8	5V UNREG	* BLK

CONN 4
2 POS

1	12V	* O-B
2	COM	* GAY-R

CONN 2
3 POS

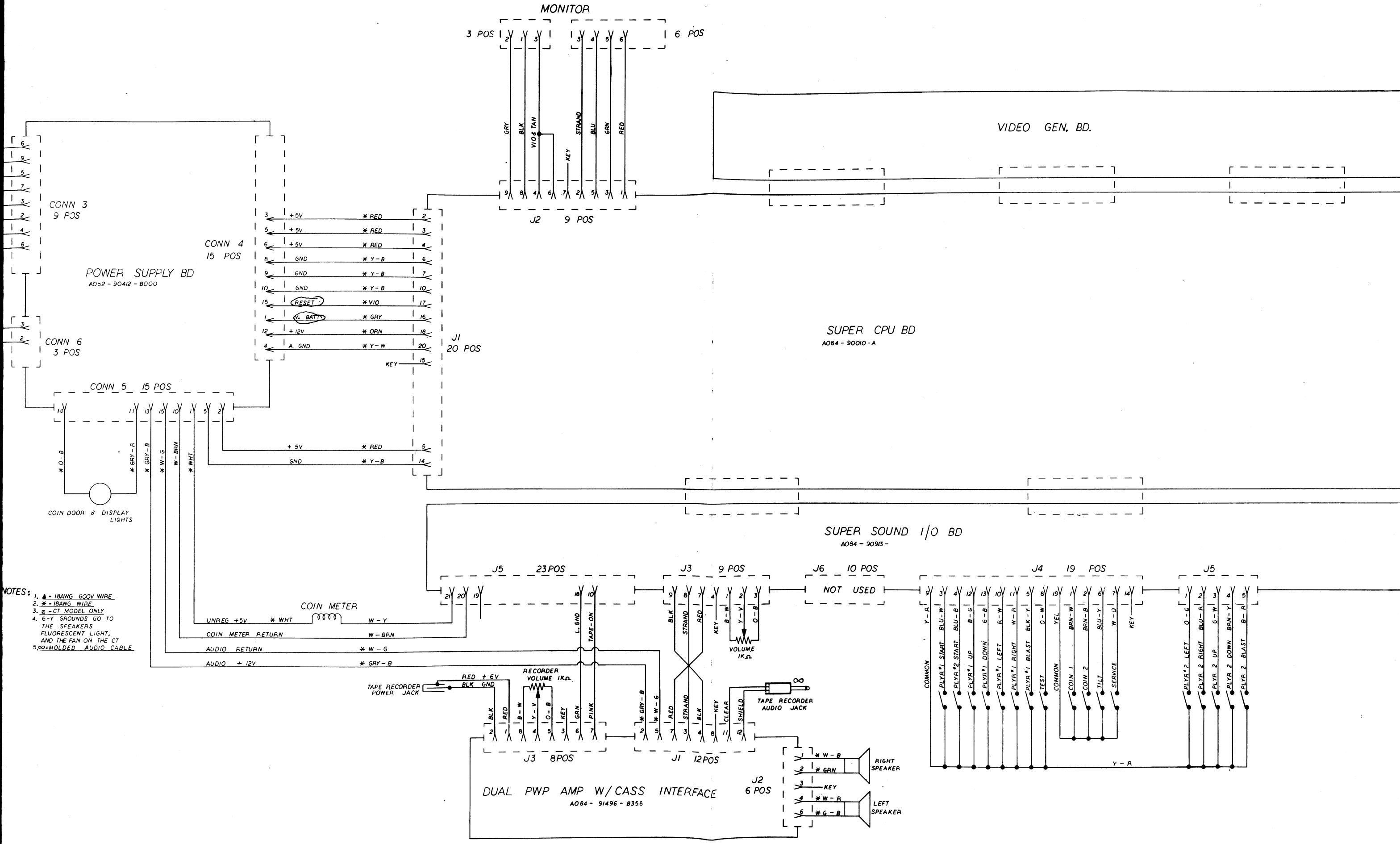
NEUTRAL
GROUND
HOT

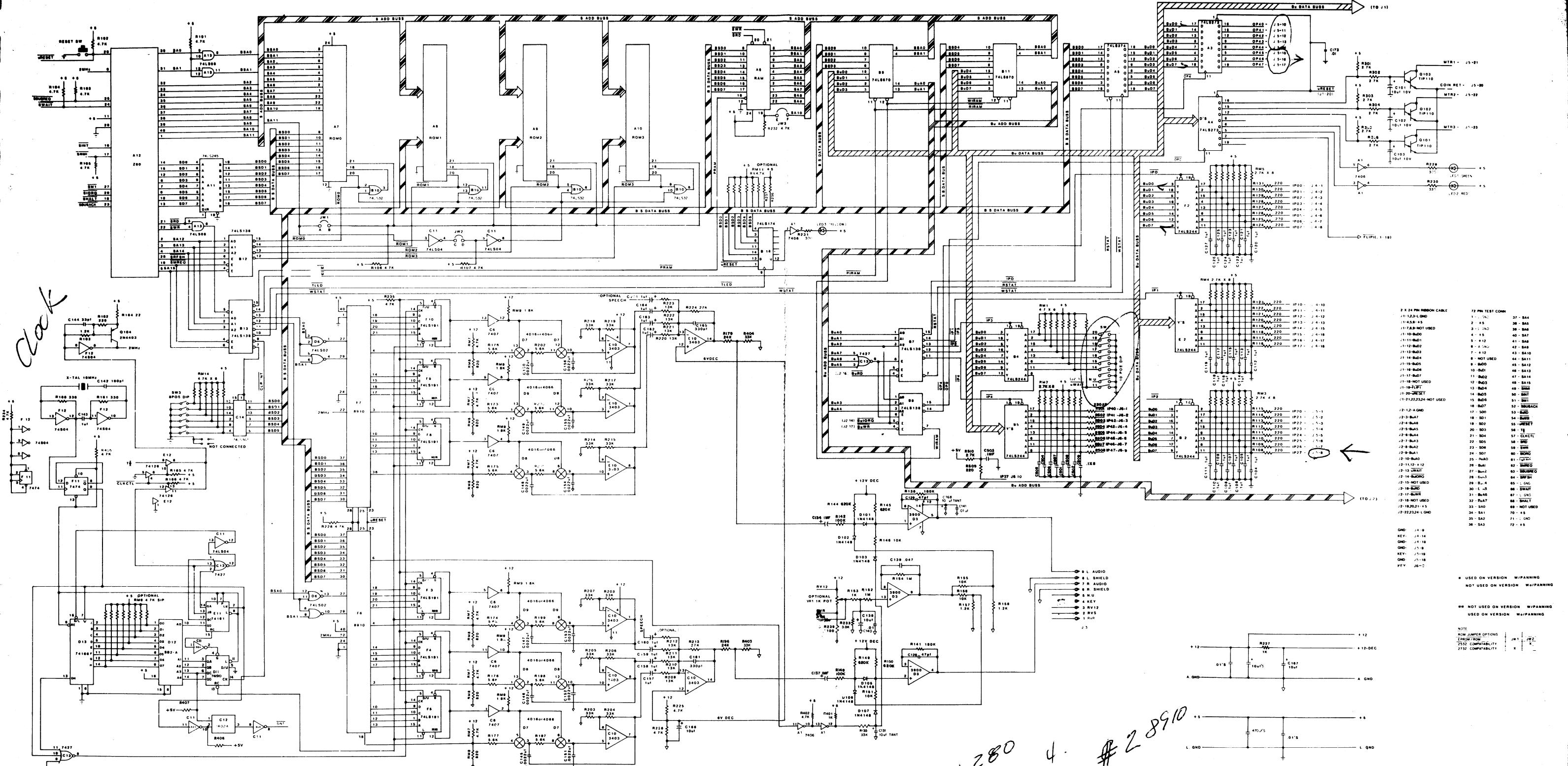
JOURNEY
M051 - 00358 - A003

Bally / MIDWAY

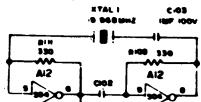
10601 W BELMONT
FRANKLIN PARK, ILL. 60131

REVISION	DATE	NAME





1. Z80
 2. ROM 4.
 3. Sound Gen #2 8910
 4. AG PAIR 180-
 5. Buffer. Transistor output-



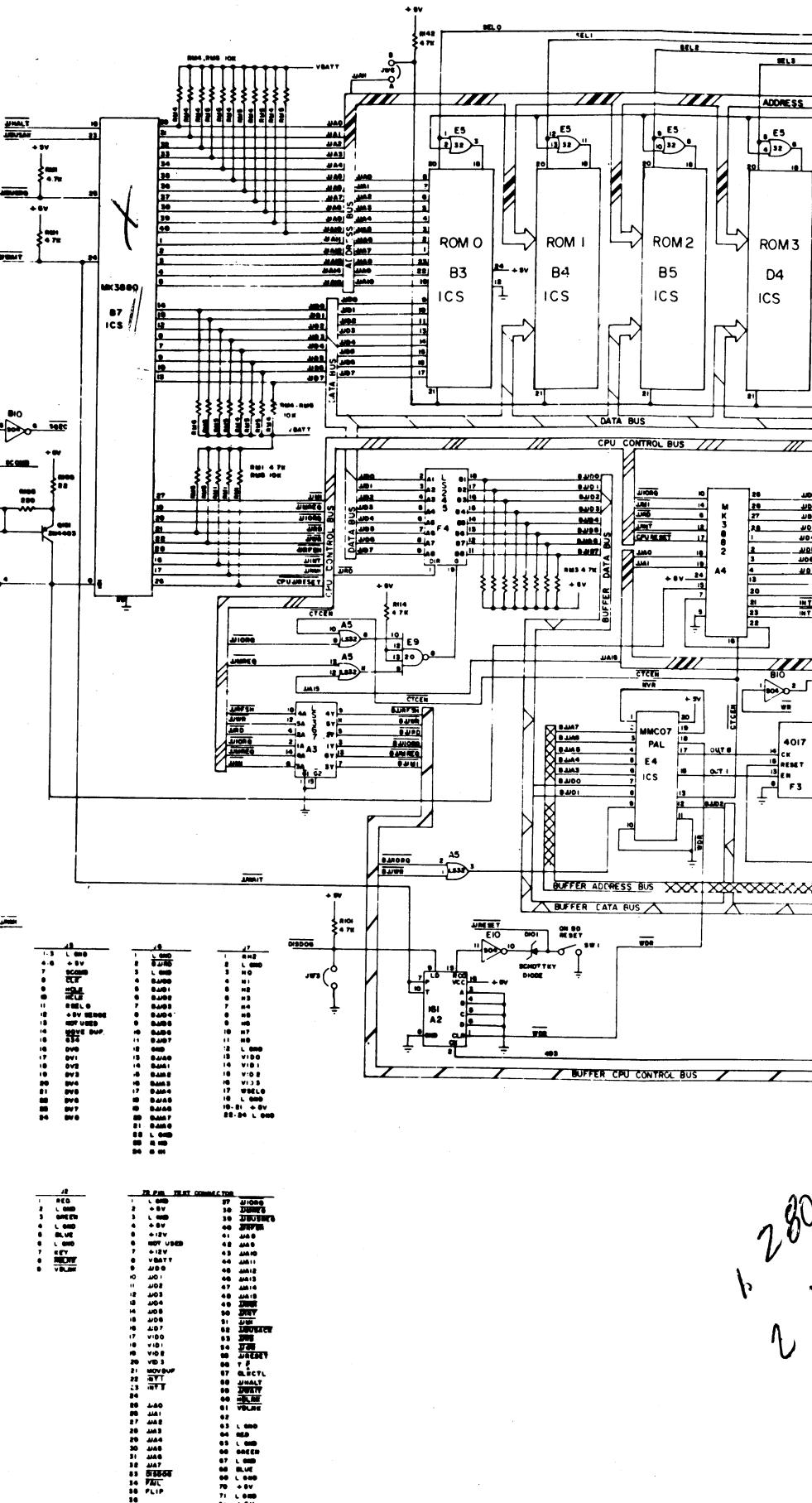
Check

1	L 000
2	L 000
3	L 000
4	L 000
5	L 000
6	L 000
7	NOT USED
8	NOT USED
9	NOT USED
10	NOT USED
11	NOT USED
12	NOT USED
13	NOT USED
14	NOT USED
15	NOT USED
16	NOT USED
17	NOT USED
18	NOT USED
19	NOT USED
20	NOT USED
21	NOT USED
22	NOT USED
23	NOT USED
24	NOT USED

1	A 000
2	A 000
3	A 000
4	A 000
5	A 000
6	A 000
7	B 000
8	B 000
9	B 000
10	B 000
11	B 000
12	B 000
13	B 000
14	B 000
15	B 000
16	B 000
17	B 000
18	B 000
19	B 000
20	B 000
21	B 000
22	L 000
23	L 000
24	L 000

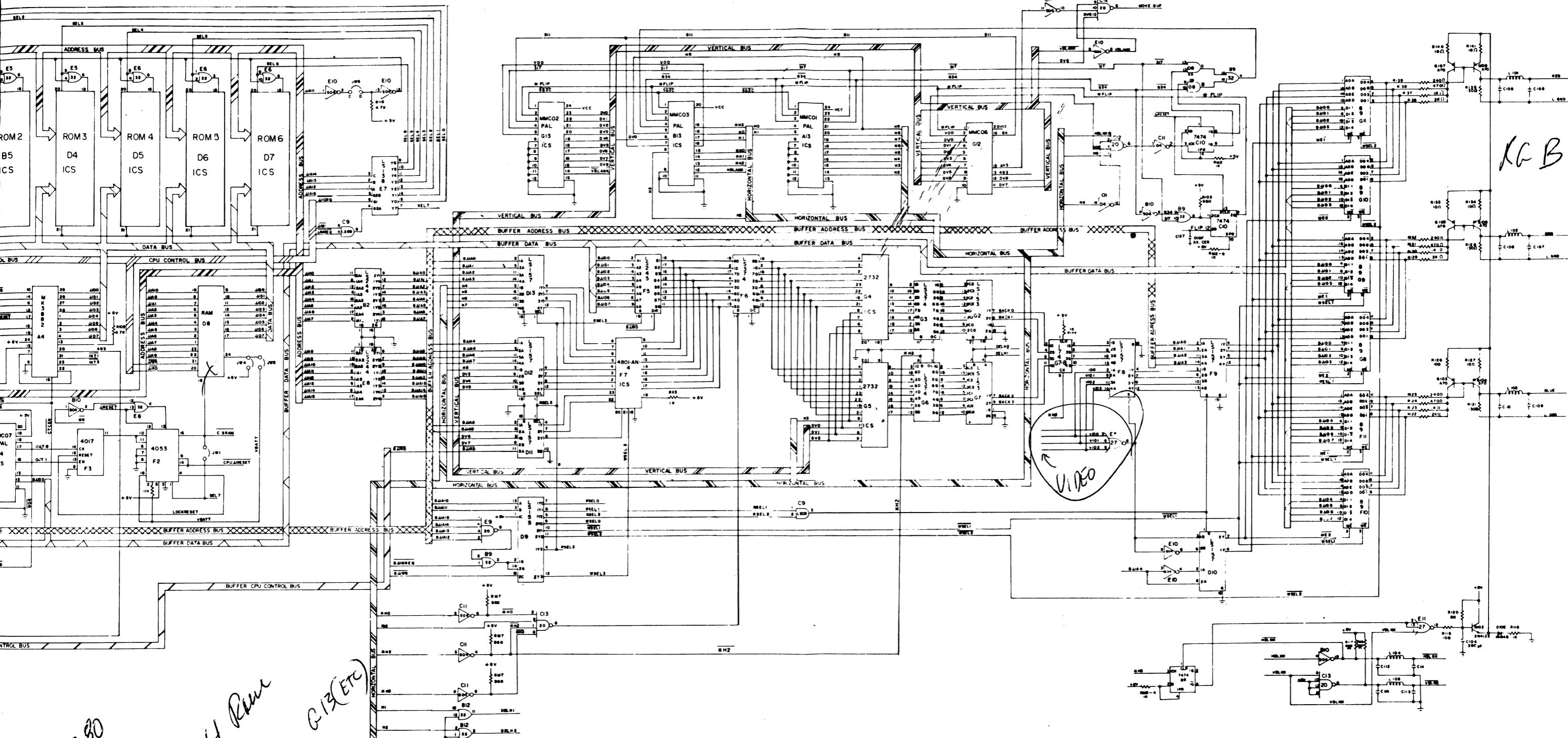
J1-1 GND SOURCE
J1-2 GND SOURCE
J1-3 +5V SOURCE
J1-4 -5V SOURCE
J1-5 VBATY
J1-6 PAR
J1-7 J18N SET
J1-8 CP133 CP128
J1-9 CP133 CP128
J1-10 CP133 CP128
J1-11 CP133 CP128
J1-12 CP133 CP128
J1-13 CP133 CP128
J1-14 CP133 CP128
J1-15 CP133 CP128
J1-16 CP133 CP128
J1-17 CP133 CP128
J1-18 CP133 CP128
J1-19 CP133 CP128
J1-20 ANALOG GND

J1-1 NOT USED
J1-2 GND
J1-3 GND
J1-4 GND



NOTES
A = ANALOG
E = EARTH
L = LOGIC

280
b
v

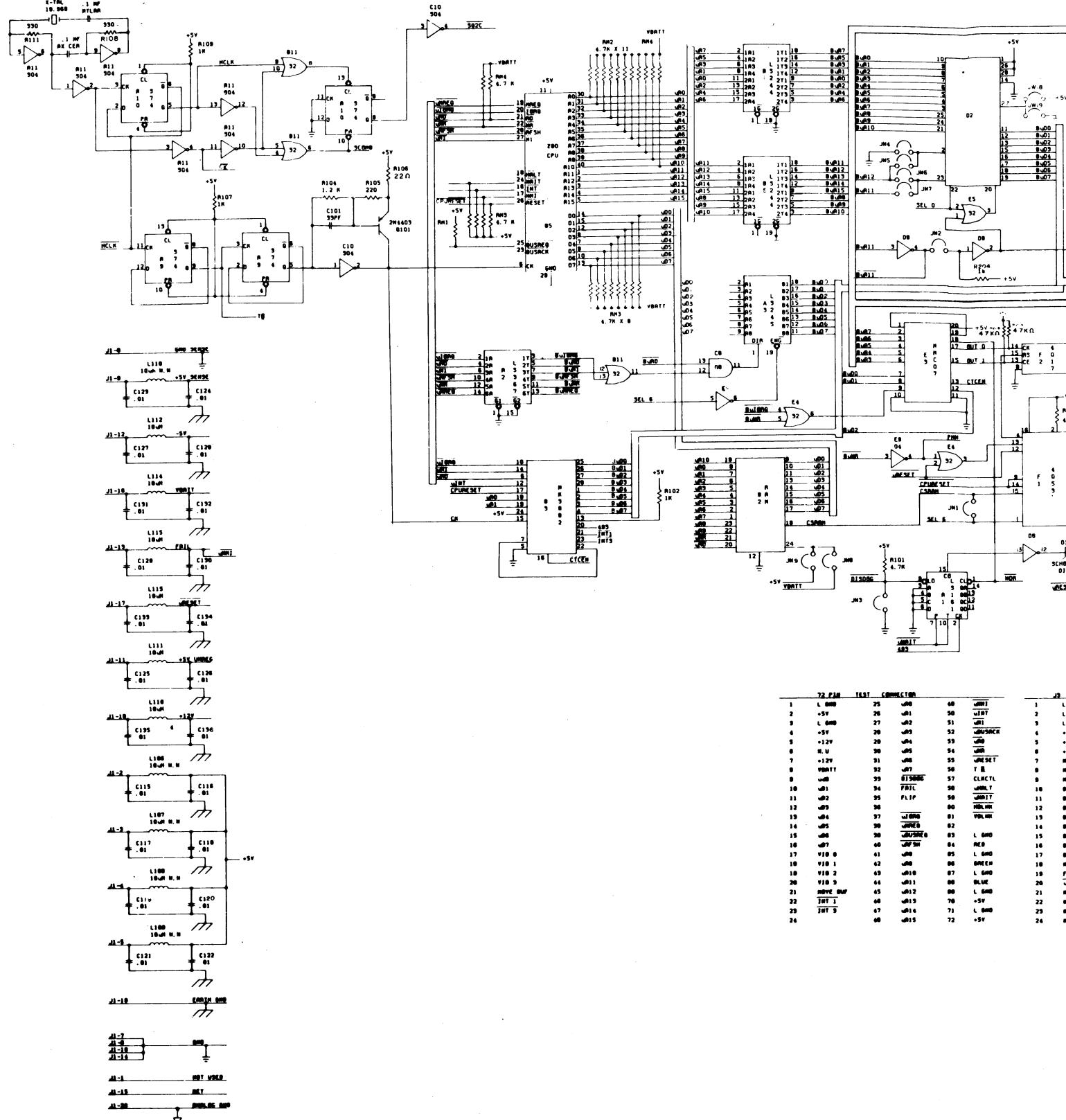


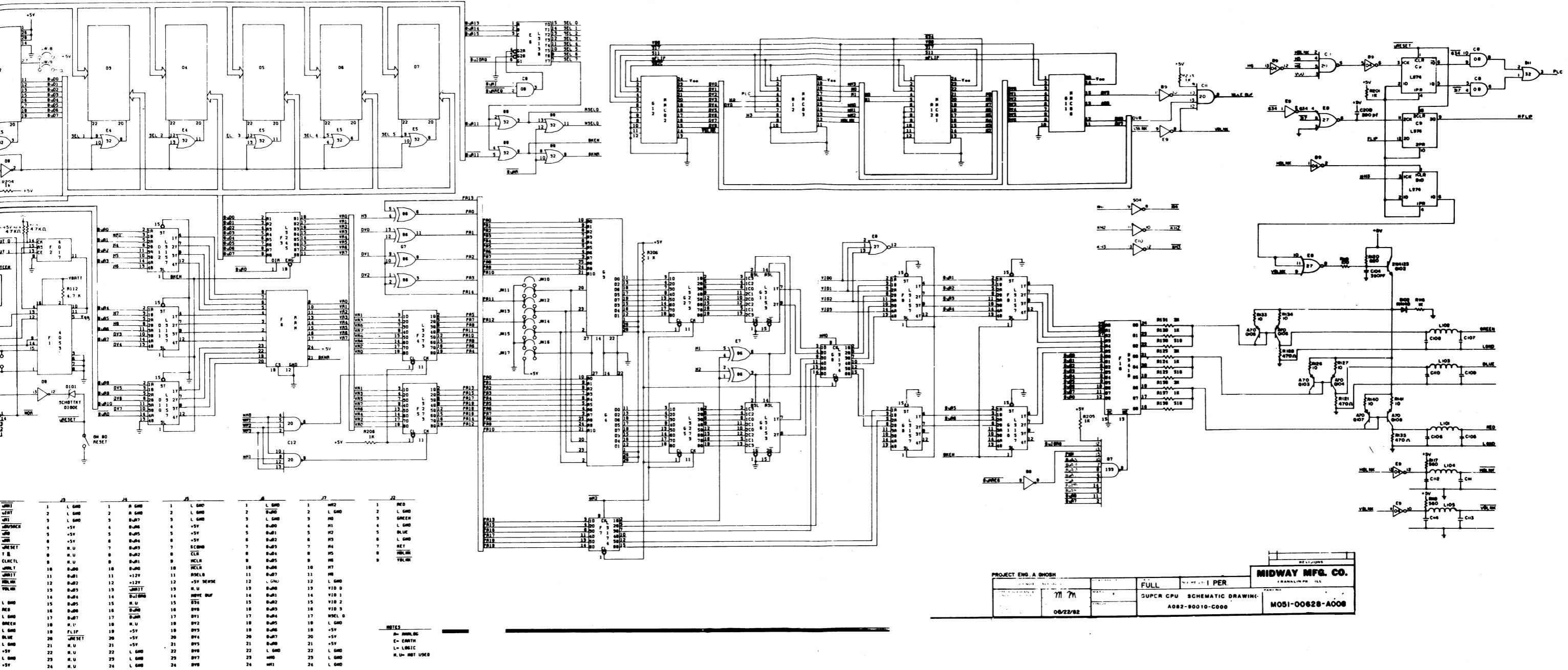
The image contains handwritten notes and a circuit diagram. The notes are arranged vertically from top to bottom:

- 1 280
- 2 ROM
- 3 P8 Butl Run
- 4 Clock Chip's Run's
- 5 B.I. Run F-1
- 6 B.I. Run Run
- 7 Color Run

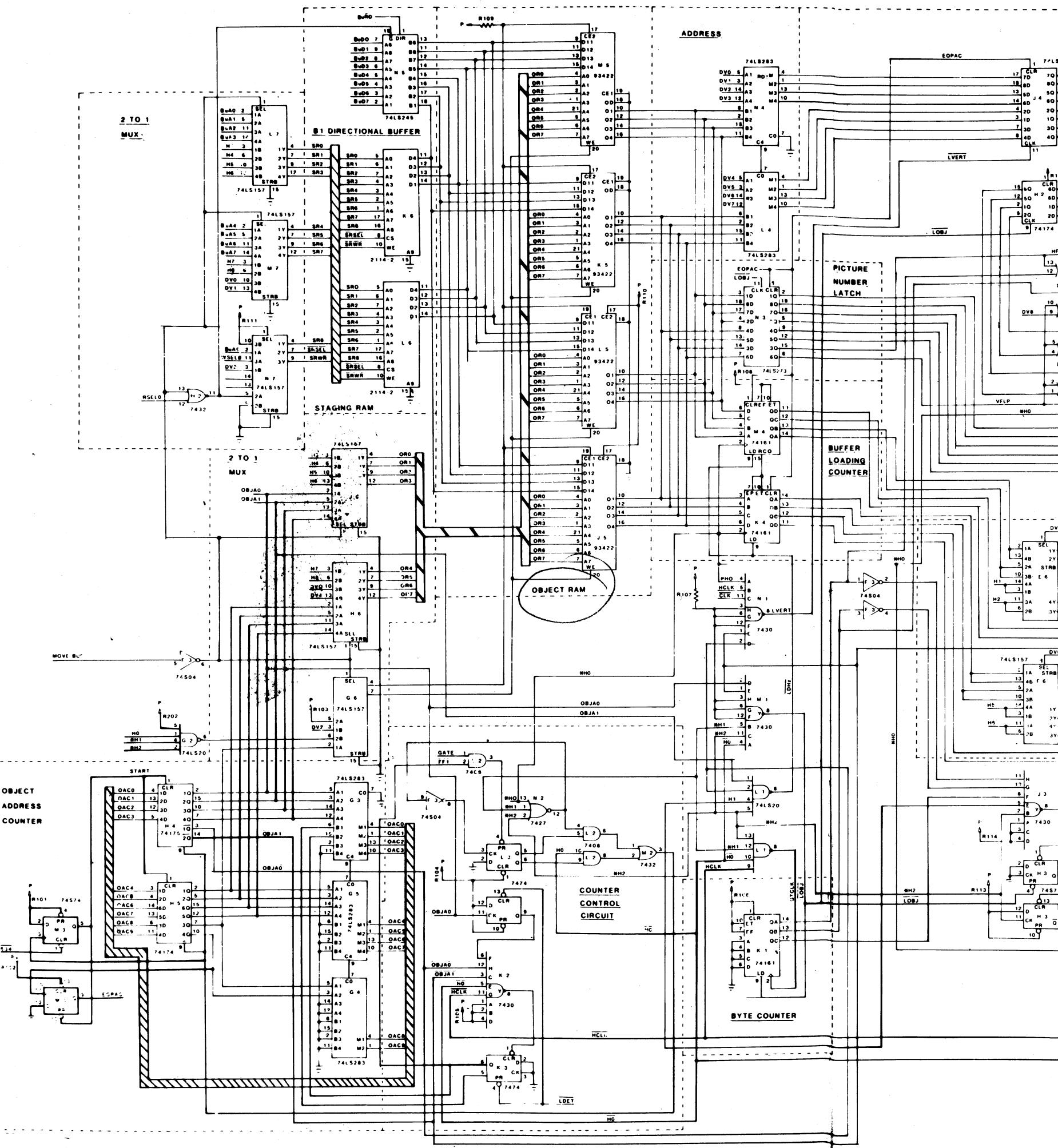
On the right side, there is a note: "7489 DFL 4 CPU Action belt". Above this, a small circle contains the number "7489". To the right of the notes, there is a circuit diagram labeled "Circuit (ETC)". The diagram shows a logic circuit with various components: a 7489 integrated circuit, resistors (R1 through R8), capacitors (C11 through C14), and diodes (D1 through D4). Power supply connections include +5V, +12V, and GND. A feedback line labeled "DBL.H1" connects the output of a 7414 inverter back to the 7489 chip.

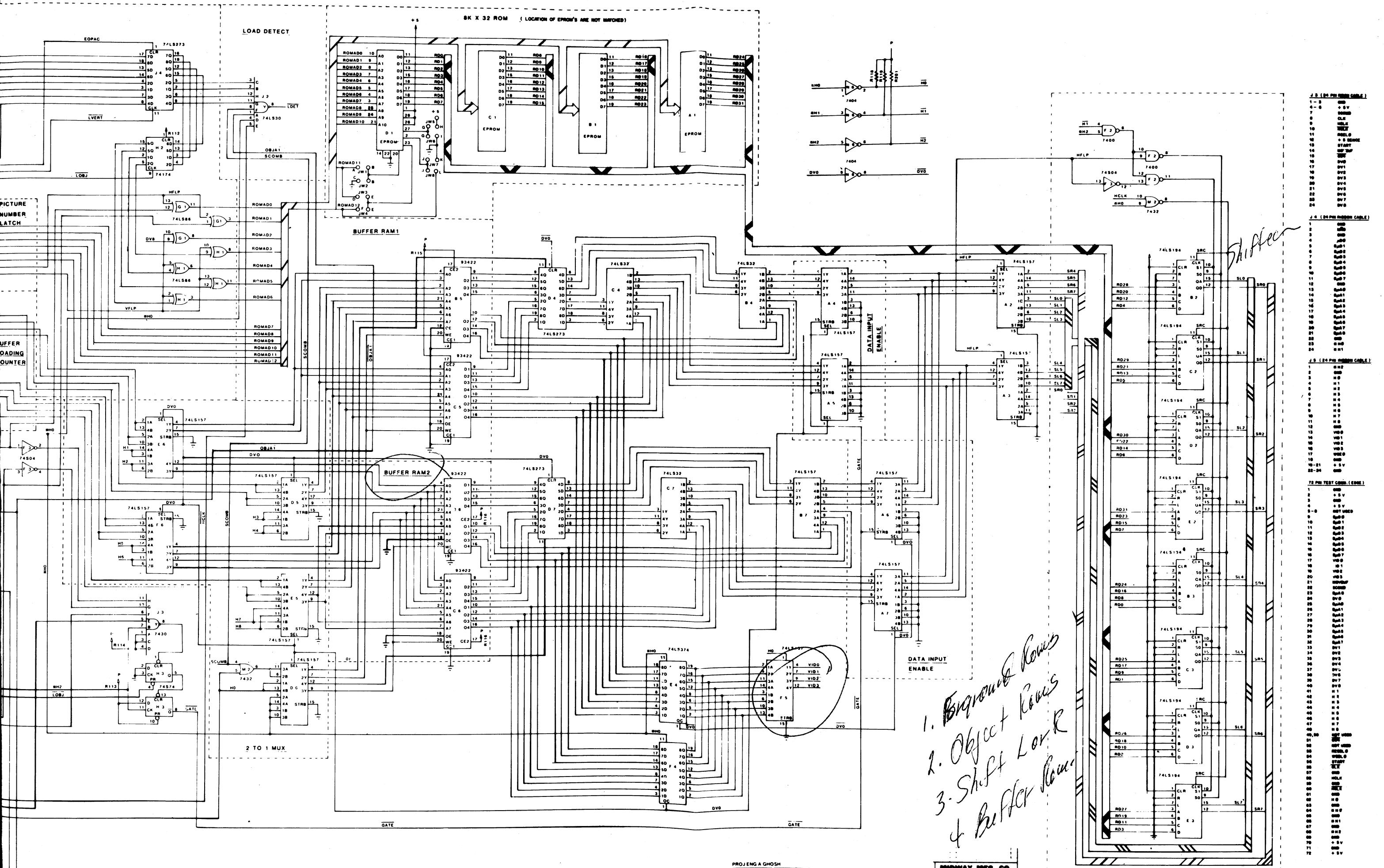
PROJECT #90 J BOYDTON	BOLARFOX	MIDWAY MFG. CO.
DE MATELL CO. 000	FULL	1 PER
37	CPU SCHEMATIC	M05/00982-A00
	A082-9000B-N000	

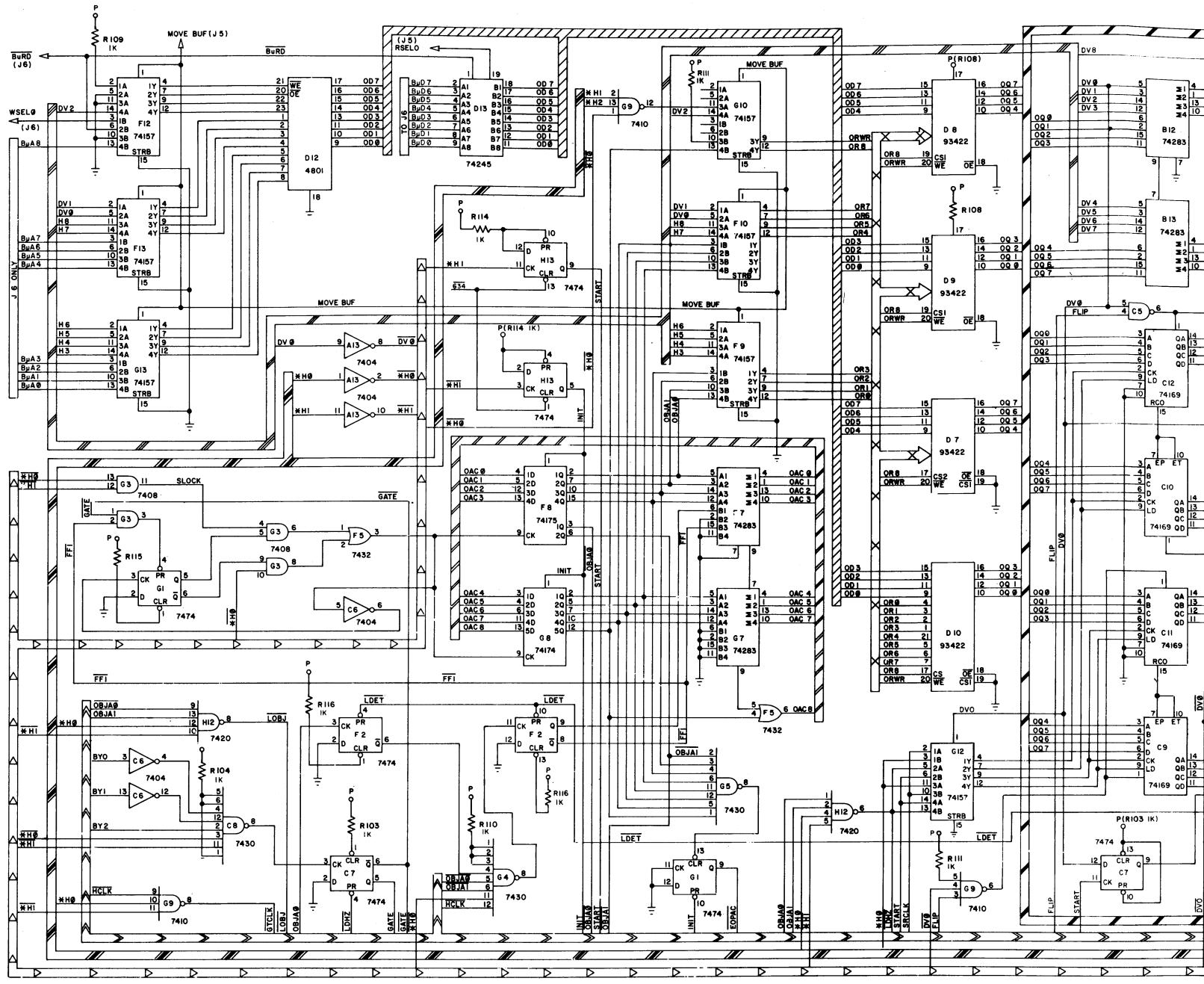


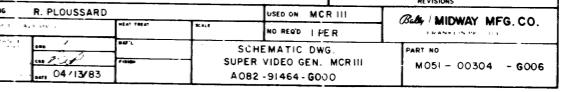
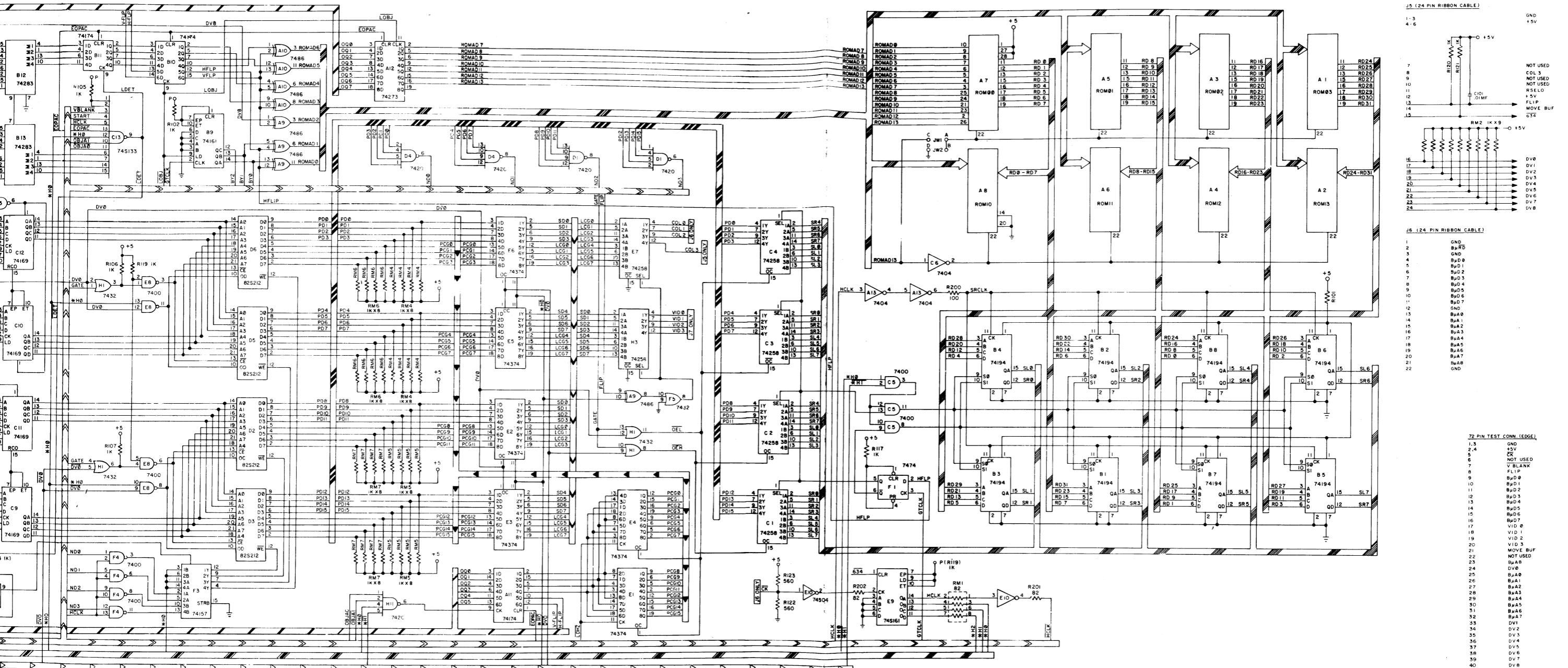


PROJECT ENG. A-GNOSH		MIDWAY MFG. CO.	
		FRANKLIN, ILL.	
		FULL	1 PER
		SUPER CPU SCHEMATIC DRAWING	
		A082-9010-C000	
		M051-00628-A008	
DATE ISSUED	RECEIVED	08/22/82	









VIDEO MONITOR



CONN. 3

WHT → 3 WHT

BLK → 6 BLK

BLU-ORN → 10 BLU-ORN

BLU-ORN → 13 BLU-ORN

BLU-WHT → 4 BLU-WHT

RED → 7 BLU-WHT

VOLTAGE SELECTION → 2 BLU-RED 125 V.

→ 12 BLU-BLK 115 V.

→ 15 BLU-YEL 105 V.

BRN-WHT → 9 BRN-WHT

BRN-WHT → 11 BRN-WHT

BRN-WHT → 14 BRN-WHT

SEE NOTE #8 → 5 RED-YEL

SAFETY SWITCH

BRN-YEL
BRN-YEL

POWER SWITCH

GRN-YEL
GRN-YEL

BLU

A.C. LINE FILTER

BLU
LINE
BRN

GRN-YEL

GRN-YEL
GRN-YEL

(B) 4 AMP SLO-BLO

BLU → TS

S L J B F T

VARISTOR

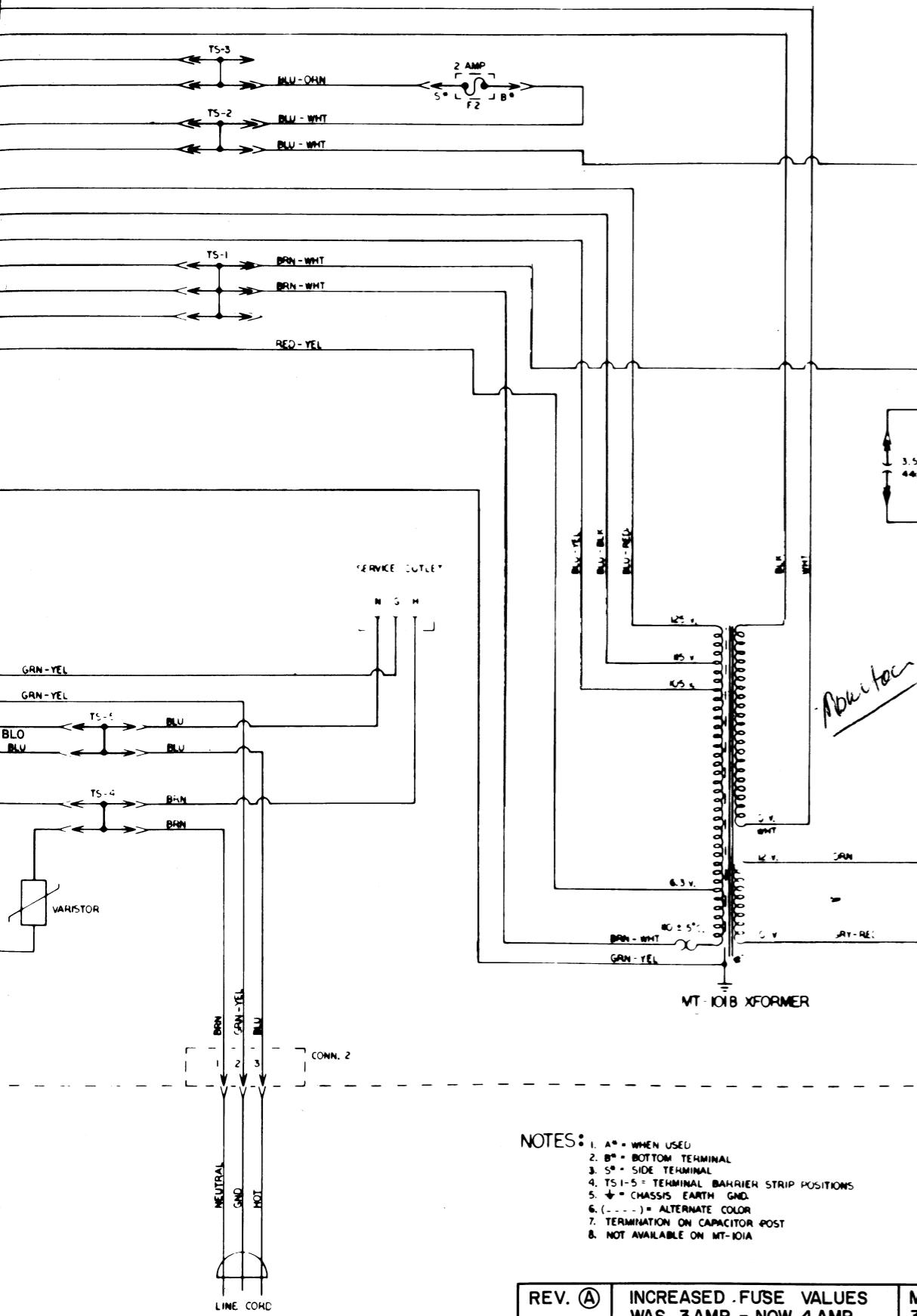
GRN-YEL

GRN-YEL

YELLOW GND STRAP

YELLOW GND STRAP TO COIN-DOOR

YELLOW GND STRAP TO CONTROL PANEL



NOTES:

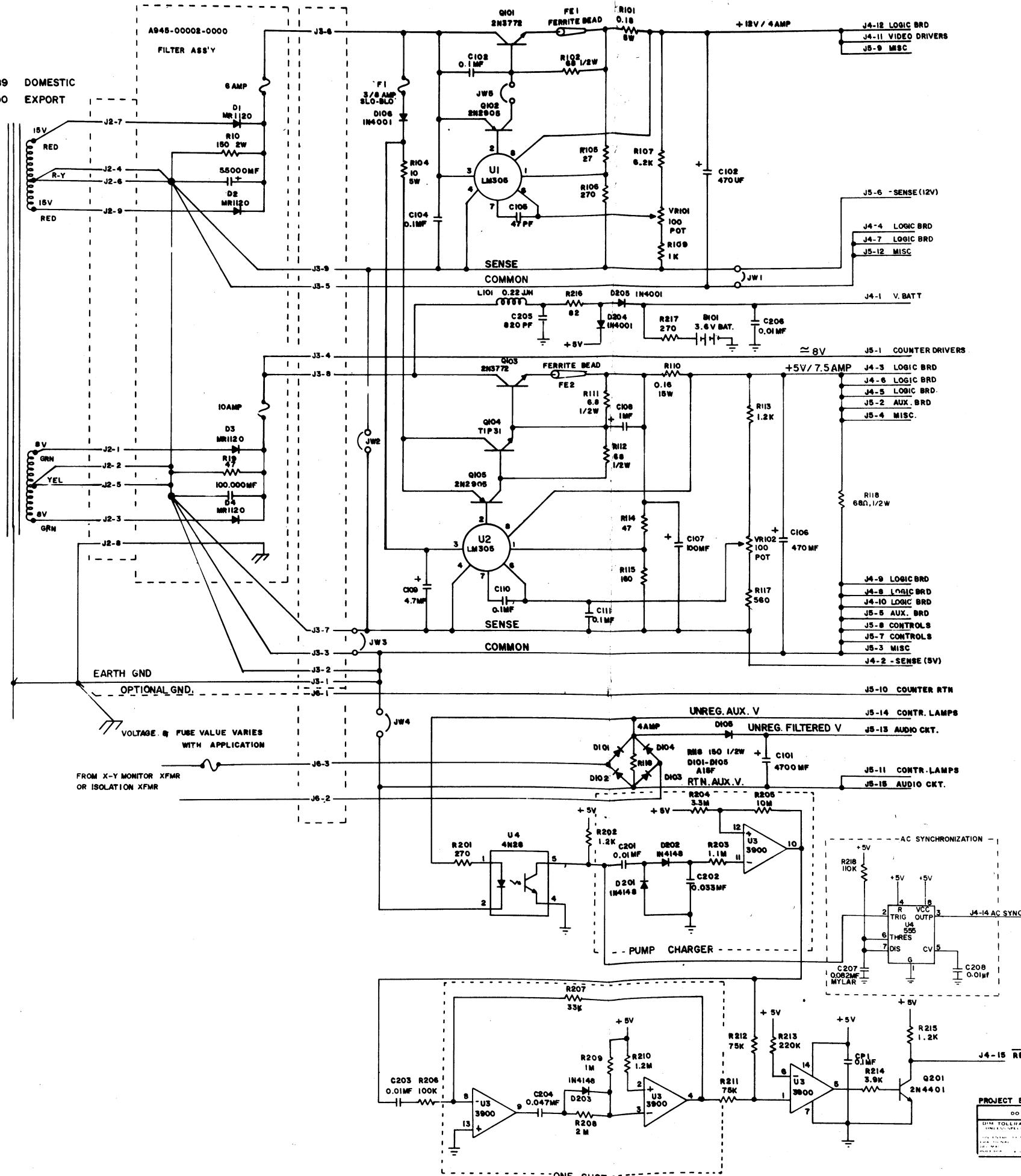
1. A* = WHEN USED
2. B* = BOTTOM TERMINAL
3. S* = SIDE TERMINAL
4. TS 1-5 = TERMINAL BAHRIER STRIP POSITIONS
5. ↓ = CHASSIS EARTH GND.
6. (- - -) = ALTERNATE COLOR
7. TERMINATION ON CAPACITOR POST
8. NOT AVAILABLE ON MT-101A

POWER CHASSIS *I25 VA
115 V. - 60 Hz.
PART NO. A945-00020-0000
DWG. NO. M051-00945-B037

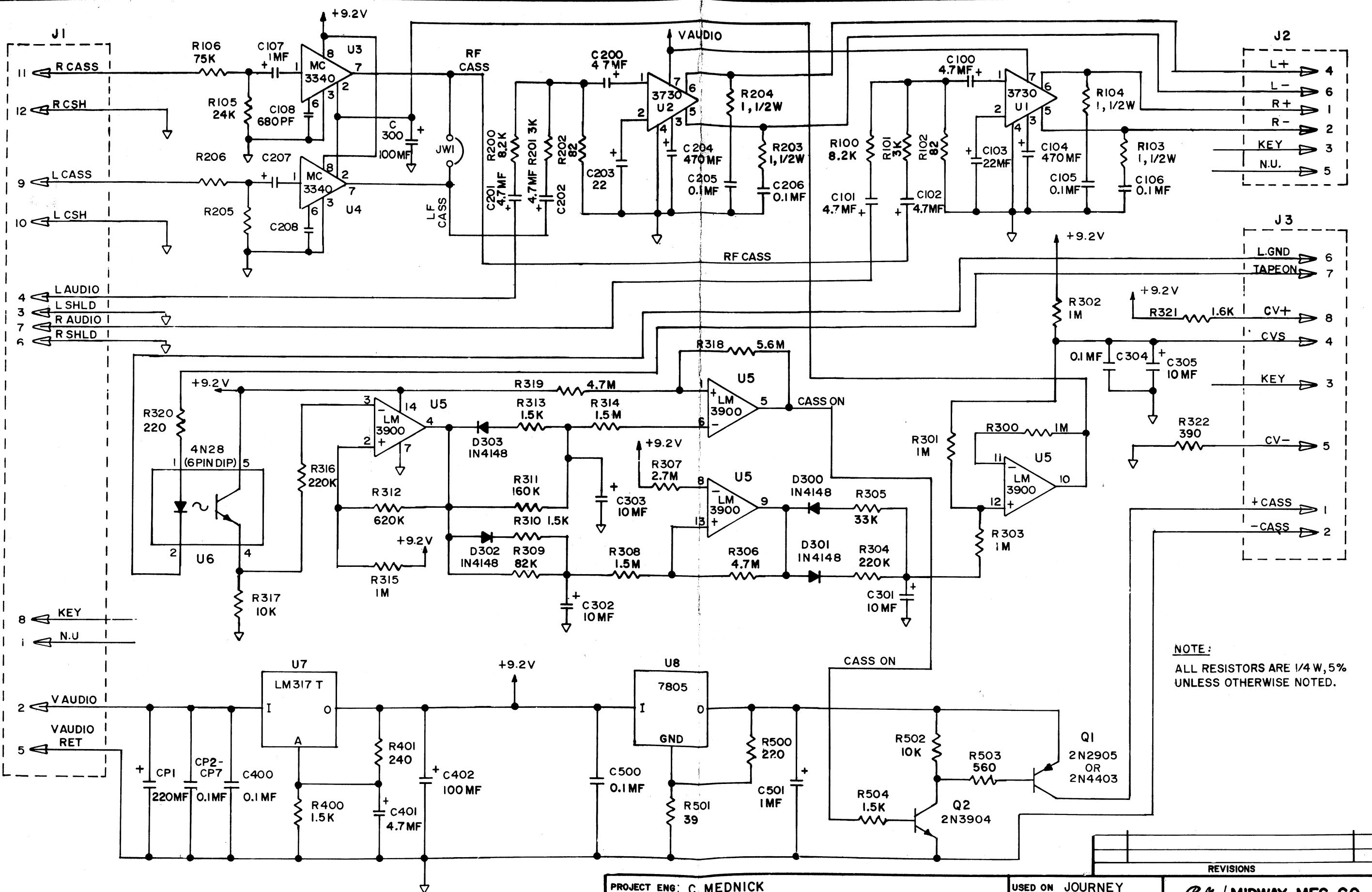
BALLY / MIDWAY
10601 W. BELMONT AVE.
FRANKLIN PARK, IL. 60131

REV. A	INCREASED FUSE VALUES WAS 3 AMP - NOW 4 AMP ADDED PART NO. (U.L.)	MB 3-15-83
REV. B	INCREASED FUSE VALUE WAS 3AMP - NOW 4AMP	MB 3-24-83

MCR-41



MCR-42



PROJECT ENCL: C MERNI

DO NOT SCALE DWG.	
DIM. TOLERANCES UNLESS SPECIFIED	
CENTRICITY TIR	.003
FRACTIONAL	.004
DECIMAL	.005
HOLE DIA	+ .002

USED ON JOURNEY

SCALE	FULL	NO. REQ'D	1 RE
-------	------	-----------	------

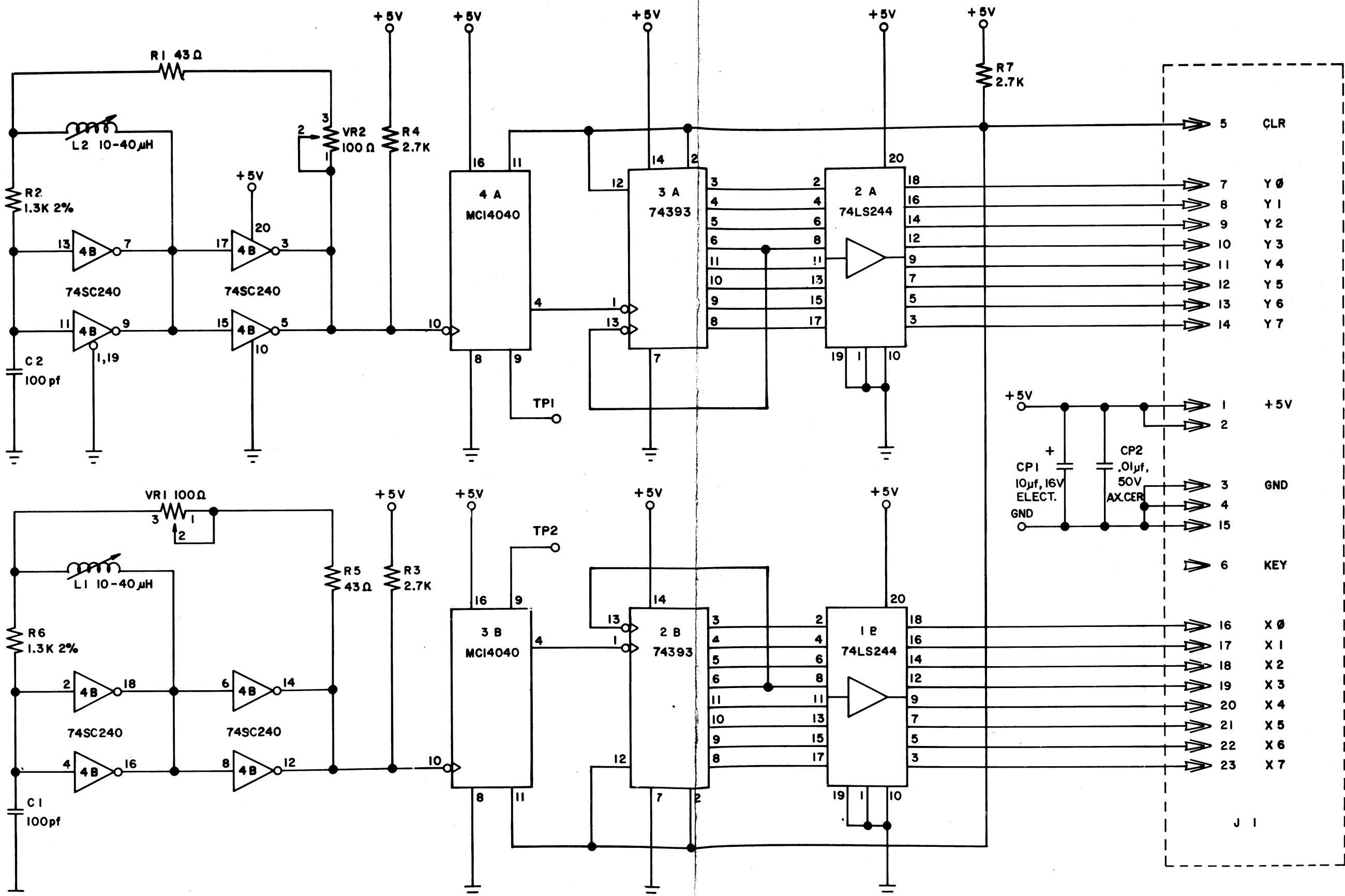
© 1999 Academic Press Inc.

MIDWAY MFU

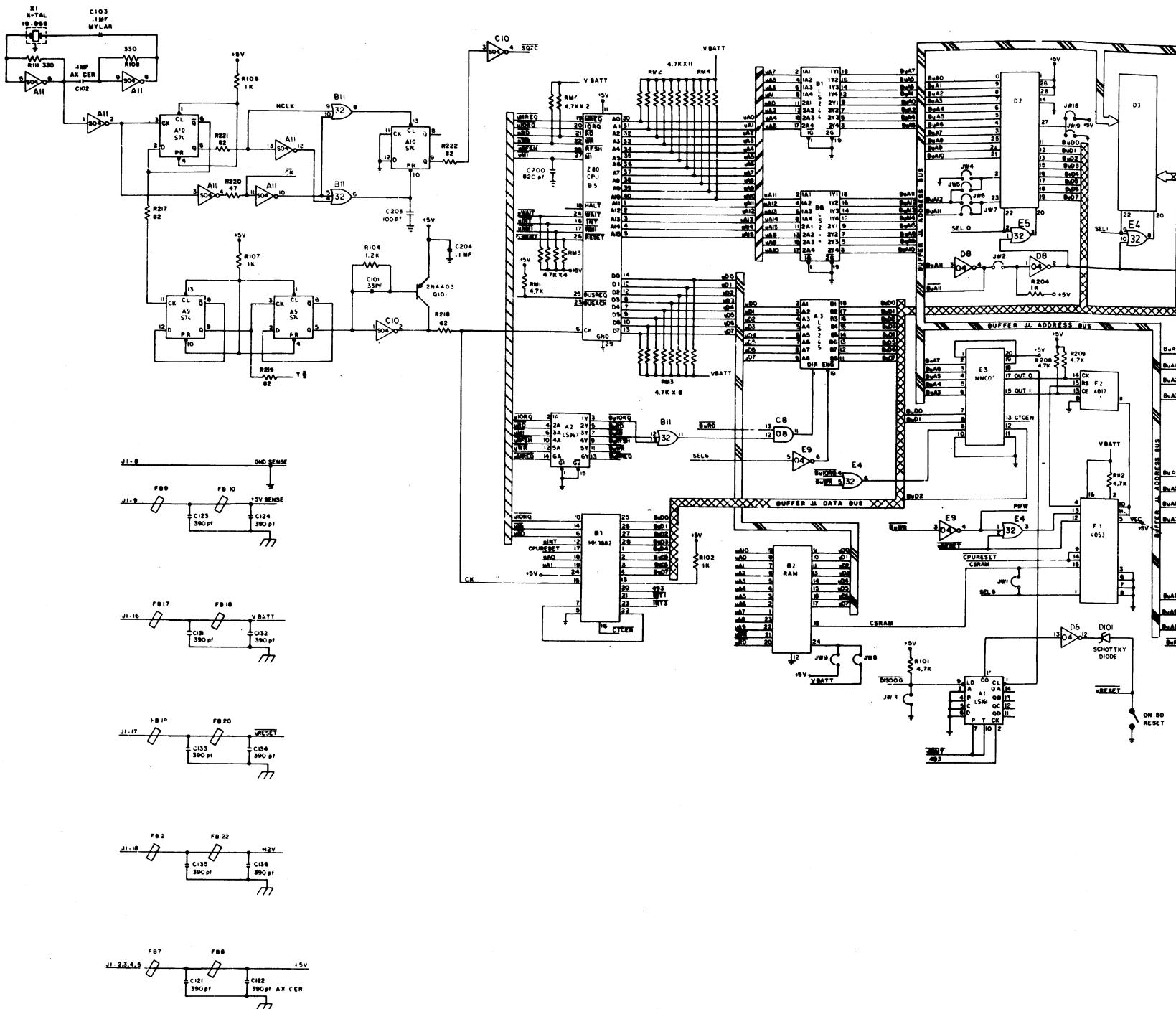
**DUAL PWR AMP W/CASS INTERFACE
SCHEMATIC DWG
A081 S1496 B358**

PART NO.

M051 - 00358 - B009



PROJECT ENG: JOHN BOYDSTON		USED ON KOZMIK KROOZ'R		Bally / MIDWAY MFG. CO.
DO NOT SCALE DWG.		HEAT TREAT	SCALE	FRANKLIN PK. ILL.
DIM. TOLERANCES UNLESS SPECIFIED		DRA. C-6	FULL	PART NO.
CONCENTRICITY T.I.R. .003		DATE 2/17/83	NO. REQ'D 1 PER	A082-91458-E000
FRACTIONAL .1/64				A084-91458-E000
DECIMAL .005				M051-00986 - E024
HOLE DIA. +.002-.000				



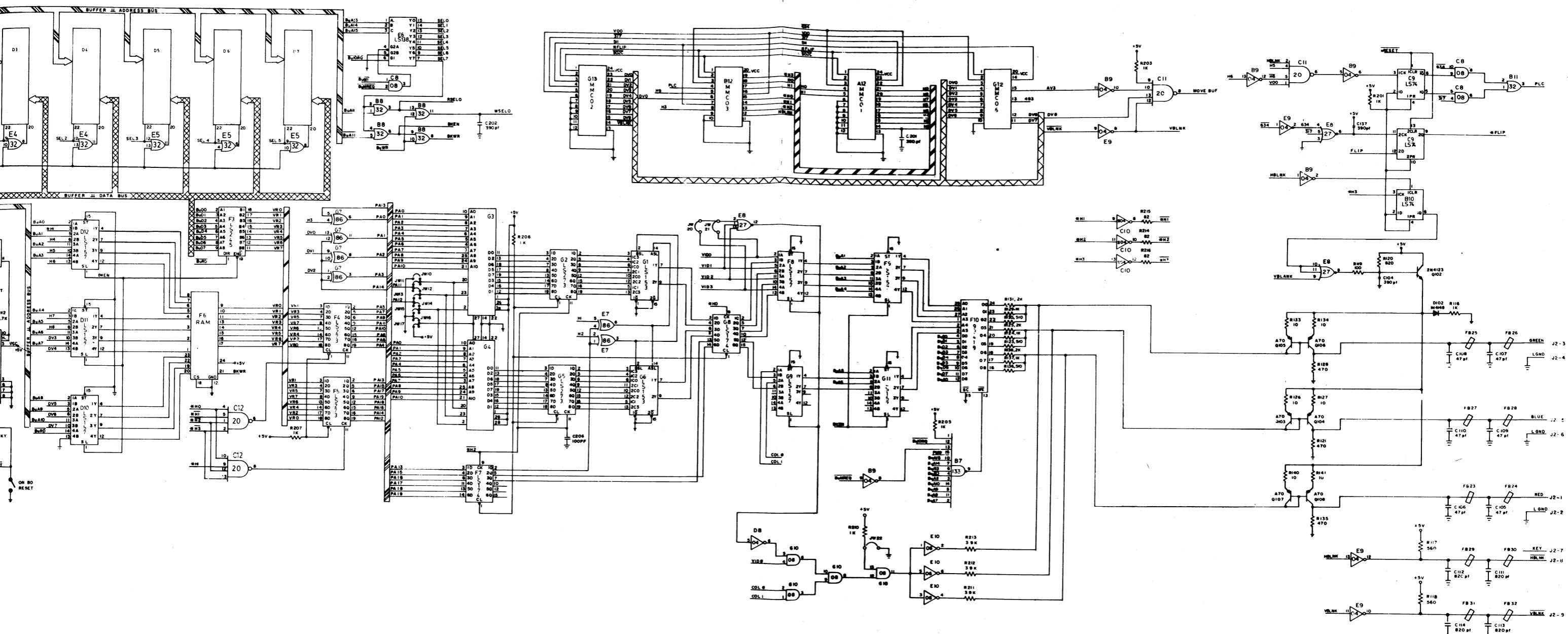
The diagram shows the following connections:

- J1-19 connects to EARTH GND.
- J1-7 connects to GND.
- J1-5 connects to GND.
- J1-10 connects to +5V.
- J1-14 connects to KEY.
- J1-1 connects to +5V.
- J1-15 connects to KEY.
- J1-20 connects to ANALOG GND.

72 PIN TEST CONNECTOR	
1 L	GND
2 -5V	26
3 GND	27
4 -12V	28
5 H2V	29
6 R1U	30
7 H2D	31
8 VATT	32
9 DIO	33
10 D01	34
11 D02	35
12 D03	36
13 D04	37
14 D05	38
15 D06	39
16 D07	40
17 VID 0	41
18 VID 1	42
19 VID 2	43
20 VID 3	45
21 H2VID	46
22 BYT	48
23 RT3	47
24	49
25	50
26	51
27	52
28	53
29	54
30	55
31	56
32	57
33	58
34	59
35	60
36	61
37	62
38	63
39	64
40	65
41	66
42	67
43	68
44	69
45	70
46	71
47	72
48	73
49	74
50	75
51	76
52	77
53	78
54	79
55	80
56	81
57	82
58	83
59	84
60	85
61	86
62	87
63	88
64	89
65	90
66	91
67	92
68	93
69	94
70	95
71	96
72	97
73	98
74	99
75	100

	-3	-4	-5	-6	-7
1 L	SND	A GND	L GND	L GND	N.U.
2 L	GK1	2 A GND	2 GND	2 GND	2 COL B
3 L	GND	3 A GND	3 GND	3 GND	3 COL C
4 L	GND	4 B GND	4 +5V	4 BUD	4 BLK D
5 L	GND	5 B GND	5 +5V	5 BUD	5 BGR E
6 L	GND	6 B GND	6 +5V	6 BUD	6 H3 F
7 L	U	7 P+2	7 N.U.	7 BUD	7 H4 G
8 L	U	8 B GND	8 N.U.	8 BUD	8 HS G
9 L	U	9 B GND	9 N.U.	9 BUD	9 HS G
10 R	ECHO	10 B GND	10 N.U.	10 BUD	10 H7 H
11 R	ECHO	11 +12V	11 PSELLO	11 BUD	11 HS I
12 R	ECHO	12 -12V	12 -SENSE 12	12 L GND	12 L BUD J
13 R	ECHO	13 -SENSE 13	13 BUD	13 L GND	13 L BUD J
14 R	ECHO	14 ECHO	14 MOVE BU	14 BUD	14 VID O
15 R	ECHO	15 N.U.	15 BUD	15 BUD	15 VID O
16 R	ECHO	16 BUD	16 DIA	16 BUD	16 VID O
17 R	ECHO	17 U	17 U	17 BUD	17 VID O
18 R	ECHO	18 N.U.	18 DV2	18 BUD	18 N.U.
19 R	FLIP	19 +5V	19 DV3	19 BUD	19 +5V
20 R	FLIP	20 -5V	20 DV4	20 BUD	20 +5V
21 R	NU	21 +5V	21 DV5	21 BUD	21 +5V
22 R	NU	22 L GND	22 DV6	22 BUD	22 L GND
23 R	NU	23 L GND	23 DV7	23 BUD	23 L GND

NOTES



PROJECT #10 R.A. PLOUSSARD		MEED ON	JOURNEY	REVISIONS
BUDGET 100-100		FULL	NO. 1 (ONE)	1
THE FIRM'S NAME RCA		SUPER CPU MCR III SCHEMATIC DWG A062-91475-D000		PART NO M051-00304-0006
04/15/83				