SP-284
1st printing

GAUNTLET™

Schematic Package Supplement to the Gauntlet™ Operators Manual

NOTE
This staple temporarily holds the schematic package together. Remove the staple before using these schematics.

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NOTE
In the schematics printed on Sheets 1-16 a slash (/) in front of a signal name indicates an active low signal. In the signal name glossary (printed at the end of this schematic package) these signals are overscored, e.g., $\overline{\text{COMPSYNC}}$.

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Gauntlet™ Game PCB Schematic Diagram

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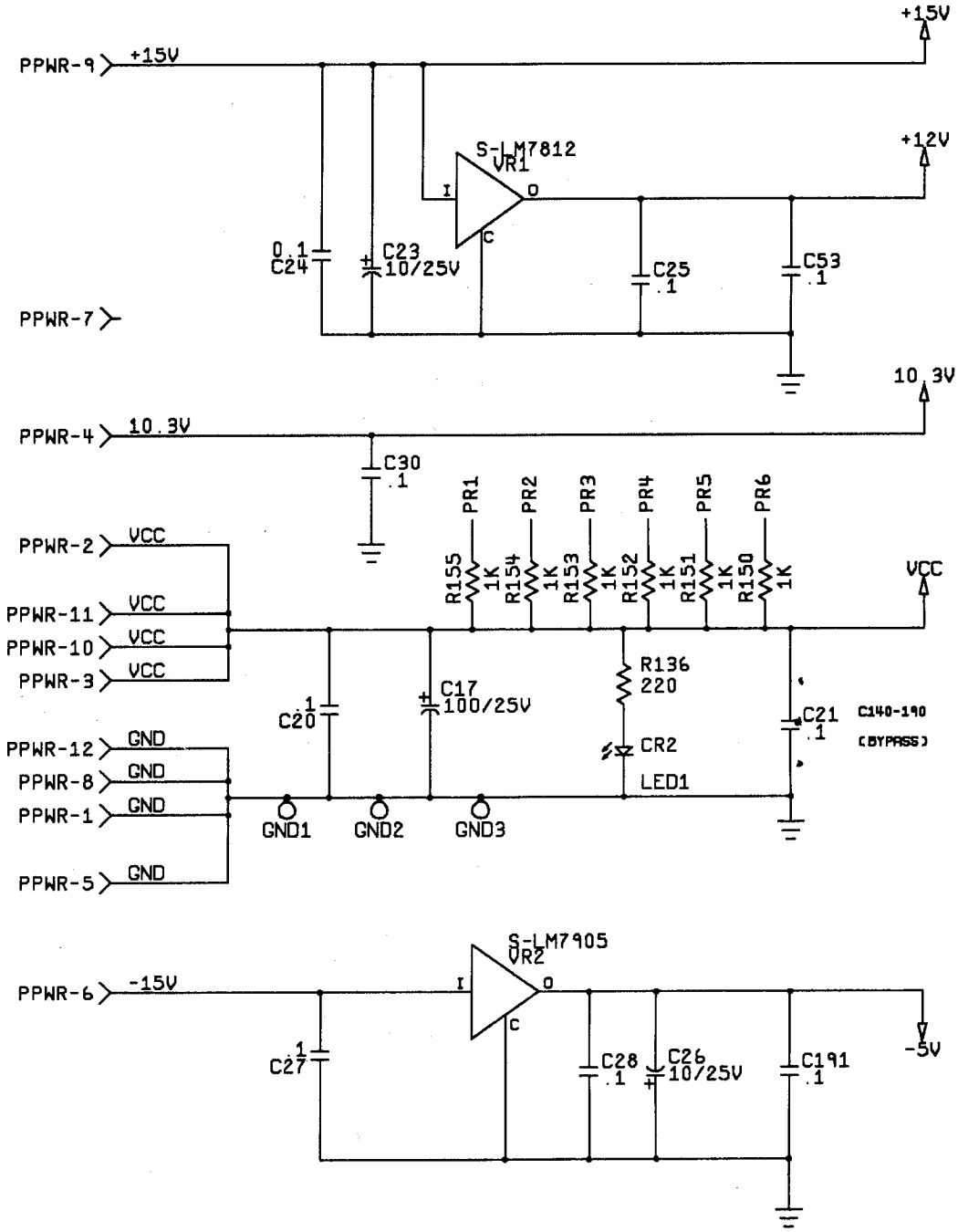
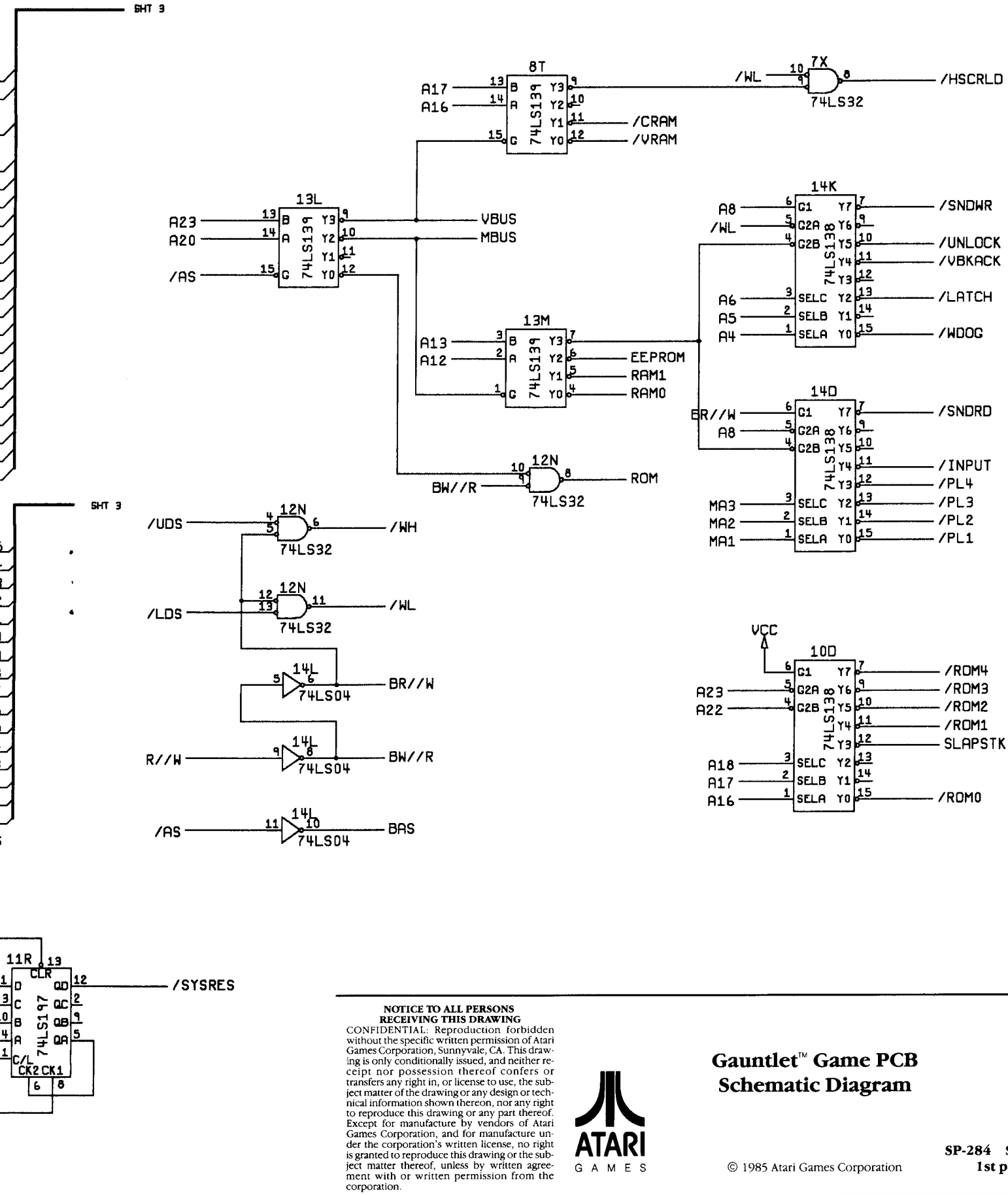

+15V
PPWR-9
+15V
S-LM7812
VR1
I
O
C
+12V
0.1
C24
C23
10/25V
C25
.1
C53
.1
PPWR-7
10.3V
PPWR-4
10.3V
C30
.1
PR1
PR2
PR3
PR4
PR5
PR6
R155
1K
R154
1K
R153
1K
R152
1K
R151
1K
R150
1K
VCC
PPWR-2
VCC
PPWR-11
VCC
PPWR-10
VCC
PPWR-3
VCC
R136
220
C17
100/25V
C20
.1
C21
.1
C140-190
(BYPASS)
CR2
LED1
PPWR-12
GND
PPWR-8
GND
PPWR-1
GND
PPWR-5
GND
GND1
GND2
GND3
S-LM7905
VR2
PPWR-6
-15V
C27
.1
C28
.1
C26
10/25V
C191
.1
-5V



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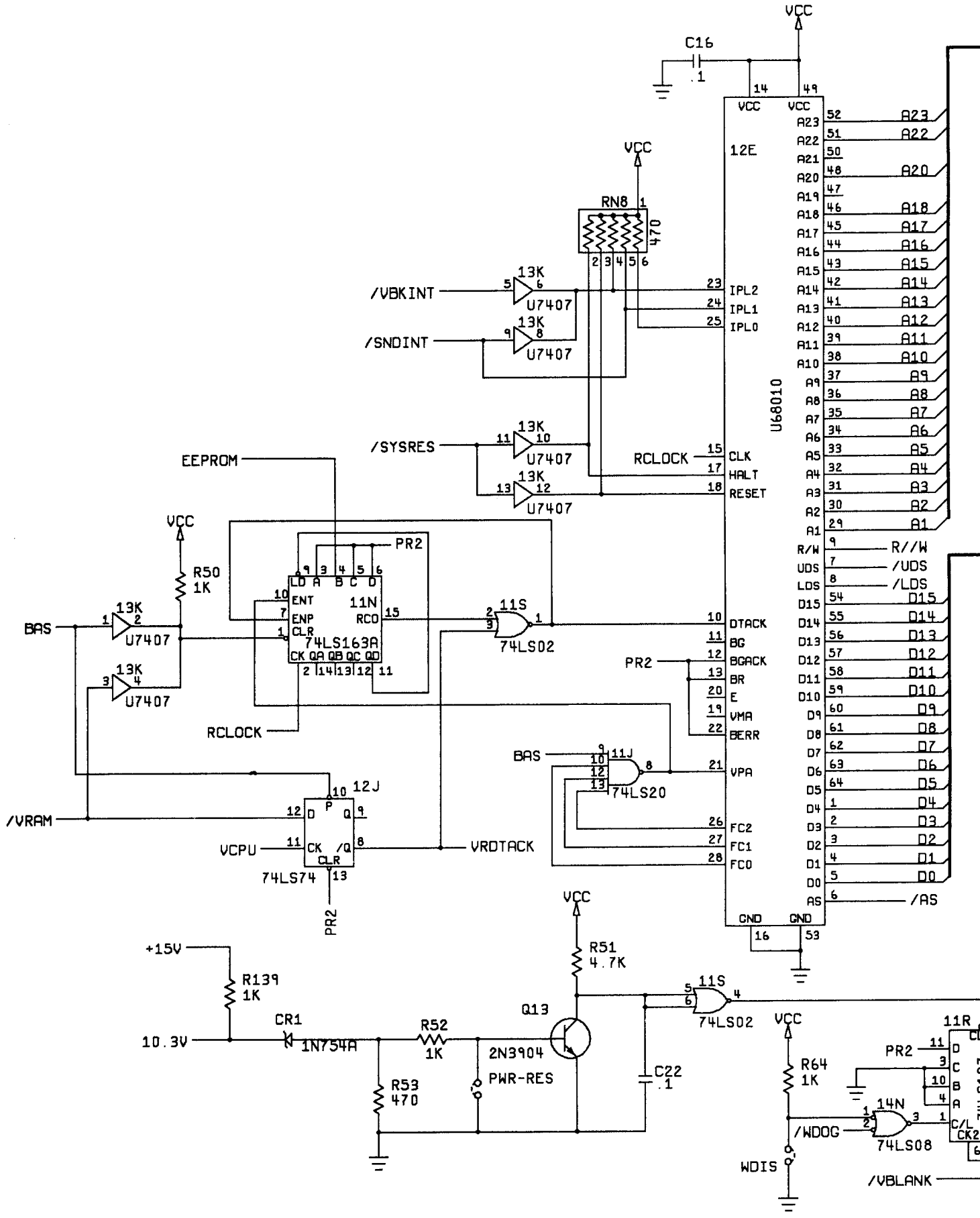
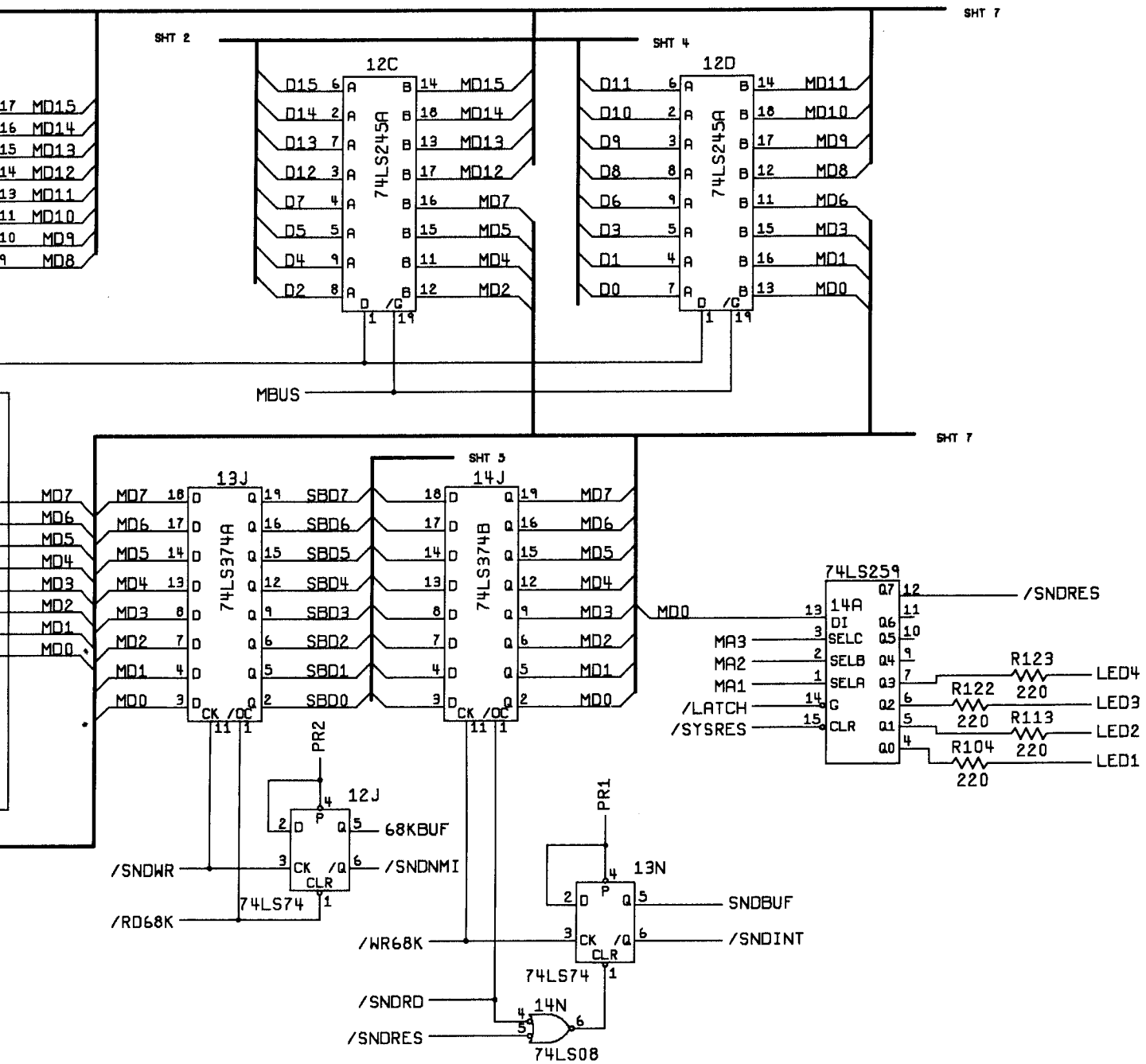

VCC
C16
.1
12E
U68010
RN8
470
/VBKINT
/SNDINT
/SYSRES
13K
U7407
IPL2
IPL1
IPL0
RCLOCK
CLK
HALT
RESET
EEPROM
R50
1K
BAS
PR2
74LS163A
11N
ENT
ENP
CLR
RCO
11S
74LS02
DTACK
BG
BGACK
BR
E
VMA
BERR
VPA
FC2
FC1
FC0
GND
A23
A22
A21
A20
A19
A18
A17
A16
A15
A14
A13
A12
A11
A10
A9
A8
A7
A6
A5
A4
A3
A2
A1
R/W
UDS
LDS
D15
D14
D13
D12
D11
D10
D9
D8
D7
D6
D5
D4
D3
D2
D1
D0
AS
/AS
/UDS
/LDS
R//W
RCLOCK
/VRAM
VCPU
VRDTACK
12J
74LS74
11J
74LS20
+15V
10.3V
R139
1K
CR1
1N754A
R52
1K
R53
470
Q13
2N3904
PWR-RES
R51
4.7K
C22
.1
R64
1K
WDIS
/WDOG
14N
74LS08
/VBLANK
11R



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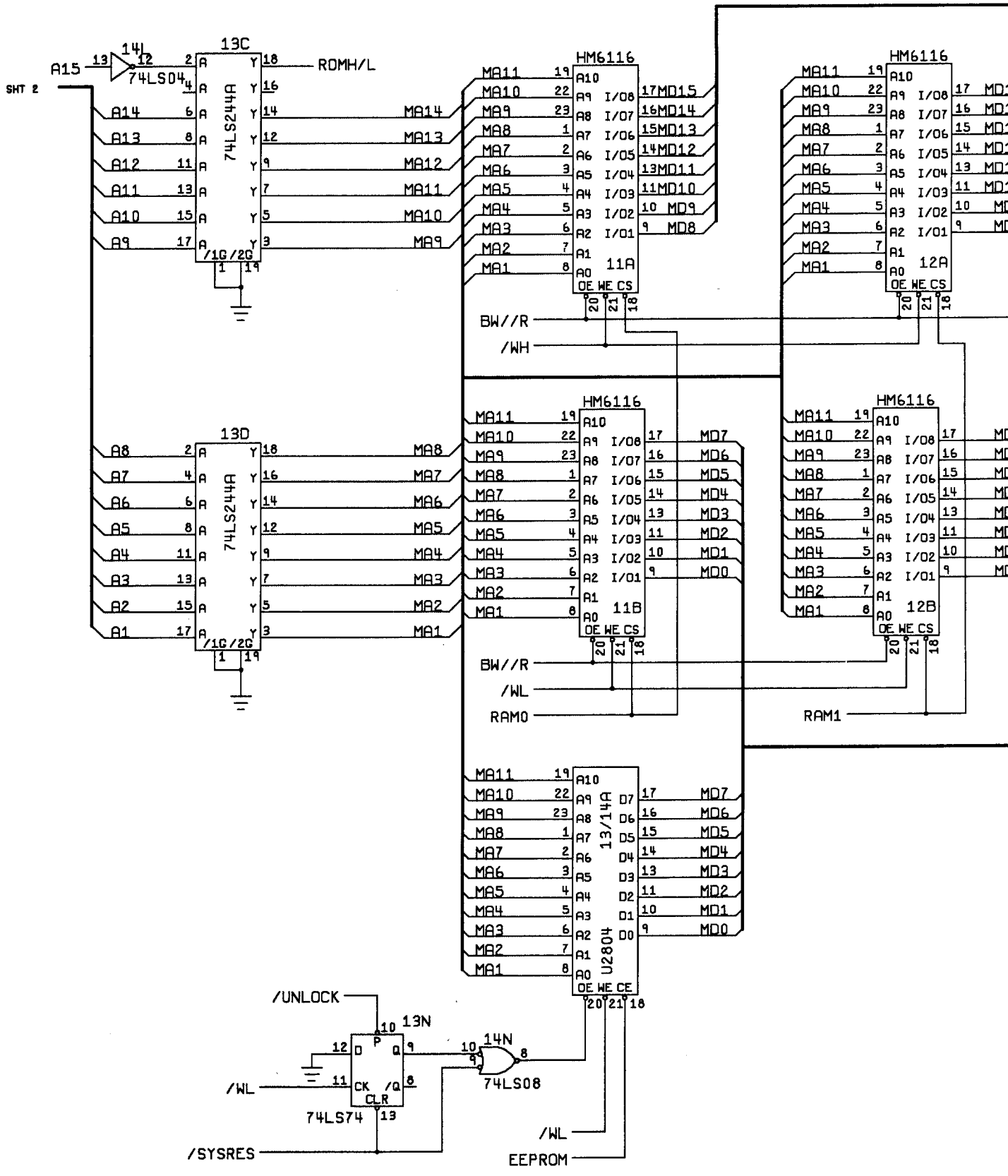
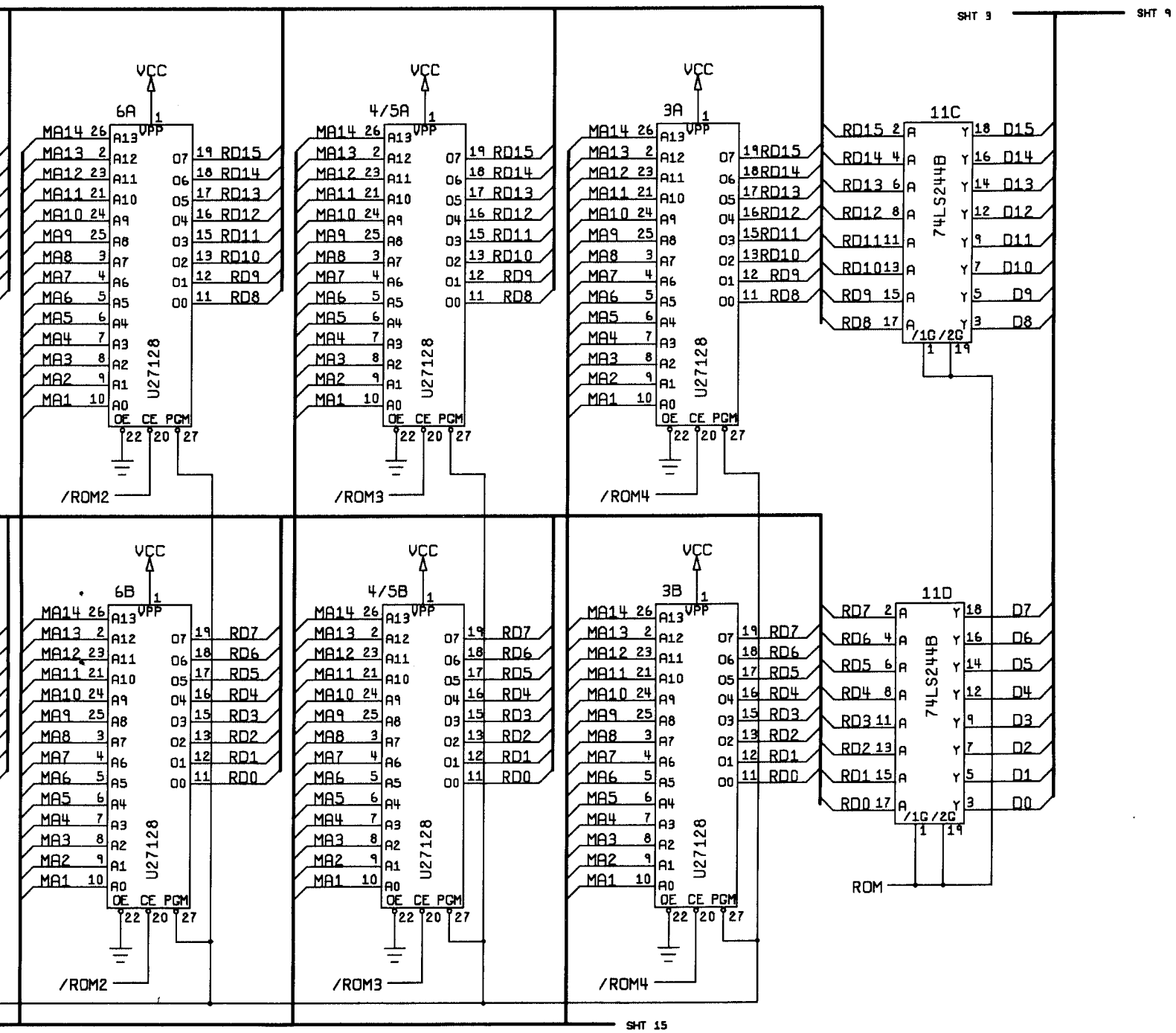

14L
74LS04
13C
74LS244A
/1G /2G
A15
SHT 2
ROMH/L
A14
A13
A12
A11
A10
A9
MA14
MA13
MA12
MA11
MA10
MA9
HM6116
11A
12A
MA11
MA10
MA9
MA8
MA7
MA6
MA5
MA4
MA3
MA2
MA1
MD15
MD14
MD13
MD12
MD11
MD10
MD9
MD8
BW//R
/WH
13D
A8
A7
A6
A5
A4
A3
A2
A1
MA8
MA7
MA6
MA5
MA4
MA3
MA2
MA1
11B
12B
MD7
MD6
MD5
MD4
MD3
MD2
MD1
MD0
/WL
RAM0
RAM1
13/14A
U2804
OE WE CE
/UNLOCK
13N
74LS74
14N
74LS08
/SYSRES
EEPROM



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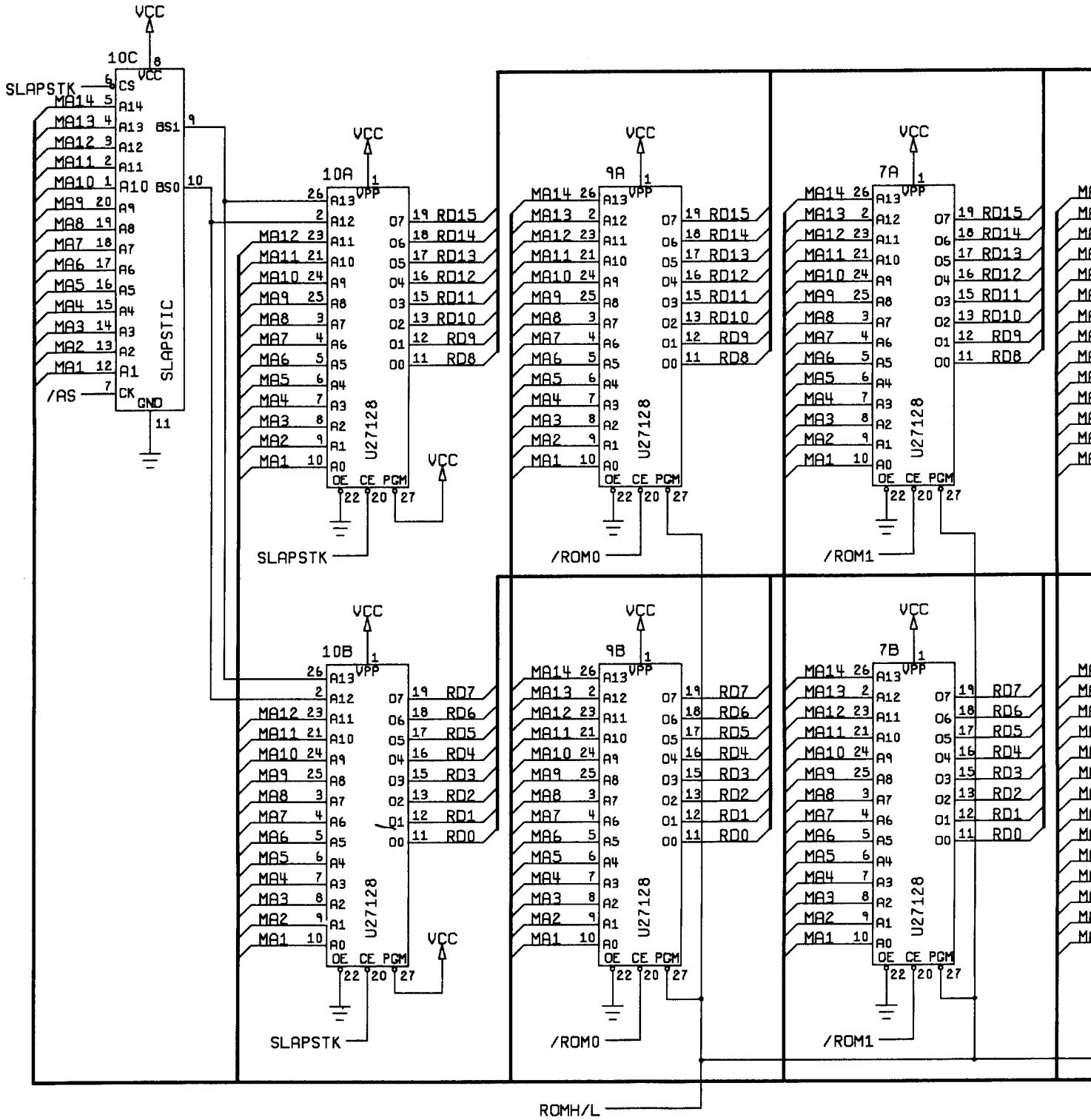
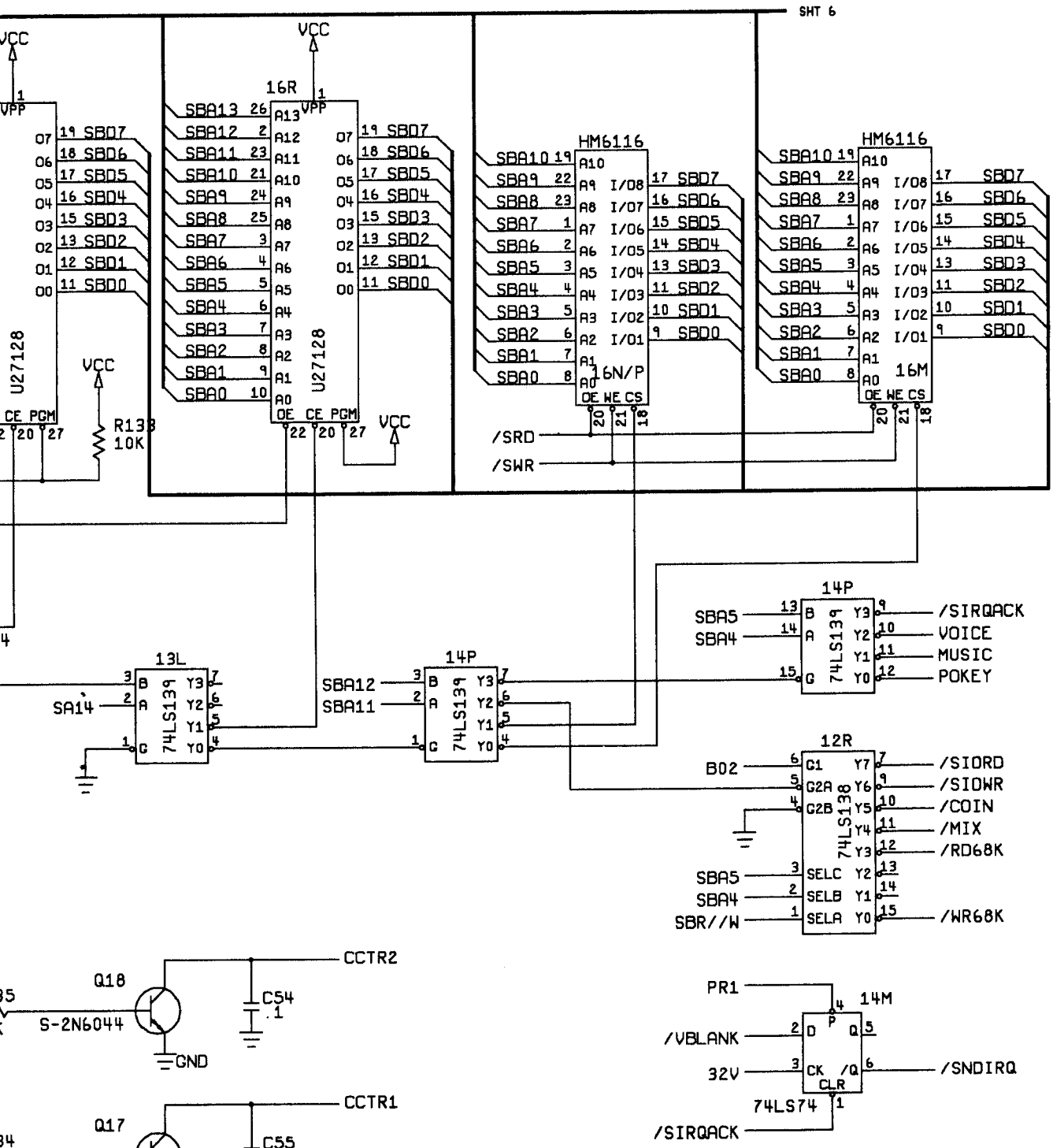

VCC
10C
SLAPSTK
/AS
SLAPSTIC
BS1
BS0
10A
10B
9A
9B
7A
7B
U27128
SLAPSTK
/ROM0
/ROM1
ROMH/L



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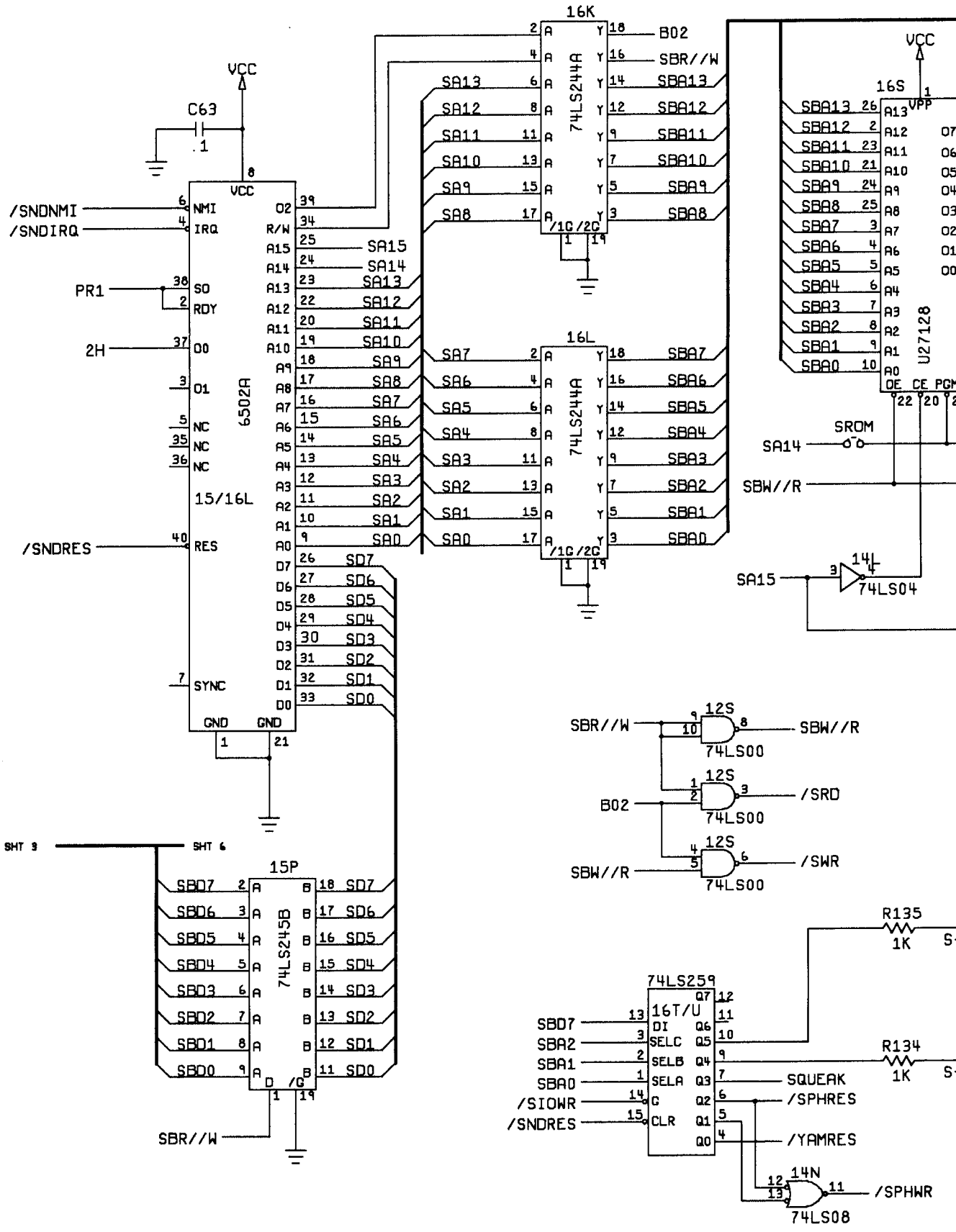
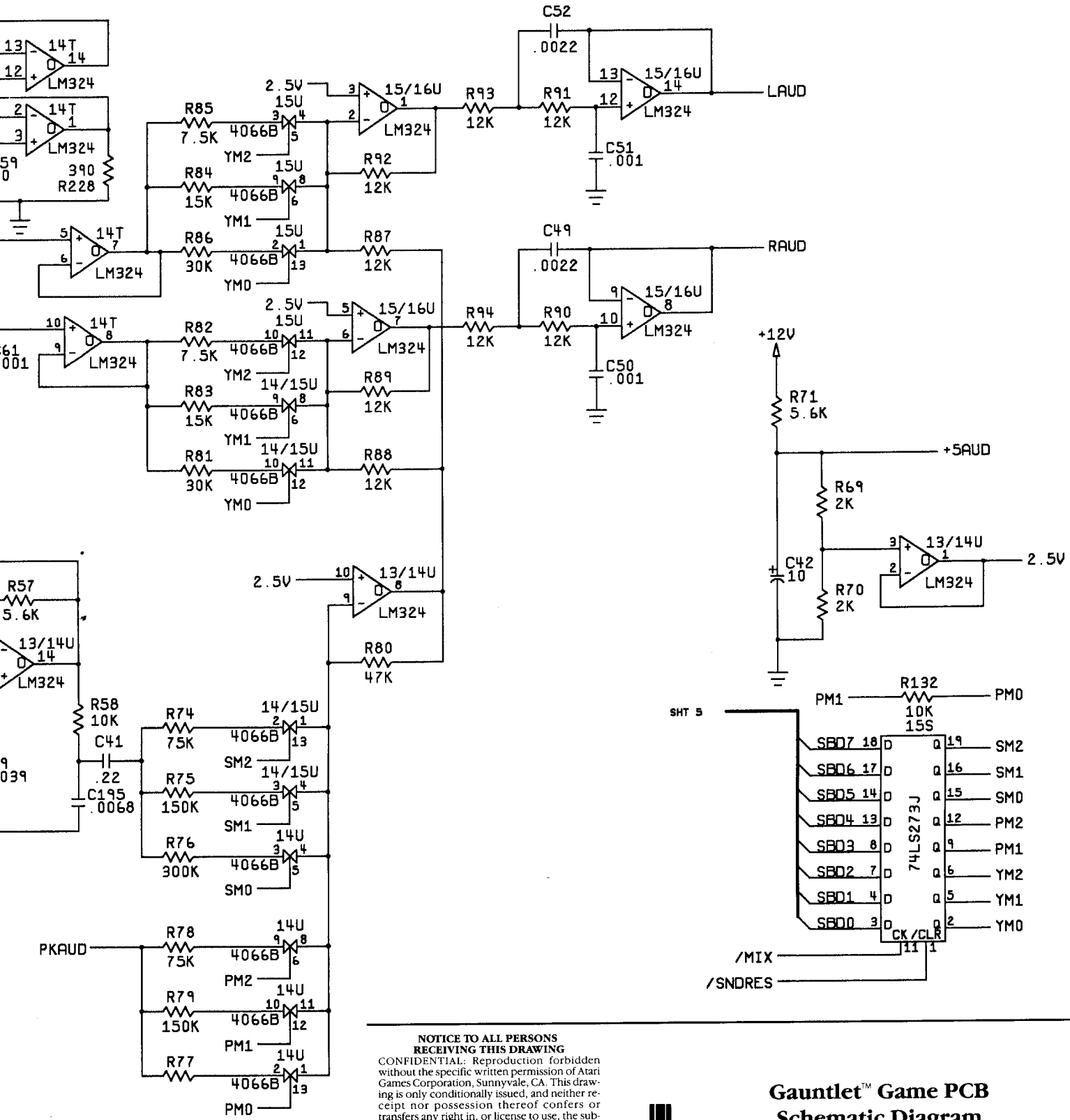

16K
74LS244A
16L
74LS244A
VCC
C63
.1
6502A
15/16L
/SNDNMI
/SNDIRQ
PR1
2H
/SNDRES
SA15
SA14
SA13
SA12
SA11
SA10
SA9
SA8
SA7
SA6
SA5
SA4
SA3
SA2
SA1
SA0
SD7
SD6
SD5
SD4
SD3
SD2
SD1
SD0
B02
SBR//W
SBA13
SBA12
SBA11
SBA10
SBA9
SBA8
SBA7
SBA6
SBA5
SBA4
SBA3
SBA2
SBA1
SBA0
16S
U27128
SROM
SBW//R
74LS04
SHT 3
SHT 6
15P
74LS245B
SBD7
SBD6
SBD5
SBD4
SBD3
SBD2
SBD1
SBD0
12S
74LS00
/SRD
/SWR
74LS259
16T/U
SBA2
SBA1
SBA0
/SIOWR
/SNDRES
SQUEAK
/SPHRES
/YAMRES
R135
R134
1K
14N
/SPHWR
74LS08



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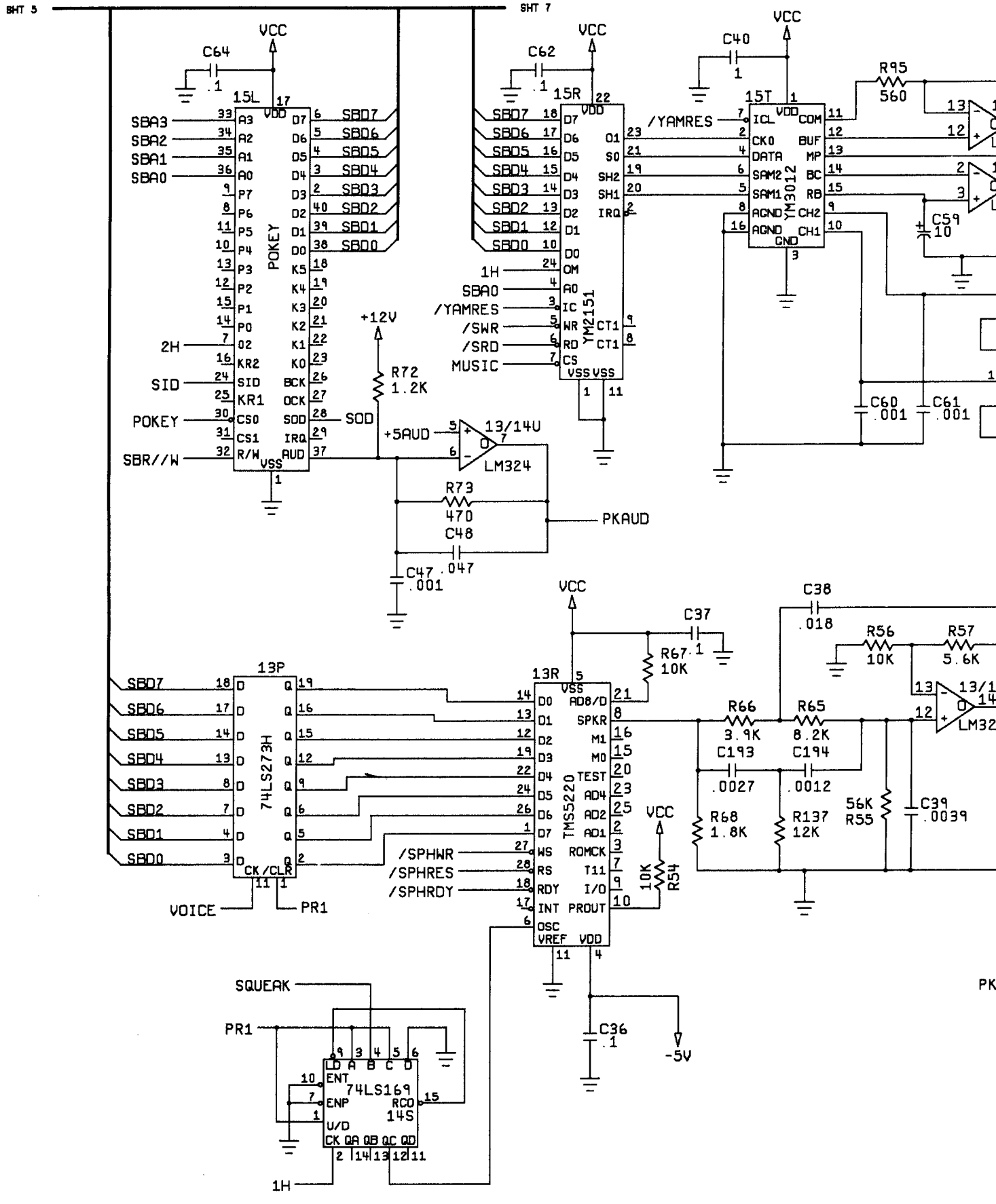
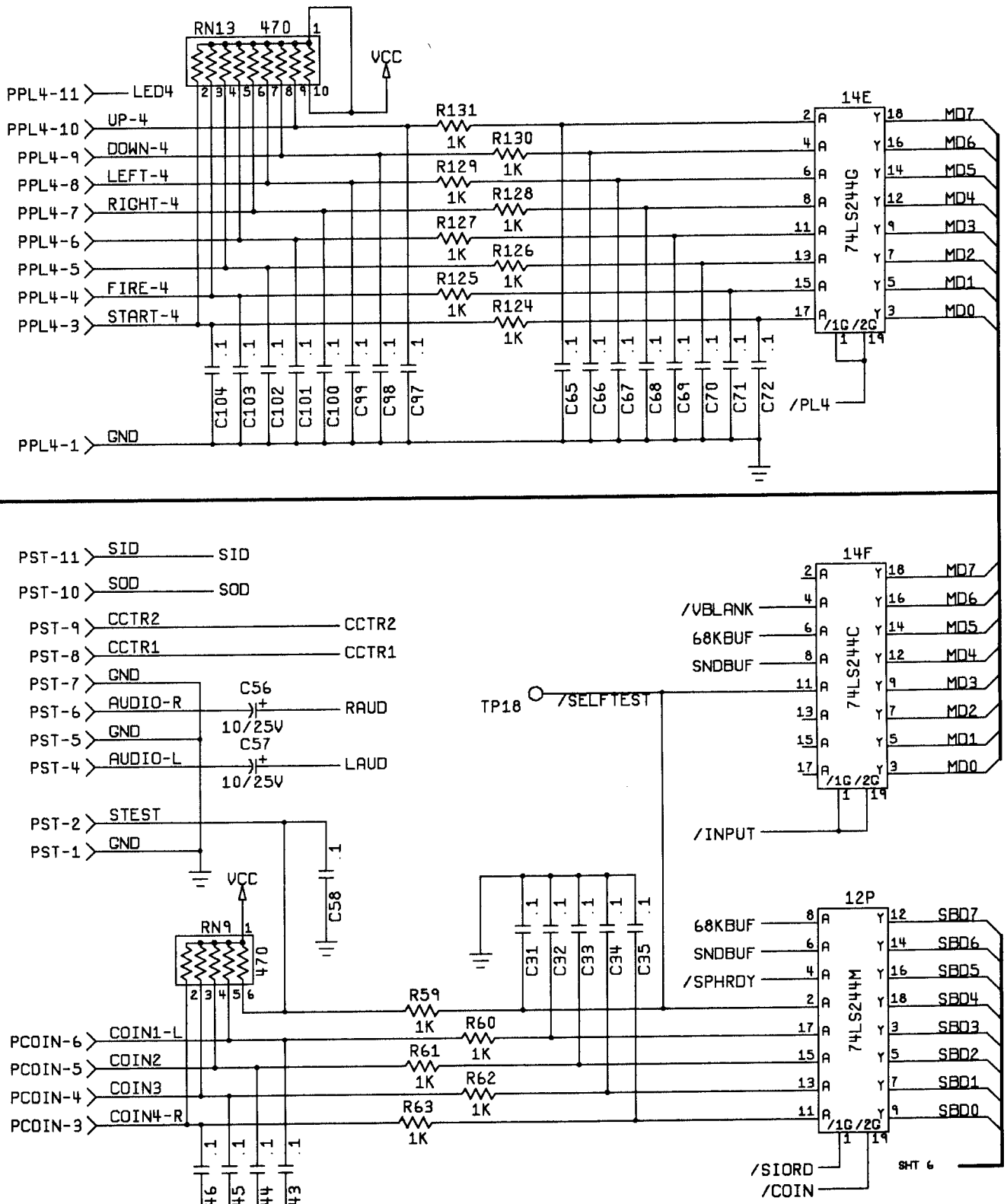

SHT 5
SHT 7
VCC
C64
.1
15L
SBA3
SBA2
SBA1
SBA0
2H
SID
POKEY
SBR//W
POKEY
SBD7
SBD6
SBD5
SBD4
SBD3
SBD2
SBD1
SBD0
VSS
+12V
R72
1.2K
SOD
+5AUD
13/14U
LM324
R73
470
C48
.047
C47
.001
PKAUD
C62
15R
1H
SBA0
/YAMRES
/SWR
/SRD
MUSIC
YM2151
C40
15T
R95
560
C59
10
C60
.001
C61
.001
YM3012
13P
74LS273H
VOICE
PR1
C37
R67
10K
13R
TMS5220
/SPHWR
/SPHRES
/SPHRDY
C38
.018
R56
10K
R57
5.6K
R66
3.9K
R65
8.2K
C193
.0027
C194
.0012
R68
1.8K
R137
12K
56K
R55
C39
.0039
R54
10K
C36
.1
-5V
SQUEAK
74LS169
1H



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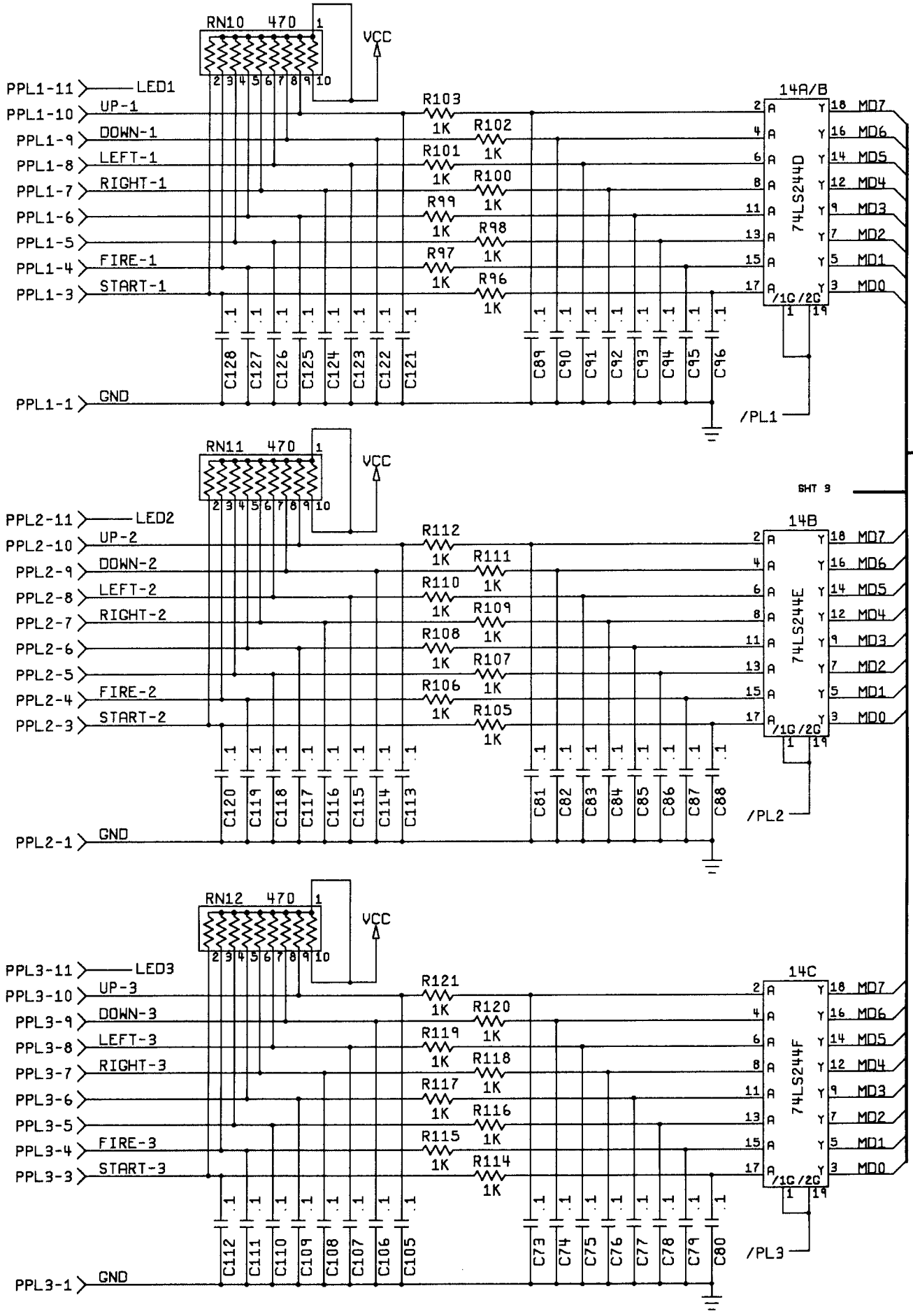
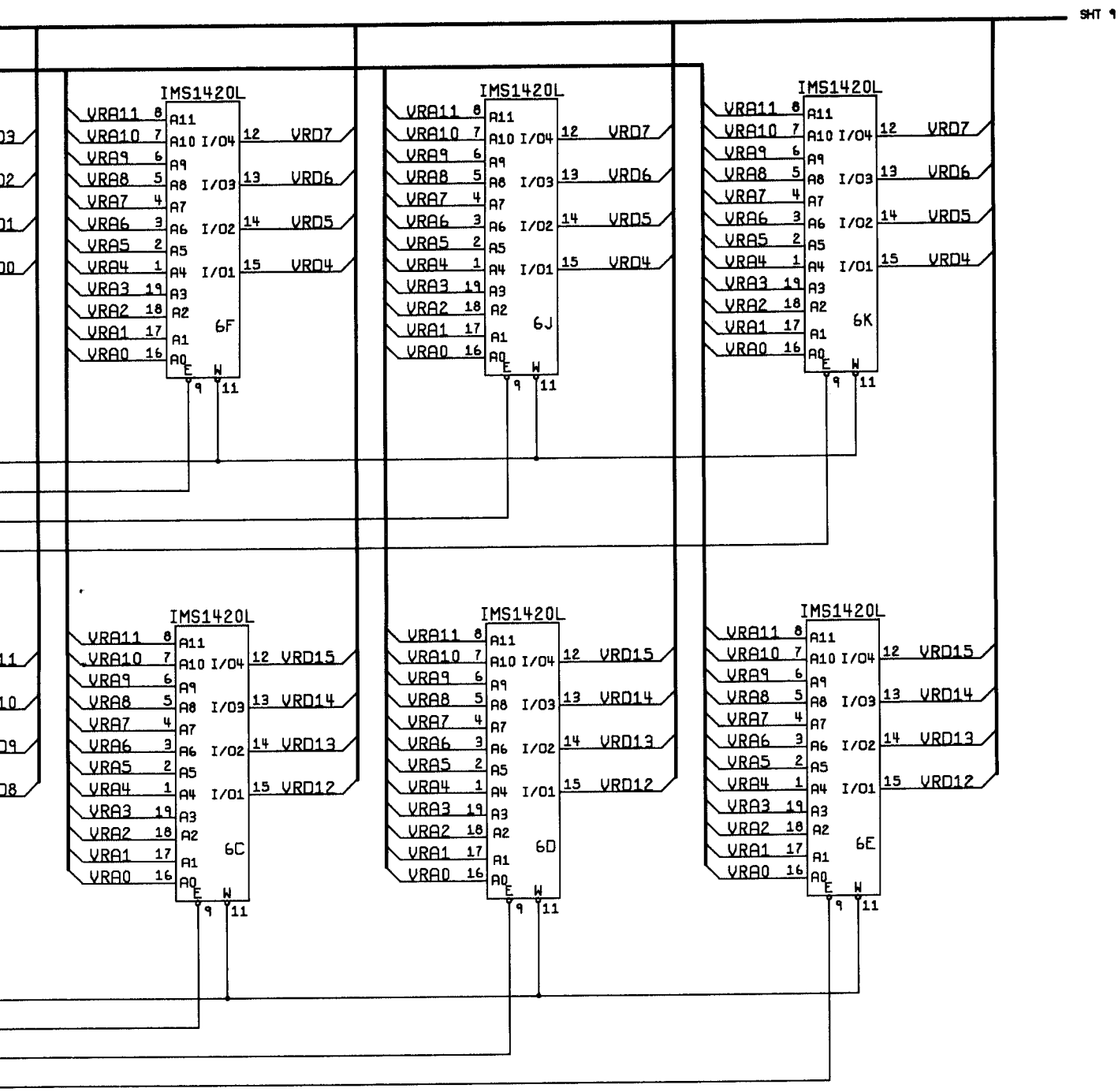

RN10 470
VCC
PPL1-11
LED1
PPL1-10
UP-1
PPL1-9
DOWN-1
PPL1-8
LEFT-1
PPL1-7
RIGHT-1
PPL1-6
PPL1-5
PPL1-4
FIRE-1
PPL1-3
START-1
PPL1-1
GND
R103 1K
R102 1K
R101 1K
R100 1K
R99 1K
R98 1K
R97 1K
R96 1K
C128 .1
C127 .1
C126 .1
C125 .1
C124 .1
C123 .1
C122 .1
C121 .1
C89 .1
C90 .1
C91 .1
C92 .1
C93 .1
C94 .1
C95 .1
C96 .1
14A/B
74LS244D
/1G /2G
/PL1
MD7
MD6
MD5
MD4
MD3
MD2
MD1
MD0
RN11 470
VCC
PPL2-11
LED2
PPL2-10
UP-2
PPL2-9
DOWN-2
PPL2-8
LEFT-2
PPL2-7
RIGHT-2
PPL2-6
PPL2-5
PPL2-4
FIRE-2
PPL2-3
START-2
PPL2-1
GND
R112 1K
R111 1K
R110 1K
R109 1K
R108 1K
R107 1K
R106 1K
R105 1K
C120 .1
C119 .1
C118 .1
C117 .1
C116 .1
C115 .1
C114 .1
C113 .1
C81 .1
C82 .1
C83 .1
C84 .1
C85 .1
C86 .1
C87 .1
C88 .1
14B
74LS244E
/1G /2G
/PL2
SHT 9
RN12 470
VCC
PPL3-11
LED3
PPL3-10
UP-3
PPL3-9
DOWN-3
PPL3-8
LEFT-3
PPL3-7
RIGHT-3
PPL3-6
PPL3-5
PPL3-4
FIRE-3
PPL3-3
START-3
PPL3-1
GND
R121 1K
R120 1K
R119 1K
R118 1K
R117 1K
R116 1K
R115 1K
R114 1K
C112 .1
C111 .1
C110 .1
C109 .1
C108 .1
C107 .1
C106 .1
C105 .1
C73 .1
C74 .1
C75 .1
C76 .1
C77 .1
C78 .1
C79 .1
C80 .1
14C
74LS244F
/1G /2G
/PL3
MD7
MD6
MD5
MD4
MD3
MD2
MD1
MD0



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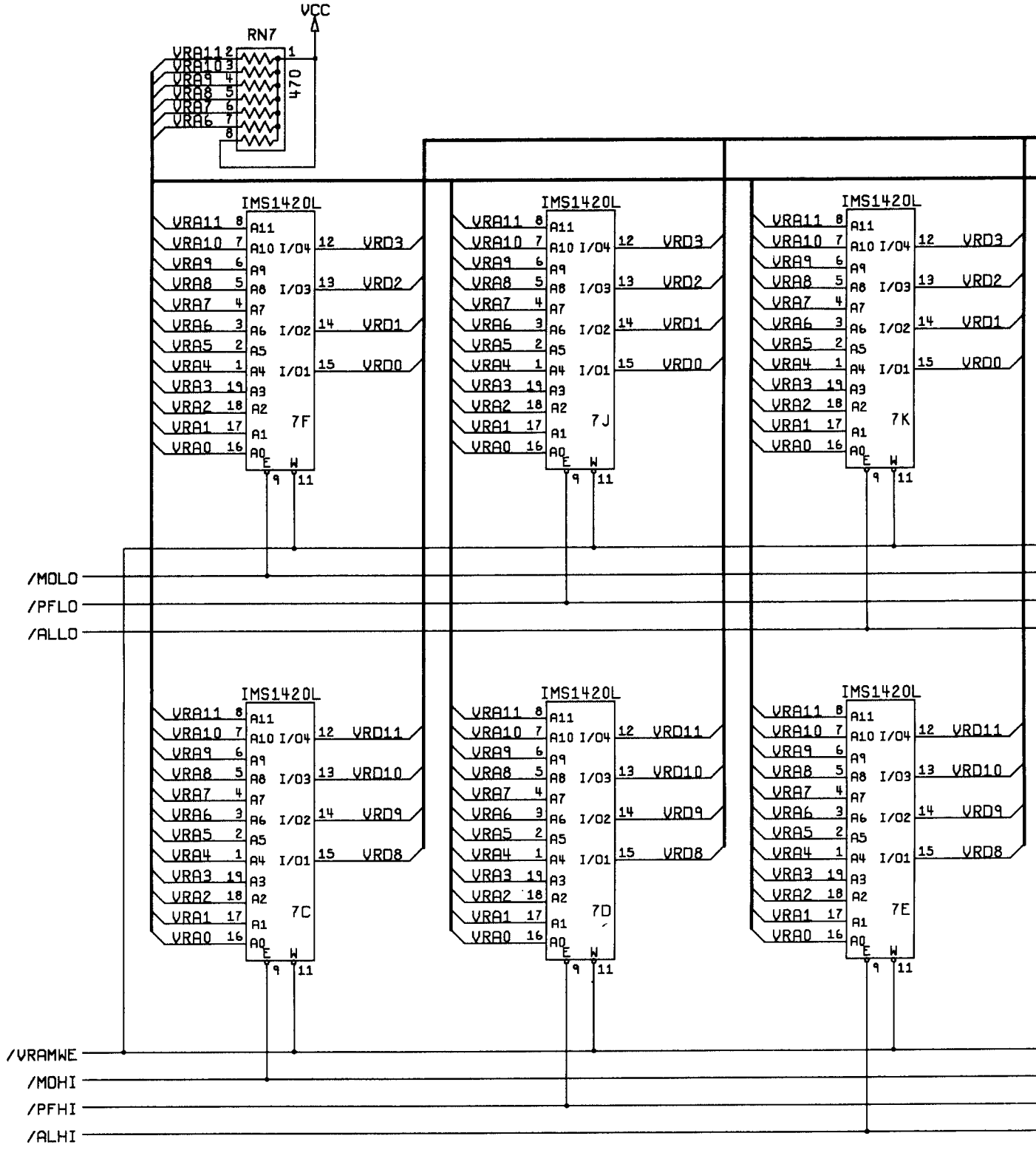
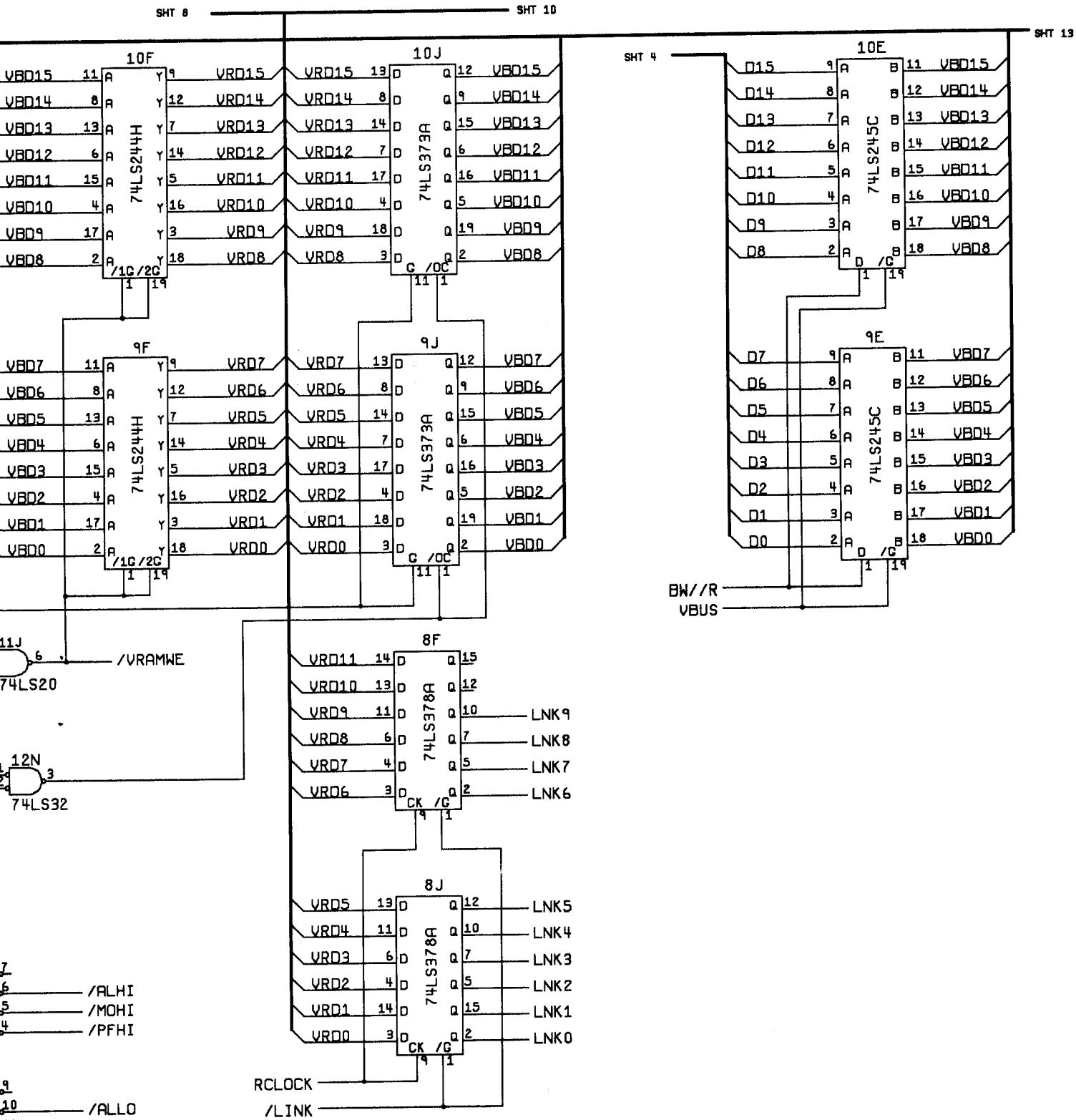

VCC
RN7
470
VRA11
VRA10
VRA9
VRA8
VRA7
VRA6
IMS1420L
7F
7J
7K
7C
7D
7E
VRD3
VRD2
VRD1
VRD0
VRD11
VRD10
VRD9
VRD8
/MOLO
/PFLO
/ALLO
/VRAMWE
/MOHI
/PFHI
/ALHI



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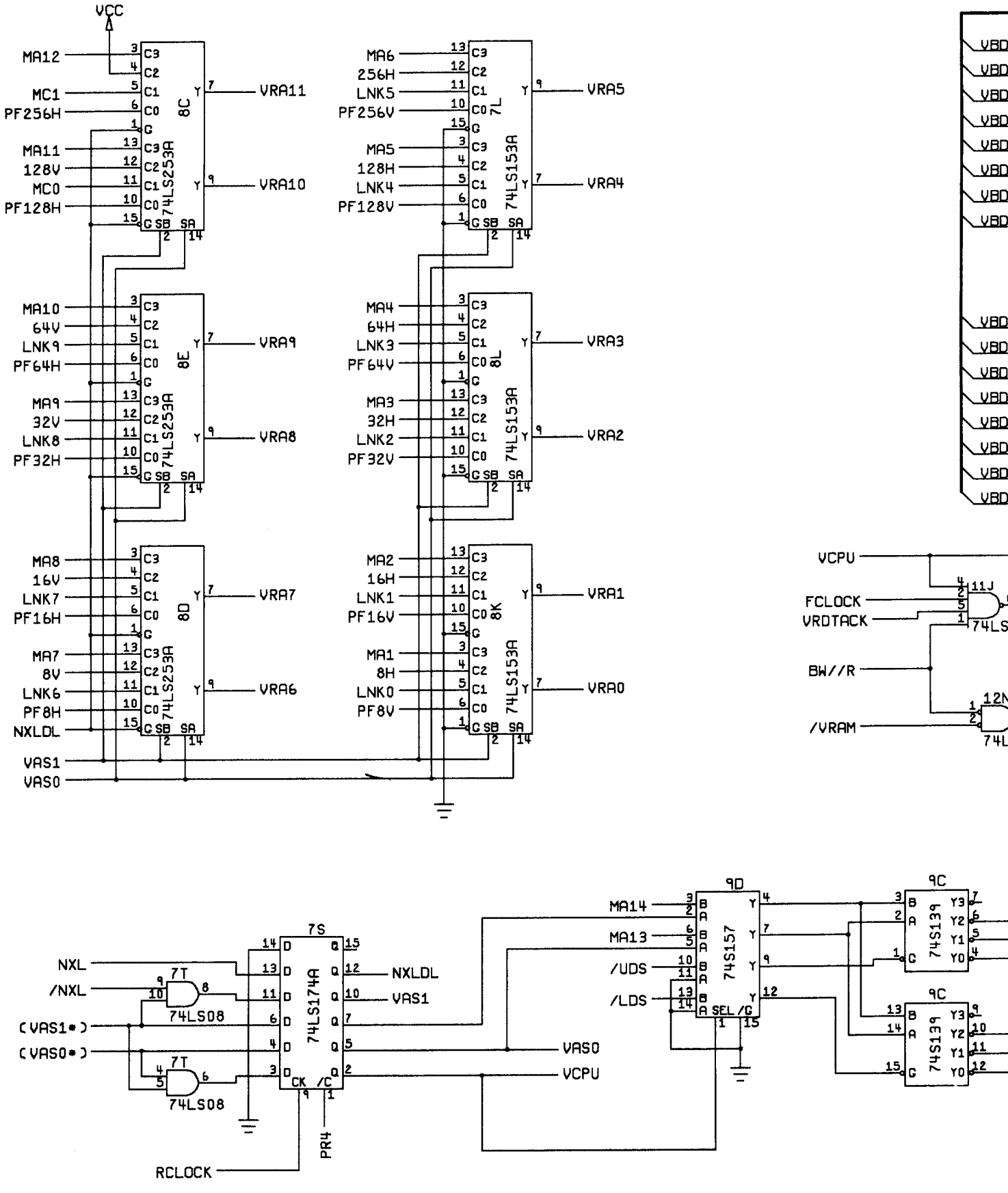
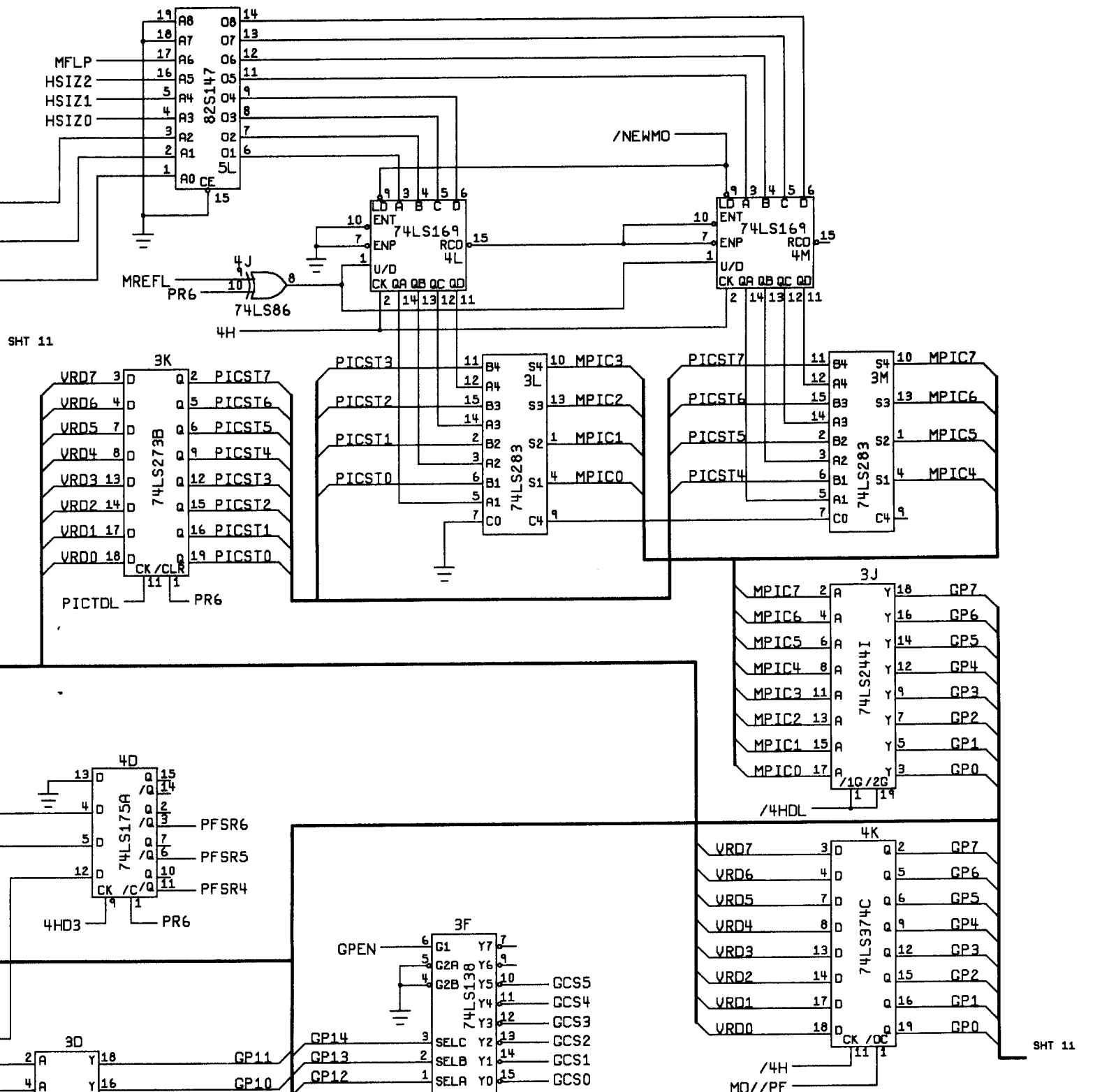

VCC
MA12
MC1
PF256H
MA11
128V
MC0
PF128H
8C
74LS253A
VRA11
VRA10
MA10
64V
LNK9
PF64H
MA9
32V
LNK8
PF32H
8E
74LS253A
VRA9
VRA8
MA8
16V
LNK7
PF16H
MA7
8V
LNK6
PF8H
NXLDL
8D
74LS253A
VRA7
VRA6
VAS1
VAS0
MA6
256H
LNK5
PF256V
MA5
128H
LNK4
PF128V
7L
74LS153A
VRA5
VRA4
MA4
64H
LNK3
PF64V
MA3
32H
LNK2
PF32V
8L
74LS153A
VRA3
VRA2
MA2
16H
LNK1
PF16V
MA1
8H
LNK0
PF8V
8K
74LS153A
VRA1
VRA0
VBD
VCPU
FCLOCK
VRDTACK
BW//R
/VRAM
11J
74LS
12N
74L
NXL
/NXL
(VAS1*)
(VAS0*)
7T
74LS08
7T
74LS08
7S
74LS174A
NXLDL
VAS1
VAS0
VCPU
RCLOCK
PR4
9D
74S157
MA14
MA13
/UDS
/LDS
SEL /G
9C
74S139
9C
74S139



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Gauntlet™ Game PCB Schematic Diagram

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SP-284 Sheet 10
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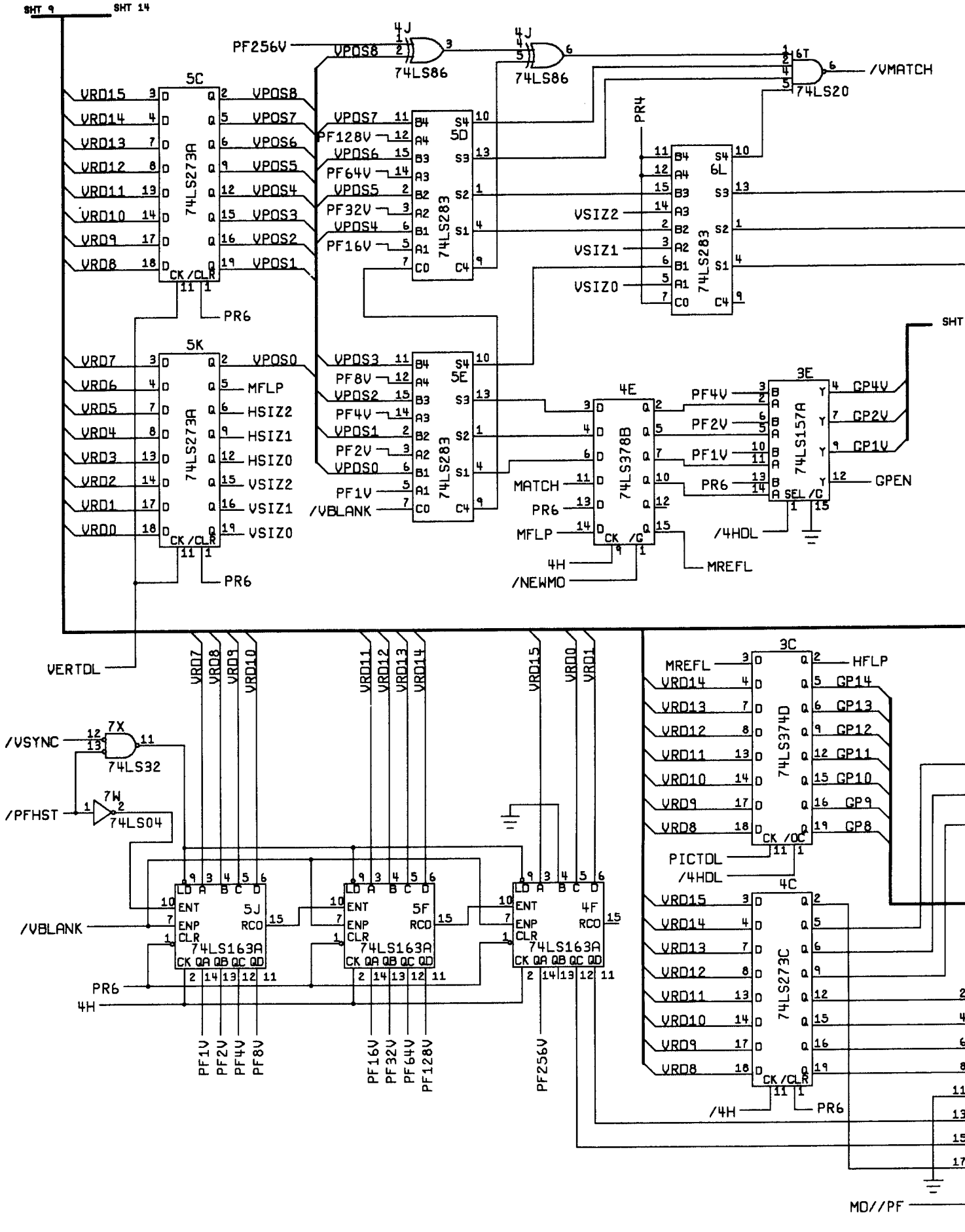
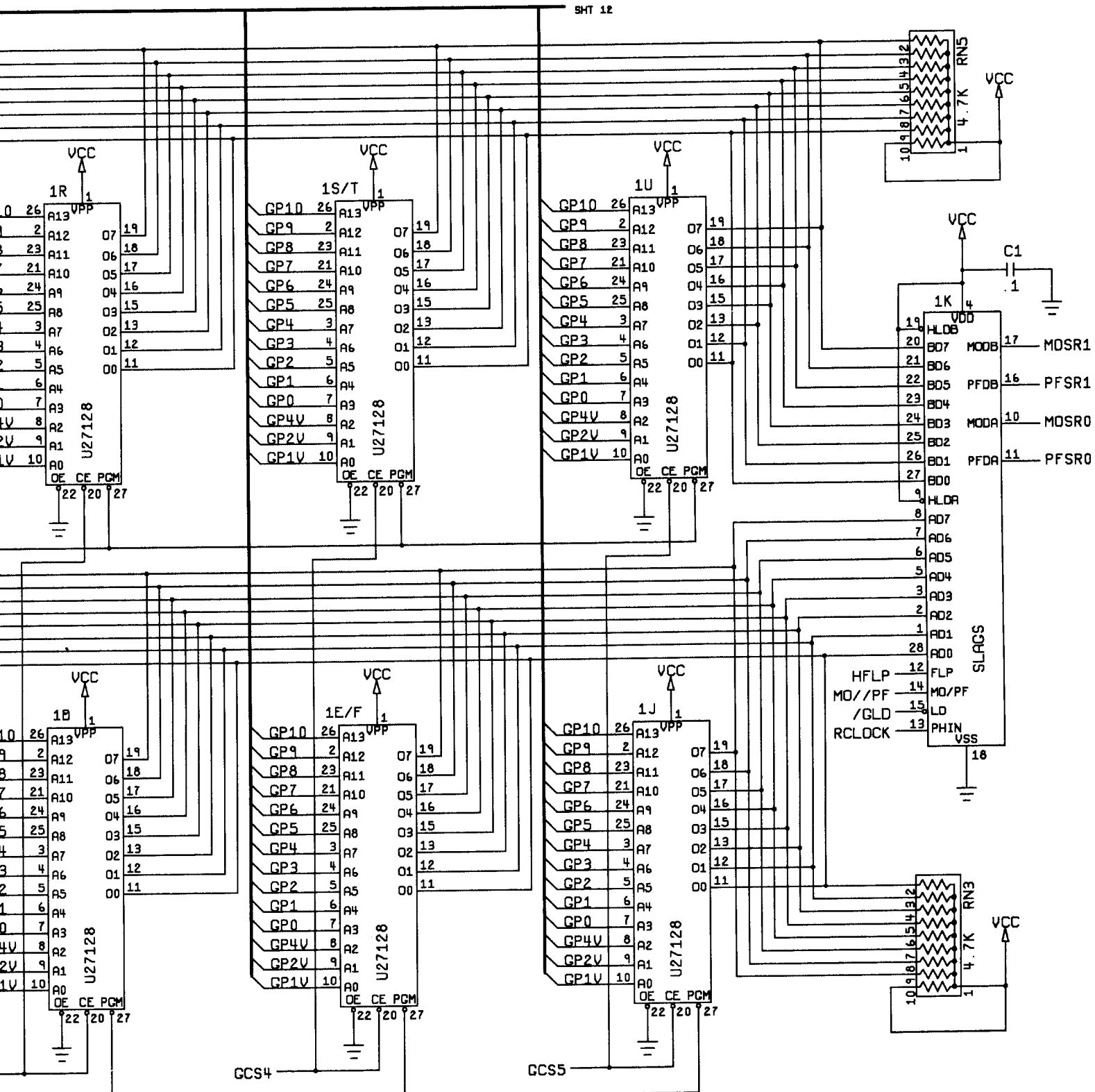

SHT 9
SHT 14
PF256V
VPOS8
4J
74LS86
4J
74LS86
6T
74LS20
/VMATCH
5C
74LS273A
VRD15
VRD14
VRD13
VRD12
VRD11
VRD10
VRD9
VRD8
VPOS8
VPOS7
VPOS6
VPOS5
VPOS4
VPOS3
VPOS2
VPOS1
CK /CLR
PR6
5D
74LS283
VPOS7
PF128V
VPOS6
PF64V
VPOS5
PF32V
VPOS4
PF16V
PR4
6L
74LS283
VSIZ2
VSIZ1
VSIZ0
5K
74LS273A
VRD7
VRD6
VRD5
VRD4
VRD3
VRD2
VRD1
VRD0
VPOS0
MFLP
HSIZ2
HSIZ1
HSIZ0
VSIZ2
VSIZ1
VSIZ0
5E
74LS283
VPOS3
PF8V
VPOS2
PF4V
VPOS1
PF2V
VPOS0
PF1V
/VBLANK
4E
74LS378B
MATCH
PR6
MFLP
4H
/NEWMO
MREFL
3E
74LS157A
PF4V
PF2V
PF1V
PR6
/4HDL
GP4V
GP2V
GP1V
GPEN
SHT
VERTDL
VRD7
VRD8
VRD9
VRD10
VRD11
VRD12
VRD13
VRD14
VRD15
VRD0
VRD1
7X
74LS32
/VSYNC
7W
74LS04
/PFHST
/VBLANK
PR6
4H
5J
74LS163A
5F
74LS163A
4F
74LS163A
PF1V
PF2V
PF4V
PF8V
PF16V
PF32V
PF64V
PF128V
PF256V
3C
74LS374D
MREFL
VRD14
VRD13
VRD12
VRD11
VRD10
VRD9
VRD8
HFLP
GP14
GP13
GP12
GP11
GP10
GP9
GP8
PICTDL
/4HDL
4C
74LS273C
VRD15
VRD14
VRD13
VRD12
VRD11
VRD10
VRD9
VRD8
/4H
PR6
MD//PF



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Gauntlet™ Game PCB Schematic Diagram

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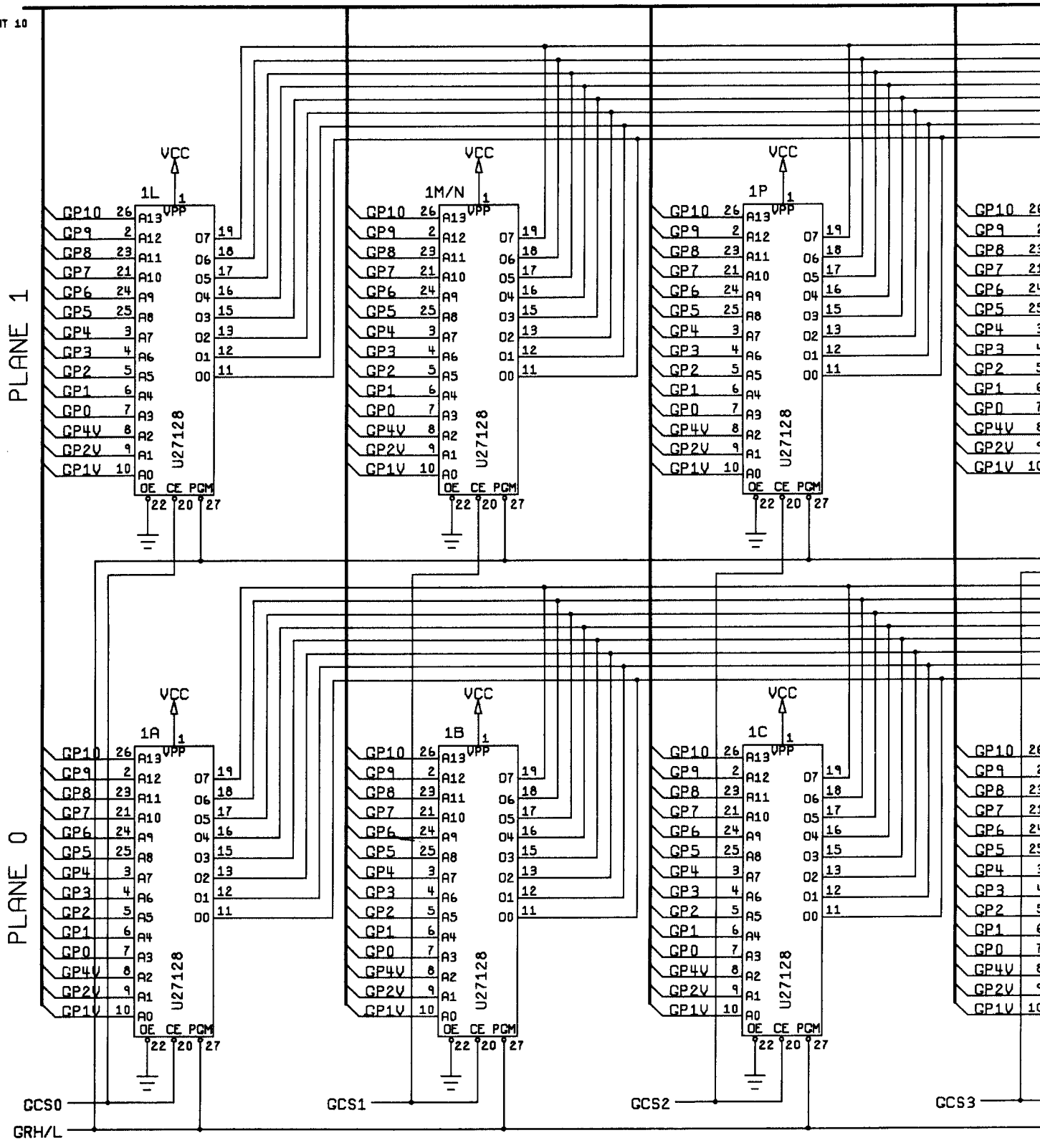
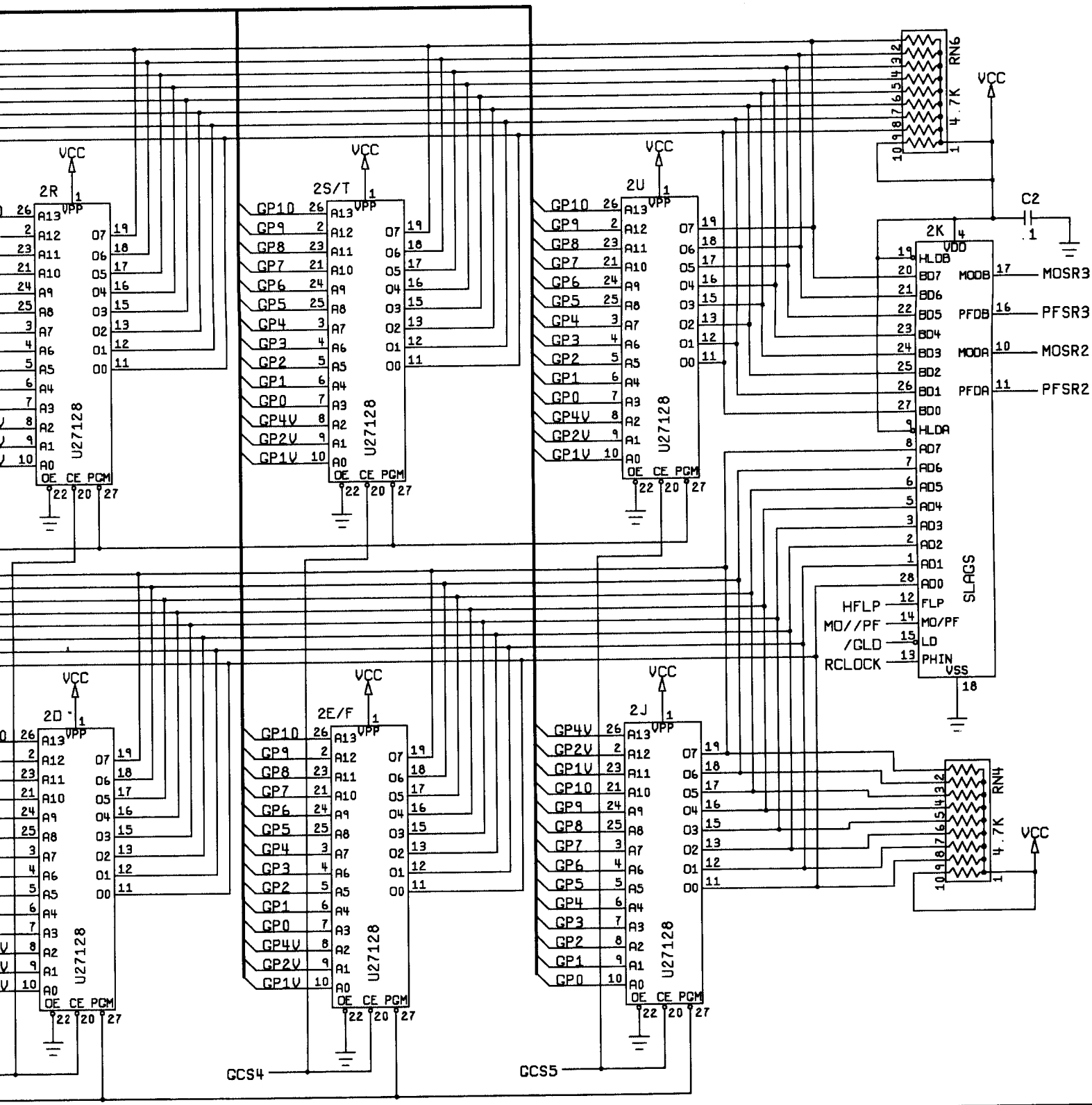

PLANE 1
PLANE 0
1L
1M/N
1P
1A
1B
1C
VCC
VPP
U27128
A13
A12
A11
A10
A9
A8
A7
A6
A5
A4
A3
A2
A1
A0
O7
O6
O5
O4
O3
O2
O1
O0
OE
CE
PGM
GP10
GP9
GP8
GP7
GP6
GP5
GP4
GP3
GP2
GP1
GP0
GP4V
GP2V
GP1V
GCS0
GCS1
GCS2
GCS3
GRH/L



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Gauntlet™ Game PCB Schematic Diagram

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SP-284 Sheet 12
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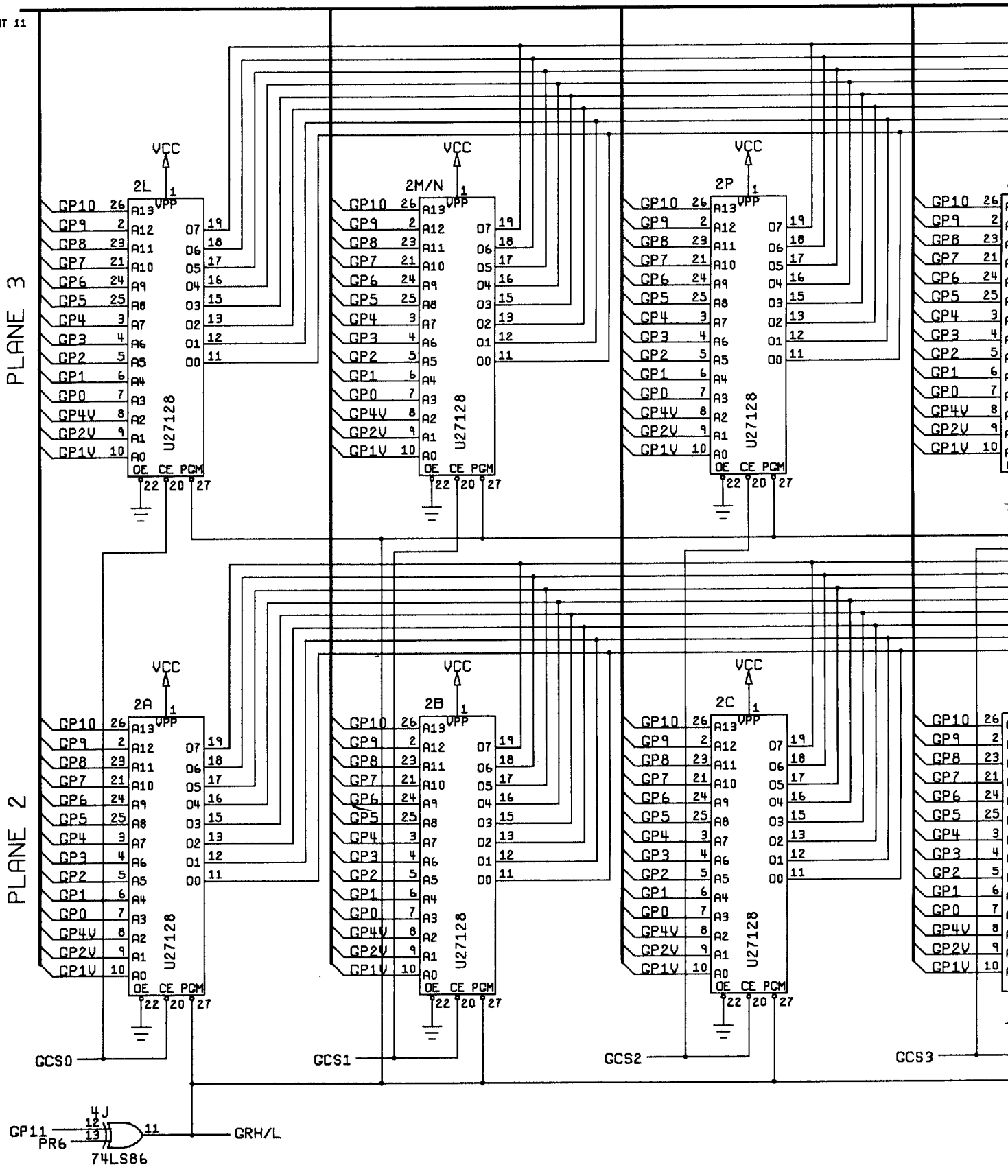
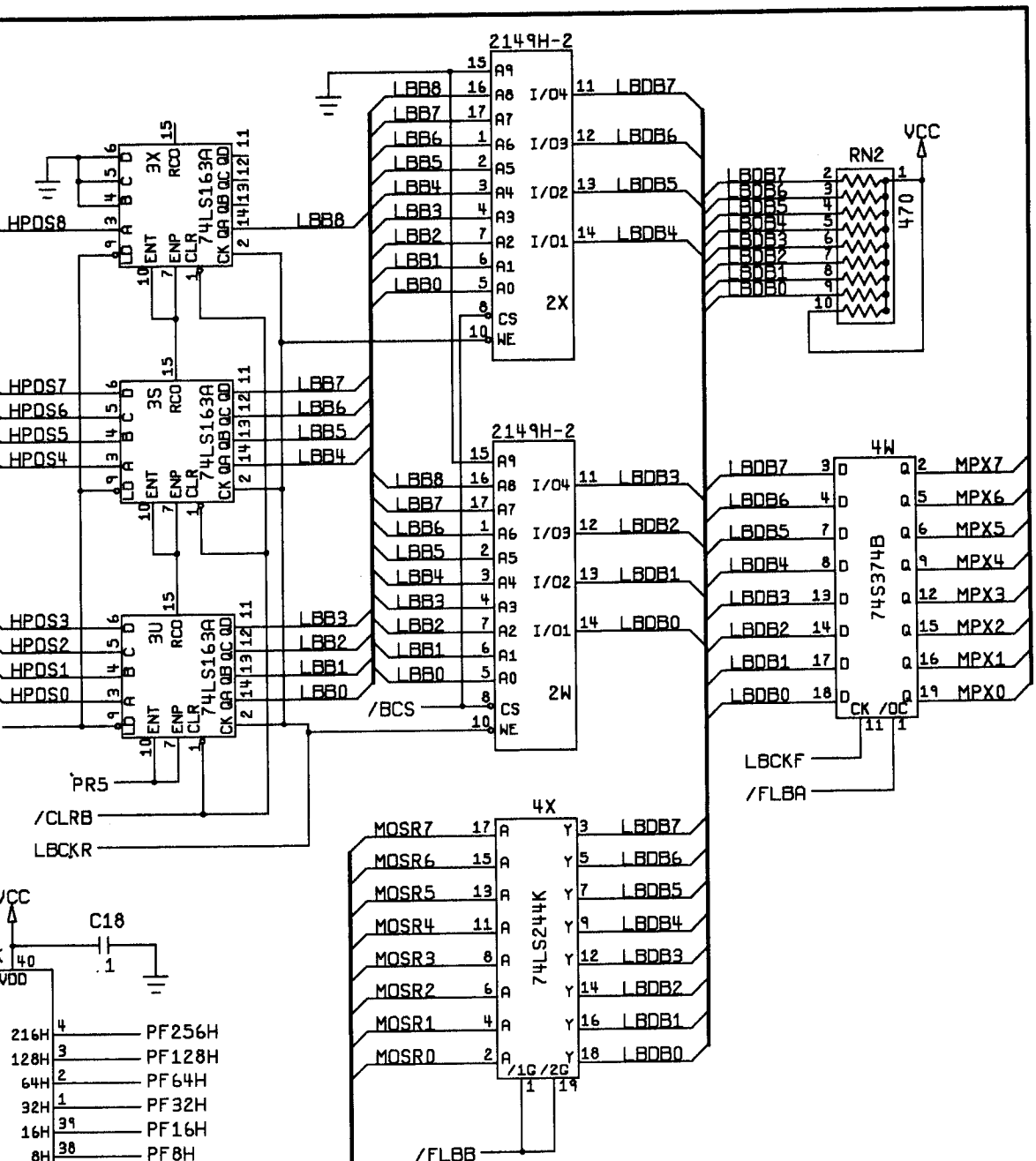

PLANE 3
PLANE 2
2L
2M/N
2P
2A
2B
2C
VCC
VPP
U27128
A13
A12
A11
A10
A9
A8
A7
A6
A5
A4
A3
A2
A1
A0
O7
O6
O5
O4
O3
O2
O1
O0
OE
CE
PGM
GP10
GP9
GP8
GP7
GP6
GP5
GP4
GP3
GP2
GP1
GP0
GP4V
GP2V
GP1V
GCS0
GCS1
GCS2
GCS3
4J
GP11
PR6
74LS86
GRH/L



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Gauntlet™ Game PCB Schematic Diagram

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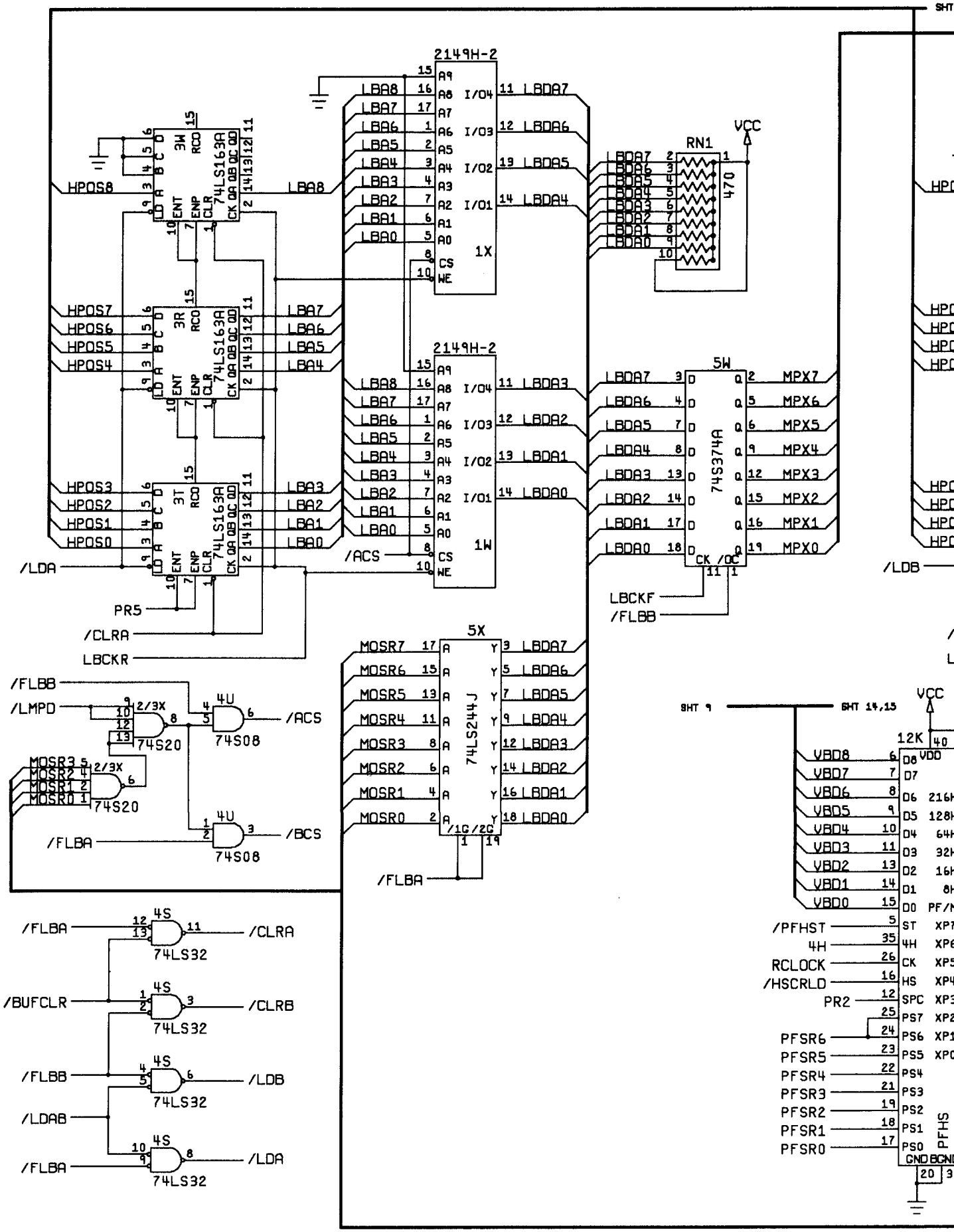
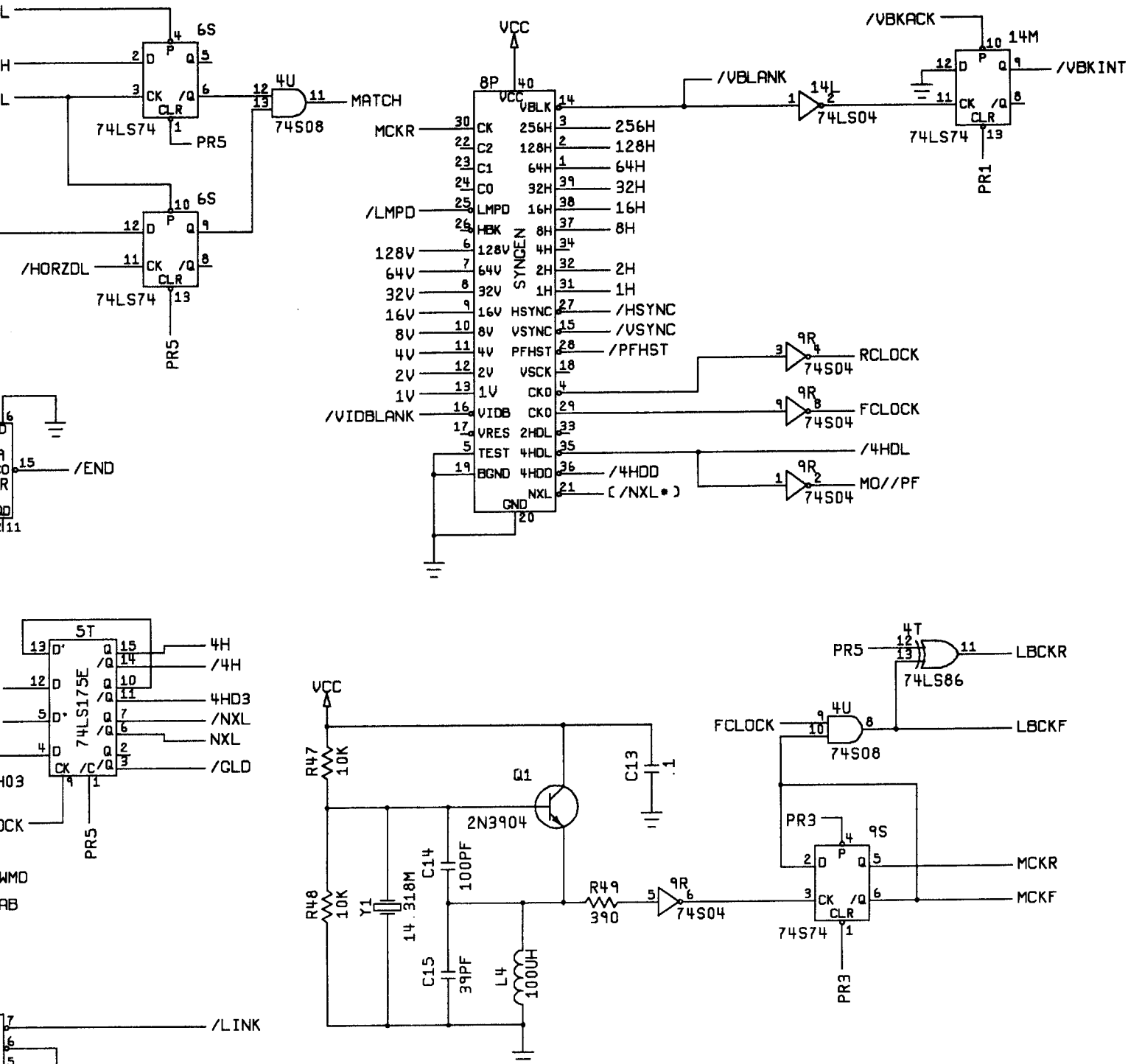

2149H-2
1X
1W
RN1
470
VCC
3W
3R
3T
74LS163A
HPOS8
HPOS7
HPOS6
HPOS5
HPOS4
HPOS3
HPOS2
HPOS1
HPOS0
LBA8
LBA7
LBA6
LBA5
LBA4
LBA3
LBA2
LBA1
LBA0
LBDA7
LBDA6
LBDA5
LBDA4
LBDA3
LBDA2
LBDA1
LBDA0
/LDA
/ACS
PR5
/CLRA
LBCKR
5W
74S374A
MPX7
MPX6
MPX5
MPX4
MPX3
MPX2
MPX1
MPX0
LBCKF
/FLBB
/LDB
5X
74LS244J
MOSR7
MOSR6
MOSR5
MOSR4
MOSR3
MOSR2
MOSR1
MOSR0
/FLBA
/LMPD
74S20
74S08
/BCS
4S
74LS32
/BUFCLR
/CLRB
/LDAB
SHT 9
SHT 14,15
12K
VBD8
VBD7
VBD6
VBD5
VBD4
VBD3
VBD2
VBD1
VBD0
/PFHST
4H
RCLOCK
/HSCRLD
PR2
PFSR6
PFSR5
PFSR4
PFSR3
PFSR2
PFSR1
PFSR0
PFHS



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Gauntlet™ Game PCB Schematic Diagram

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SP-284 Sheet 14
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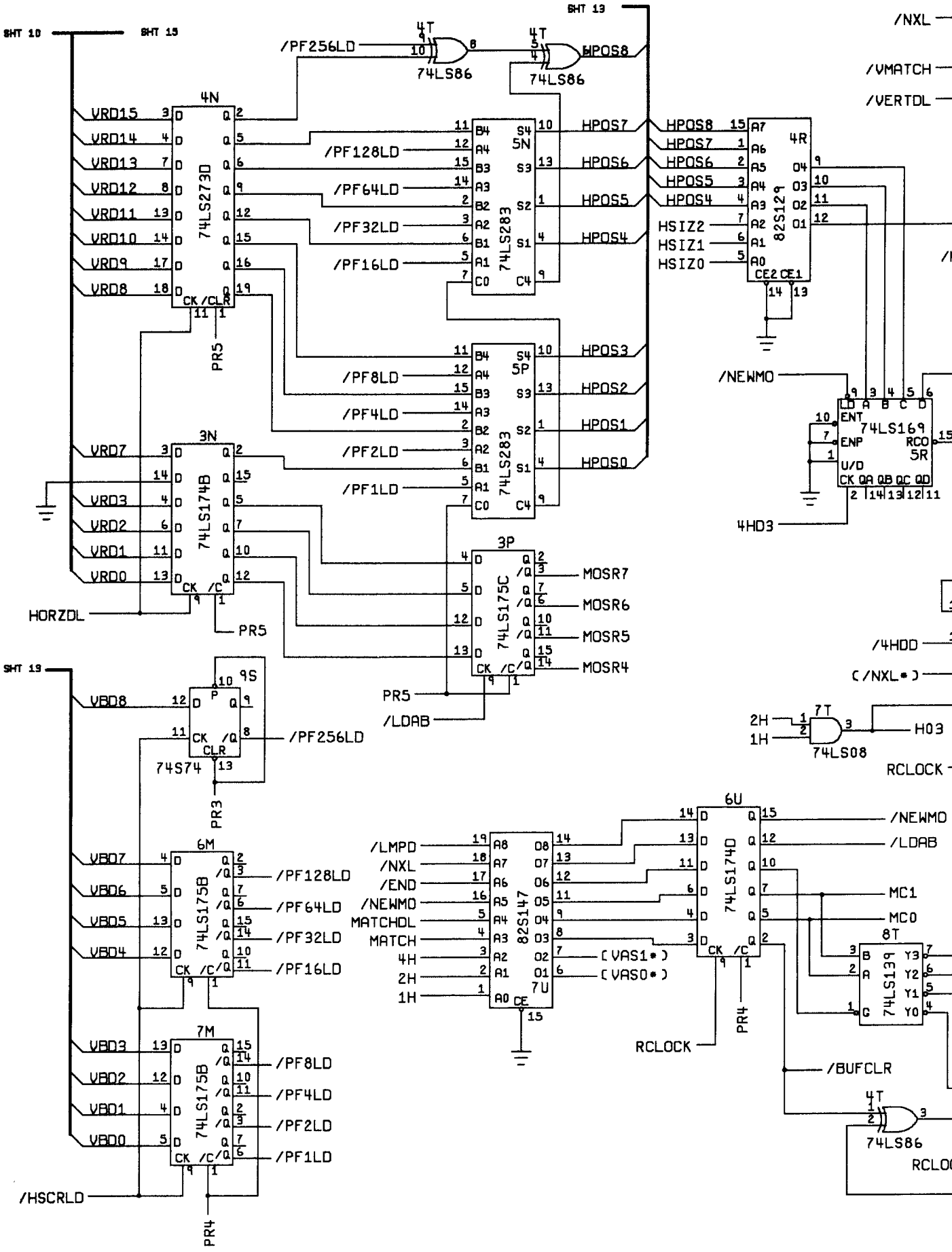
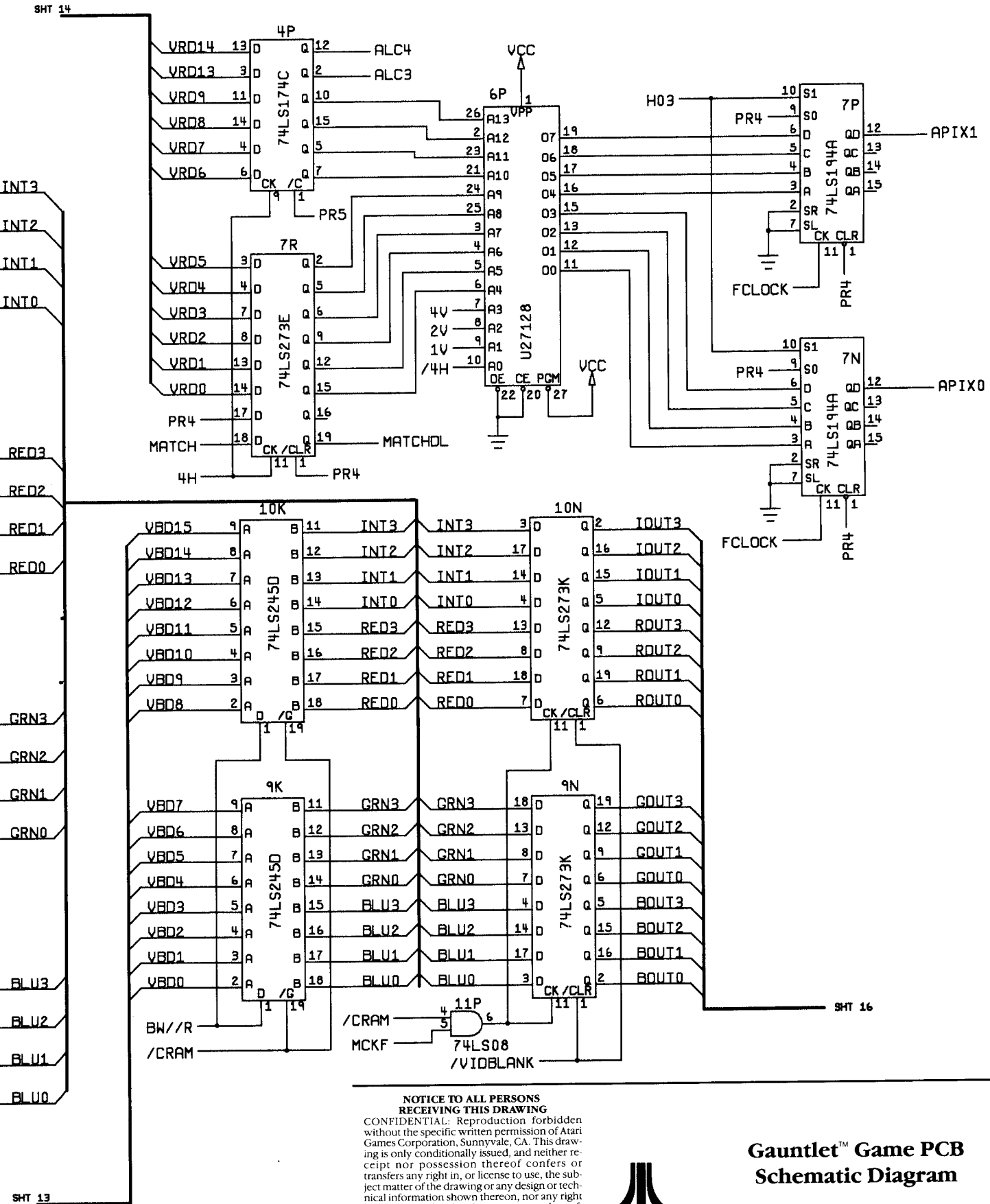

SHT 10
SHT 15
SHT 13
/PF256LD
4T
74LS86
HPOS8
4N
VRD15
VRD14
VRD13
VRD12
VRD11
VRD10
VRD9
VRD8
74LS273D
CK /CLR
PR5
5N
/PF128LD
/PF64LD
/PF32LD
/PF16LD
74LS283
HPOS7
HPOS6
HPOS5
HPOS4
5P
/PF8LD
/PF4LD
/PF2LD
/PF1LD
HPOS3
HPOS2
HPOS1
HPOS0
4R
82S129
HPOS8
HPOS7
HPOS6
HPOS5
HPOS4
HSIZ2
HSIZ1
HSIZ0
/NXL
/VMATCH
/VERTDL
/NEWMO
74LS169
ENT
ENP
U/D
RCO
5R
4HD3
3N
VRD7
VRD3
VRD2
VRD1
VRD0
74LS174B
HORZDL
PR5
3P
74LS175C
MOSR7
MOSR6
MOSR5
MOSR4
/LDAB
/4HDD
(/NXL*)
2H
1H
7T
74LS08
H03
RCLOCK
9S
VBD8
74S74
/PF256LD
PR3
6M
VBD7
VBD6
VBD5
VBD4
74LS175B
/PF128LD
/PF64LD
/PF32LD
/PF16LD
7M
VBD3
VBD2
VBD1
VBD0
/PF8LD
/PF4LD
/PF2LD
/PF1LD
/HSCRLD
PR4
/LMPD
/NXL
/END
/NEWMO
MATCHDL
MATCH
4H
2H
1H
82S147
7U
(VAS1*)
(VAS0*)
6U
74LS174D
/NEWMO
/LDAB
MC1
MC0
8T
74LS139
RCLOCK
PR4
/BUFCLR
74LS86



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Gauntlet™ Game PCB Schematic Diagram

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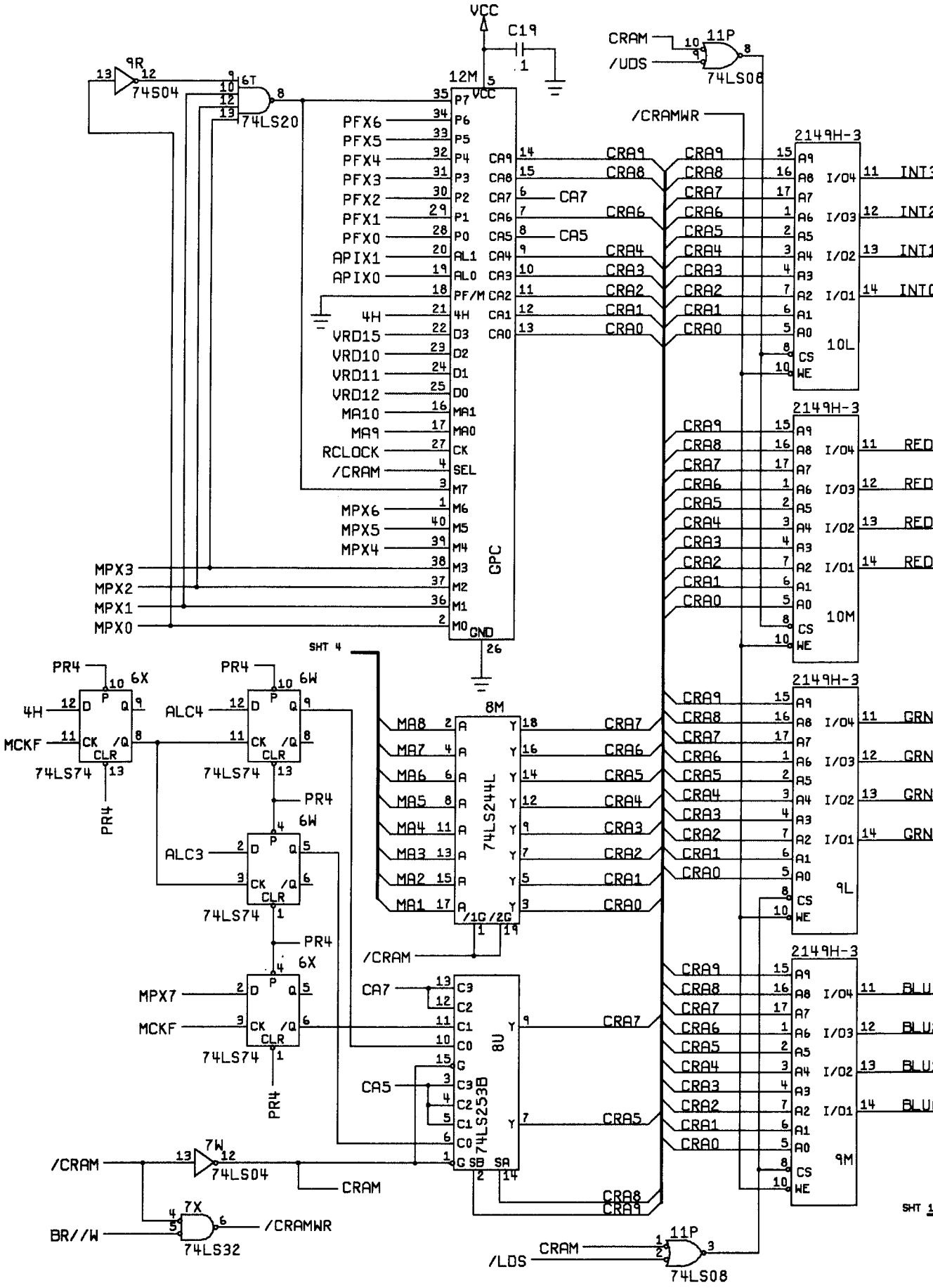
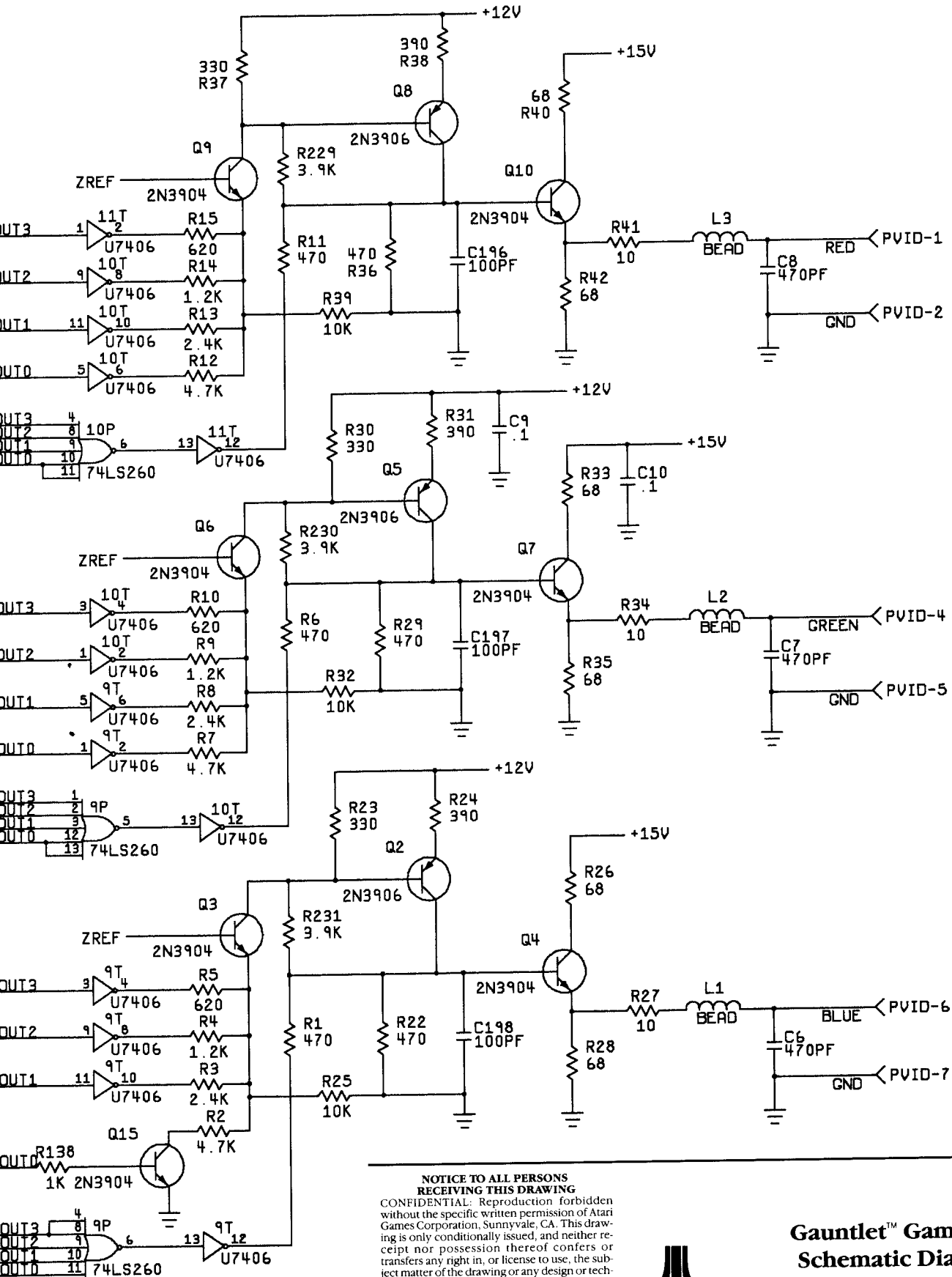


VCC
C19
.1
12M
GPC
9R
74S04
6T
74LS20
PFX6
PFX5
PFX4
PFX3
PFX2
PFX1
PFX0
APIX1
APIX0
4H
VRD15
VRD10
VRD11
VRD12
MA10
MA9
RCLOCK
/CRAM
MPX6
MPX5
MPX4
MPX3
MPX2
MPX1
MPX0
CA7
CA5
CRAM
/UDS
11P
74LS08
/CRAMWR
2149H-3
10L
10M
9L
9M
INT3
INT2
INT1
INT0
RED
GRN
BLU
SHT 4
SHT 1
PR4
6X
6W
74LS74
ALC4
ALC3
MCKF
MPX7
8M
74LS244L
8U
74LS253B
7W
74LS04
7X
74LS32
BR//W
/LDS



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Gauntlet™ Game PCB Schematic Diagram

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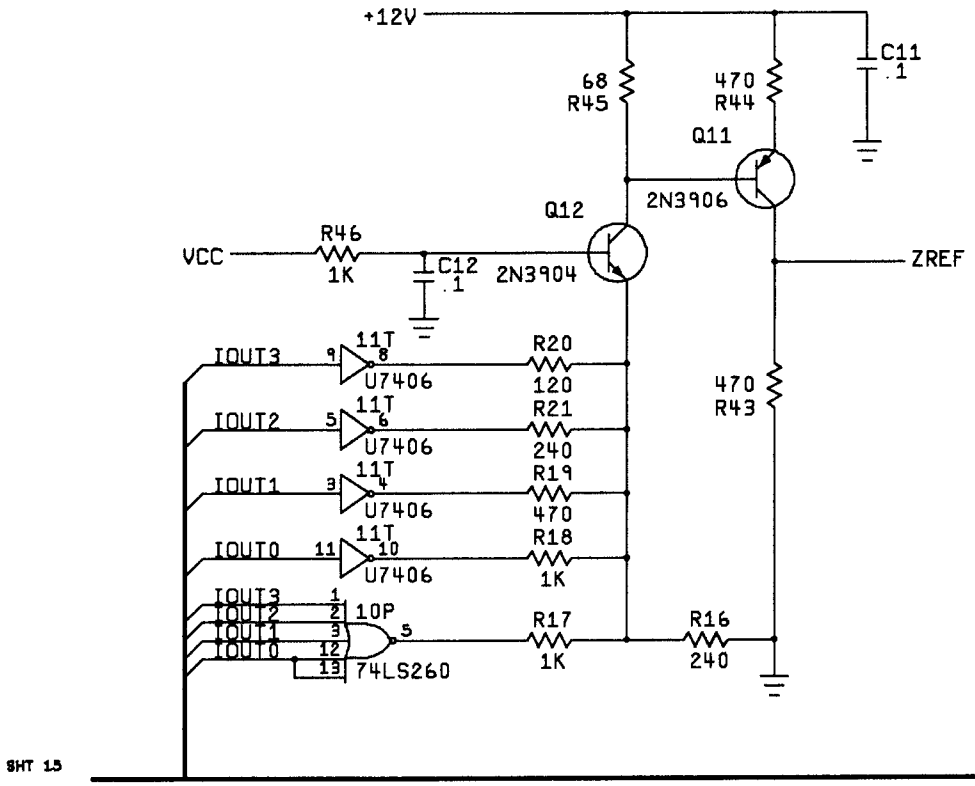
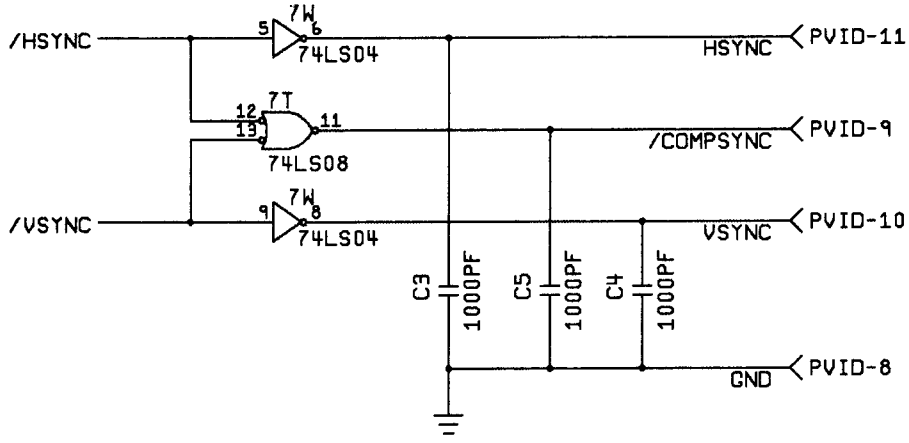
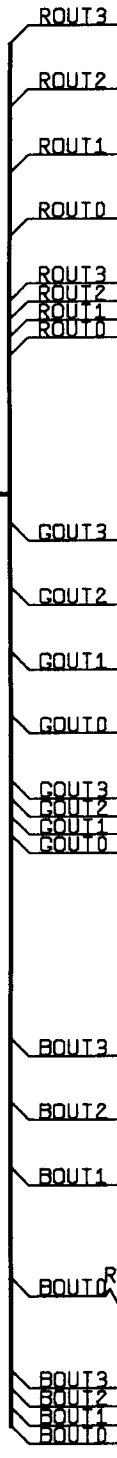
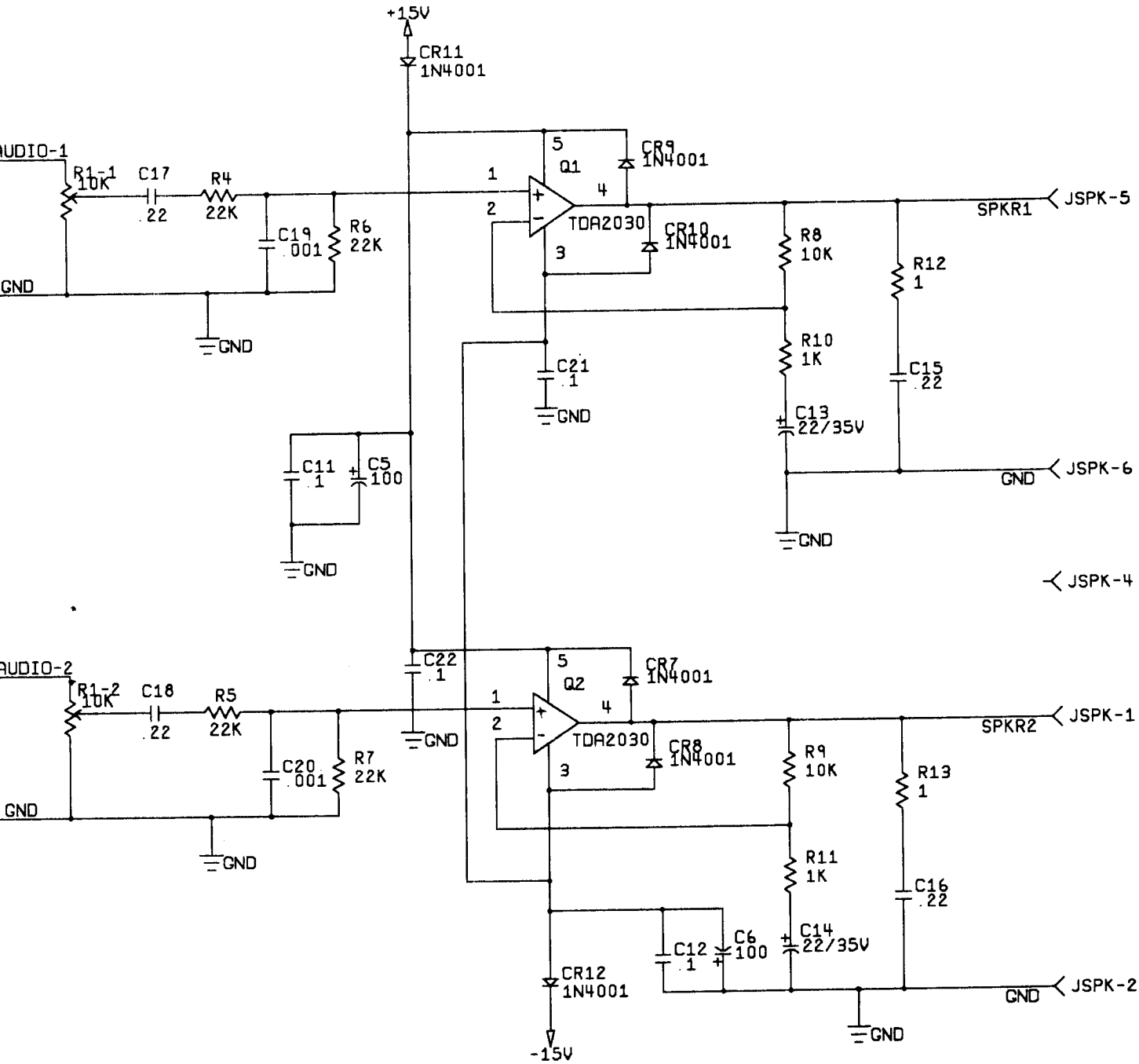

+12V
68
R45
470
R44
C11
.1
Q11
2N3906
Q12
R46
1K
VCC
C12
.1
2N3904
ZREF
IOUT3
IOUT2
IOUT1
IOUT0
11T
U7406
R20
120
R21
240
R19
470
R18
1K
470
R43
10P
74LS260
R17
1K
R16
240
SHT 15


/HSYNC
/VSYNC
7W
74LS04
7T
74LS08
HSYNC
/COMPSYNC
VSYNC
GND
PVID-11
PVID-9
PVID-10
PVID-8
C3
C5
C4
1000PF


ROUT3
ROUT2
ROUT1
ROUT0
GOUT3
GOUT2
GOUT1
GOUT0
BOUT3
BOUT2
BOUT1
BOUT0



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Audio PCB Assembly Schematic Diagram (U.S.)

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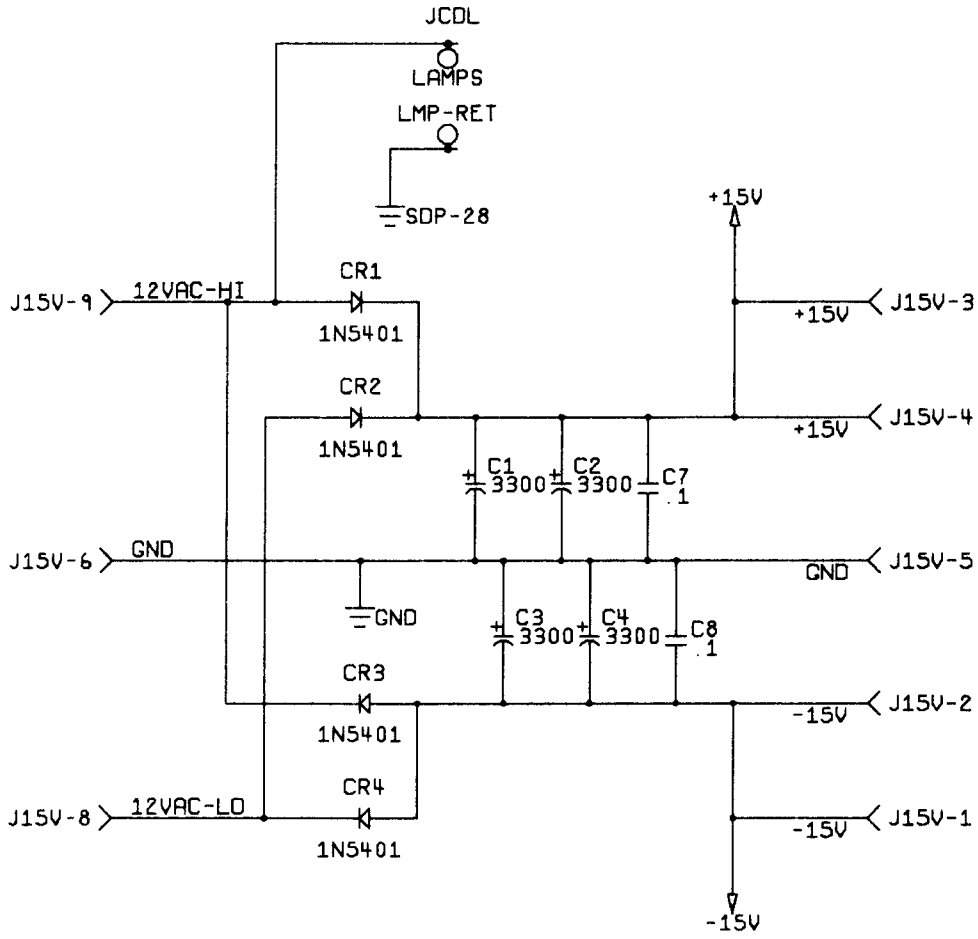
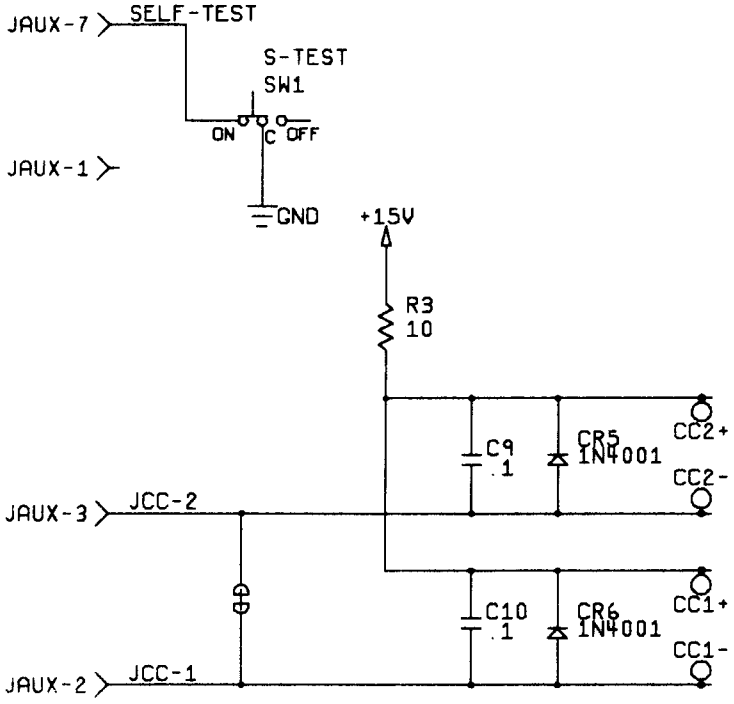
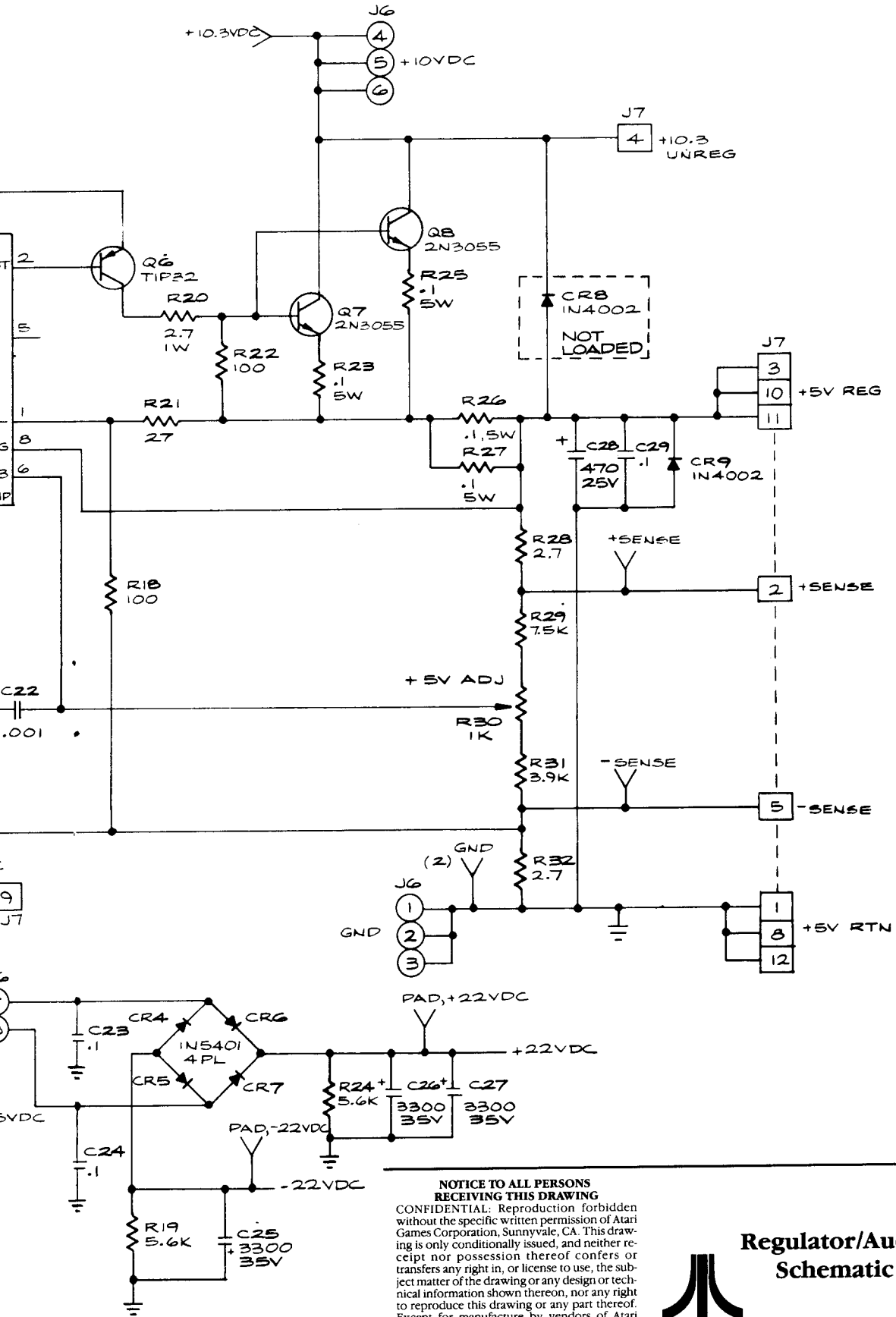

JCDL
LAMPS
LMP-RET
SDP-28
+15V
J15V-9
12VAC-HI
CR1
1N5401
+15V
J15V-3
CR2
1N5401
+15V
J15V-4
C1
3300
C2
3300
C7
.1
J15V-6
GND
GND
J15V-5
GND
C3
3300
C4
3300
C8
.1
CR3
1N5401
-15V
J15V-2
J15V-8
12VAC-LO
CR4
1N5401
-15V
J15V-1
-15V


JAUX-7
SELF-TEST
S-TEST
SW1
ON
C
OFF
JAUX-1
GND
+15V
R3
10
C9
.1
CR5
1N4001
CC2+
CC2-
JAUX-3
JCC-2
C10
.1
CR6
1N4001
CC1+
CC1-
JAUX-2
JCC-1



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Regulator/Audio III PCB Assembly Schematic Diagram (Ireland)

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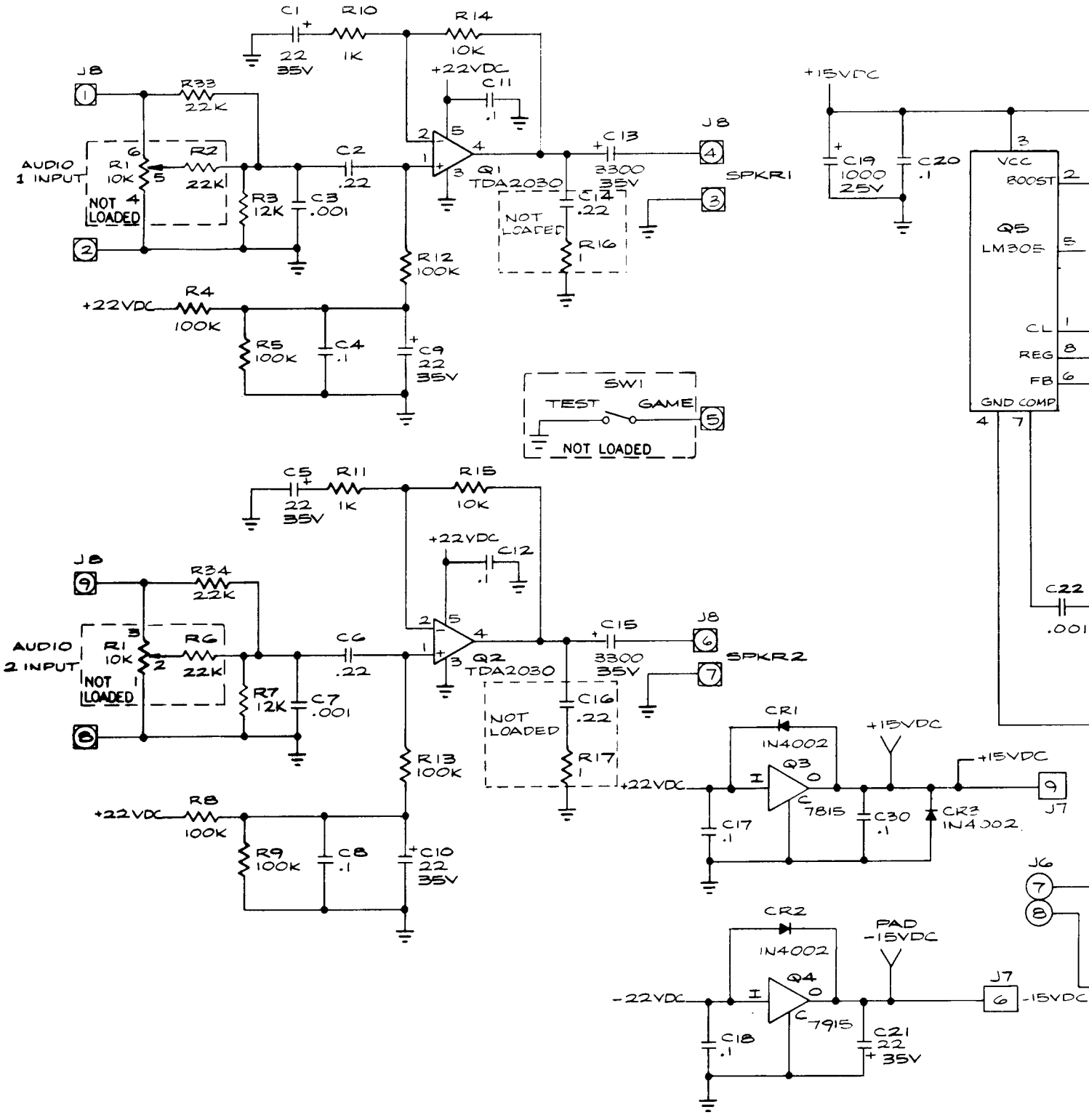
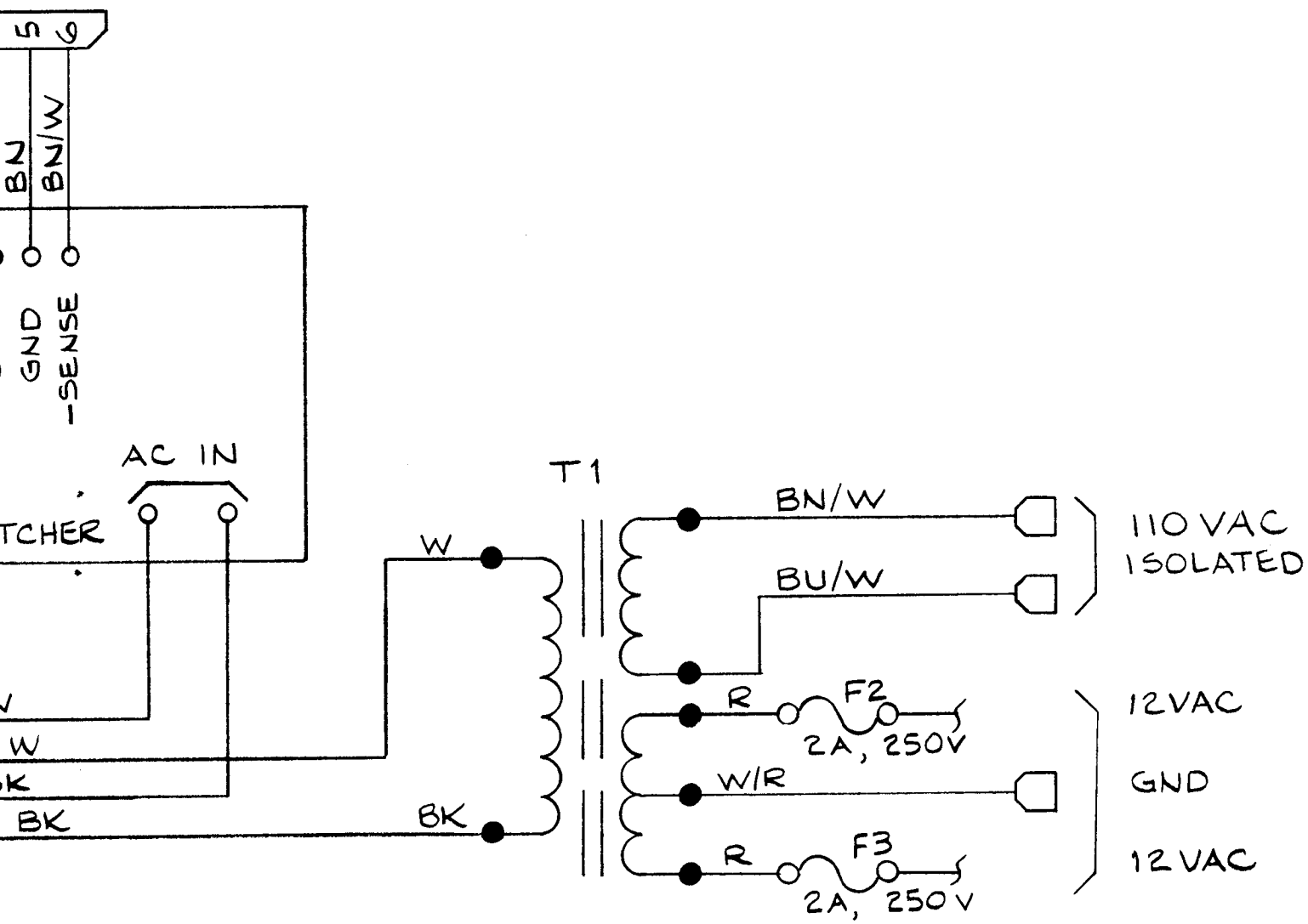

C1
22
35V
R10
1K
R14
10K
+22VDC
C11
.1
J8
R33
22K
AUDIO
1 INPUT
R1
10K
R2
22K
NOT
LOADED
C2
.22
R3
12K
C3
.001
Q1
TDA2030
C13
3300
35V
J8
SPKR1
C14
.22
NOT
LOADED
R16
R12
100K
R4
100K
+22VDC
R5
100K
C4
.1
C9
22
35V
SW1
TEST
GAME
NOT LOADED
+15VDC
C19
1000
25V
C20
.1
VCC
BOOST
Q5
LM305
CL
REG
FB
GND COMP
C22
.001
C5
22
35V
R11
1K
R15
10K
+22VDC
C12
.1
J8
R34
22K
AUDIO
2 INPUT
R1
10K
R6
22K
NOT
LOADED
C6
.22
R7
12K
C7
.001
Q2
TDA2030
C15
3300
35V
J8
SPKR2
C16
.22
NOT
LOADED
R17
R13
100K
R8
100K
+22VDC
R9
100K
C8
.1
C10
22
35V
CR1
IN4002
Q3
7815
+15VDC
+22VDC
C17
.1
C30
.1
CR3
IN4002
J7
J6
CR2
IN4002
Q4
7915
PAD
-15VDC
-22VDC
C18
.1
C21
22
35V
J7
-15VDC



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ATARI GAMES

Switching/Linear (SL) Power Supply Wiring Diagram (U.S.)

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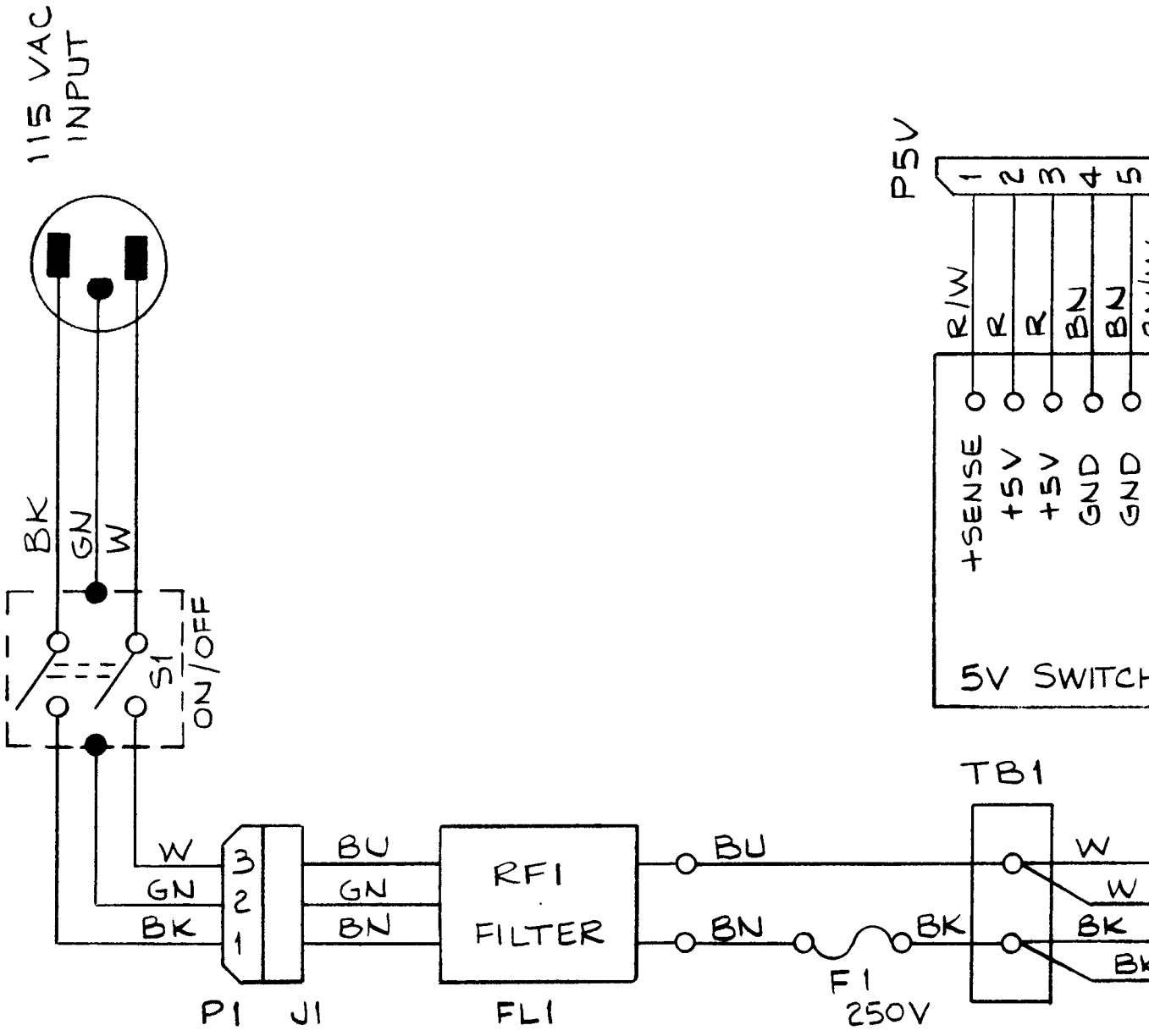
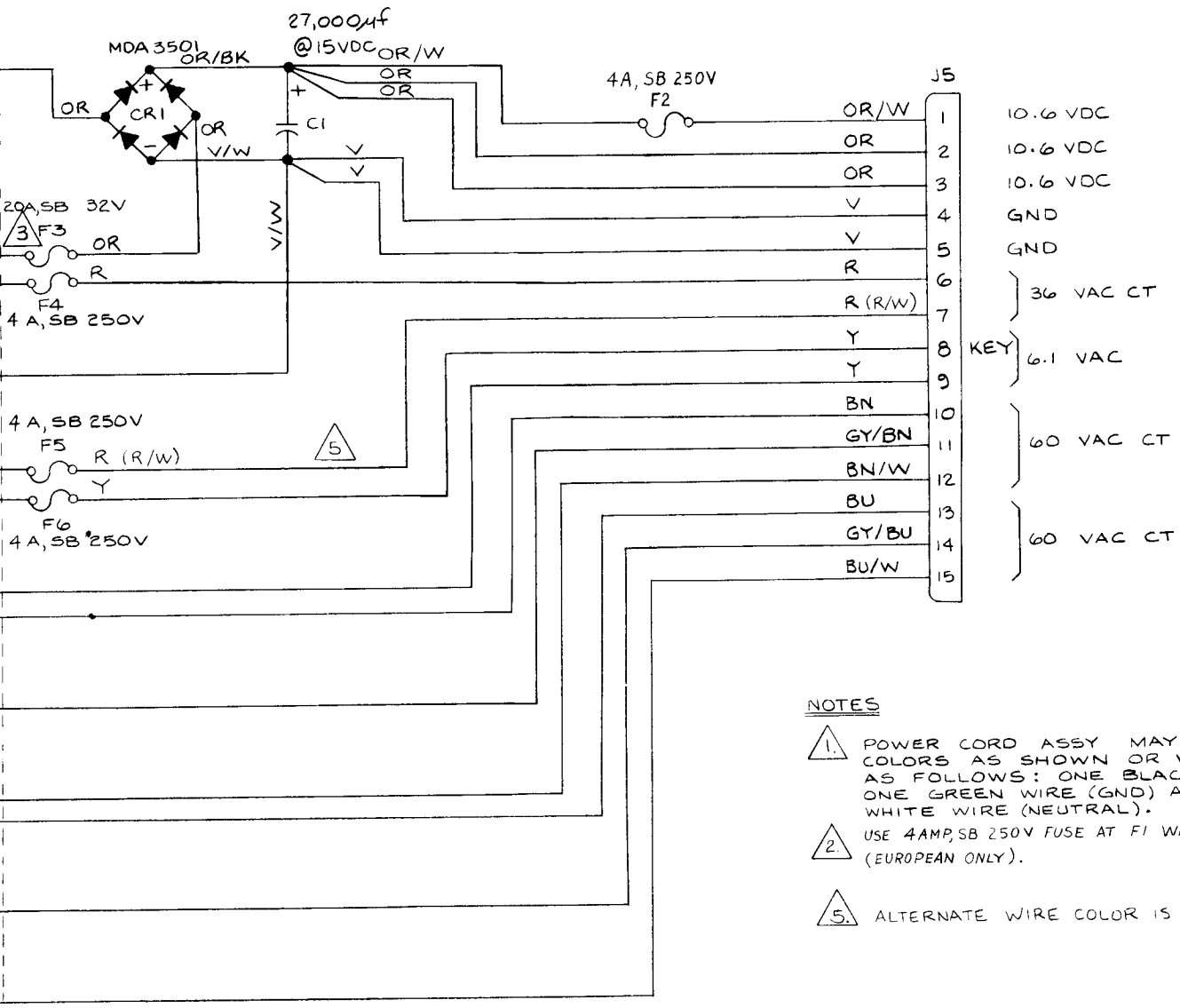

115 VAC
INPUT
BK
GN
W
S1
ON/OFF
P5V
1
2
3
4
5
R/W
R
R
BN
BN
+SENSE
+5V
+5V
GND
GND
5V SWITCH
TB1
W
GN
BK
3
2
1
P1
J1
BU
GN
BN
RFI
FILTER
FL1
BU
BN
BK
F1
250V
W
W
BK
BK



NOTES

1. POWER CORD ASSY MAY HAVE WIRE COLORS AS SHOWN OR WIRE COLORS AS FOLLOWS: ONE BLACK WIRE (AC), ONE GREEN WIRE (GND) AND ONE WHITE WIRE (NEUTRAL).
2. USE 4AMP, SB 250V FUSE AT F1 WITH 220V & 240V (EUROPEAN ONLY).
5. ALTERNATE WIRE COLOR IS IN PARENTHESES ( ).

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ATARI GAMES

Linear Power Supply Wiring Diagram (Ireland)

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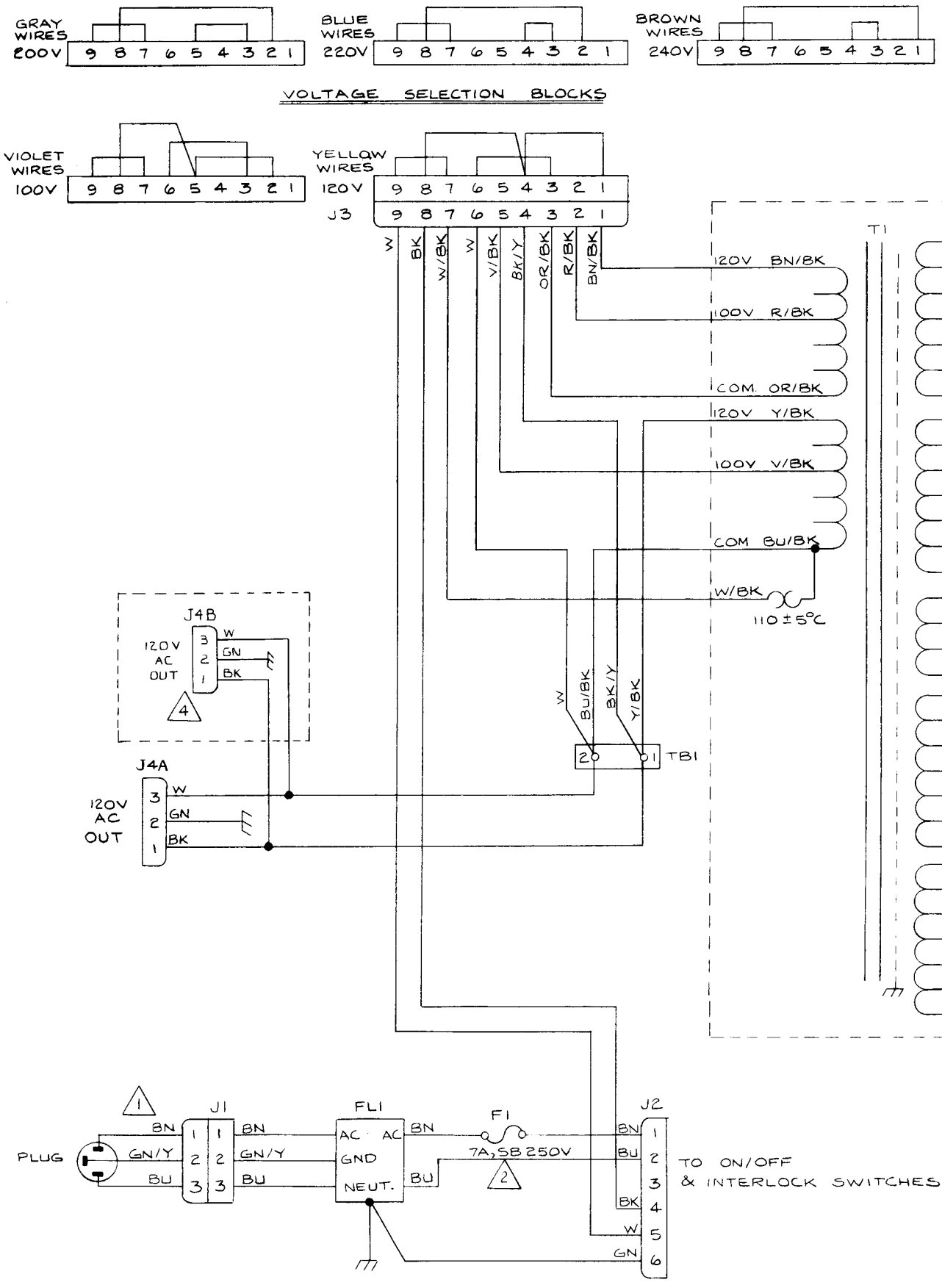
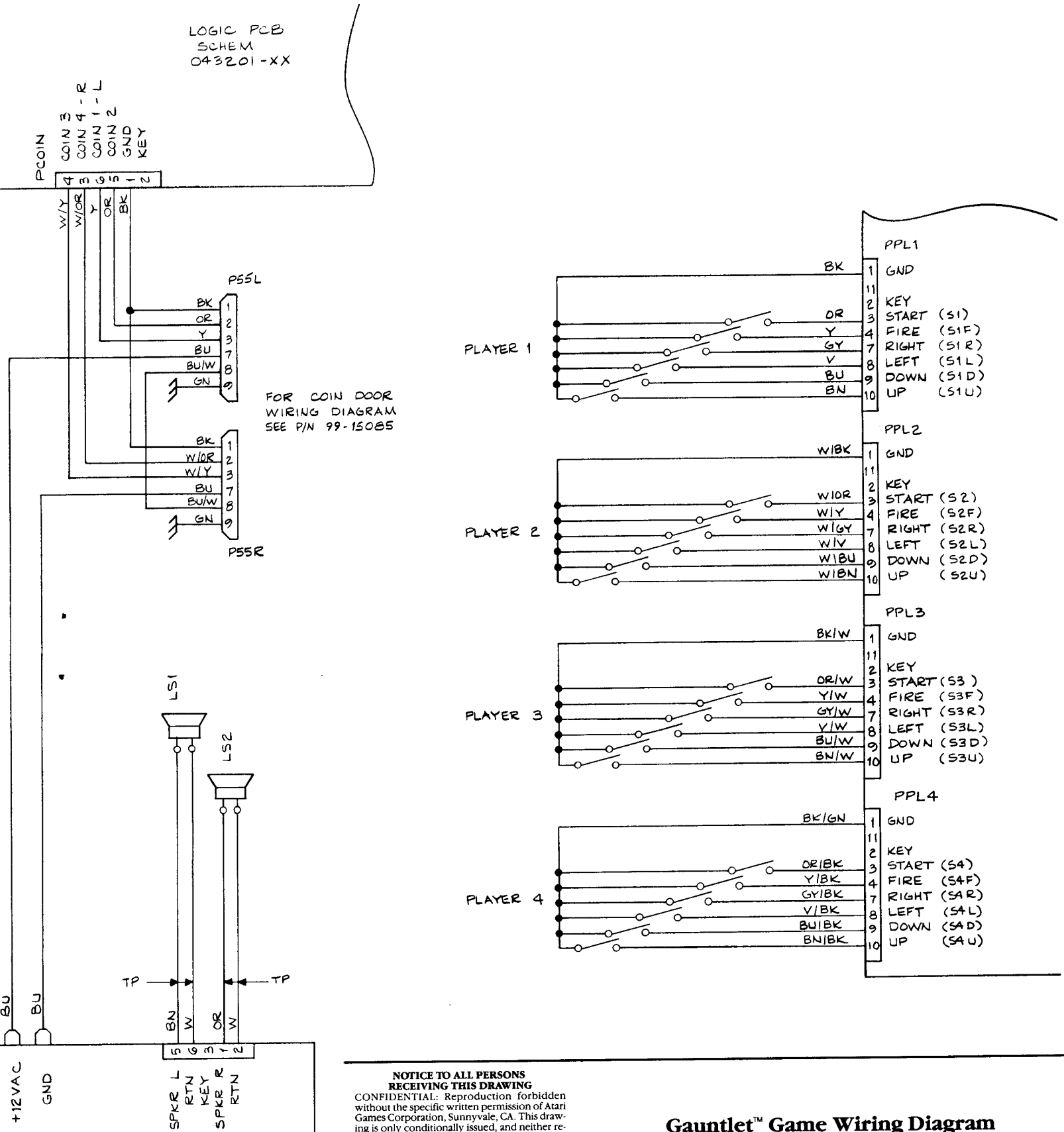
SP-284 Sheet 20
1st printing


GRAY WIRES
200V
9 8 7 6 5 4 3 2 1
BLUE WIRES
220V
9 8 7 6 5 4 3 2 1
BROWN WIRES
240V
9 8 7 6 5 4 3 2 1
VOLTAGE SELECTION BLOCKS
VIOLET WIRES
100V
9 8 7 6 5 4 3 2 1
YELLOW WIRES
120V
9 8 7 6 5 4 3 2 1
J3
9 8 7 6 5 4 3 2 1
W
BK
W/BK
W
Y/BK
BK/Y
OR/BK
R/BK
BN/BK
T1
120V BN/BK
100V R/BK
COM. OR/BK
120V Y/BK
100V V/BK
COM BU/BK
W/BK
110±5°C
OR
OR
R
V/W
R
Y
Y
BN
GY/BN
BN/W
BU
GY/BU
BU/W
J4B
120V AC OUT
3 W
2 GN
1 BK
4
J4A
120V AC OUT
3 W
2 GN
1 BK
W
BU/BK
BK/Y
Y/BK
2
1
TB1
1
PLUG
BN
GN/Y
BU
J1
FL1
AC
GND
NEUT.
F1
7A, SB 250V
2
J2
TO ON/OFF & INTERLOCK SWITCHES



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Gauntlet™ Game Wiring Diagram

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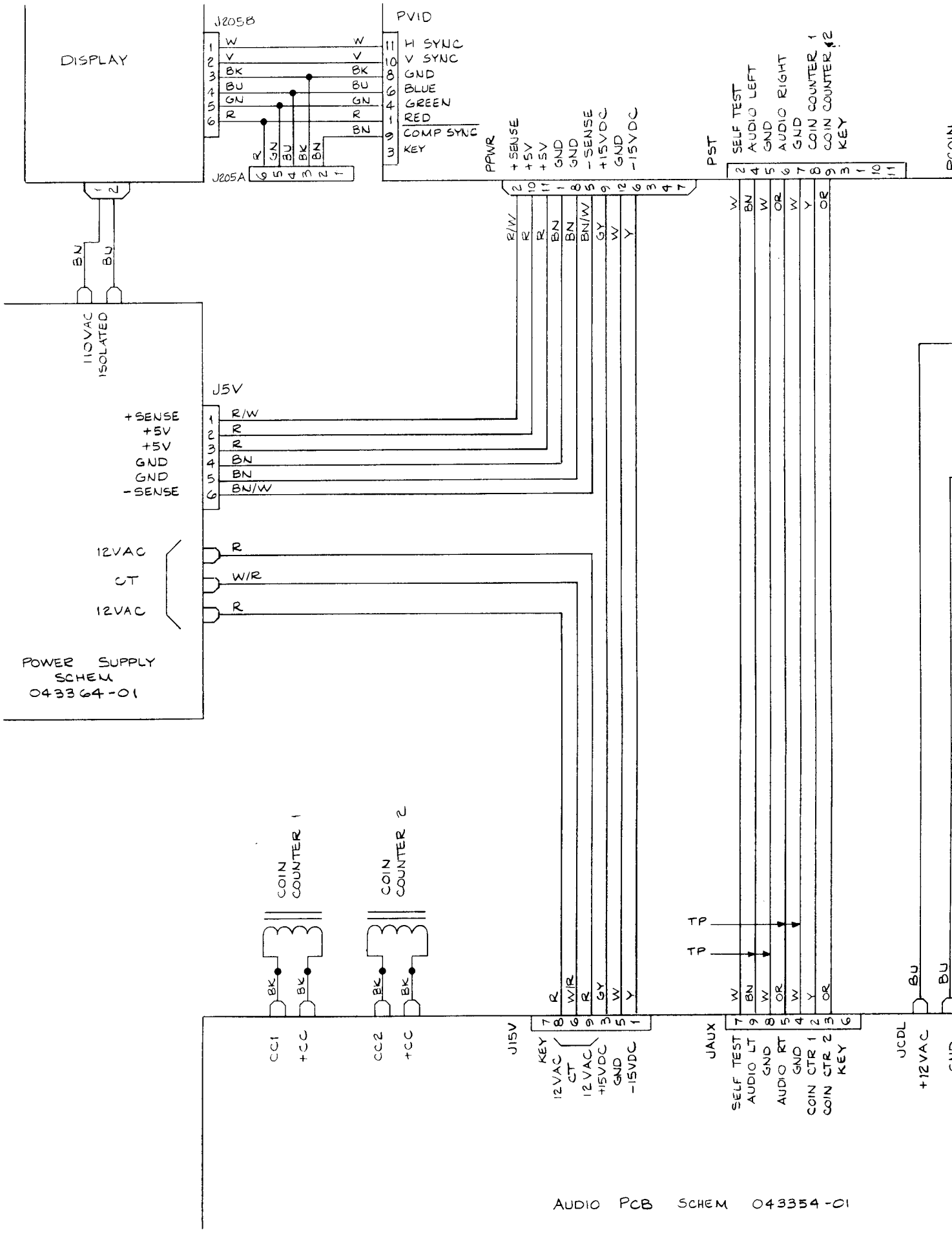
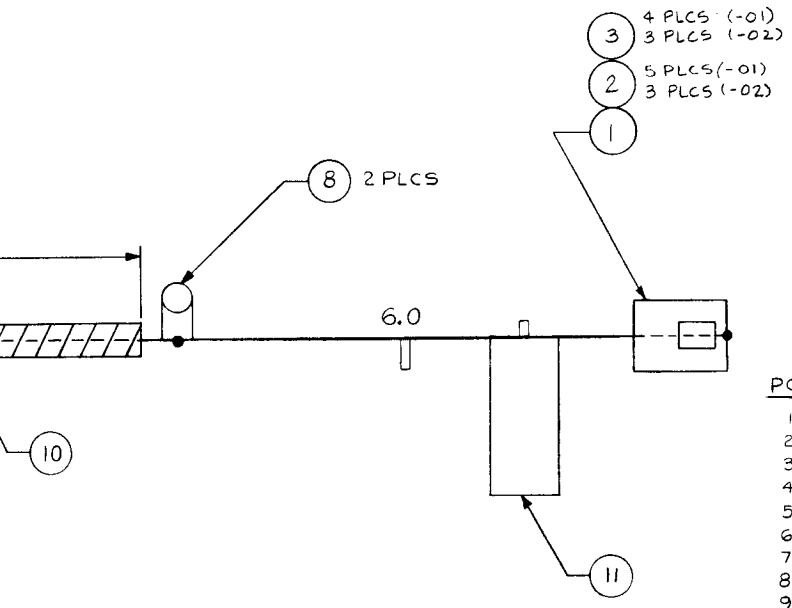
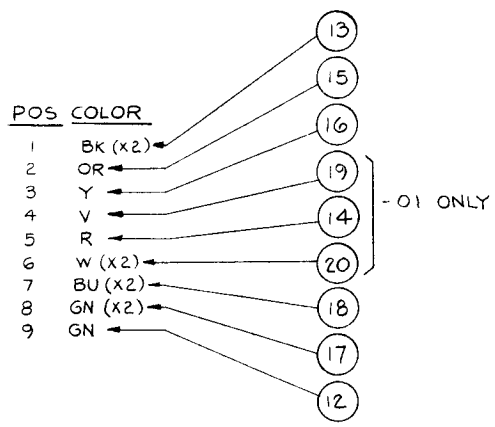
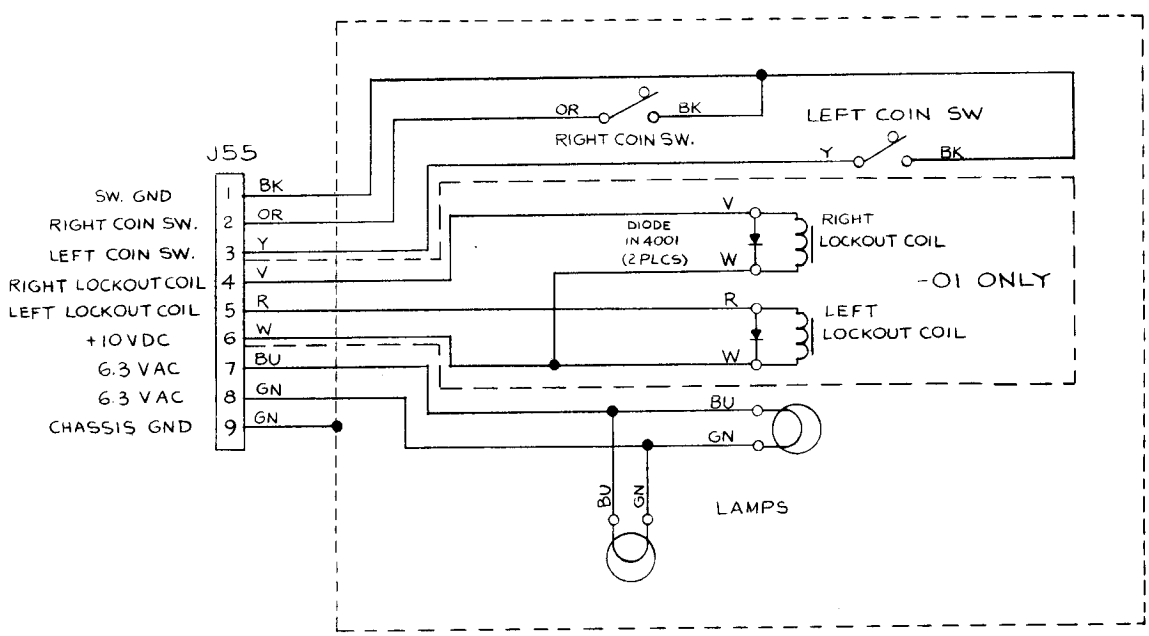
SP-284 Sheet 21
1st printing



AUDIO PCB SCHEM 043354-01







COIN DOOR WIRING DIAGRAM

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Coin Door Wiring Diagram

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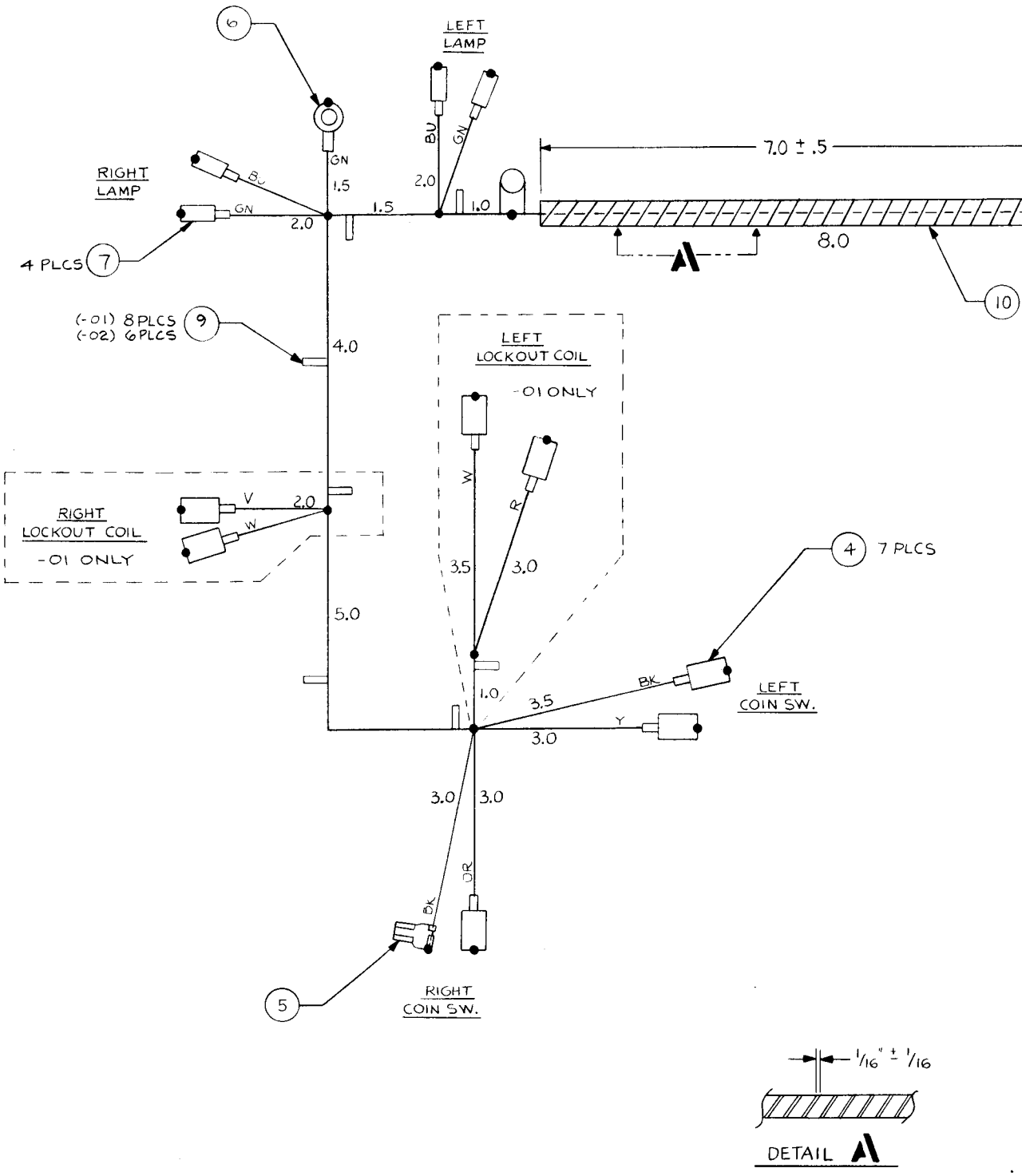
6
LEFT LAMP
BU
GN
7.0 ± .5
RIGHT LAMP
BU
GN
GN
1.5
2.0
1.5
2.0
1.0
8.0
4 PLCS 7
10
(-01) 8 PLCS
(-02) 6 PLCS
9
4.0
LEFT LOCKOUT COIL
-01 ONLY
W
R
RIGHT LOCKOUT COIL
-01 ONLY
V
2.0
W
3.5
3.0
4
7 PLCS
5.0
1.0
3.5
BK
LEFT COIN SW.
Y
3.0
3.0
3.0
OR
BK
5
RIGHT COIN SW.
1/16" ± 1/16
DETAIL A

Gauntlet™ 6502 Memory Map

FUNCTION	ADDRESS	R/W	DATA
Program RAM	0000–0FFF	R/W	D0–D7
Write 68010 Port (Output Buffer)	1000	W	D0–D7
Read 68010 Port (Input Buffer)	1010	R	D0–D7
Audio Mix:			
Speech Mix	1020	W	D5–D7
Effects Mix	1020	W	D3, D4
Music Mix	1020	W	D0–D2
Coin 1 (Left)	1020	R	D3
Coin 2	1020	R	D2
Coin 3	1020	R	D1
Coin 4 (Right)	1020	R	D0
Data Available (@ 1010) (Active High)	1030	R	D7
Output Buffer Full (@ 1000) (Active High)	1030	R	D6
Speech Ready (Active Low)	1030	R	D5
Self-Test (Active Low)	1030	R	D4
Music Reset (Low Reset)	1030	W	D7
Speech Write (Active Low)	1031	W	D7
Speech Reset (Active Low)	1032	W	D7
Speech Squeak (Low = 650KHz Clock)	1033	W	D7
Coin Counter Right (Active High)	1034	W	D7
Coin Counter Left (Active High)	1035	W	D7
Effects	1800–180F	R/W	D0–D7
Music	1810–1811	R/W	D0–D7
Speech	1820	W	D0–D7
Interrupt Acknowledge	1830	R/W	xx
Program ROM (48k bytes)	4000–FFFF	R	D0–D7

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ATARI GAMES

Gauntlet™ 68010 and 6502 Microprocessor Memory Maps

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Gauntlet™ 68010 Memory Map

FUNCTION	ADDRESS	R/W	DATA
Program ROM/Operating System	000000–00FFFF	R	D0–D15
Program ROM/SLAPSTIC	038000–03FFFF	R	D0–D15
Program ROM/Main	040000–07FFFF	R	D0–D15
Spare RAM	800000–801FFF	R/W	D0–D15
EEPROM	802001–802FFF	R/W	D7–D0
Player 1 Input (see detail below)	803001	R	D0–D71
Player 2 Input	803003	R	D0–D7
Player 3 Input	803005	R	D0–D7
Player 4 Input	803007	R	D0–D7
Player Inputs:			
Joystick Up			D7
Joystick Down			D6
Joystick Left			D5
Joystick Right			D4
Spare			D3
Spare			D2
Fire			D1
Magic/Start			D0
VBLANK (Active Low)	803009	R	D6
Output/Buffer Full (@ 803170) (Active High)	803009	R	D5
Input/Buffer Full (@ 80300F) (Active High)	803009	R	D4
Self-Test (Active Low)	803009	R	D3
Read Sound Processor (6502)	80300F	R	D0–D7
Watchdog (128 msec. timeout)	803100	W	xx
LED-1 (Low On)	803121	W	D0
LED-2 (Low On)	803123	W	D0
LED-3 (Low On)	803125	W	D0
LED-4 (Low On)	803127	W	D0
Sound Processor Reset (Low Reset)	80312F	W	D0
VBlank Acknowledge	803140	W	xx
Unlock EEPROM	803150	W	xx
Write Sound Processor (6502)	803171	W	D0–D7
Playfield RAM	900000–901FFF	R/W	D0–D15
Motion Object Picture	902000–9027FF	R/W	D0–D15
Motion Object Horizontal Position	902800–902FFF	R/W	D0–D15
Motion Object Vertical Position	903000–9037FF	R/W	D0–D15
Motion Object Link	903800–903FFF	R/W	D0–D15
Spare RAM	904000–904FFF	R/W	D0–D15
Alphanumerics RAM	905000–905FFF	R/W	D0–D15
Playfield Vertical Scroll	905F6E, 905F6F	R/W	D7–D15
Playfield ROM Bank Select	905F6F	R/W	D0, D1
Color RAM Alpha	910000–9101FF	R/W	D0–D15
Color RAM Motion Object	910200–9103FF	R/W	D0–D15
Color RAM Playfield Shadow	910400–9104FF	R/W	D0–D15
Color RAM Playfield	910500–9105FF	R/W	D0–D15
Color RAM (Spare)	910600–9107FF	R/W	D0–D15
Playfield Horizontal Scroll	930000, 930001	W	D0–D8

NOTE

All addresses can be accessed in byte or word mode.

Gauntlet Signal Name Glossary, continued

HSIZ0–HSIZ2	Motion object horizontal size
HSYNC, $\overline{\text{HSYNC}}$	Horizontal sync output
$\overline{\text{INPUT}}$	68010 miscellaneous inputs buffer select
INT0–INT3	Color intensity RAM data
IOUT0–IOUT3	Intensity latched digital video output
$\overline{\text{LATCH}}$	68010 miscellaneous latched outputs chip select
LAUD	Summed left channel audio
LBA0–LBA8	Line buffer "A" address bus
LBB0–LBB8	Line buffer "B" address bus
LBCKF	Line buffer clock inverted phase
LBCKR	Line buffer clock
LBDA0–LBDA7	Line buffer "A" data bus
LBDB0–LBDB7	Line buffer "B" data bus
$\overline{\text{LDA}}$	Load line buffer "A" address counters
$\overline{\text{LDAB}}$	Load line buffer "A" or "B" address counters
$\overline{\text{LDB}}$	Load line buffer "B" address counters
$\overline{\text{LDS}}$	68010 lower data strobe
LED1–LED4	LED outputs, players 1–4
LEFT-1–LEFT-4	Joystick left switch inputs, players 1–4
$\overline{\text{LINK}}$	Latch motion object link data
$\overline{\text{LMPD}}$	Stop motion object processing for line buffer changeover
LNK0–LNK9	Motion object link data
MA1–MA14	68010 address bus buffered
MATCH	Motion object H and V data matches current playfield position
MATCHDL	Previous MATCH state
MBUS	68010 "M" data bus buffers enable
MC0, MC1	Motion object parameter control select
$\overline{\text{MCEN}}$	Motion object parameter control enable
MCKF	Master clock, inverted phase
MCKR	Master clock
MD0–MD15	68010 "M" data bus
MFLP	Motion object horizontal flip parameter
$\overline{\text{MIX}}$	Latch audio mix data
MO/$\overline{\text{PF}}$	Motion object or playfield picture select
$\overline{\text{MOHI}}$, $\overline{\text{MOLO}}$	Motion object RAM chip selects
MOSR0–MOSR3	Motion object pixel data, before the line buffers
MOSR4–MOSR7	Motion object pixel palette data, before the line buffers
MPIC0–MPIC7	The lower 8 bits of the motion object picture address
MPX0–MPX7	Motion object pixel data, after the line buffers
MREFL	Motion object stamp horizontal flip state
MUSIC	Music chip select
$\overline{\text{NEWMO}}$	Start a new motion object
NXL, $\overline{\text{NXL}}$	Next line
($\overline{\text{NXL}}$*)	NXL one clock cycle early
NXLDL	NXL delayed one clock cycle
$\overline{\text{PF1LD}}$–$\overline{\text{PF256LD}}$	Latched playfield horizontal scroll data
PF1V–PF256V	Playfield vertical address counter chain
PF8H–PF256H	Playfield horizontal address counter chain
PFBANK0, PFBANK1	Playfield picture bank select
$\overline{\text{PFHI}}$, $\overline{\text{PFLO}}$	Playfield RAM chip selects
$\overline{\text{PFHST}}$	Playfield scroll control
PFSR0–PFSR3	Playfield pixel data, before PFHS
PFSR4–PFSR6	Playfield pixel palette data, before PFHS
PFX0–PFX6	Playfield pixel data after PFHS
PICST0–PICST7	Motion object picture start address
$\overline{\text{PICT}}$	Latch motion object picture data
PICTDL	PICT delayed one clock cycle
PKAUD	Effects chip audio
$\overline{\text{PL1}}$–$\overline{\text{PL4}}$	Player input chip selects, players 1–4
PM0–PM2	Effects audio mix control bits
POKEY	Effects chip select
PR1–PR6	Pull-up resistors
R/$\overline{\text{W}}$	68010 read/write control, unbuffered

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ATARI GAMES

Gauntlet™ Signal Name Glossary

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Gauntlet Signal Name Glossary

2.5V	2.5 volts audio amplifier reference
+5AUD	5 volts audio amplifier reference
10.3V	Power-on-reset control voltage
+12V	+12 volts regulated
+15V	+15 volts unregulated
-15V	-15 volts unregulated
-5V	-5 volts regulated
1H–256H	Screen horizontal address counter chain
1V–128V	Screen vertical address counter chain
$\overline{4H}$	Inverted 4H signal
4HD3, $\overline{4HD3}$	4H signal delayed three clock cycles
$\overline{4HDD}$	4H signal delayed two clock cycles
$\overline{4HDL}$	4H signal delayed one clock cycle
68KBUF	68010 output buffer full (to 6502)
A1–A23	68010 address bus unbuffered
$\overline{ACS}$	"A" line buffer RAMs chip select
ALC3, ALC4	Alphanumerics palette data bits 3 and 4
$\overline{ALHI}$, $\overline{ALLO}$	Alphanumerics RAM chip selects
APIX0, APIX1	Alphanumerics pixel data
$\overline{AS}$	68010 address strobe
AUDIO-L, AUDIO-R	Left and right audio outputs (5V peak-to-peak)
B02	6502 buffered phase 2 (Φ2)
BAS	Buffered address strobe (see $\overline{AS}$)
$\overline{BCS}$	"B" line buffer RAMs chip select
BLU0–BLU3	Blue color RAM data
BLUE	Blue analog video output
BOUT0–BOUT3	Blue latched digital video output
BR/$\overline{W}$	68010 read/write control, buffered
$\overline{BUFCLR}$	Swap "A" and "B" line buffers, clear line buffer counter chain
BW/$\overline{R}$	68010 read/write inverted, buffered
CA5, CA7	Color RAM address bits 5 and 7
CCTR1, CCTR2	Coin counter outputs 1 and 2
$\overline{CLRA}$	Clear line buffer "A" address counters
$\overline{CLRB}$	Clear line buffer "B" address counters
$\overline{COIN}$	Coin input buffer chip select
COIN1-L, COIN2, COIN3, COIN4-R	Four coin switch inputs
$\overline{COMPSYNC}$	Negative composite sync output
CRA0–CRA9	Color RAM address
$\overline{CRAM}$, CRAM	68010 address decode for color RAM
$\overline{CRAMWR}$	Color RAM write enable
D0–D15	68010 data bus, unbuffered
DOWN-1–DOWN-4	Joystick down switch inputs, players 1–4
EEPROM	Electrically erasable PROM chip select
$\overline{END}$	Current motion object finished
FCLOCK	System clock inverted phase
FIRE-1–FIRE-4	Fire switch inputs, players 1–4
$\overline{FLBA}$	Line buffer "A" fill control
$\overline{FLBB}$	Line buffer "B" fill control
GCS0–GCS5	Graphics ROMs chip select
$\overline{GLD}$	Graphics load (to SLAGS chips)
GND	System ground
GOUT0–GOUT3	Green latched digital video output
GP0–GP14	Graphics picture address
GP1V, GP2V, GP4V	Graphics picture stamp sub-address
GPEN	Graphics picture enable
GREEN	Green analog video output
GRH/L	Graphics ROM high/low select (A14 on a 27256)
GRN0–GRN3	Green color RAM data
H03	Alphanumerics load (to shift registers)
HFLP	Graphics stamp horizontal flip
$\overline{HORZ}$	Latch motion object horizontal data and palette data
HORZDL, $\overline{HORZDL}$	HORZ delayed one clock cycle
HPOS0–HPOS8	Motion object horizontal position data
$\overline{HSCRLD}$	Latch playfield horizontal scroll data

NOTE

In this signal name glossary all active-low signals are overscored, e.g., $\overline{COMPSYNC}$. In the schematics printed on Sheets 1–16 a slash (/) in front of a signal name indicates an active-low signal.

Gauntlet Signal Name Glossary, continued

VBUS	68010 "V" bus enable (for video RAM)
VCC	System V_{CC} (5 volts regulated)
VCPU	68010-to-video-RAM synchronization control
$\overline{\text{VERT}}$	Latch motion object vertical data and size data
VERTDL, $\overline{\text{VERTDL}}$	VERT delayed one clock cycle
$\overline{\text{VIDBLANK}}$	Video blank (horizontal and vertical blank mixed)
$\overline{\text{VMATCH}}$	Motion object vertical parameter matches current playfield vertical position
VOICE	Speech chip select
VPOS0–VPOS8	Motion object vertical position data
VRA0–VRA11	Video RAM address bus
$\overline{\text{VRAM}}$	68010 address decode for video RAM
$\overline{\text{VRAMRD}}$	68010 read from video RAM
$\overline{\text{VRAMWE}}$	68010 write to video RAM
VRD0–VRD15	Video RAM data bus, unbuffered
VRDTACK	Video RAM to 68010 data acknowledge
VSIZ0–VSIZ2	Motion object vertical size parameter
VSYNC, $\overline{\text{VSYNC}}$	Vertical sync
$\overline{\text{WDOG}}$	Watchdog control
$\overline{\text{WH}}$	68010 write high byte
$\overline{\text{WL}}$	68010 write low byte
$\overline{\text{WR68K}}$	6502 write to output buffer (to 68010)
$\overline{\text{YAMRES}}$	Music chip reset
YM0–YM2	Music audio mix control bits
ZREF	Intensity reference for video output

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ATARI GAMES

Gauntlet™ Signal Name Glossary, Continued

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Gauntlet Signal Name Glossary, continued

RAM0, RAM1	68010 working RAM chip selects
RAUD	Summed right channel audio
RCLOCK	System clock
RD0–RD15	68010 ROM data bus
$\overline{\text{RD68K}}$	6502 read 68010 output buffer
RED	Red analog video output
RED0–RED3	Red color RAM data
RIGHT-1–RIGHT-4	Joystick right switch inputs, players 1–4
ROM	68010 ROM data bus enable
$\overline{\text{ROM0}}$–$\overline{\text{ROM4}}$	68010 program ROM chip selects
ROMH/L	68010 program ROM high/low select (A14 on a 27256)
ROUT0–ROUT3	Red latched digital video output
SA0–SA15	6502 address bus unbuffered
SBA0–SBA13	6502 buffered address bus
SBD0–SBD7	6502 buffered data bus
SBR/$\overline{\text{W}}$	6502 buffered read/write control
SBW/$\overline{\text{R}}$	6502 buffered read/write control inverted
SD0–SD7	6502 data bus unbuffered
$\overline{\text{SELFTEST}}$	Self-test switch input test pad
SID	Serial input data
$\overline{\text{SIORD}}$	6502 miscellaneous input read control
$\overline{\text{SIOWR}}$	6502 output latch control
$\overline{\text{SIRQACK}}$	6502 interrupt acknowledge
SLAPSTK	SLAPSTIC chip select
SM0–SM2	Speech audio mix control bits
SNDBUF	6502 output buffer full (to 68010)
$\overline{\text{SNDINT}}$	68010 interrupt from 6502
$\overline{\text{SNDIRQ}}$	6502 4-millisecond interrupt
$\overline{\text{SNDNMI}}$	6502 non-maskable interrupt
$\overline{\text{SNDRD}}$	68010 read buffer from 6502
$\overline{\text{SNDRES}}$	6502 master reset (controlled by 68010)
$\overline{\text{SNDWR}}$	68010 write to output buffer (to 6502)
SOD	Serial output data
$\overline{\text{SPHRDY}}$	Speech chip ready
$\overline{\text{SPHRES}}$	Speech chip reset
$\overline{\text{SPHWR}}$	Speech chip write
SQUEAK	Speech chip operating frequency control
$\overline{\text{SRD}}$	6502 read phase
START-1–START-4	Start switch inputs, players 1–4
STEST	Self-test switch input
$\overline{\text{SWR}}$	6502 write phase
$\overline{\text{SYSRES}}$	System reset (power up)
$\overline{\text{UDS}}$	68010 upper data strobe
$\overline{\text{UNLOCK}}$	EEPROM write enable control
UP-1–UP-4	Joystick up switch inputs, players 1–4
VAS0, VAS1	Video RAM address control
(VAS0*), (VAS1*)	VAS0 and VAS1 before being latched
VBD0–VBD15	Video RAM buffered data bus
$\overline{\text{VBKACK}}$	Vertical blank interrupt acknowledge
$\overline{\text{VBKINT}}$	Vertical blank interrupt
$\overline{\text{VBLANK}}$	Vertical blank