MIDWAY'S

CARD RACK SYSTEM

PART I

#926-MINI

#927-COCKTAIL

#873-UPRIGHT

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FORM-00237-8012

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WARNING

THIS GAME MUST BE GROUNDED. FAILURE TO DO SO MAY RESULT IN DESTRUCTION TO ELECTRONIC COMPONENTS.

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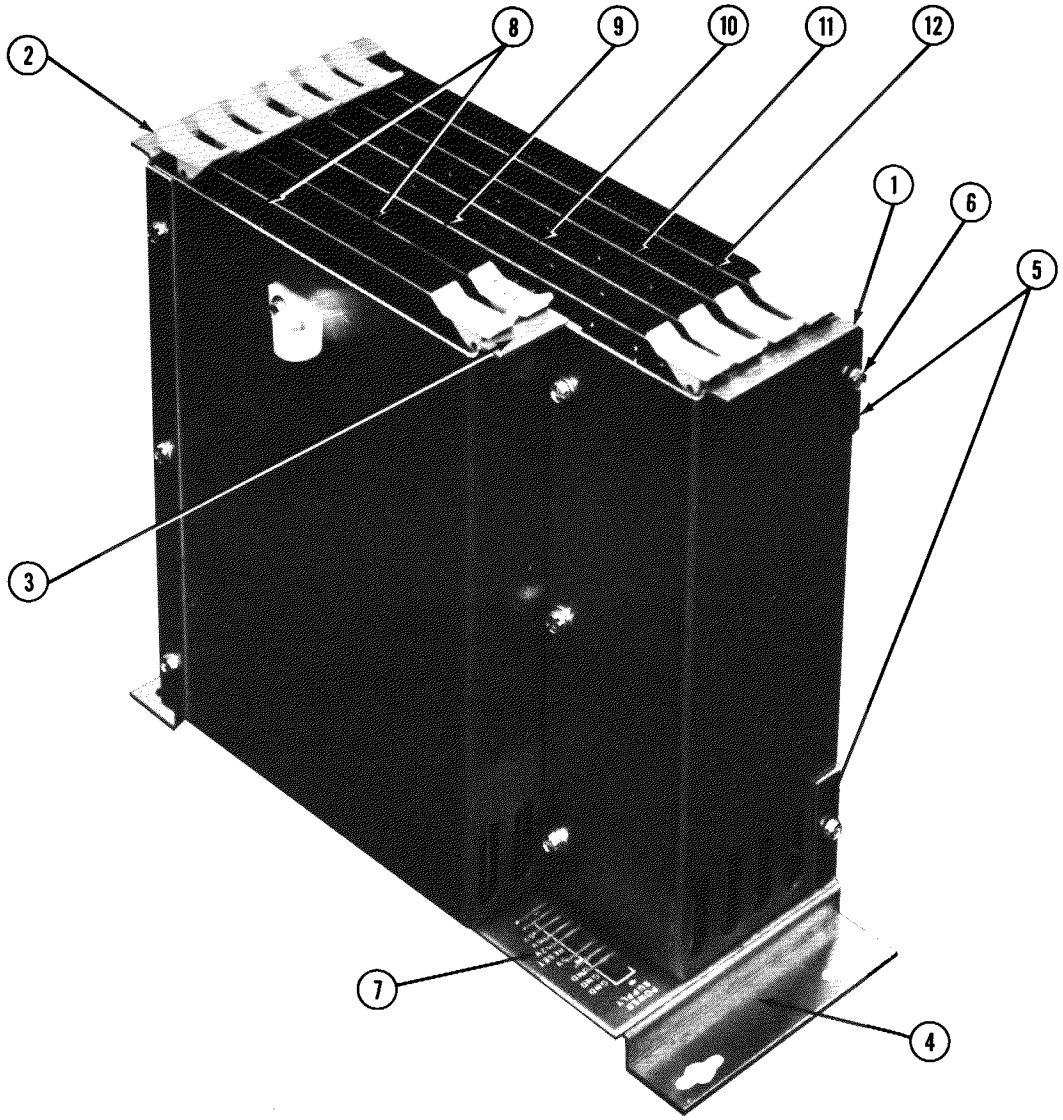
COMMERCIAL CARD RACK ASSY.



ITEM	PART Nº	DESCRIPTION
1	A789-00003-0000	P.C. RACK ASSY. - RIGHT
2	A789-00004-0000	P.C. RACK ASSY. - LEFT
3	A789-00005-0000	P.C. RACK ASSY. - BASE
4	0789-00100-0000	MTG. BRKT. SUPPORT (2 REQ'D.)
5	0789-00106-0000	RACK STRAP (2 REQ'D.)
6	0017-00101-0099	#6 x 1/4 SLT. HEX HD. SCREW (11 REQ'D.)
	0017-00104-0019	#6 FLAT WASHER (3 REQ'D.)
7	A082-90006-B000	BACK PANEL P.C. ASSY. (MOTHER BOARD)
8	A082-91356-C000	RAM BOARD ASSY.
9	A082-91354-F000	CPU BOARD ASSY.
10	A082-91355-C000	PATTERN TRANSFER BOARD ASSY.
11	A084-91364-A873	PROGRAMMED ROM/RAM BOARD ASSY.
12	A084-90708-C873	GAME LOGIC BOARD ASSY.
	0017-00007-0153	P.C. BOARD SUPPORT (2 REQ'D.) (NOT SHOWN)

SWITCH ADJUSTMENT - WIZARD OF WOR

OPTION SWITCH SETTINGS

Option switches are located on the game P.C.B. in the commercial card rack

COINS PER CREDIT

LEFT HAND COIN SLOT IS CONTROLLED BY SW. #1

SW. #1		
OFF	1 COIN	1 CREDIT
ON	2 COINS	1 CREDIT

RIGHT HAND COIN SLOT IS CONTROLLED BY SW. #2 AND SW. #3

SW. #3	SW. #2		
OFF	OFF	1 COIN	1 CREDIT
OFF	ON	2 COINS	1 CREDIT
ON	OFF	1 COIN	3 CREDITS
ON	ON	1 COIN	5 CREDITS

LANGUAGE

SW. #4	
OFF	ENGLISH
ON	FOREIGN LANGUAGE (REQUIRES A082-91374-A000)

WORRIORS PER CREDIT

SW. #5	
OFF	1 CREDIT = 2 WORRIORS / 2 CREDITS = 5 WORRIORS
ON	1 CREDIT = 3 WORRIORS / 2 CREDITS = 7 WORRIORS

BONUS PLAYER AWARDED:

SW. # 5	
OFF	BONUS WORRIOR AFTER 3RD DUNGEON
ON	BONUS WORRIOR AFTER 4TH DUNGEON

PLAY MODE

SW. #7	
OFF	COIN PLAY
ON	FREE PLAY

GAME ATTRACTION SOUNDS

SW. #8	
OFF	CONTINUOUS SOUND DURING "ATTRACT MODE"
ON	SOUND DURING ATTRACT MODE ONLY IF GAME CONTROLS ARE TOUCHED. (WHEN ANY BUTTON OR CONTROL IS TOUCHED, GAME PROVIDES SOUND FOR ONE COMPLETE CYCLE ON THE "ATTRACT MODE". IT WILL THEN BE QUIET UNTIL TOUCHED AGAIN).

PART NO. M051-00961-A021

SWITCH ADJUSTMENT — GORF

ADJUSTMENT SWITCHES

LEFT HAND COIN SLOT IS CONTROLLED BY SW. #1

SWITCH #1		
OFF	1 COIN	1 PLAY
ON	2 COINS	1 PLAY

RIGHT HAND COIN SLOT IS CONTROLLED BY SW. #2 & #3

SWITCH #2	SWITCH #3		
OFF	OFF	1 COIN	1 PLAY
ON	OFF	2 COINS	1 PLAY
OFF	ON	1 COIN	3 PLAYS
ON	ON	1 COIN	5 PLAYS

SWITCH #4	ENGLISH
ON	OTHER LANGUAGE REQUIRES A082-91374-A000.

NUMBER OF BASES PER GAME

SWITCH #5	
OFF	TWO BASES PER CREDIT
ON	THREE BASES PER CREDIT
SWITCH #6	BONUS BASE AWARDED AFTER MISSION #5
ON	NO BONUS BASE
SWITCH #7	
OFF	COIN PLAY
ON	FREE PLAY
SWITCH #8	
OFF	GAME ATTRACTION SOUNDS DURING GAME OVER
ON	NO GAME ATTRACTION SOUNDS DURING GAME OVER

M051-00873-A14.

RAM-ROM TEST - SPACE ZAP

PLACING THE TEST SWITCH, (LOCATED ON THE AUDIO AMPLIFIER ASSEMBLY IN THE COIN BOX AREA) TO ON PERFORMS THE FOLLOWING FUNCTIONS:

(1) REMOVES ALL ACCUMULATED CREDITS
(2) TESTS THE SCREEN RAM
(3) TESTS THE STATIC RAM
(4) TESTS THE GAME ROM/EPROM
(5) REPEATS ALL TESTS INDEFINITELY

PLACING THE TEST SWITCH IN THE OFF POSITION RETURNS THE GAME TO NORMAL OPERATION AFTER COMPLETION OF THE ROM TEST. IF YOU WERE TO TURN THE TEST SWITCH OFF DURING THE SCREEN RAM TEST, IT WOULD TAKE APPROXIMATELY 15 SECONDS BEFORE THE GAME WOULD RE-APPEAR.

THE GAME DOES A MODIFIED FORM OF RAM TEST UPON POWER-UP OR WHENEVER THE DOOR-SLAM SWITCH IS ACTIVATED. IF AN ERROR IS FOUND, THE PROGRAM CONTINUES THE TEST UNTIL THE ERROR IS CLEARED. THEREFORE, IT IS POSSIBLE THAT THE GAME WILL NEVER START AND/OR THERE MAY BE NO INDICATION OF ANYTHING ON THE SCREEN IF THERE IS A RAM ERROR.

ERROR INDICATIONS

IF ALL RAM AND ROM ARE GOOD, THE ONLY INDICATION WILL BE AN OCCASIONAL FLASH ON THE SCREEN (APPROXIMATELY EVERY 16 SECONDS). THIS INDICATES THAT IT HAS PASSED ALL TESTS AND IS STARTING THE TEST SEQUENCE OVER AGAIN.

IF AN ERROR IS FOUND IN THE SCREEN RAM, YOU WILL SEE THE FLASH ON THE SCREEN FOLLOWED BY FLASHING RANDOM HORIZONTAL BARS. IT WILL THEN CYCLE THROUGH THE TEST AGAIN UNTIL THE ERROR IS CLEARED.

IF AN ERROR IS FOUND IN THE STATIC RAM, THERE WILL BE SHORT BURSTS OF FLASHING HORIZONTAL BARS DISPLAYED ON THE SCREEN. IT WILL THEN CYCLE THROUGH THE SCREEN RAM TEST AND THE STATIC RAM TEST AGAIN UNTIL THE ERROR IS CLEARED. THE CYCLE TIME IS APPROXIMATELY 3 SECONDS.

RAM-ROM TEST - SPACE ZAP

A BAD ROM/EPROM IS INDICATED BY A NUMBER 1, 2, 3, 4, 5, 6, 7, OR 8 DISPLAYED ON THE SCREEN. IF MORE THAN ONE ROM/EPROM IS BAD BOTH NUMBERS WILL APPEAR ON THE SCREEN.

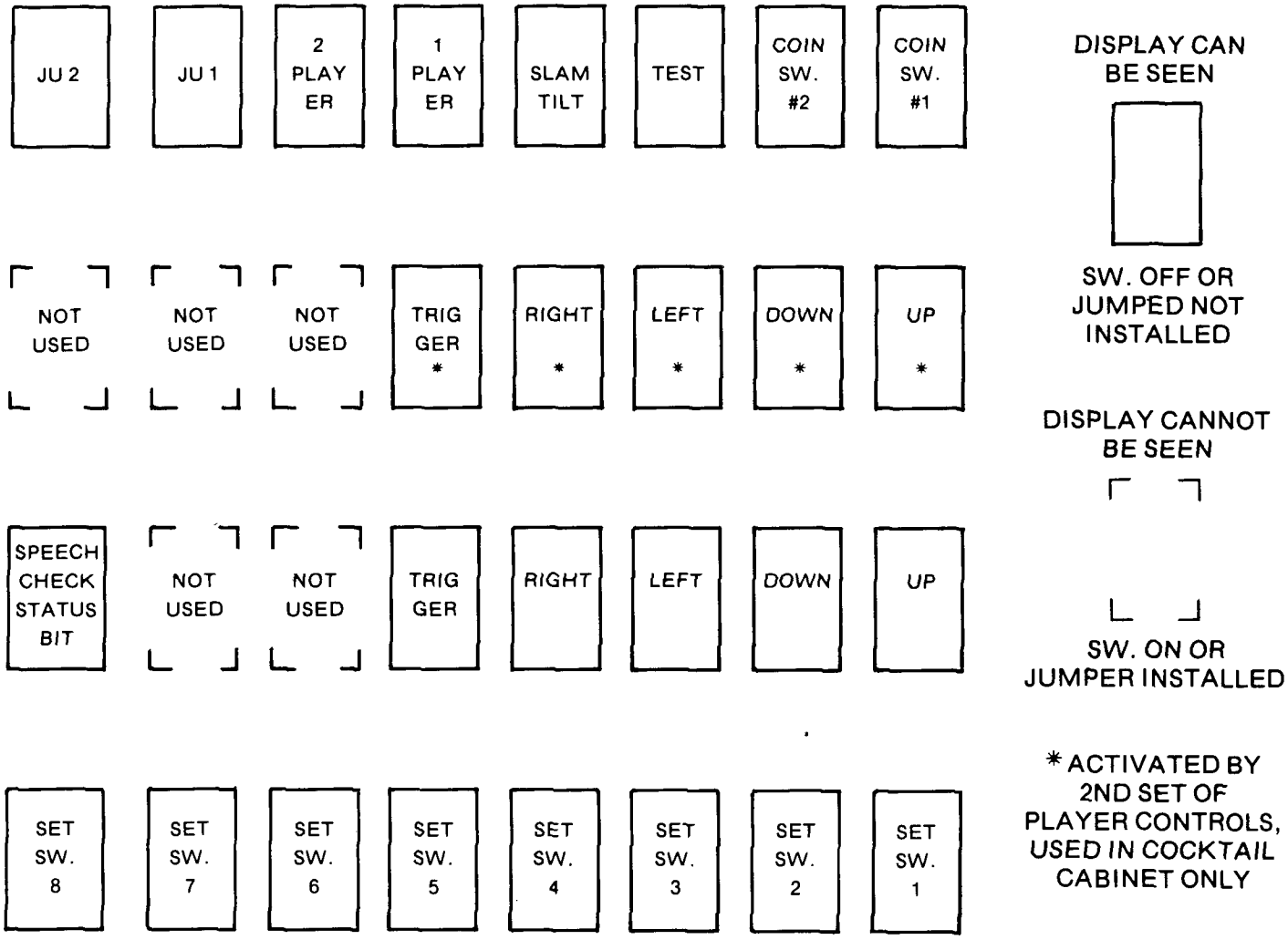
IF YOU HAVE 8 2K ROMS/EPROMS

NUMBER DISPLAYED	BAD ROM/EPROM IN SOCKET
1	X1
2	X2
3	X3
4	X4
5	X5
6	X6
7	X7
8	X8

IF YOU HAVE 4 4K ROMS/EPROMS

NUMBER DISPLAYED	BAD ROM/EPROM IN SOCKET
1	X1
2	X1
3	X3
4	X3
5	X5
6	X5
7	X7
8	X7

TEST DISPLAY FOR GORF



A B C D E F G H

A LETTER APPEARING HERE INDICATES A BAD ROM/E PROM

Placing the test switch (located on the Audio amplifier assy. in the coin box area) to "on" performs the following functions:

1. Removes all accumulated credits.
2. Test the screen rams.
3. Test the static rams.
4. Test all switches.

If a screen ram is defective random bars will flash on screen.

If a static ram is defective a random dotted pattern will flash on screen.

Dotted pattern will flash on the screen. If all rams are good the switch test pattern will appear on the screen.

All switches must be "off" to get the pattern shown above. When each switch is turned on the position of that switch will disappear.

Time delay between returning test switch to "off" and game over sequence is normal approx. 25 seconds.

CARD RACK BOARD TEST

RAM TEST

1. Remove Game Card PC A084-90708-A902 & Rom Ram Card A082-91364-A000.
2. Remove Pattern Card PC A084-91355-C000.
3. Remove Ram Card in position J-2 PC A082-91356-B000.
4. The Ram Card in position J-1 must remain and be a known good card.
5. Do not remove the CPU Card A082-91354-E000.
6. Insert the Card Rack Board Tester PC A080-91517-A000 into position J-4.
7. Insert the Ram Test Card into position J-6 PC A080-91516-A000.
8. Insert the bad Ram Card into 18 pin connector of Ram Card Tester.
9. Connect video cable to connector J-2 of Card Rack Board Tester pins 11 and 12.
10. Move black slide switch on Card Rack Board Tester into position #1.
11. The dip switch settings must be as follows: 1 - 3 - 5 - 7 OFF and 2 - 4 - 6 - 8 ON.
12. Press Red reset button (S-1) on Ram Test Card to clear system.
13. A bad Ram location will flash on video screen and on flashing Rams indicate all Rams are good.
14. Move black slide switch on Card Rack Board Tester to position #2.
15. Clear system again by pressing Red reset button on Ram Test Card S1.
16. If the Rainbow test shows Garbage, check the video output. (74LS166)
17. When Rams are all good and Rainbow pattern is clear this indicates a good Ram Card.
18. Proceed to Pattern Card Test.

PATTERN BOARD TEST

1. Remove Ram Test Card PC A080-91516-A000.
2. Remove Card Rack Board Tester Card from J-4 and insert it into J-6 A080-91517-A000.
3. Remove the two Ram Test Proms located at X-4 and X-5 of Card Rack Board Tester.
4. Insert two Pattern Test Proms at location X-4 and X-5.
5. Connect video cable to connector J-2 of Card Rack Board Tester pins 11 and 12.
6. Insert bad Pattern Card into 50 pin connector of Card Rack Board Tester.
7. Press Red reset button to clear system.
8. A bad Pattern Card will display area of trouble on video screen.
9. A good Pattern Card will display the words (''LOOKS GOOD'').
10. Connectors J-1 and J-5 are not used at this time.
11. The Dip Switch is for future use.

NOTE: When chip U-2 (74S138) is removed the Card Rack Board Tester Card PC A080-91517-A000 can be used as an extender card for powering up the CPU, Pattern and Game Cards.

The black slide switch should be in position #1 when X4 & X5 Roms are in proper location.

For proper Pattern Test, two Ram Cards must be used. PC A082-91356-B000.

MIDWAY'S CARD RACK SYSTEM

PATTERN BOARD TEST

FATAL ERRORS		LOCATION
DATA LATCHES		U19 & U10 74LS175
FLUSH DATA BIT 08		U21 PIN 10 74174
DIRECTION DATA BIT 01		U21 PIN 2 74174
AREA AND LINEAR HIGH 2 BITS	LINEAR:	U7 PIN 3 & 13 U8 PIN 10 & 13
	AREA:	U9 PIN 3 & 13 U8 PIN 11 & 14
TRI - STATE BUFFERS		U20 & U11 74LS367
CONTROL LOGIC (CLOCK)		U5 - 74LS161 U6 - 74LS04 U12 - 74LS00

1. U21 74LS174 IS THE STATUS LATCH.

   PIN 2 DIRECTION
   PIN 5 EXPAND
   PIN 7 CONSTANT
   PIN 10 FLUSH
   PIN 12 FLIP
   PIN 15 FLOP

   THE U21 STATUS CHIP WILL CONTROL THE SHIFTING OF DATA IN A CERTAIN DIRECTION, MAKING A LARGER OBJECT, MOVING THE SAME SIZE OBJECT, TURNING OR ROTATING THE OBJECT, ETC.

2. THE HEX. CODE 08 AND 01 IS CONVERTED INTO A BINARY CODE:

   08 = 00001000
   01 = 00000001

3. FLUSH SETS MEMORY TO A FIX COLOR.

MIDWAY'S CARD RACK SYSTEM

PATTERN BOARD TEST

ERRORS	LOCATION
1. DATA BUS	U10 & U19
2. LINEAR	U7, U16, U25 & U34
3. AREA LD	U27, U30, U36 & U39
4. X WIDE	U31, U32, U33, U40, U41 & U42
5. FEED BK	U28, U29, U37 & U38
6. STATUS	U21
7. LINEAR CT	U7, U8, U16, U17, U25, U26, U33 & U34
8. AREA CT	U9, U15, U17, U18, U23 & U24

STATUS (U21)

ERRORS	LOCATION
FLOP	PIN 15
FLIP	PIN 12
FLUSH	PIN 10
CONSTANT	PIN 7
EXPAND	PIN 5
DIRECTION	PIN 2

PATTERN BOARD THEORY OF OPERATION

MIDWAY'S CARD RACK SYSTEM

This explanation of the theory of operation is intended to be very basic and not a chip-by-chip or signal-by-signal explanation. There are some complicated features of this assembly that would take too much room to explain nor would it serve any useful purpose for the service technician.

The function of this board is to move blocks of data from one memory location to another at a fast rate. In the Card Rack System this translates into the ability to transfer a pattern on the screen (or from ROM) to another location on the screen.

Parameters are passed to the Pattern Board by a series of output instructions to ports 78 through 7E. IC's U1, U2, U4 and portions of U3, U6 and U14 perform the port decoding.

The follwing is a sequence of events in a typical operation of transferring a color encoded pattern from ROM to screen RAM.

The mode control byte is loaded into U21 by an output instruction to port 7A. Here the various modes of operation are selected.

The sixteen-bit linear address (which is usually the source address) is loaded into U34, U25, U16 and U7. The low-order eight bits are loaded into U34 and U25 by an output instruction to port 78. The high-order eight bits are loaded into U16 and U7 by an output instruction to port 79.

The sixteen-bit area address (which is usually the destination) is loaded into U39, U30, U18 and U9. The low-order eight bits are loaded into U39 and U30 with an output instruction to port 7B. The high-order eight bits are loaded into U18 and U9 with an output instruction to port 7C.

A line offset value is loaded into U39 and U30 with an output instruction to port 7B.

The width of the pattern is loaded into U41 and U32 with an output instruction to port 7D. The height of the pattern is loaded into U40 and U31 with an output to port 7E. This instruction also starts the following sequence to perform the actual pattern transfer.

The output to port 7E persets one-half of U13 sending the signal $\overline{\text{BUSREQ}}$ low. The Z-80 (located on the CPU board) responds by tri-stating its address, data and control signals and then asserting $\overline{\text{BUSACK}}$ low.

When $\overline{\text{BUSACK}}$ goes low, the control signal buffers for $\overline{\text{RD}}$, $\overline{\text{WR}}$, $\overline{\text{MREQ}}$ and $\overline{\text{IORQ}}$ are enabled placing the control signals on the bus; the tri-state address multiplexers U35, U26, U17, U8 and data buffers U20 and U11 are enabled placing their signals on the bus; and the master clock generator U5 starts counting. During the time that this Pattern Board has control of the bus, the signal appear identical to those created by the Z-80.

The first cycle is a read from the address contained by the linear address counters with the data going into the data hold registers U19 and U10.

The next cycle is a write cycle to the address contained in the area address counters. The data is placed on the data bus by the tri-state buffers U20 and U11.

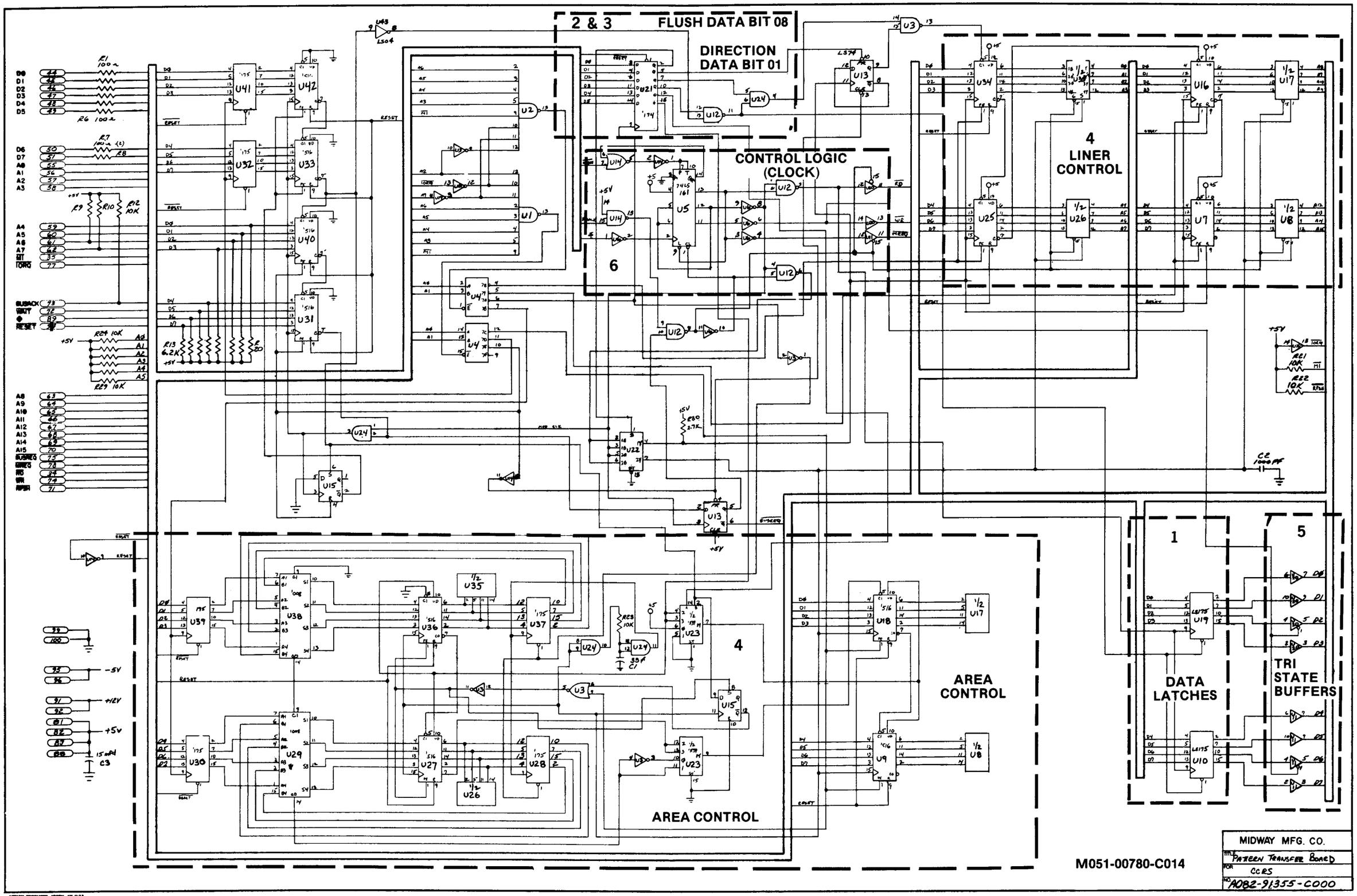
This typical read-write cycle continues until the width counters U42 and U33 count down to zero. This completes one horizontal line of data transfer.

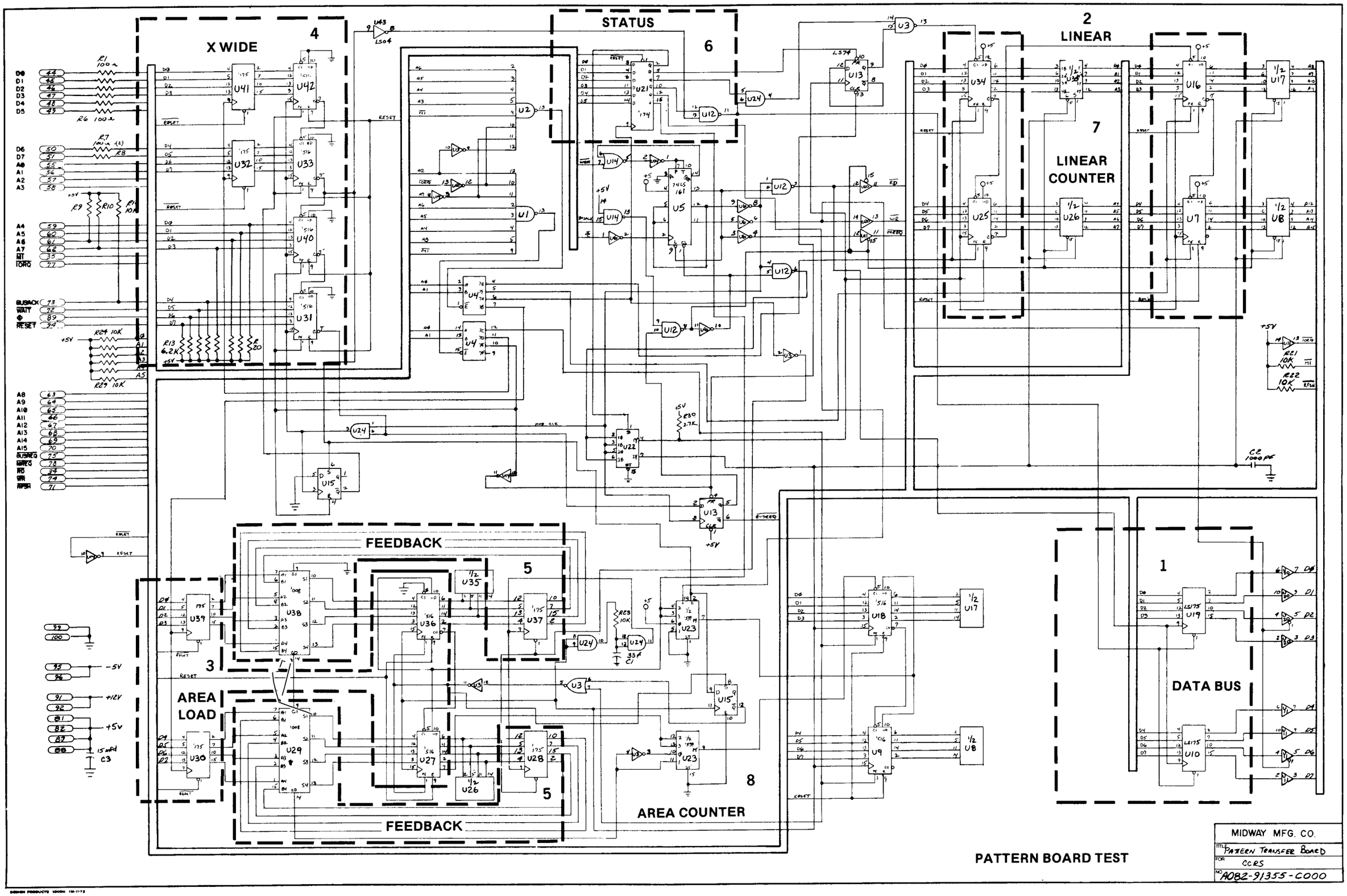
To prepare for the next horizontal line of data transfer two things must occur. First, the width count contained in U41 and U32 is loaded into U42 and U33. Simultaneously the height count contained in U40 and U33 is decremented. Second, the distance to the starting point on the next line, contained in U39 and U30 is added (through U38 and U29) to the present count contained in U37 and U28 and then loaded into counters U36 and U27.

These line transfers count until the height counters U40 and U31 reach zero.

At this time, $\overline{\text{BUSREQ}}$ is taken high disabling the clock generator U5 from any further activity. Also all data, address and control lines are tri-stated off of the bus returning control to the Z-80. The Z-80 responds by taking $\overline{\text{BUSACK}}$ high and continuing with its normal operation.

PATTERN BOARD SCHEMATIC




X WIDE
4
STATUS
6
2
LINEAR
7
LINEAR COUNTER
FEEDBACK
5
3
AREA LOAD
FEEDBACK
5
8
AREA COUNTER
1
DATA BUS
PATTERN BOARD TEST
MIDWAY MFG. CO.
TITLE PATTERN TRANSFER BOARD
FOR CCRS
NO A082-91355-C000

TROUBLE SHOOTING CARD RACK SYSTEM

All test points are found on the rear side of the Back Panel Board PC A082-93006-C/D000.

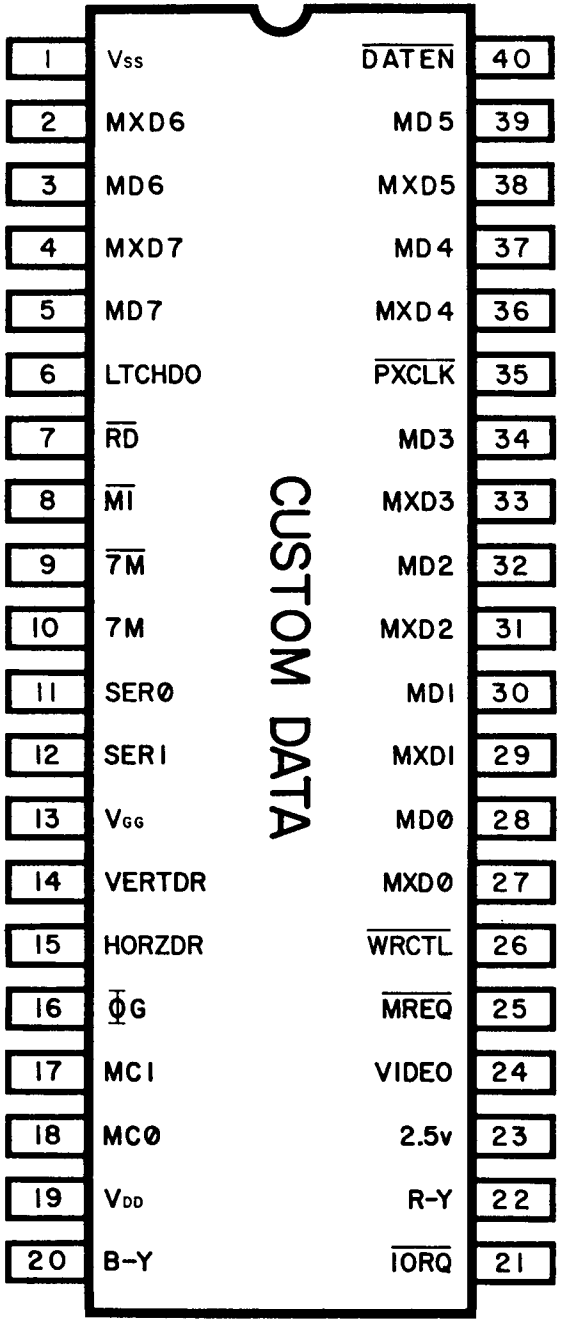
1. +5VDC PINS 87 AND 88.
2. +12VDC PINS 91 AND 92.
3. -5VDC PINS 95 AND 96.
4. LOGIC GROUND PINS 99 AND 100.
5. SYSTEM CLOCK 7.1MHZ PINS 97 AND 98.
6. VIDEO CLOCL 3.5MHZ PINS 93 (CHROM).
7. CPU CLOCK 1.7MHZ PINS 89 AND 90.
8. CPU RESET PIN 94 (NORMALLY HIGH).
9. DATA BITS (0-7) PINS 44 TO 51.
10. ADDRESS BITS (0-15) PINS 55 TO 70.
11. COMPOSITE VIDEO PIN 85.

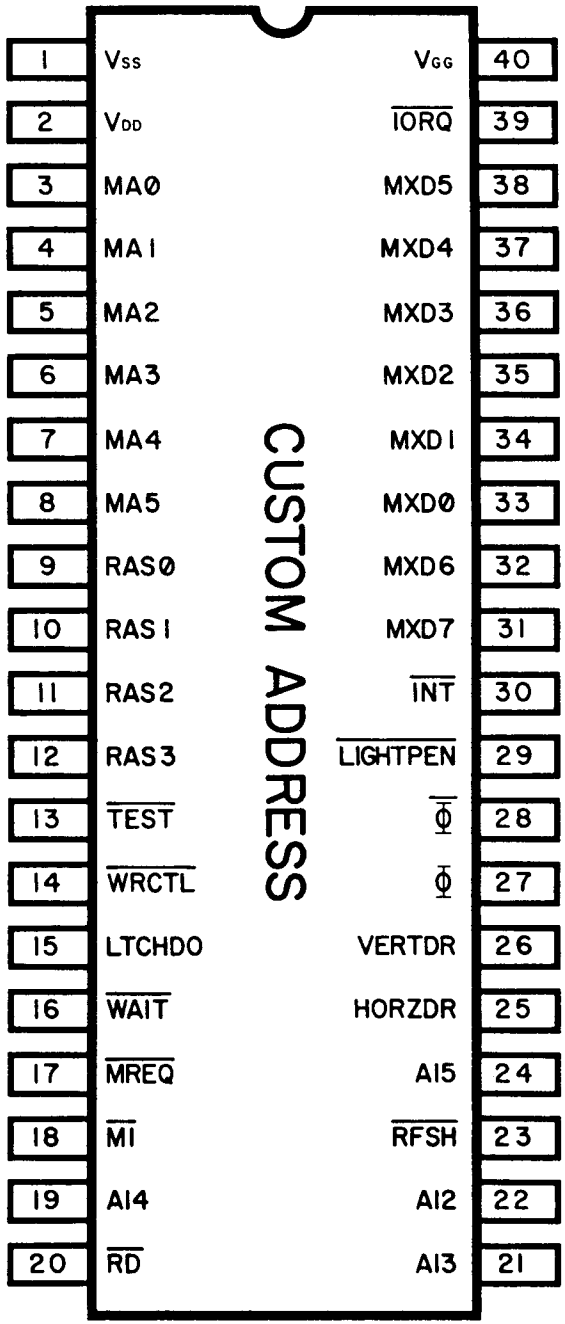
For all Additional Test Points refer to Page #15.

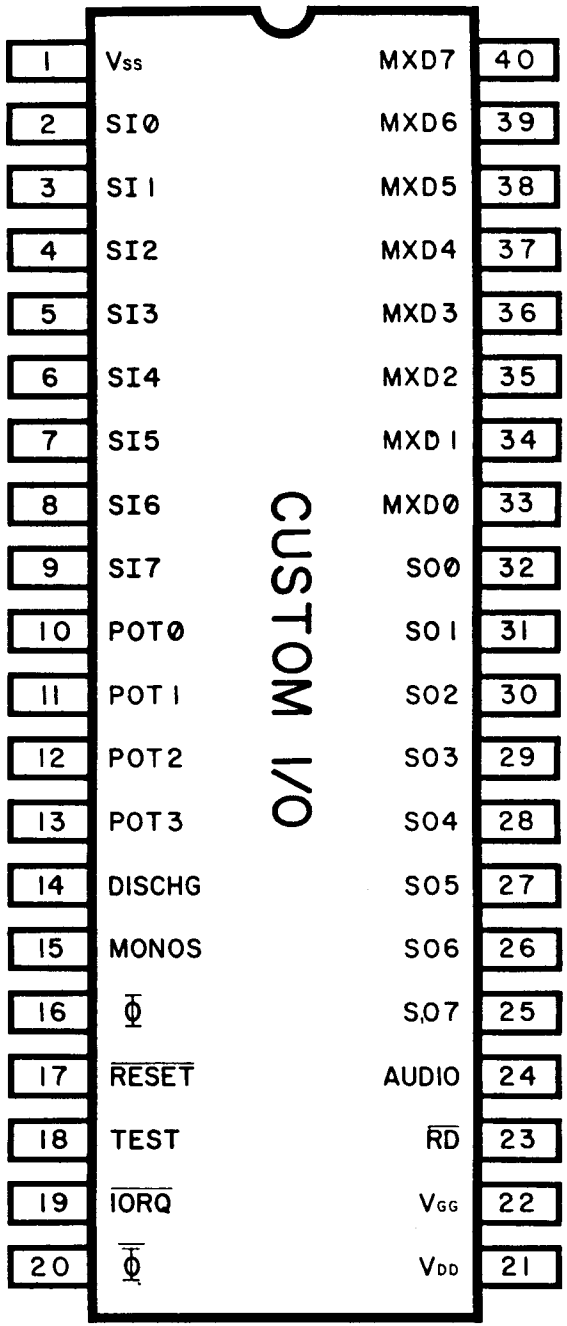
BACK PANEL BOARD PC A082-93006 C/D000

PIN	DESIGNATION	DESCRIPTION
1	S/$\overline{L}$	Screen RAM Video Load Strobe
2	$\overline{WE}$	Write Enable
3	SER1	Serial Data 1
4	SER0	Serial Data 0
5	$\overline{RAS3}$	Row Address Strobe 3
6	$\overline{RAS2}$	Row Address Strobe 2
7	$\overline{RAS1}$	Row Address Strobe 1
8	$\overline{RAS0}$	Row Address Strobe 0
9	$\overline{CAS}$	Column Address Strobe
10	DATEN	Data Write Enable
11	MA0	Multiplexed Address Bit 0
12	MA1	Multiplexed Address Bit 1
13	MA	Multiplexed Address Bit 2
14	MA	Multiplexed Address Bit 3
15	MA	Multiplexed Address Bit 4
16	MA5 25	Multiplexed Address Bit 5
17	MD7	Memory Data Bus Bit 7
18	MD6	Memory Data Bus Bit 6
19	MD5	Memory Data Bus Bit 5
20	MD4	Memory Data Bus Bit 4
21	MD3	Memory Data Bus Bit 3
22	MD2	Memory Data Bus Bit 2
23	MD1	Memory Data Bus Bit 1
24	MD0	Memory Data Bus Bit 0
25	BUFA0	Buffered Address Bit 0
26	BUFA1	Buffered Address Bit 1
27	$\overline{BUZOFF}$	Microcycle Data Bus Disable
28	$\overline{WATCHDOG}$	Automatic Reset
29	$\overline{LIGHTPEN}$	Lightpen Interrupt
30	VERTDR	Vertical Sync
31	HORZDR	Horizontal Sync
32	MC0	Microcycle Control 0
33	MC1	Microcycle Control 1
34	$\overline{RD}$	Read
35	$\overline{M1}$	Machine Opcode Cycle
36	MXD0	Microcycle Data Bus Bit 0
37	MXD1	Microcycle Data Bus Bit 1
38	MXD2	Microcycle Data Bus Bit 2
39	MXD3	Microcycle Data Bus Bit 3
40	MXD4	Microcycle Data Bus Bit 4
41	MXD5	Microcycle Data Bus Bit 5
42	MXD6	Microcycle Data Bus Bit 6
43	MXD7	Microcycle Data Bus Bit 7
44	D0	Data Bit 0
45	D1	Data Bit 1
46	D2	Data Bit 2
47	D3	Data Bit 3
48	D4	Data Bit 4
49	D5	Data Bit 5
50	D6	Data Bit 6

PIN	DESIGNATION	DESCRIPTION
51	D7	Data Bit 7
52	$\overline{SCREEN}$	Screen RAM Decode
53	RMC0	Refresh Microcycle Control 0
54	RMC1	Refresh Microcycle Control 1
55	A0	Address Bit 0
56	A1	Address Bit 1
57	A2	Address Bit 2
58	A3	Address Bit 3
59	A4	Address Bit 4
60	A5	Address Bit 5
61	A6	Address Bit 6
62	A7	Address Bit 7
63	A8	Address Bit 8
64	A9	Address Bit 9
65	A10	Address Bit 10
66	A11	Address Bit 11
67	A12	Address Bit 12
68	A13	Address Bit 13
69	A14	Address Bit 14
70	A15	Address Bit 15
71	$\overline{RFSH}$	Dynamic RAM Refresh
72	$\overline{WAIT}$	Wait
73	$\overline{BUSACK}$	Bus Acknowledge
74	$\overline{WR}$	Write
75	$\overline{BUSREQ}$	Bus Request
76	$\overline{NMI}$	Non-maskable Interrupt
77	$\overline{IORQ}$	Input/Output Request
78	$\overline{MREQ}$	Memory Request
79	$\overline{HALT}$	Halt CPU stopped
80	$\overline{INT}$	Interrupt Request
81	+5v	Positive 5 volt Power Supply
82	+5v	Positive 5 volt Power Supply
83	R-Y	Red minus Video
84	B-Y	Blue minus Video
85	VIDEO	Composite Video
86	+2.5vREF	2.5 volt Chroma Center Reference
87	+5v	Positive 5 volt Power Supply
88	+5v	Positive 5 volt Power Supply
89	Φ	CPU Clock 1.7897725 Mhz
90	$\overline{\Phi}$	Opposite phase CPU Clock 1.7897725 Mhz
91	+12v	Positive 12 volt Power Supply
92	+12v	Positive 12 volt Power Supply
93	CHROMA	3.579545 Mhz Chroma Subcarrier
94	$\overline{RESET}$	Reset
95	-5v	Negative 5 volt Power Supply
96	-5v	Negative 5 volt Power Supply
97	7M	System Clock 7.15909 Mhz
98	$\overline{7M}$	Opposite phase system clock 7.15909 Mhz
99	GND	System Power and Logic Ground
100	GND	System Power and Logic Ground


CUSTOM DATA
1 Vss
2 MXD6
3 MD6
4 MXD7
5 MD7
6 LTCHDO
7 RD
8 MI
9 7M
10 7M
11 SER0
12 SER1
13 VGG
14 VERTDR
15 HORZDR
16 ΦG
17 MC1
18 MC0
19 VDD
20 B-Y
40 DATEN
39 MD5
38 MXD5
37 MD4
36 MXD4
35 PXCLK
34 MD3
33 MXD3
32 MD2
31 MXD2
30 MD1
29 MXD1
28 MD0
27 MXD0
26 WRCTL
25 MREQ
24 VIDEO
23 2.5v
22 R-Y
21 IORQ


CUSTOM ADDRESS
1 Vss
2 VDD
3 MA0
4 MA1
5 MA2
6 MA3
7 MA4
8 MA5
9 RAS0
10 RAS1
11 RAS2
12 RAS3
13 TEST
14 WRCTL
15 LTCHDO
16 WAIT
17 MREQ
18 MI
19 AI4
20 RD
40 VGG
39 IORQ
38 MXD5
37 MXD4
36 MXD3
35 MXD2
34 MXD1
33 MXD0
32 MXD6
31 MXD7
30 INT
29 LIGHTPEN
28 Φ
27 Φ
26 VERTDR
25 HORZDR
24 AI5
23 RFSH
22 AI2
21 AI3


CUSTOM I/O
1 Vss
2 SI0
3 SI1
4 SI2
5 SI3
6 SI4
7 SI5
8 SI6
9 SI7
10 POT0
11 POT1
12 POT2
13 POT3
14 DISCHG
15 MONOS
16 Φ
17 RESET
18 TEST
19 IORQ
20 Φ
40 MXD7
39 MXD6
38 MXD5
37 MXD4
36 MXD3
35 MXD2
34 MXD1
33 MXD0
32 SO0
31 SO1
30 SO2
29 SO3
28 SO4
27 SO5
26 SO6
25 SO7
24 AUDIO
23 RD
22 VGG
21 VDD

I/O CHIP DESCRIPTION

The Z-80 communicates with the I/O Chip through Input and Output instructions. The state of an 8 x 8 switch matrix can be read through the Switch Scan circuit. When an Input instruction is executed, one of the SO0-SO7 lines will be activated. When a line is activated, the switch matrix will feed back eight bits of data on SI0-SI7. This data is in turn fed to the Z-80 through MUXD0 - MUXD7.

The Z-80 can read the position of four potentiometers (pots) through the A-D Converter circuit. The pots are continuously scanned by the A-D Converter and the results of the conversion are stored in a RAM with Input instructions.

The Z-80 loads data into the Music Processor with Output instructions. This data determines the characteristics of the audio that is generated.

ADDRESS CHIP DESCRIPTION

THE Microcycle Decoder generates twelve bits of Z-80 address from the 8-bit Microcycle Data Bus. This address is then fed through MUX I and MUX II to MA0-5 which go to the RAM. The Scan Address Generator generates a 12-bit address which is used to read video data from the RAM. This address goes from 0 to FFFH once every frame (1/60 sec.).

MUX I sends either the Scan Address of Z-80 Address to its 12 outputs. An output of the Scan Address Generator controls MUX I. If the Scan Address Generator and the Z-80 request a memory cycle at the same time, the Scan Address Gererator will have higher priority and the Z-80 will be required to wait (by the $\overline{WAIT}$ output). The Scan Address Generator never requires the memory for more than one consecutive memory cycle, so the Z-80 is never required to wait for the memory for more than one cycle. HORIZ DR and VERT DR synchronize the Scan Address Generator with the Data Chip and the TV Scan.

The purpose of MUX II is to multiplex its 12 inputs to the six address bits in the two time slices required for 4K x 1 16 pin RAMS.

The Memory Cycle Generator controls memory cycles generated by either the Z-80 or Scan Address Generator. $\overline{MREQ}$, $\overline{RD}$, $\overline{M1}$, $\overline{RFSH}$, and A12-A15 are from the Z-80. A12-A15 are fed directly from the Z-80 because if they were brought out of the Microcycle Decoder, they would arrive too late in the memory cycle. The RAS0 - RAS3 outputs are used to activate memory cycle and all four RAS's are used to control four banks of RAM (16K x 8). WRCTL and LTCHD0 are control signals to the Data Chip. WRCTL tells the Data Chip when to place data to be written to memory on the Memory Data Bus. LTCHDO tells the Data Chip when valid data from RAM is present on the Memory Data Bus.

DATA CHIP DESCRIPTION

The TV Sync Generator uses 7M and $\overline{7M}$ (7.159090 MHZ square waves) to generate NTSC standard sync and blank to be sent to the Video Generator. It also generates HORIZ DR and VERT DR for synchronization with the Address Chip. HORIZ DR occurs once every horizontal line (63.5 usec), and VERT DR occurs once every frame (16.6 msec).

The Shift Register loads parallel data from the memory data bus (MD0 - MD7) and shifts it out of its two serial outputs. The TV Sync Generator controls when data is loaded or shifted. In a commercial game SERIAL 0 and SERIAL 1 are sent through the MUX I to MUX II. The two bits from MUX I select 8 bits to be sent through MUX II to the Video Generator. These 8 bits then determine the analog values of VIDEO, R-Y, and B-Y. 2.5V is a 2.5V D C reference level.

The Clock Generator generates 0G and $\overline{PX}$ from 7M. These are the clocks for the rest of the system. The frequency of $\overline{PX}$ is half that of 7M and the frequency of 0G is half that of $\overline{PX}$.

The Microcycle Generator generates the microcycle control bits, MC0 and MC1, from $\overline{IORQ}$, $\overline{MREQ}$, $\overline{RD}$, and $\overline{M1}$, all from the Z-80.

In memory write cycles WRCTL is activated and the Memory Control circuit generates $\overline{DATEN}$. The Magic Function Generator takes the data from the Z-80 on MUXD0 - D7 and transfers it to MD0 - MD7. If a Magic write is being done, the Magic Function Generator will modify the data as required before it places it on the memory data bus.

CARD RACK LOGIC BOARDS

SPACE ZAP GAME BOARD (PC A084-90708-A902)

CHIP NUMBER	FUNCTION
74LS02	Quad 2 input Nor
74LS08	Quad 2 input And
74LS32	Quad 2 input Or
74LS74	Dual "D" Flip-Flop
74LS133	13 input Nand
74LS138	3 to 8 line decoder
74LS139	Dual 2 to 4 line decoder
MC14078	8 input Nor
MC14174	Hex "D" Flip-Flop
2114	RAM
2716-8516	PROM 16K
9316	ROM 16K
2720-(0066-117)	I & O custom chip
Additional Devices:	
TIP110	NPN transistor
2N4401	NPN transistor
2N4403	PNP transistor
IN4004	Diode

CPU BOARD (PC A082-91354-D000)

CHIP NUMBER	FUNCTION
74LS00	Quad 2 input Nand
74LS02	Quad 2 input Nor
74LS04	Hex inverter
74LS08	Quad 2 input And
74LS10	Triple 3 input Nand
74LS20	Dual 4 input Nand
74LS74	Dual "D" Flip-Flop
74LS157	Quad 2 input multiplexer
74LS174	Hex "D" Flip-Flop
74LS175	Quad "D" Flip-Flop
Z80	CPU
2719-(0066-115)	Address custom chip
2721-(0066-116)	Data custom chip
74LS245	Octal bus transceiver
74LS257	Quad 2 input multiplexer
74S74	Dual "D" Flip-Flop
7416	Hex buffer
MC14024	7 stage ripple counter
Additional Devices:	
2N4401	NPN transistor
T1S-137	PNP transistor
IN4004	Diode
IN4148	Diode
14.31818	Crystal
47 Ω	Resistor
82 Ω	Resistor
220 Ω	Resistor
510 Ω	Resistor
680 Ω	Resistor
1K Ω	Resistor

PATTERN BOARD (PC A082-91355-C000)

CHIP NUMBER	FUNCTION
74LS00	Quad 2 input Nand
74LS04	Hex inverter
74LS74	Dual "D" Flip-Flop
74LS157	Quad 2 input multiplexer
74LS161	4 bit binary counter
74LS175	Quad "D" Flip-Flop
74LS257	Quad 2 input multiplexer
74LS367	Hex bus driver
CD4555	Dual binary 1 or 4 decoder
MC14008	4 bit full adder
MC14013	Dual "D" Flip-Flop
MC14068	8 input Nand
MC14174	Hex "D" Flip-Flop
MC14175	Quad "D" Flip-Flop
MC14516	Binary up/down counter
MC14539	Dual 4 input multiplexer
MC14572	Multiple gate package

RAM BOARD (PC A082-91356-C000)

CHIP NUMBER	FUNCTION
74LS08	Quad input And
74LS14	Hex schmitt trigger
74LS166	Parallel to serial shift register
74LS253	Dual 4 input multiplexer
MK4027 (MK4015)	RAM
Additional Devices:	
110 Ω	Resistor
220 Ω	Resistor
1K Ω	Resistor
0.1 μfd	Capacitor
15 μfd	Capacitor

AUDIO AMPLIFIER BOARD
(PC A082-90903-A000)

CHIP NUMBER	FUNCTION
2N4403	PNP transistor
TIP 31	NPN transistor
IN4004	Diode

POWER SUPPLY (PC A082-90411-A000)

CHIP NUMBER	FUNCTION
LM317	Voltage regulator
LM339	Quad voltage comparator
SG3532	General purpose regulator
Additional Devices:	
79M05	Negative five voltage regulator
IN3235	Zener diode
2N3055	NPN transistor

MONITOR INTERFACE BOARD
(PC A082-91373-B000)

CHIP NUMBER	FUNCTION
LM339	Quad voltage comparator
LM360	Differential comparator
Additional Devices:	
MPS AZ0	Transistor
MPS A70	Transistor

NOTE: When an IC is a LS, it should be replaced by a LS device (low schottky).

GORF GAME BOARD
PC A084-90708-A873

CHIP NUMBER	FUNCTION
74LS04	Hex inverter
74LS30	8 input Nand
74LS74	Dual "D" Flip-Flop
74LS86	Quad 2 input exclusive or
74LS153	Dual 4 to 1 line multiplexer
74LS161	4 bit binary counter
74LS164	8 bit shift register
74LS174	Hex "D" Flip-Flop
74LS257	Quad 2 to 1 line multiplexer tri-state
74LS367	Hex bus driver-tri-state
0066-117XX (2720)	Custom I/O chip
MC14066	Quad bilateral switch - Cmos
MC14099	8 bit addressable - latch -
MC14099	8 bit addressable latch - Cmos
MC14539	Dual 4 to 1 line multiplexer - Cmos
SC01	Voice sound generator

GORF ROM/RAM BOARD
PC A082-91364-A000

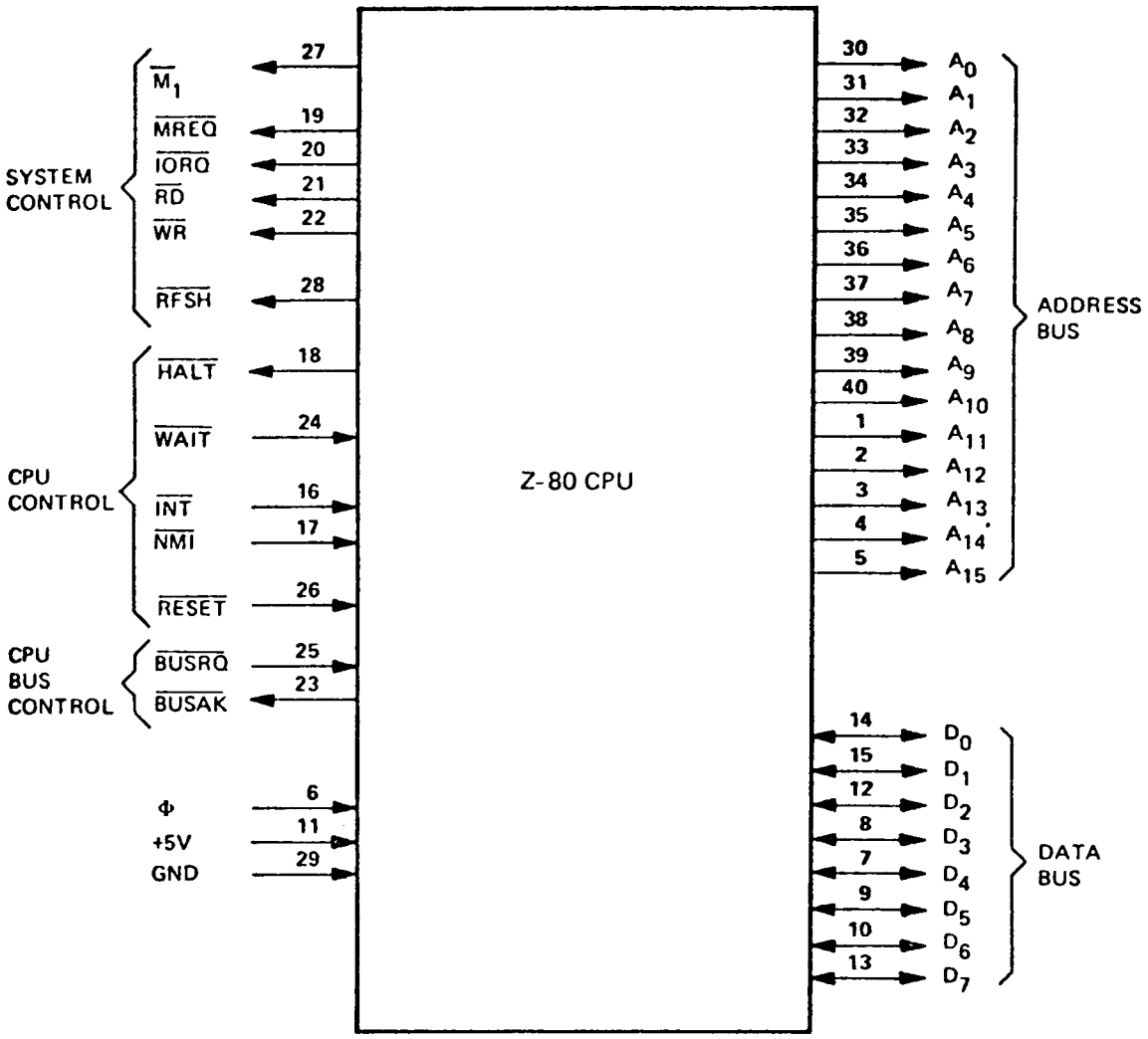
CHIP NUMBER	FUNCTION
74LS02	Quad 2 input Nor
74LS08	Quad 2 input And
74LS30	8 input Nand
74LS32	Quad 2 input Or
74LS74	Dual "D" Flip-Flop
74LS133	13 input Nand
74LS138	3 to 8 line decoder/ multiplexer
74LS244	Octal buffer
MC14078	8 input Nor - Cmos
2114	1K X 4 - Ram
9332	4K X 8 - Rom

WIZARD OF WOR GAMEBOARD
PC A084-90708-A961

CHIP NUMBER	FUNCTION
74LS04	Hex inverter
74LS30	8 input Nand
74LS74	Dual "D" Flip-Flop
74LS86	Quad 2 input exclusive or
74LS153	Dual 4 to 1 line multiplexer
74LS161	4 bit binary counter
74LS164	8 bit shift register
74LS174	Hex "D" Flip-Flop
74LS257	Quad 2 to 1 line multiplexer tri-state
74LS367	Hex bus driver-tri-state
0066-117XX (2720)	Custom I/O chip
LM358	OP-AMP
MC14099	8 bit addressable - latch -
MC14099	8 bit addressable latch - Cmos
MC14539	Dual 4 to 1 line multiplexer - Cmos
SC01	Voice sound generator

Z-80 CPU PIN DESCRIPTION

The Z-80 CPU is packaged in an industry standard 40 pin Dual In-Line Package. The I/O pins are shown in figure 3.0-1 and the function of each is described below.



Z-80 PIN CONFIGURATION
FIGURE 3.0-1

STRAPPING CHART

EXTRA BASES & SPACE ZAP

	JU1	JU2	JU3	JU4	JU5	JU6	JU7	JU8	JU9
Single +5 Volt 2716 EPROM	X			X		X		X	
2316E ROM		X		X		X		X	
2332 ROM		X			X		X	X	
2364 ROM			X		X		X		X

	JU10	JU11
UPRIGHT CABINET	X	
COCKTAIL		X

	JU12	JU13
U8, U9, U10 are 74LS08	X	
U8, U9, U10 are 74LS32		X

STRAPPING CHART GORF

ROM / RAM BOARD

DOMESTIC FOR ROMS

	1	2	3	4	5	6	7	8	9
X-31 X-32	CLOSED	OPEN	OPEN	OPEN	CLOSED	OPEN	CLOSED	CLOSED	OPEN
X-33	CLOSED	OPEN	CLOSED	OPEN	OPEN	CLOSED	CLOSED	OPEN	

DOMESTIC FOR PROMS

	1	2	3	4	5	6	7	8	9
X-31 X-32	CLOSED	OPEN	CLOSED	OPEN	OPEN	OPEN	CLOSED	CLOSED	OPEN
X-33	CLOSED	OPEN	CLOSED	OPEN	OPEN	CLOSED	CLOSED	OPEN	

FOREIGN ROMS

	1	2	3	4	5	6	7	8	9
X-31	CLOSED	OPEN	CLOSED	OPEN	OPEN	CLOSED	OPEN	CLOSED	OPEN
X-32	CLOSED	OPEN	OPEN	OPEN	CLOSED	CLOSED	OPEN	CLOSED	OPEN
X-33	CLOSED	OPEN	CLOSED	OPEN	OPEN	CLOSED	CLOSED	OPEN	

RAM/ROM BOARD

CUT JUMPER JU 20 FOR 74LS241 LOCATION U15
* CUT JUMPER JU 21 FOR 74LS244 LOCATION U15

CUT JUMPER JU 22 FOR 74LS32 LOCATIONS U2, U3, U4, U5
* CUT JUMPER JU 23 FOR 74LS08 LOCATIONS U2, U3, U4, U5

GORF GAME BOARD

CUT JUMPER JU 2 FOR VOCAL SOUND

JUMPER JU 1 IN FOR COCKTAIL
JUMPER JU 1 OUT FOR UPRIGHT

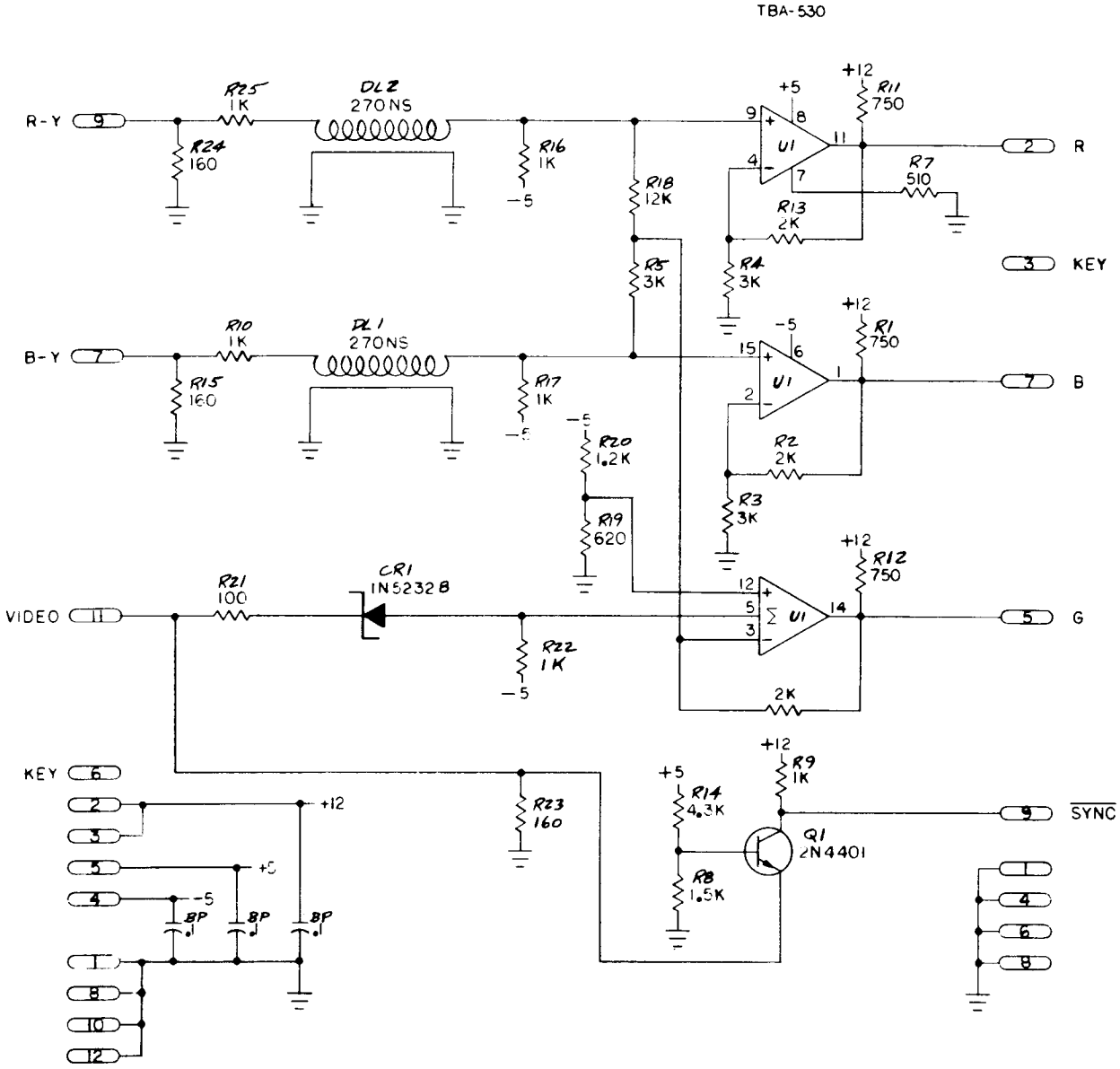
LOGIC TERMS Z-80 SYSTEM

ADD	Address
AUDIN	Audio In
BUSAK	Bus Acknowledge
BUSRO	Bus Request
BUZOFF	External Control
B-Y	Blue Minus Video
BYTE	Has Four Pixels
CE	Chip Select
CAS	Column Address Strobe
CASEN	CAS Enable
D-O	Data Out
D-1	Data In
DATEN	Data Enable
I or Q	Input-Output Request
HD	Horizontal Drive (63.5 us)
INT	Interrupt Request
I & O	Input - Output Signals
LTCHDA	Latch Data
LITE PEN	Interrupt Control
MD	Memory Data
MA	Memory Address
M1	Machine Cycle One
MREQ	Memory Request
MUXD	Multiplex Data
MC	Micro Cycle Control
MENEN	Memory Enable
NMI	Non Muskable Interrupt

OG	Phi-G Clock 1.7 MHZ
PX	Monitor Picture Clock 3.5 MNZ
POT	Control Potentionmeter
PIXEL	Smallest spot on color monitor screen with information
RAS	Row Address Strobe
RFSH	Refresh
RAMSEL	Ram Select
RD	Memory Read
R-Y	Red Minus Video
SYSEN	System Enable
SI	Signal In
SO	Signal Out
VD	Vertical Drive (16.6 MS)
VIDOT	Video Out
WE	Write
WRTCL	Write Control
WR	Memory Write

RESET	Normally high an active low resets the Z-80

R G B BOARD SCHEMATIC



M051-00873-A030

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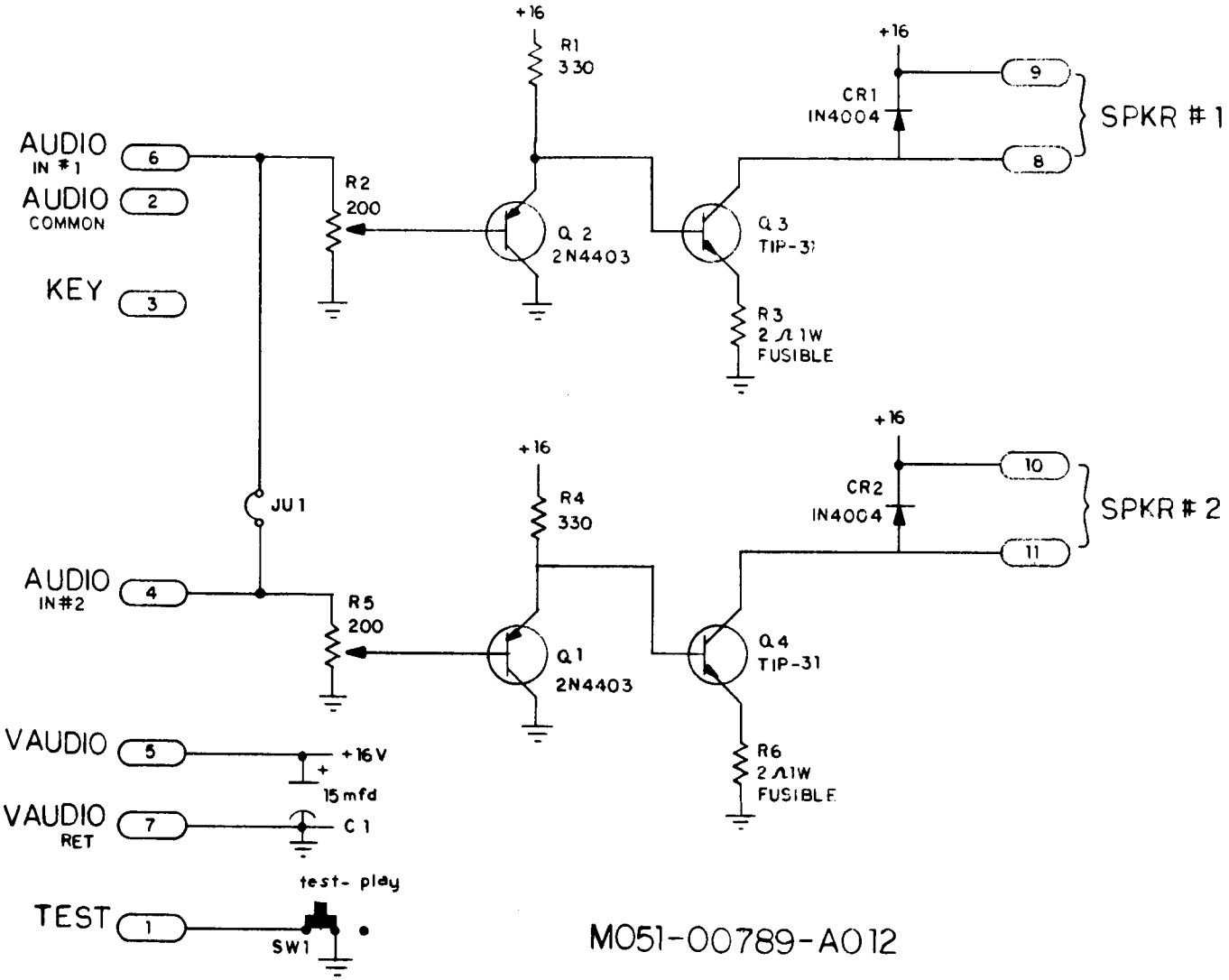
				FOR CCRS
RELEASED FOR PROD 9/26/80				NO A082-91363-A000

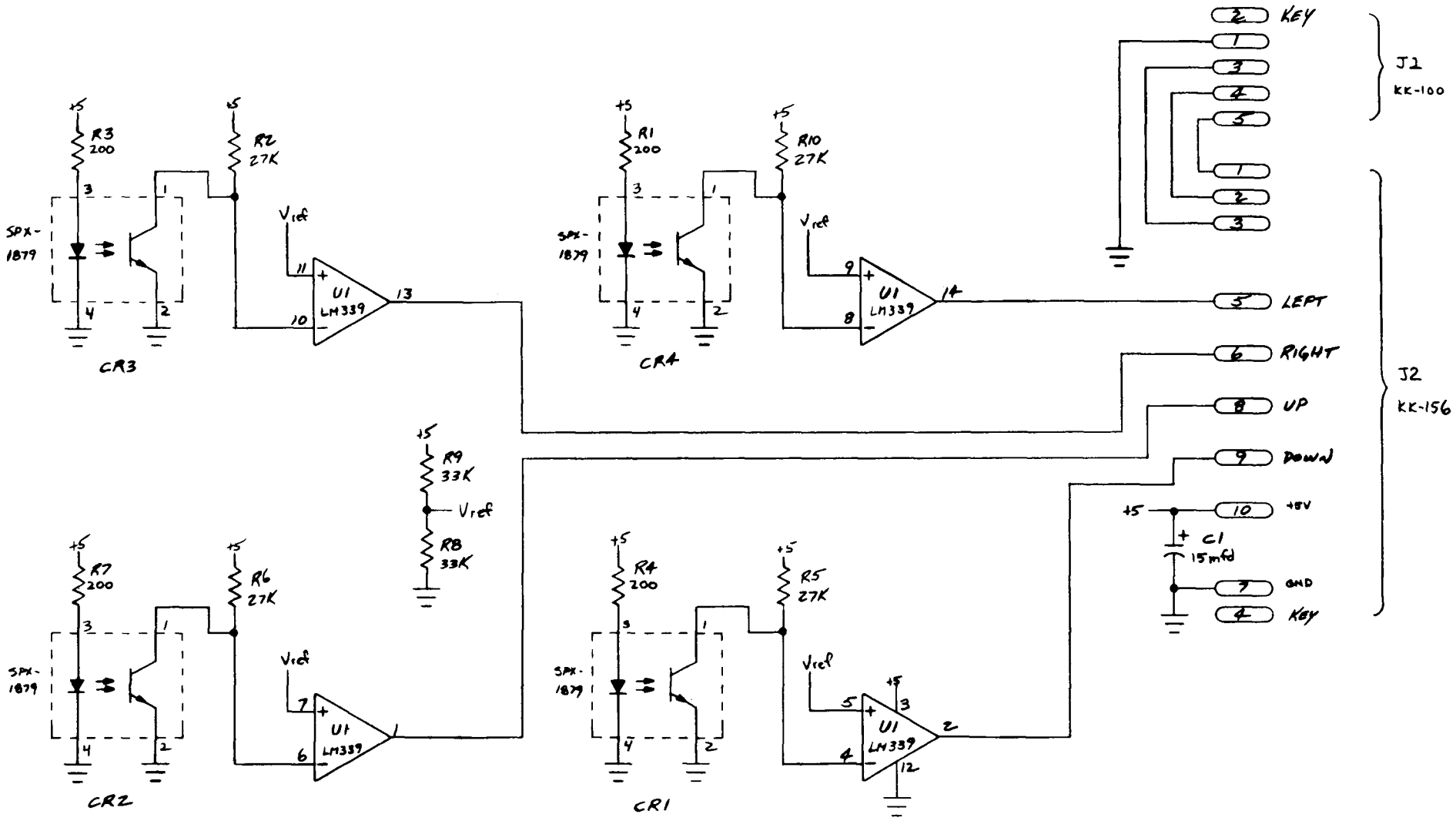


NOTE ✳

✳ FOR MONO 1/2 CIRCUIT SHOWN IS USED FOR DUEL MONO BOTH CIRCUITS ARE USED JUMPER JU1 IS USED FOR STERO BOTH CIRCUITS ARE USED JUMPER JU1 IS NOT USED

M051-00789-A012

AUDIO AMP BOARD	PART NO. A082-90903-A000



28A

M051-00873-A025 MIDWAY MFG. CO.

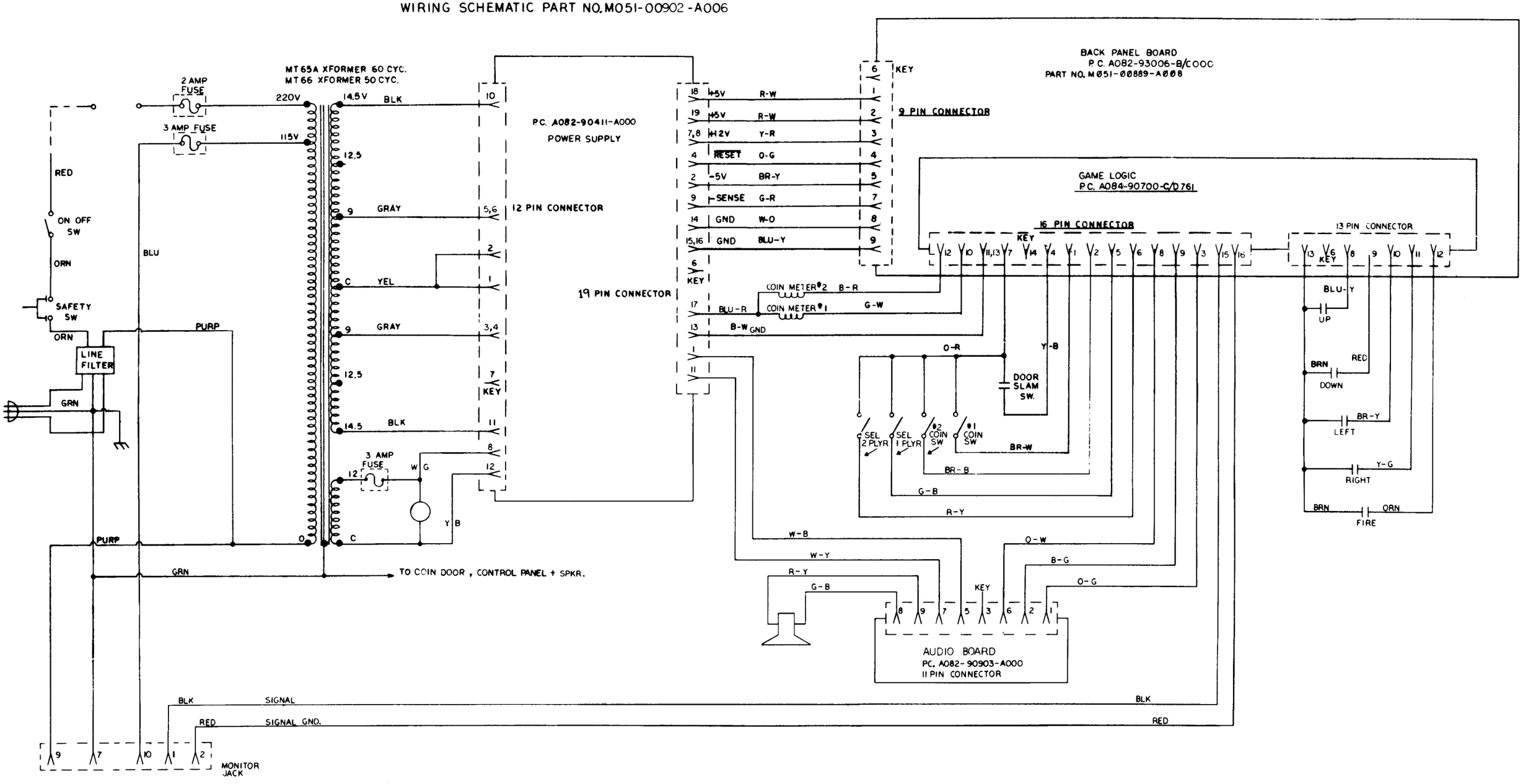
CONTROL GRIP PC ASSY

A082-91379-A000

"SPACE ZAP"

MIDWAY MFG. CO.
10750 W. GRAND AVE.
FRANKLIN PARK, IL. 60131

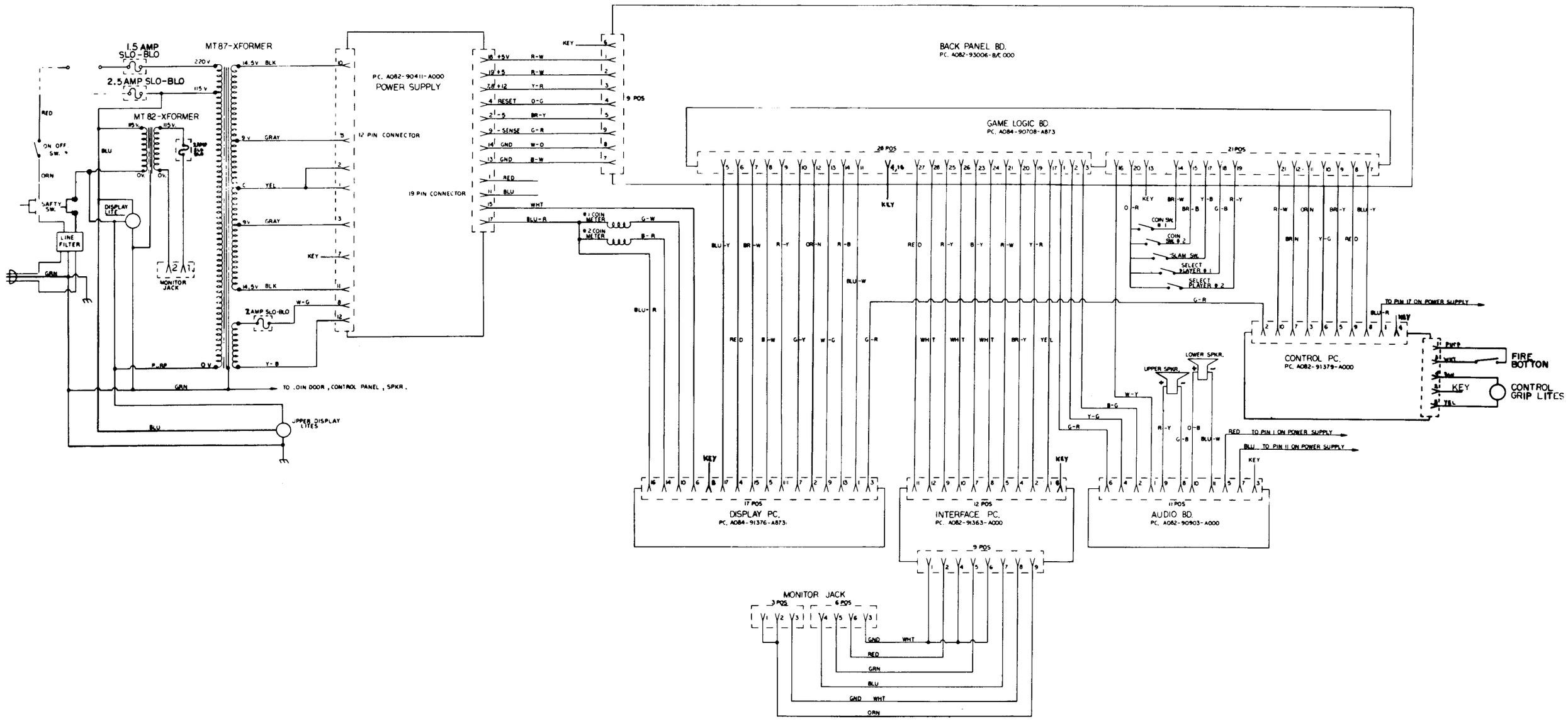
WIRING SCHEMATIC PART NO. M051-00902-A006



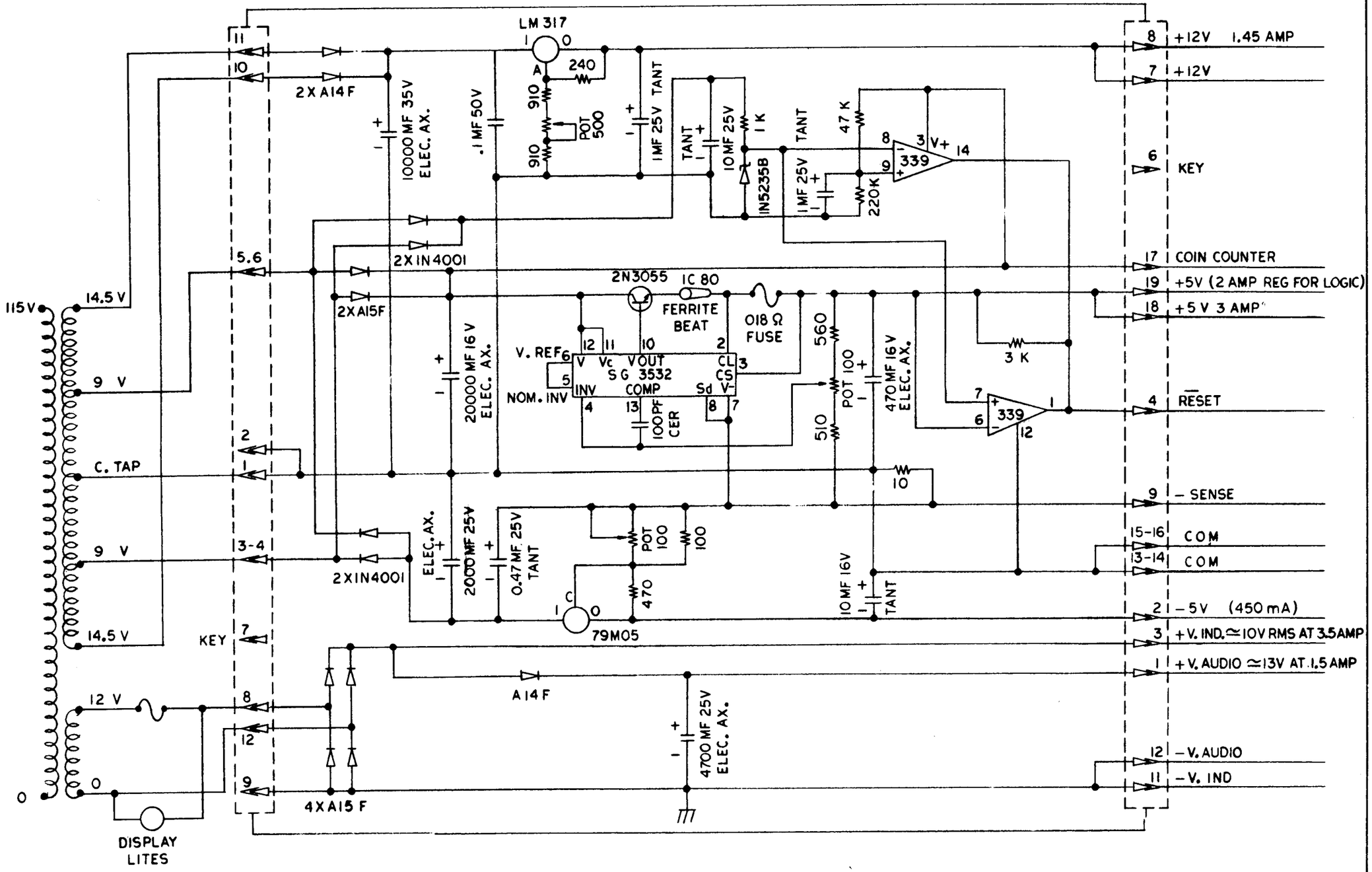
WIRING SCHEMATIC — GORF

GORF U.R.
MIDWAY MFG. CO.
10750 W. GRAND AVE.
FRANKLIN PARK, IL. 60131

WIRING SCHEMATIC # M051-00873-A037



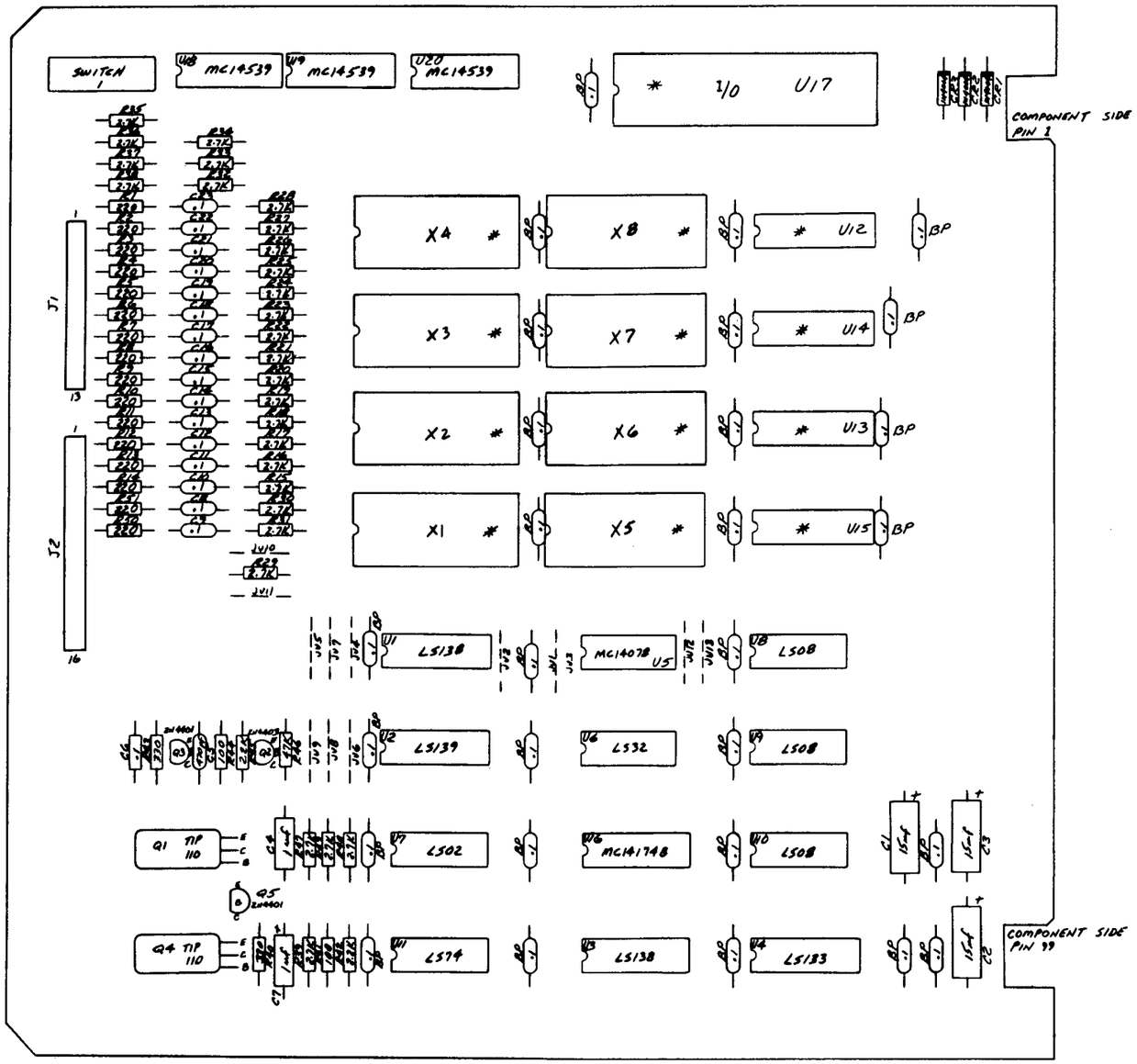
POWER SUPPLY SCHEMATIC



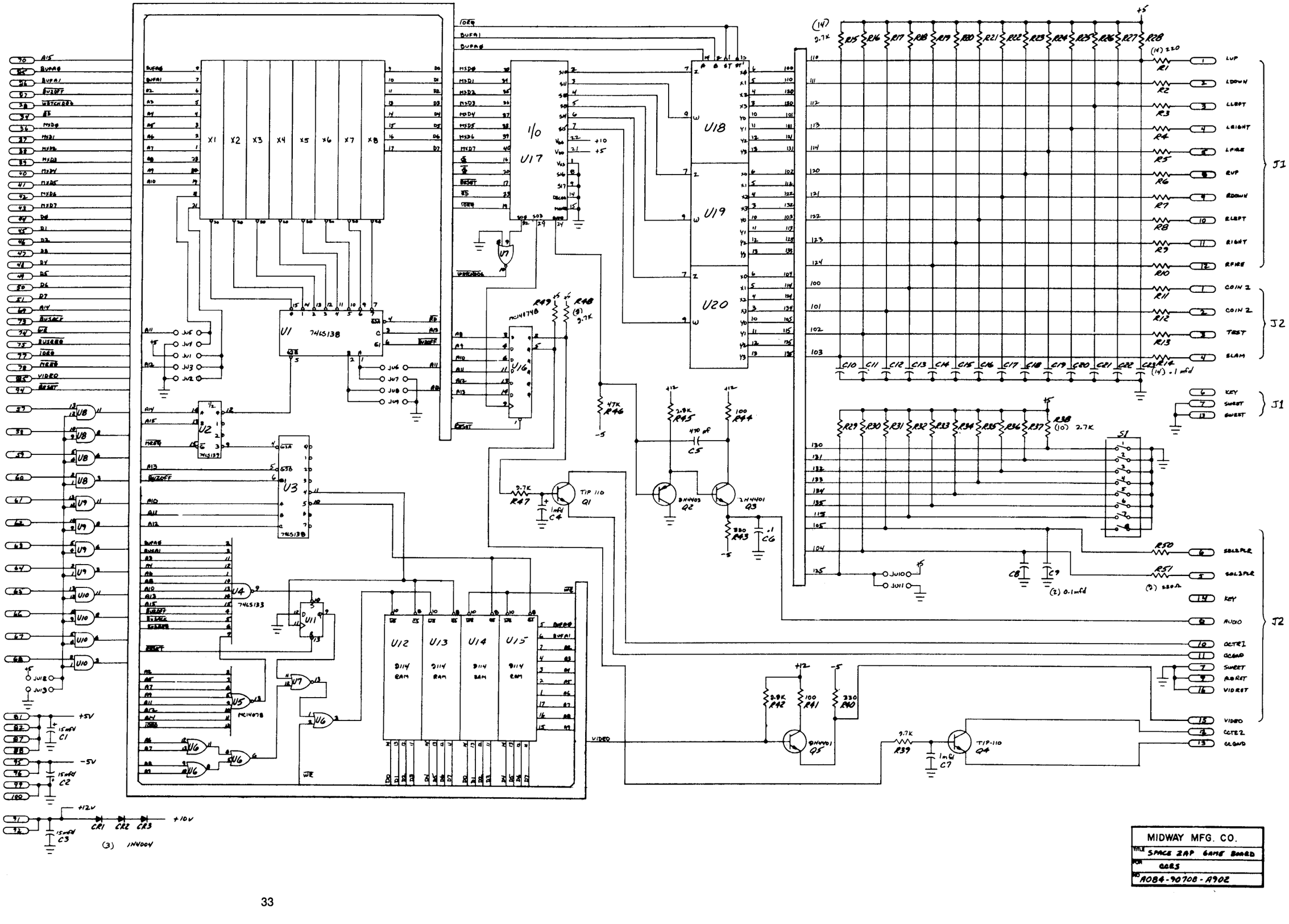
DRAWING NO. M051-00789-A011

COMMERCIAL CARD RACK PWR SPLY SCHEMATIC	A082-90411-A000

GAME BOARD LAYOUT — SPACE ZAP

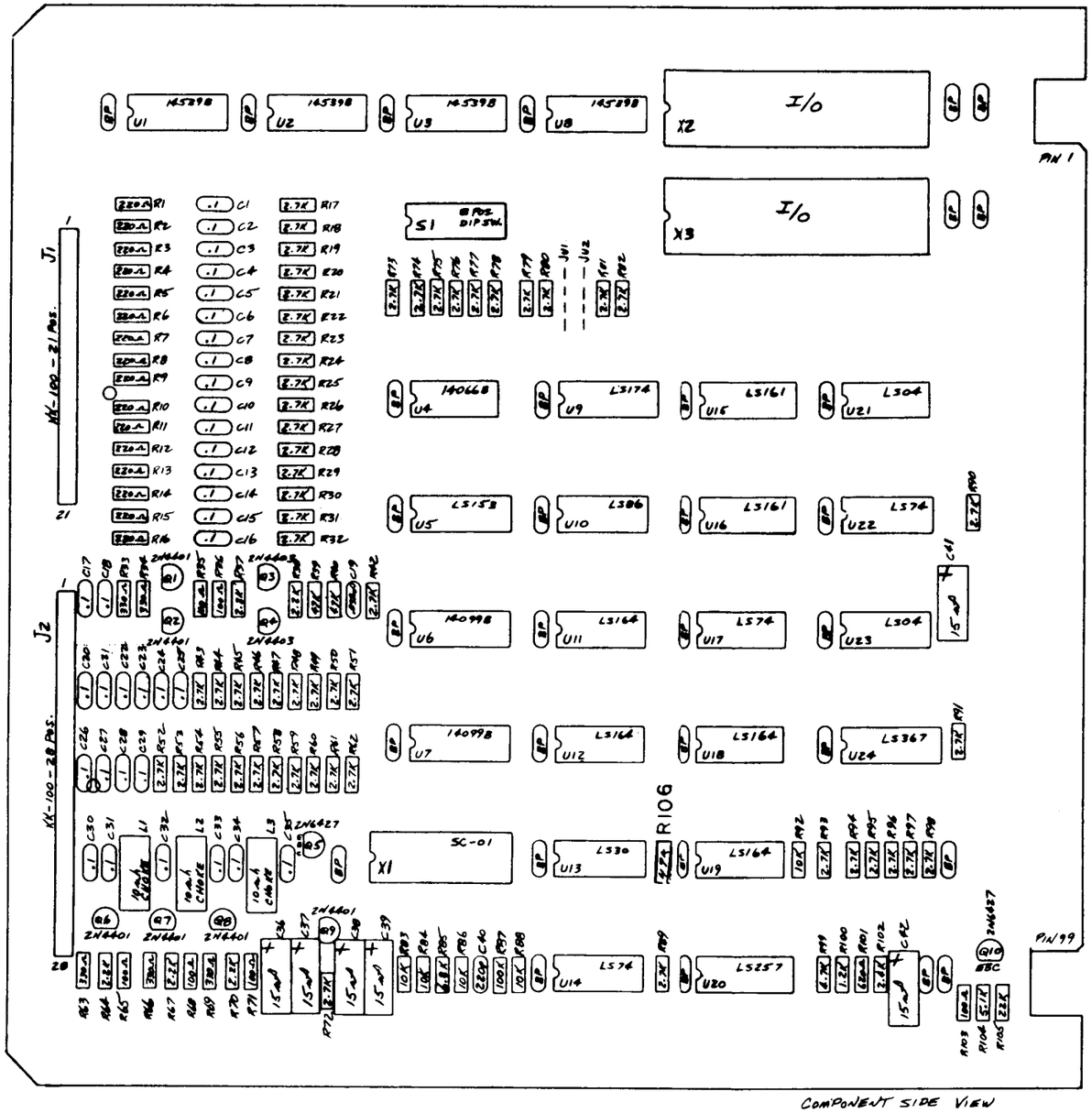


GAME BOARD SCHEMATIC — SPACE ZAP



MIDWAY MFG. CO.	
TITLE	SPACE ZAP GAME BOARD
FOR	GAME
NO	A084-90708-A902

GAME BOARD LAYOUT — GORF



M051-00873-C038

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B	11-7-80			
	10-10-80			

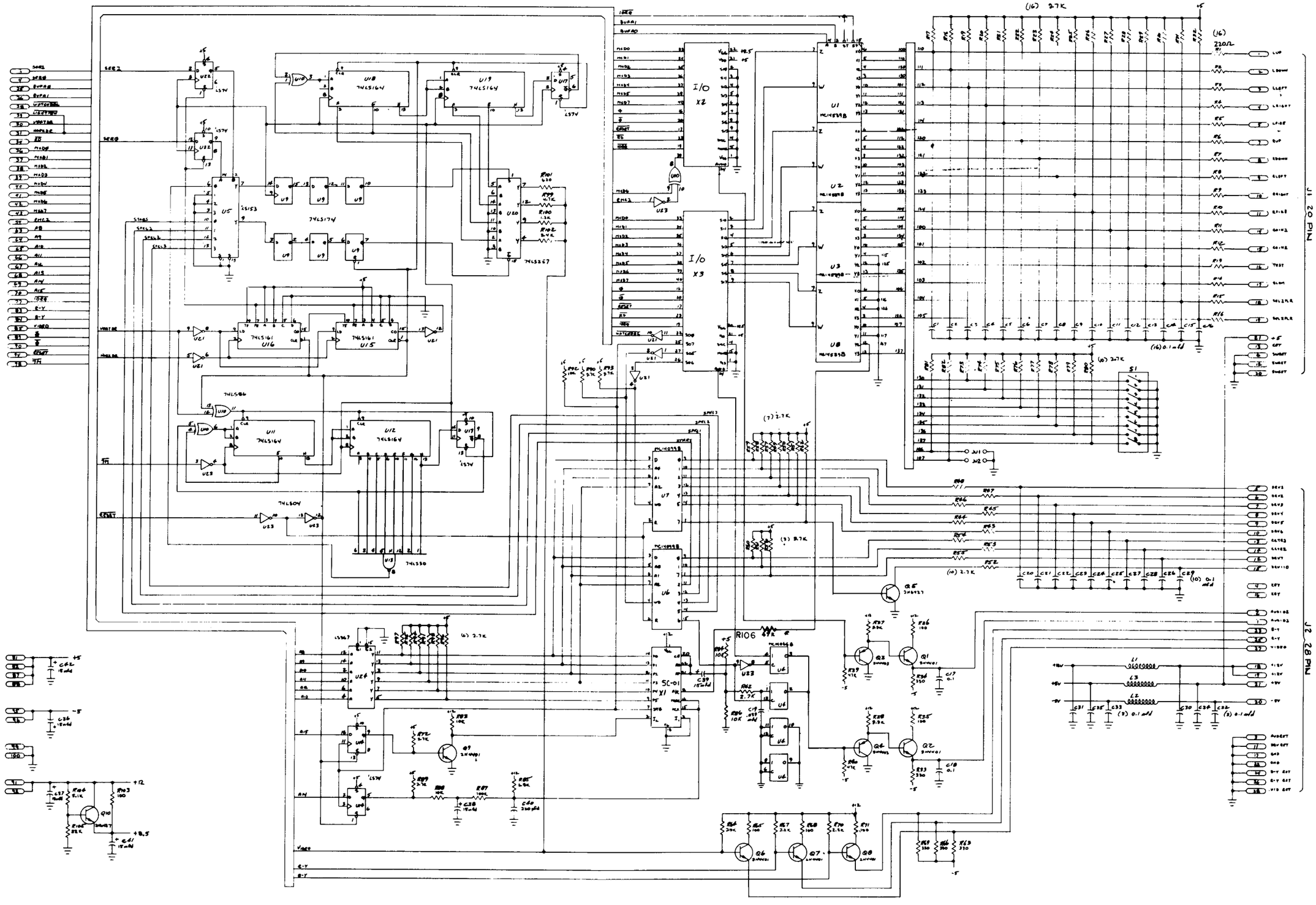
MIDWAY MFG. CO.

TITLE GORF GAME BD

FOR CCR

NO. A084-90708-C873

GAME BOARD SCHEMATIC — GORF

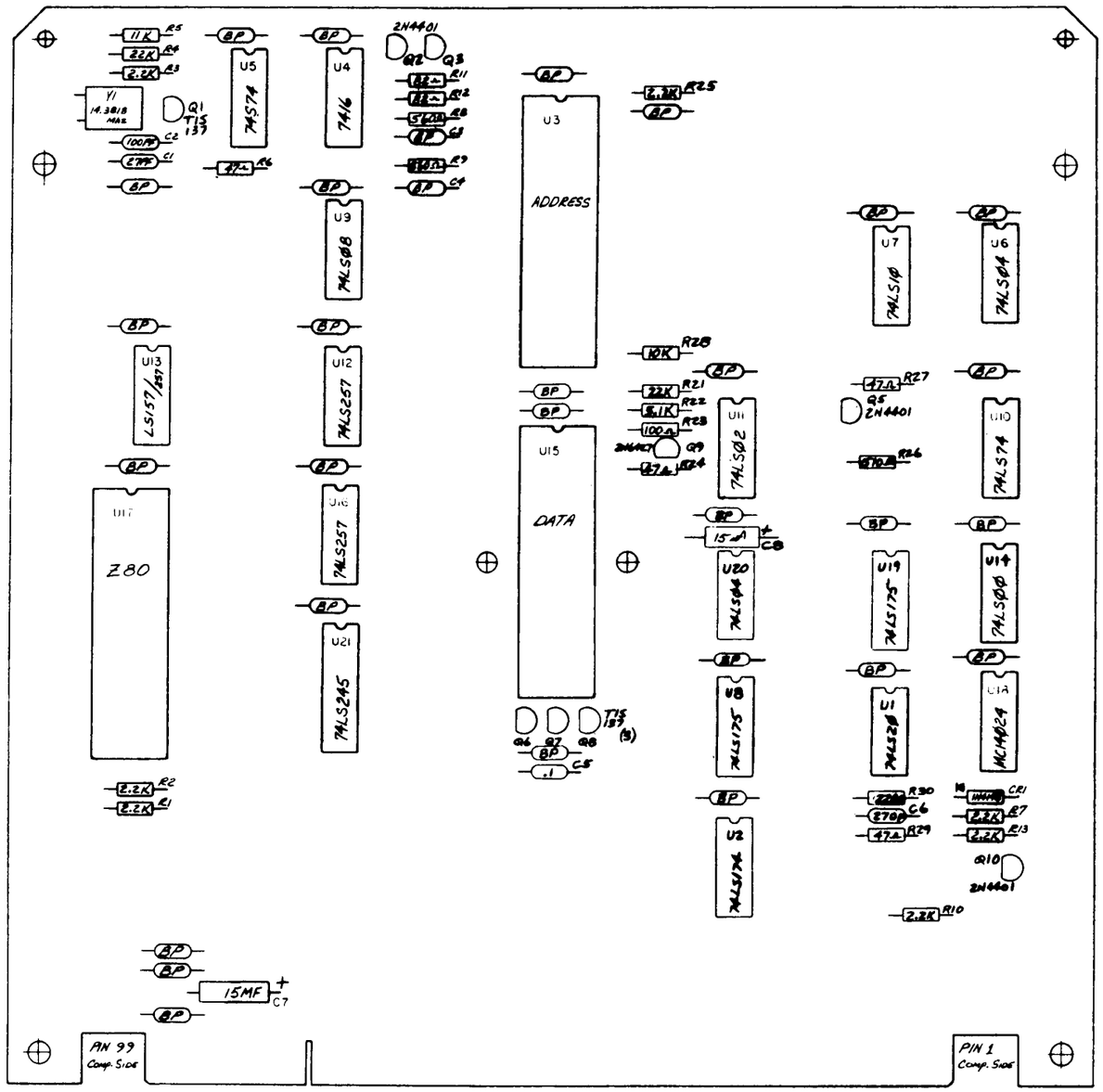


GORF GAME BOARD

A084-90708-C873

M051-00873-C024

CPU BOARD LAYOUT

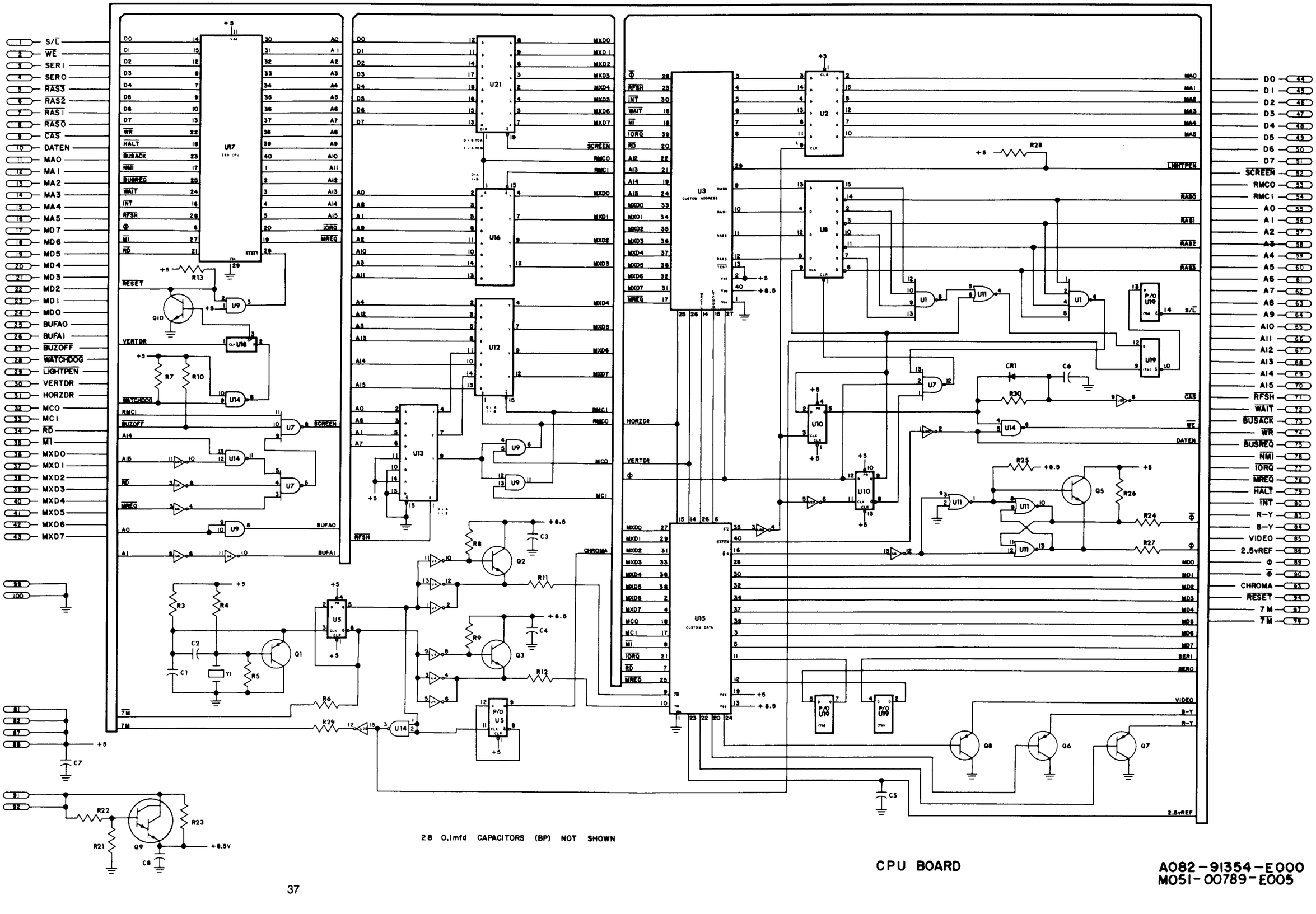


COMPONENT SIDE

M051-00789-A006

TITLE	CPU BOARD
DWN	C.V.M. CARD RACK
NO	A082-91354-E000

CPU BOARD SCHEMATIC

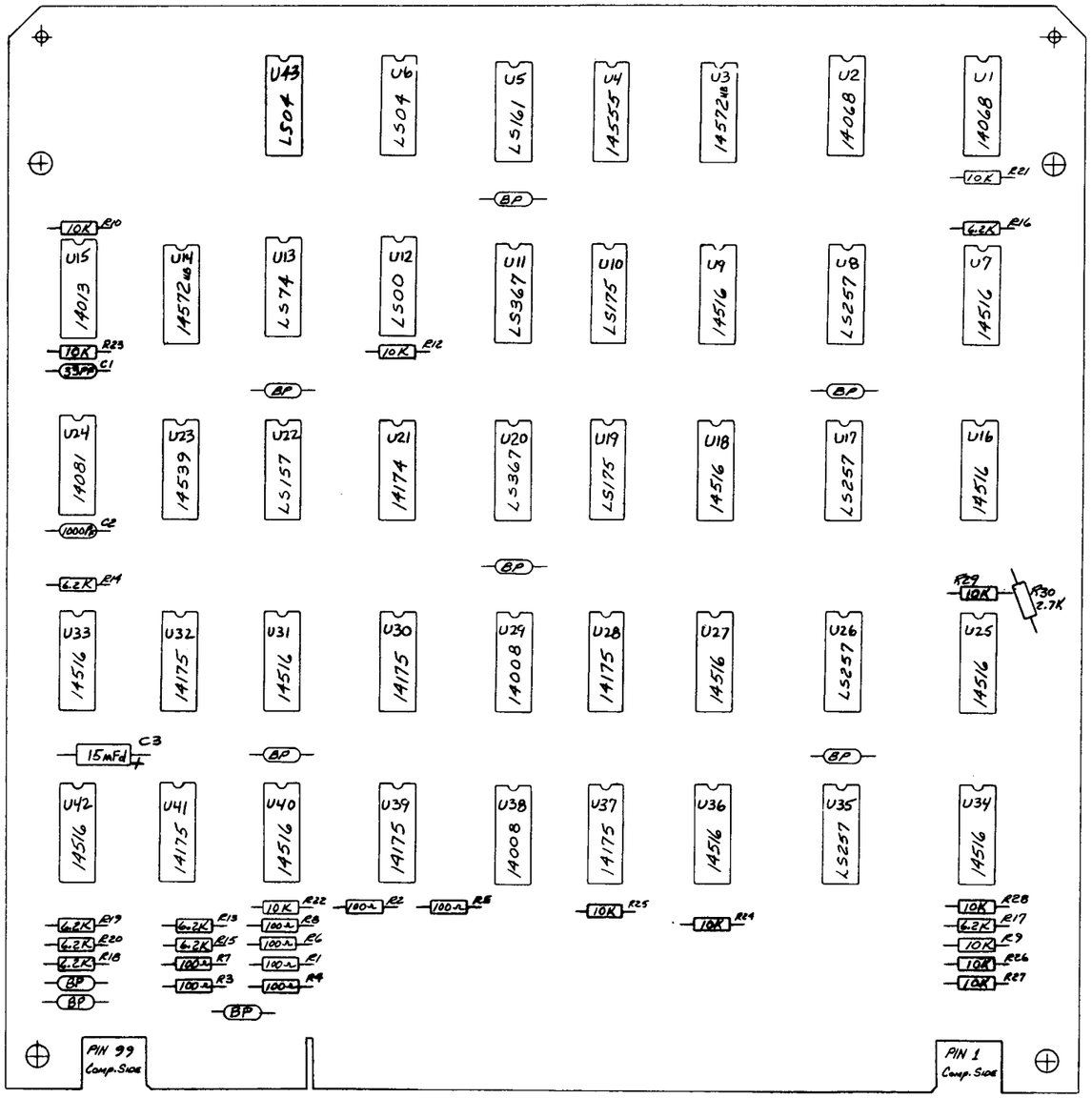


28 0.1mfd CAPACITORS (BP) NOT SHOWN

CPU BOARD

A082-91354-E000
M051-00789-E005

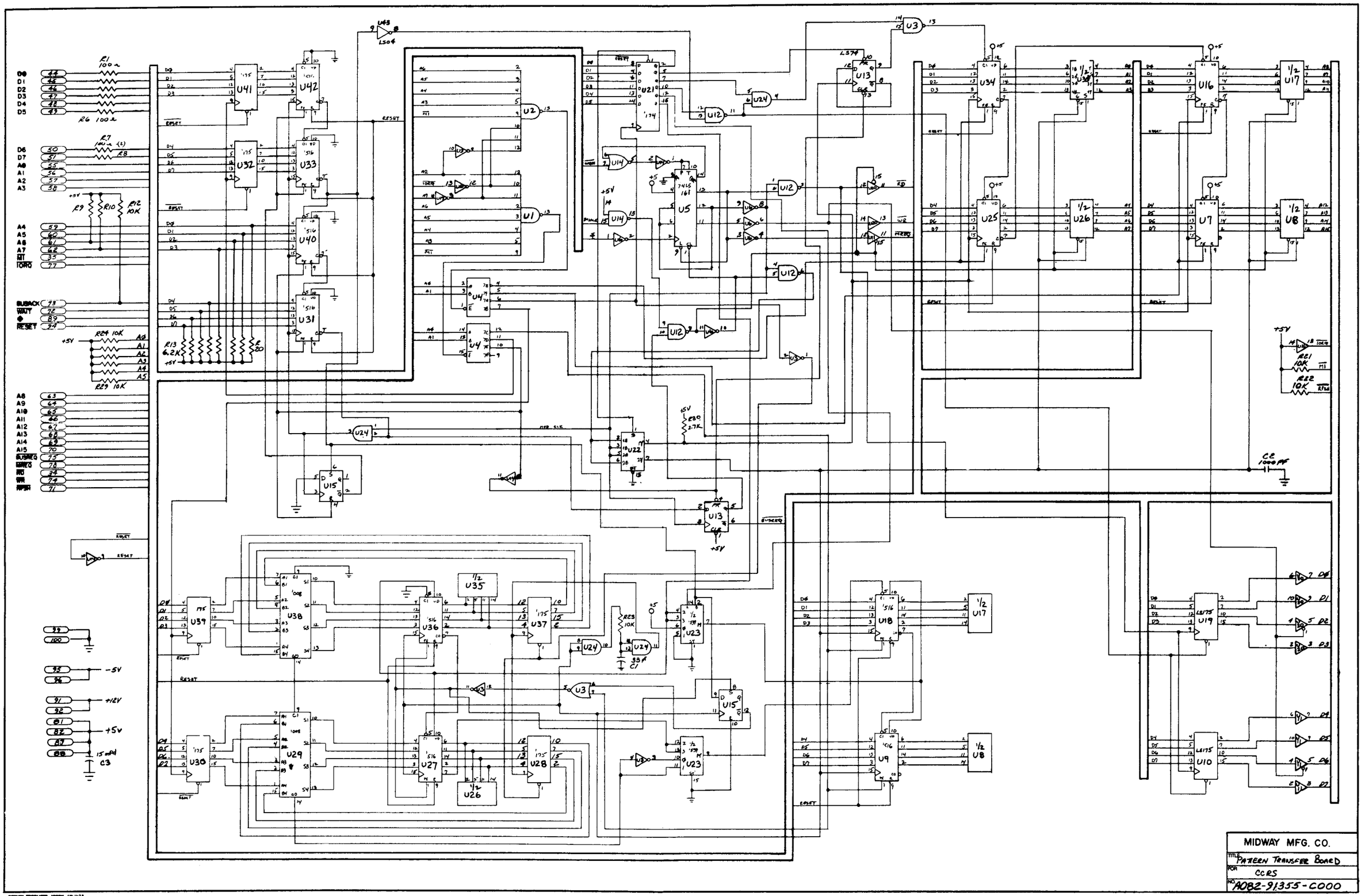
PATTERN BOARD LAYOUT



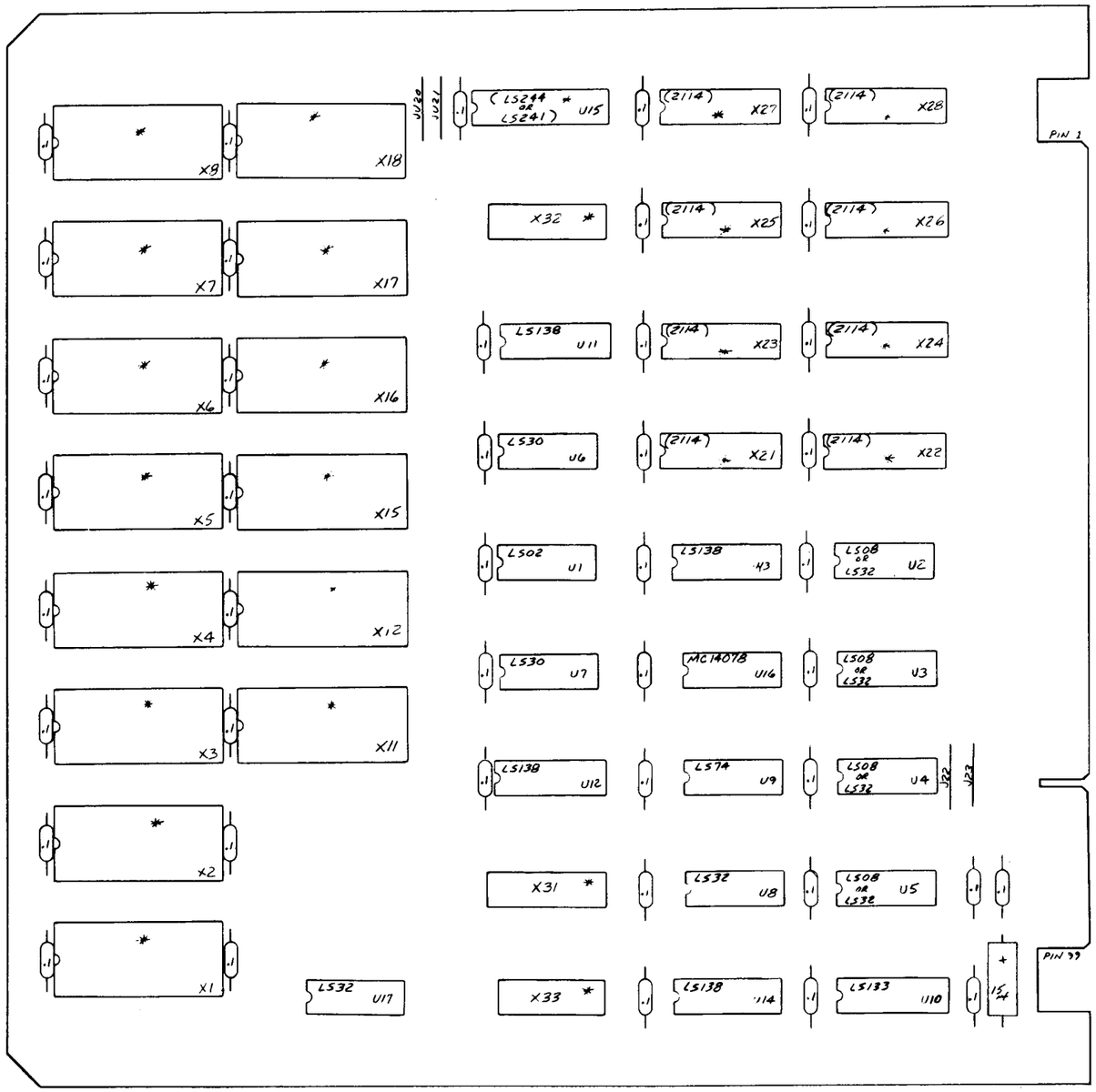
COMPONENT SIDE
A082-91355-C000
PATTERN BOARD
COMM. CARD RACK

MIDWAY MFG. CO.	
TITLE	PATTERN BOARD
FOR	COMM. CARD RACK
NO.	A082-91355-C000

PATTERN BOARD SCHEMATIC



RAM/ROM BOARD LAYOUT — FOREIGN



COMPONENT SIDE

* - DENOTES WHICH POSITION RECIEVES I.C. SOCKET.

M051-00873-A031

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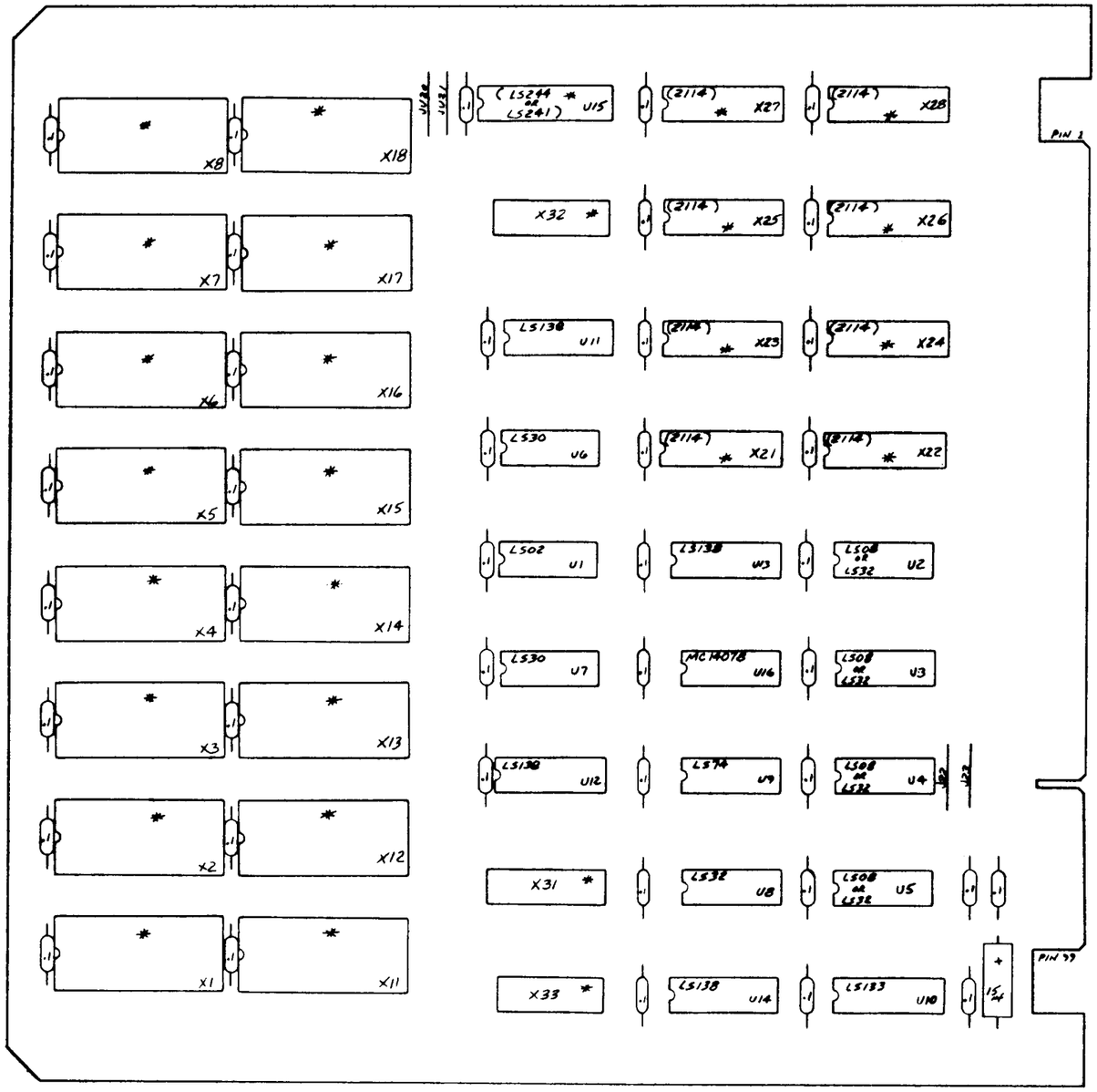
	TOLERANCES .XX ± .01 .XXX ± .005 ANGULAR ±			FOR
PROD RELEASE 10/10/80				NO. A082 - 91374-A000

FOREIGN

RAM/ROM BOARD LAYOUT — DOMESTIC



COMPONENT SIDE

* - DENOTES WHICH POSITION RECIEVES I.C. SOCKET.

M051-00873-A032

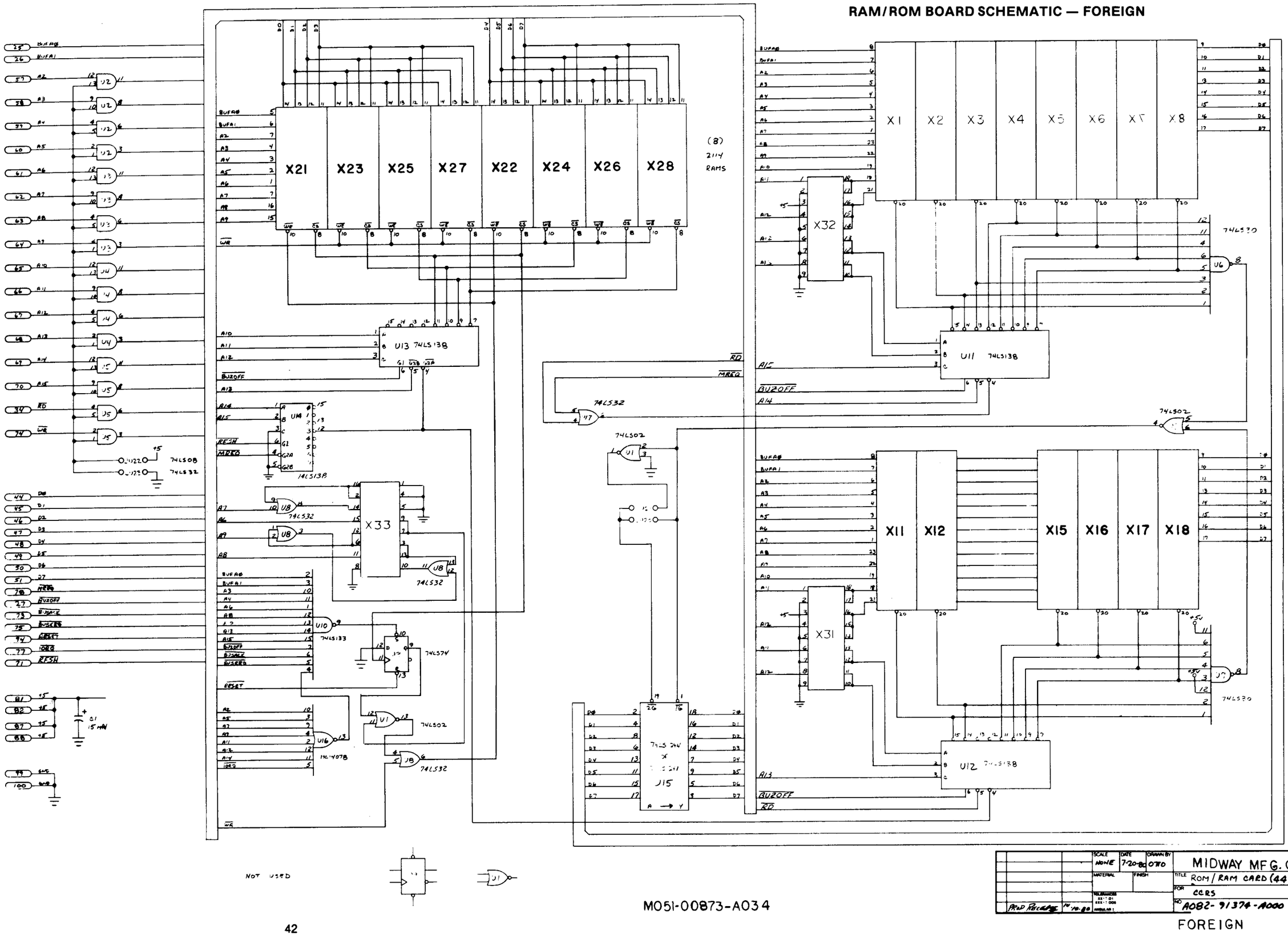
MIDWAY MFG. CO.

Rom/Ram Board

A082-91364-A000

DOMESTIC

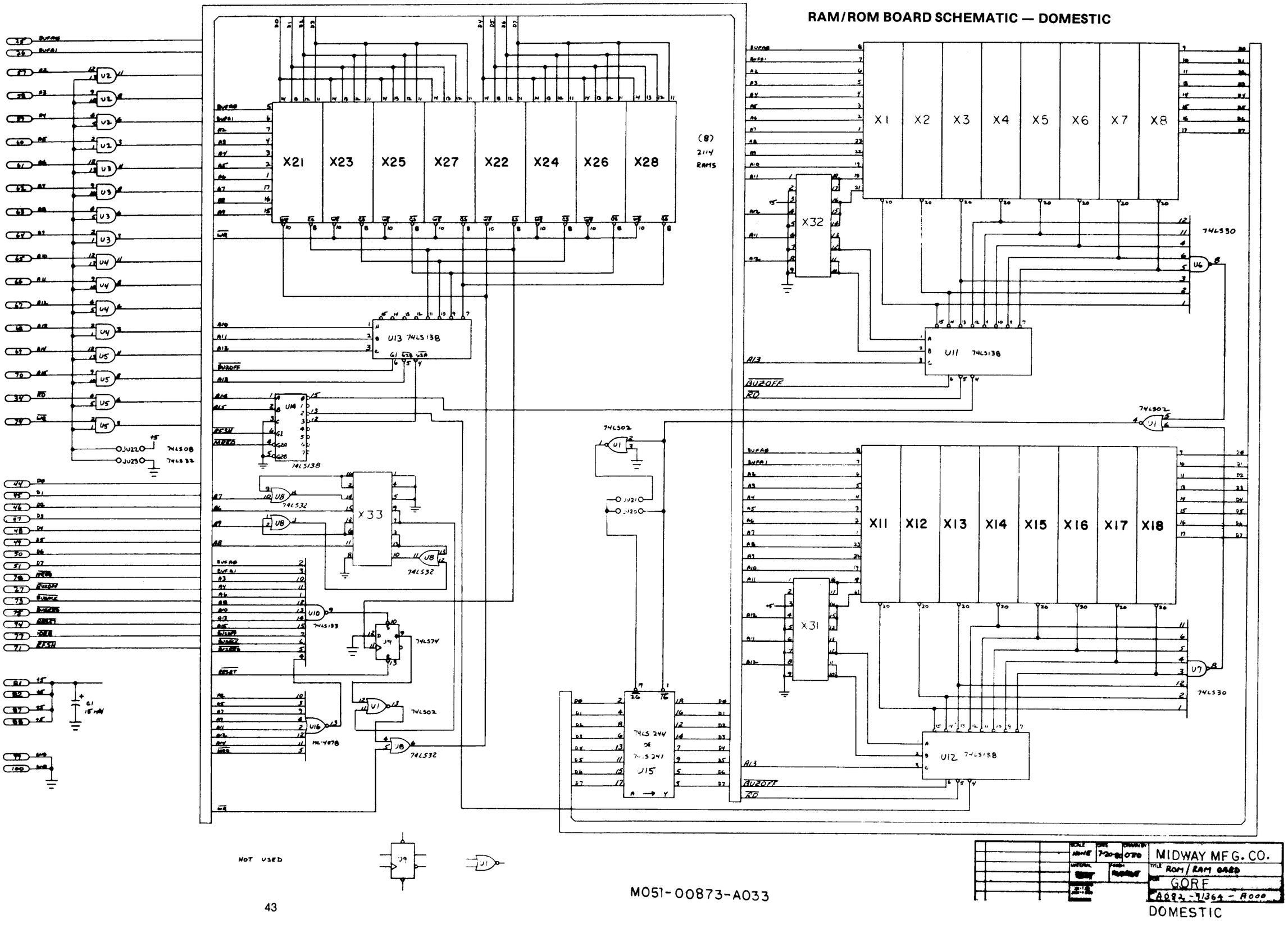
RAM/ROM BOARD SCHEMATIC — FOREIGN



NOT USED

M051-00873-A034

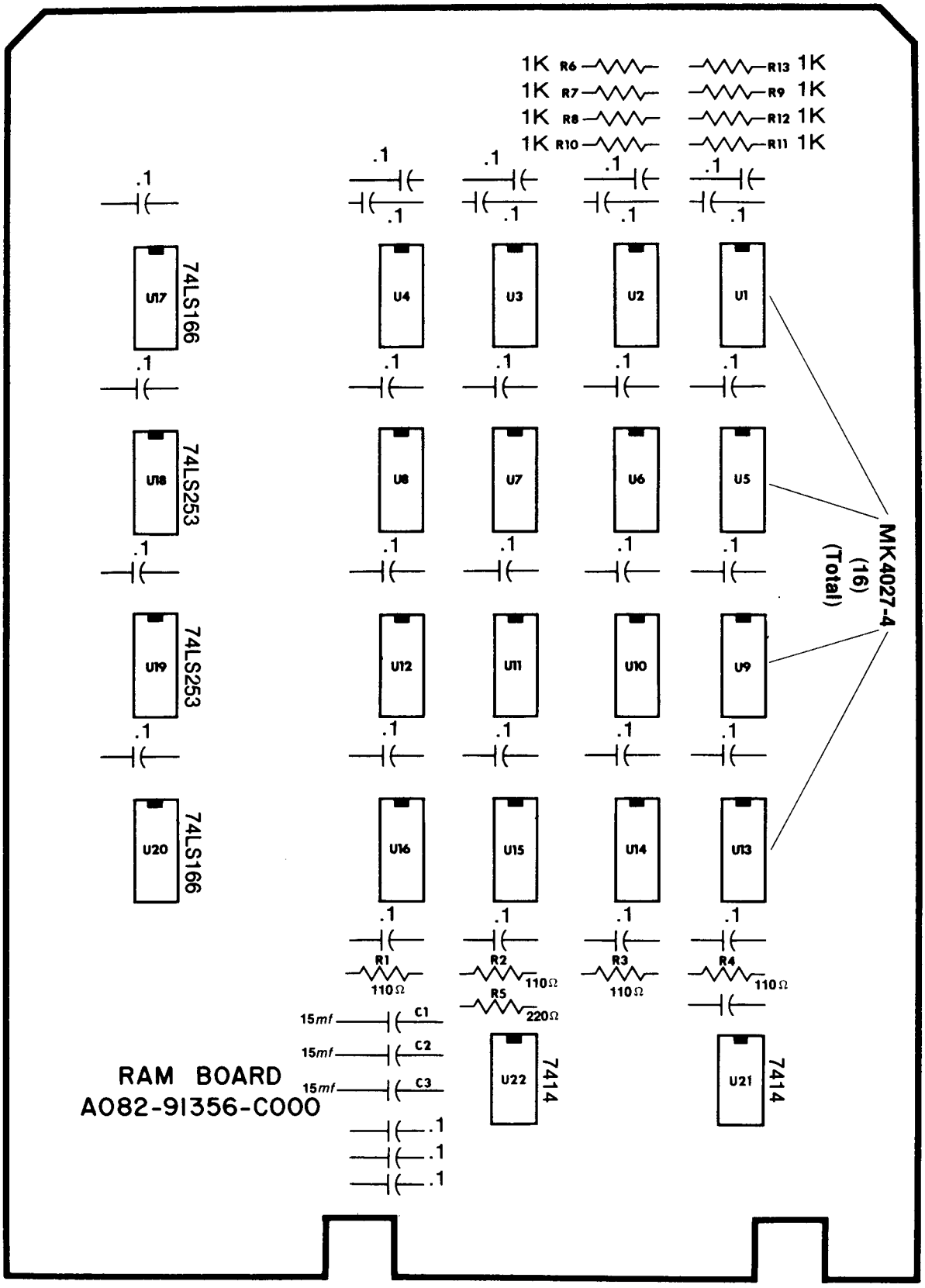
RAM/ROM BOARD SCHEMATIC — DOMESTIC



MIDWAY MFG. CO.
TITLE ROM/RAM CARD
GORF
A082-91364-A000
DOMESTIC

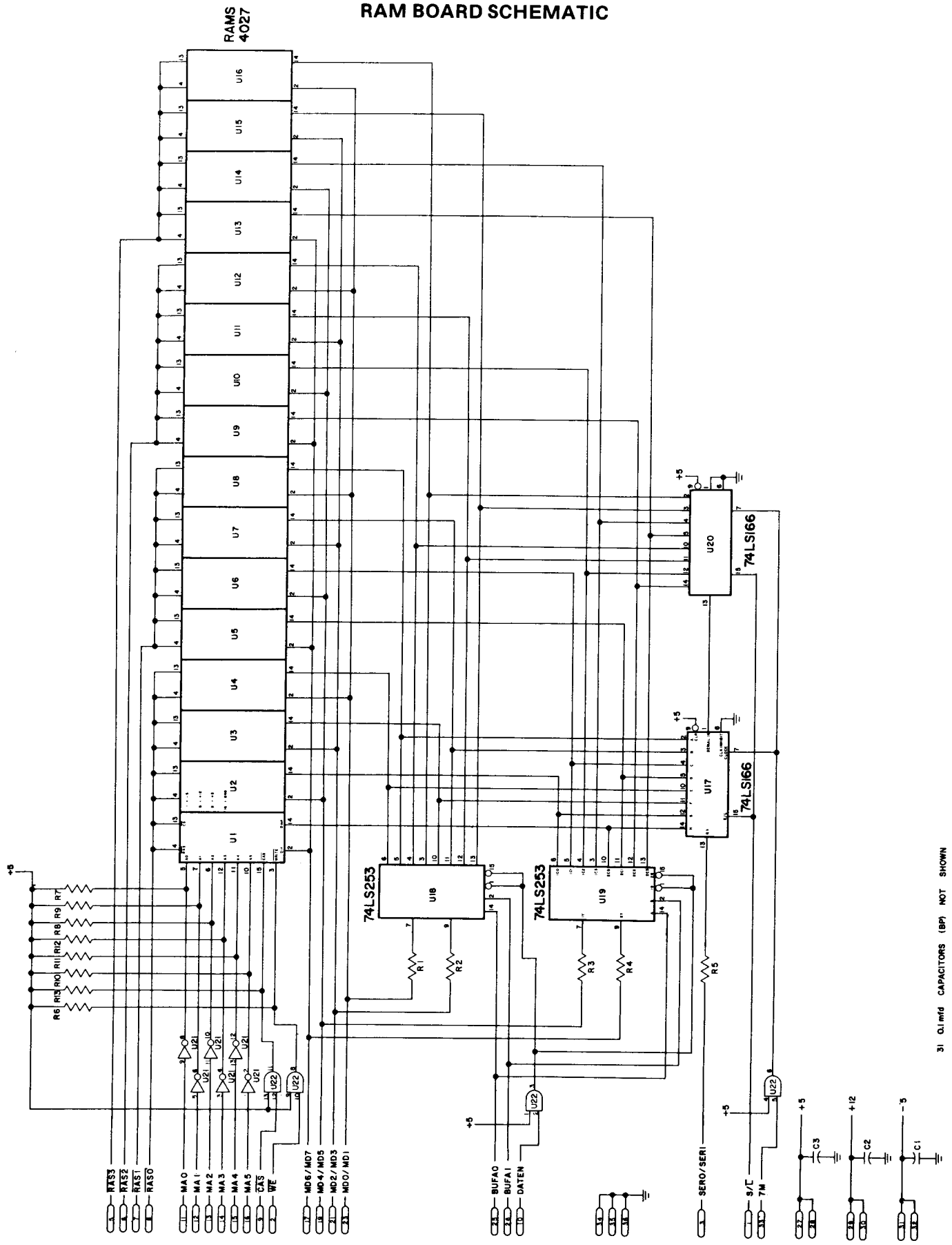
M051-00873-A033

RAM BOARD LAYOUT



COMPONENT PART NO. M051-00789-C003

RAM BOARD SCHEMATIC



RAM BOARD

SCHEMATIC PART NO. M051-00789-A002

A082-91356-C000

SERVICE BULLETIN

GAME: GORF

SUBJECT: NEW 6 CARD Z-80 SYSTEM USING A CARD RACK

GAME CARD (PC A082-90708-A873)
- I & O CUSTOM CHIP (TWO)
- TALKING CHIP - SC-01

ROM & RAM CARD (A082-91364-A000)
- DOMESTIC & FOREIGH (A082-91374-A000)
- RAMS 2114
- ROMS 9316 OR 9332

CPU CARD (A082-91354-E000)
- Z80 CPU
- ADDRESS CUSTOM CHIP
- DATA CUSTOM CHIP
- CRYSTAL 14,318

RAM CARD (A082-91356-0000)
- TWO RAM CARDS
- 16 RAM EACH (M4027)

PATTERN CARD (PC 082-91355C000)
- SHIFTS INFORMATION AT A FASTER RATE

POWER SUPPLY (PC 082-90411-A000)
- SAME AS SPACE ZAP

NOTE: ALL PC CARDS EDGE CONNECTORS ARE GOLD PLATED.

ANDY DUCAY
SERVICE MANAGER

SERVICE BULLETIN

GAME: SPACE ZAP, GORF & WIZARD OF WOR

SUBJECT: Custom chip identification (I/O, Address, and Data)

The following numbers will identify the special custom chip used in Space Zap mother board (PC 084-900002-B625).

I / O. . . . . 2720 or 0066-117XX

Address. . . . . 2719 or 0066-115XX

Data. . . . . 2721 or 0066-116XX or 2860

SERVICE BULLETIN

November 19, 1980

GAME: SPACE ZAP, GORF & WIZARD OF WOR

SUBJECT: Card Rack System Test Equipment

To aid board repair the following test cards are available

1. A Ram Test Card to locate a bad Ram. A082-91516-A000

2. A Card Rack Test Card which is used with the Ram Test Card and will also test the pattern card. A082-91517-A000

3. Order test cards from the Midway's Parts Department.

Andy Ducay
Service Manager

AD/dc

SERVICE BULLETIN
INTERFACING DYNAMIC 4027 RAMS TO THE Z80

Sixteen-pin dynamic RAM's are increasingly being used as the memory component for data storage in microprocessor - based systems. Their popularity over static and 18 or 22-pin dynamic RAM's has been the result of a maturing memory technology and the characteristics of the devices themselves. Their main features are low cost/bit and high bit density; additional features include a low standby power mode, TTL-compatible inputs and outputs and system-upgrading expansion capability. Replacing the chip-select pin on the 4K device with an additional address line effectively quadruples memory capacity to 16K bits. It is now possible, for example, to assemble a full 65K-byte memory system on a single printed-circuit board in an area of less than 50 sq. in.

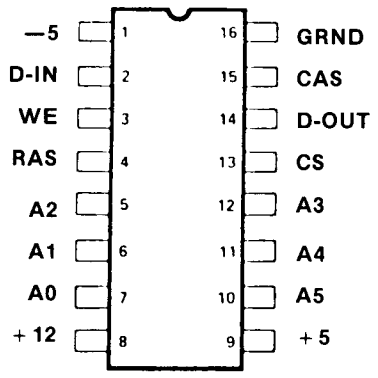
Now however, the system designer must be concerned with the interface requirements of 16-pin dynamic RAMs. The characteristics of this memory element require that refreshing of the memory be performed at periodic intervals in order to retain the stored data. This, coupled with the requirement for multiplexing address lines, has been the main drawback to their use. A typical interface requires approximately 12 to 20 standard TTL devices and includes timing generators, decode logic, multiplexer circuitry, refresh logic and buffers.

The Zilog Z80A microprocessor is designed to simplify this interface with built-in refresh logic, which allows totally transparent RAM refresh without the need for a refresh counter or it's associated multiplexer.

16-PIN DYNAMIC RAM ADDRESSING

Each cell of a dynamic RAM array is arranged in a matrix. Selection of a unique bit location within this matrix in a 4 K RAM requires 12 address lines, while a 16 K RAM requires 14. For a 16-pin RAM to accommodate these lines, it must divide them into two groups - row addresses and column addresses (six each for the 4K RAM and seven each for the 15K RAM).

Each group is applied to the RAM on the same input lines through an external multiplexer and is latched into the chip by applying two clock strobes in succession. The first clock, the row-address strobe (RAS), latches the row address bits (A-0 to A-5 for 4K, A-0 to A-6 for 16K) into the RAM. The second clock, the column address bits (A-6 to A-11 for 4K, A-7 to A-11 for 16K) into the RAM.

Each cell therefore is uniquely addressed by row and column. When RAS goes active, all of the cells in the selected row respond (there are 64 rows in the 4K RAM matrix and 128 rows in the 16K RAM matrix) and are grated to sense amplifiers where the logic level of each cell is discriminated, latches and rewritten. CAS activates a column in the matrix (there are 64 columns in the 4K RAM matrix and 128 columns in the 16K RAM matrix) that uniquely identifies the cell in the row output and yields the required bit to the output buffer.

PIN CONFIGURATION
4027