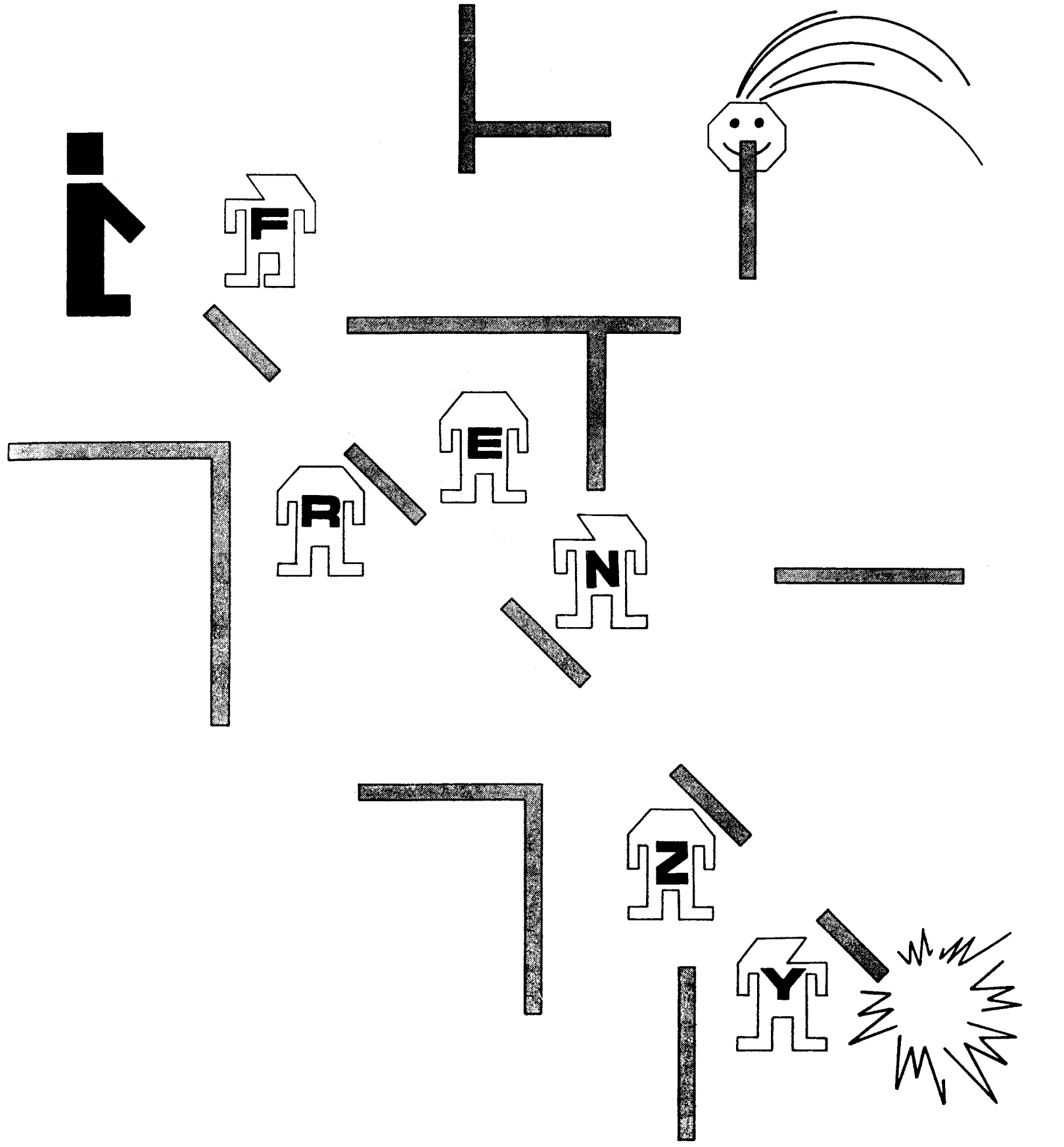

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ELECTRONICS, INC.
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1.1 INTRODUCTION

This game has been STERN final tested and is ready to play, but on all games there are some items that must be checked first after shipment. Making these visual inspections may avoid time consuming service work later. Minor troubles caused by abusive handling in shipment are unavoidable, such as cable connectors that may have been loosened. Check ALL CONNECTORS on the game to make sure they are firmly seated. Examine the exterior of the game cabinet for dents, chips or broken parts. Check all major subassemblies, control panel and T.V. monitor to make sure that they have not loosened up during shipment.

1.2 VISUAL INSPECTION BEFORE PLUGGING IN LINE CORD

1. Check that the primary wiring of the transformer corresponds to the location voltage (See Figure E).
2. Check the transformer for any foreign material shorting across wiring lugs.
3. Check that fuses are firmly seated and making good contact.
4. Check the T.V. for any foreign material that could cause shorts (VISUAL INSPECTION ONLY).
5. Check game boards for any foreign material that could cause shorts. Make sure all circuit boards are connected properly.

1.3 ON/OFF POWER INTERLOCK SWITCHES

1. The on/off power switch is located on the top right side 12" from the front.
2. There are two interlock main power switches, one by the front door (See Figure A) and one on the back access panel (See Figure B).
3. Interlock switches interrupt all power from game except service outlet and flourescent lights for Marquee. Interlock switches can be locked in "ON" position by pulling stem out when servicing game.

1.4 GENERAL INFORMATION

1. On the front door there is a bookkeeping switch (See Figure A). Depressing this switch will step through bookkeeping functions one at a time for each time switch is pressed. Pressing fire button will clear whatever bookkeeping function you are in. (See Page 14 for bookkeeping function).
2. There are two coin chutes on the front door. They can be adjusted to work separately. (See Page 13).
3. Game adjustment switches are located on ZPU board. (See Pages 10, 12 & 13 for adjustments and location).
4. Volume control for electronic sound is located inside the front door on right side. (See Figure B).
5. Power supply has an adjustment for the +5 VDC regulator, this MUST BE SET BETWEEN +5.0 VDC and +5.25 VDC as measured at TP4, VSU-1000. (See Figure D for test points on power supply and adjustment pot).

FRENZY

FRONT CABINET

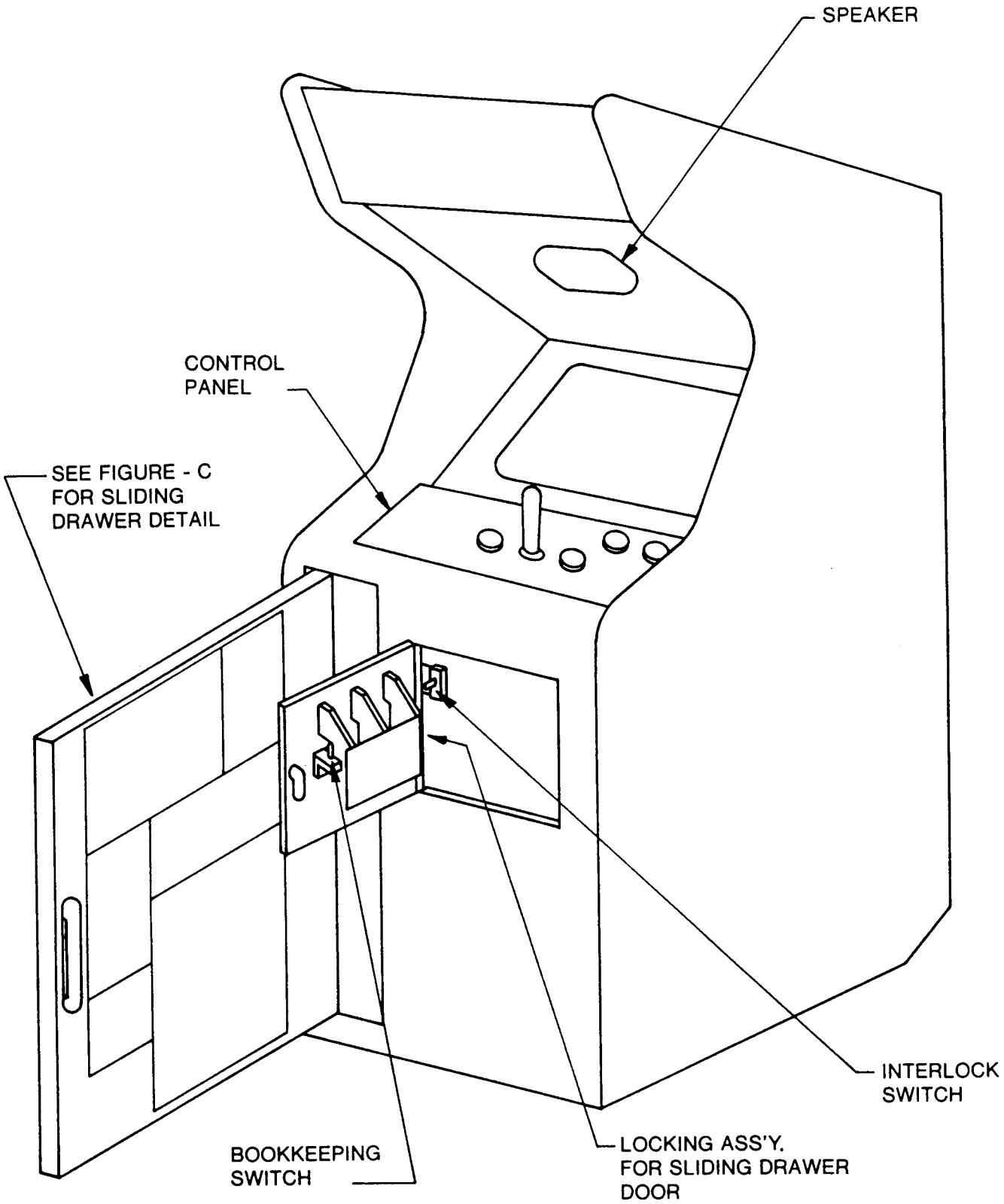


FIGURE - B

FRENZY

REAR CABINET

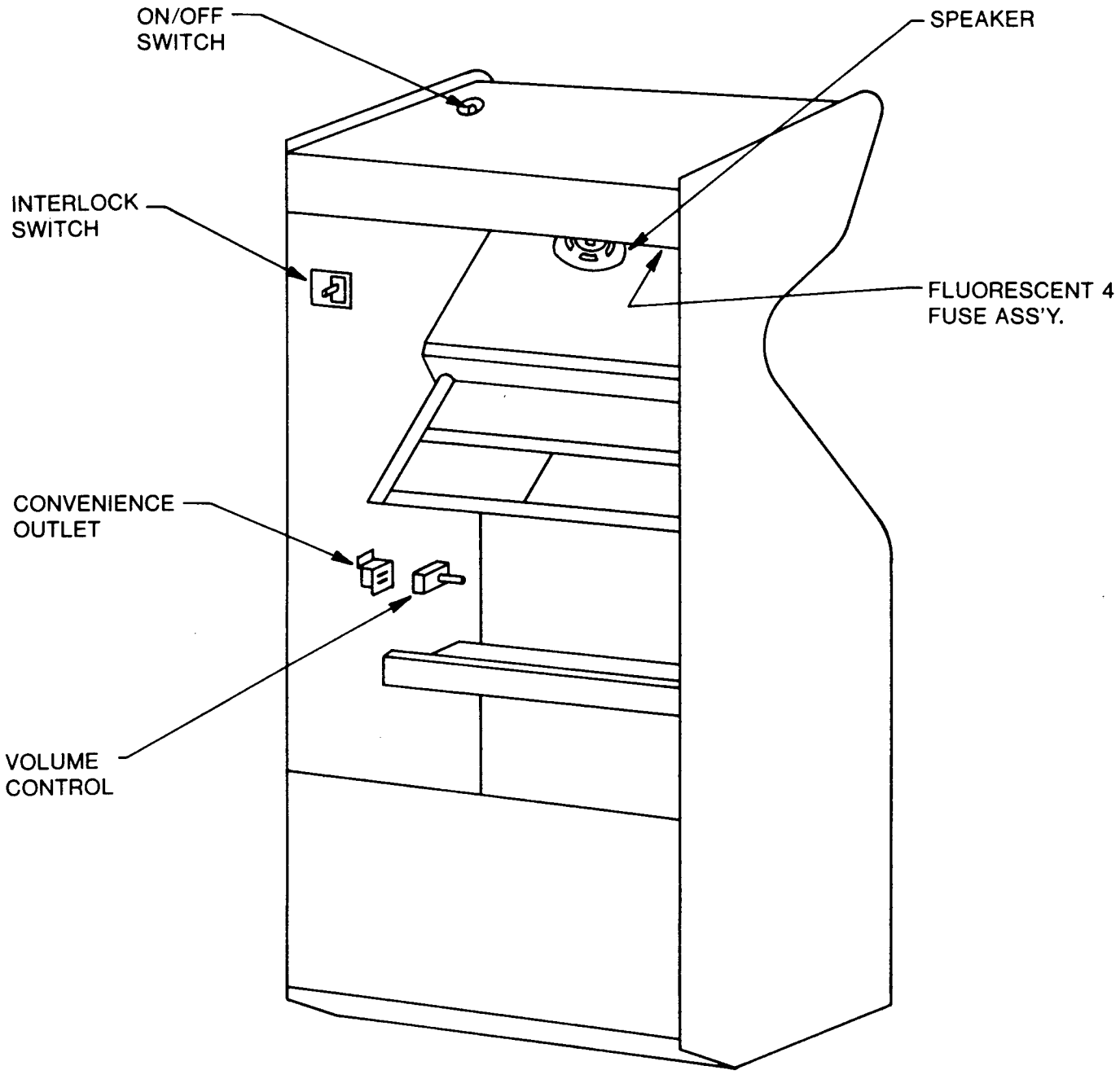


FIGURE - C

SLIDING DRAWER

ADJUSTMENTS & FUSES

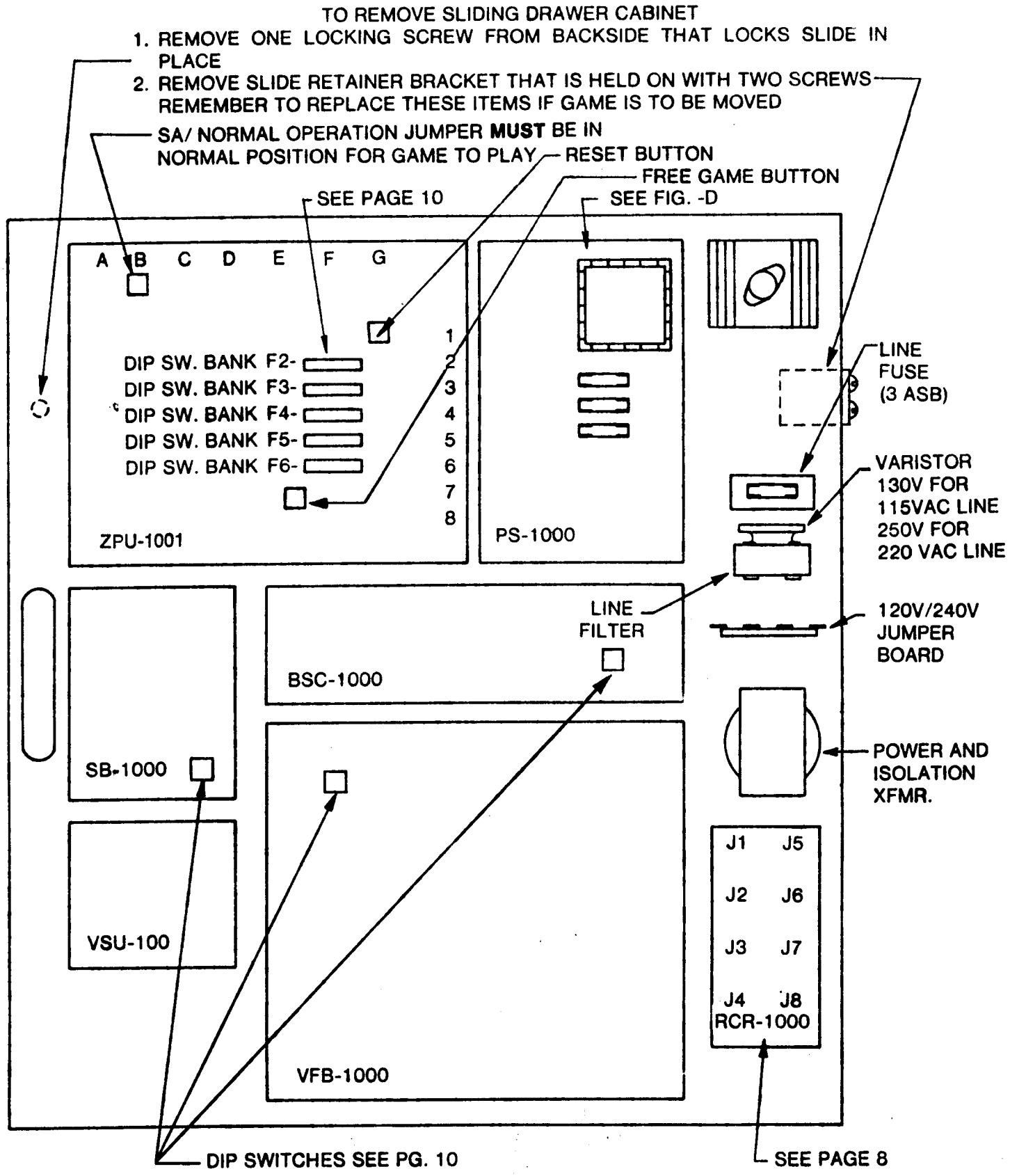
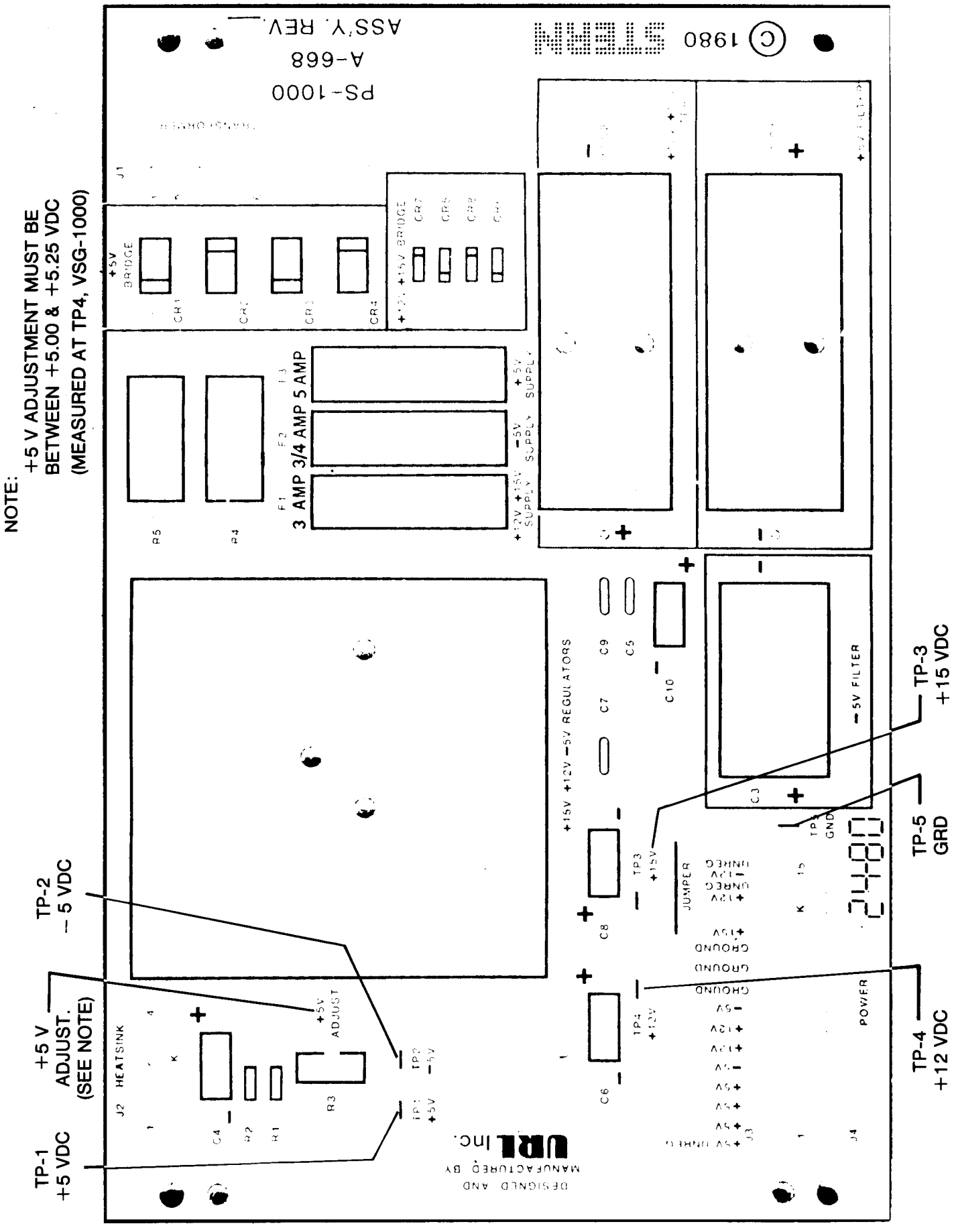
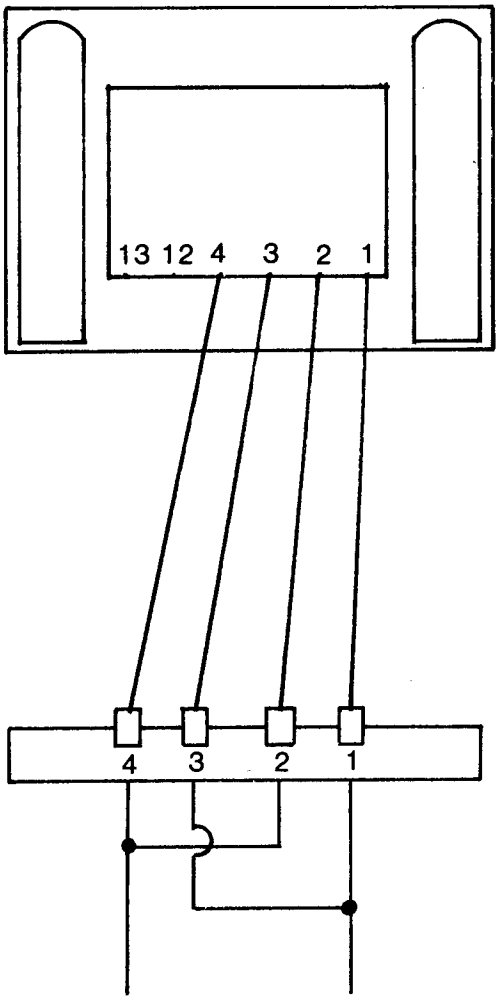


FIGURE D

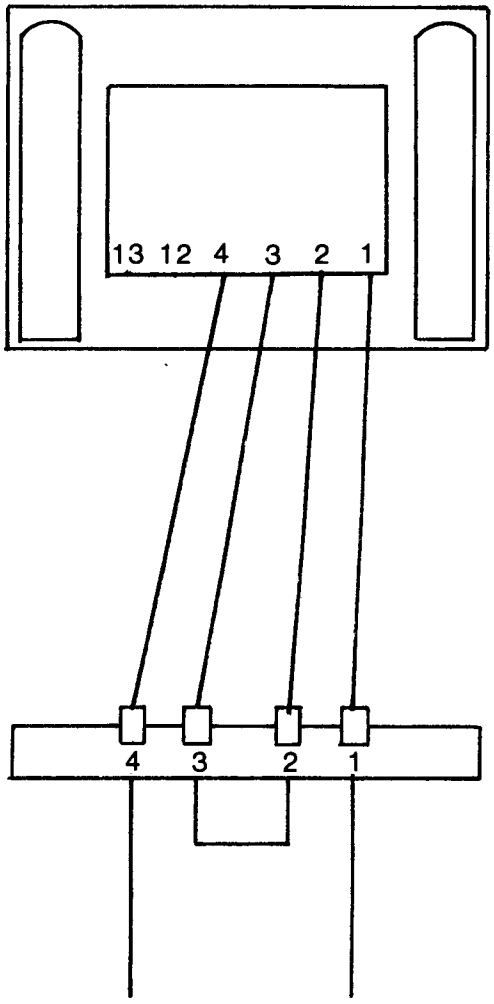

NOTE:
+5 V ADJUSTMENT MUST BE BETWEEN +5.00 & +5.25 VDC (MEASURED AT TP4, VSG-1000)
TP-1 +5 VDC
+5 V ADJUST. (SEE NOTE)
TP-2 − 5 VDC
TP-3 +15 VDC
TP-5 GRD
TP-4 +12 VDC
PS-1000
A-668
ASS'Y. REV.
© 1980 STERN
3 AMP 3/4 AMP 5 AMP
+15V +12V −5V REGULATORS
−5V FILTER
HEATSINK
DESIGNED AND MANUFACTURED BY
URI Inc.

TRANSFORMER
STERN 16D-13

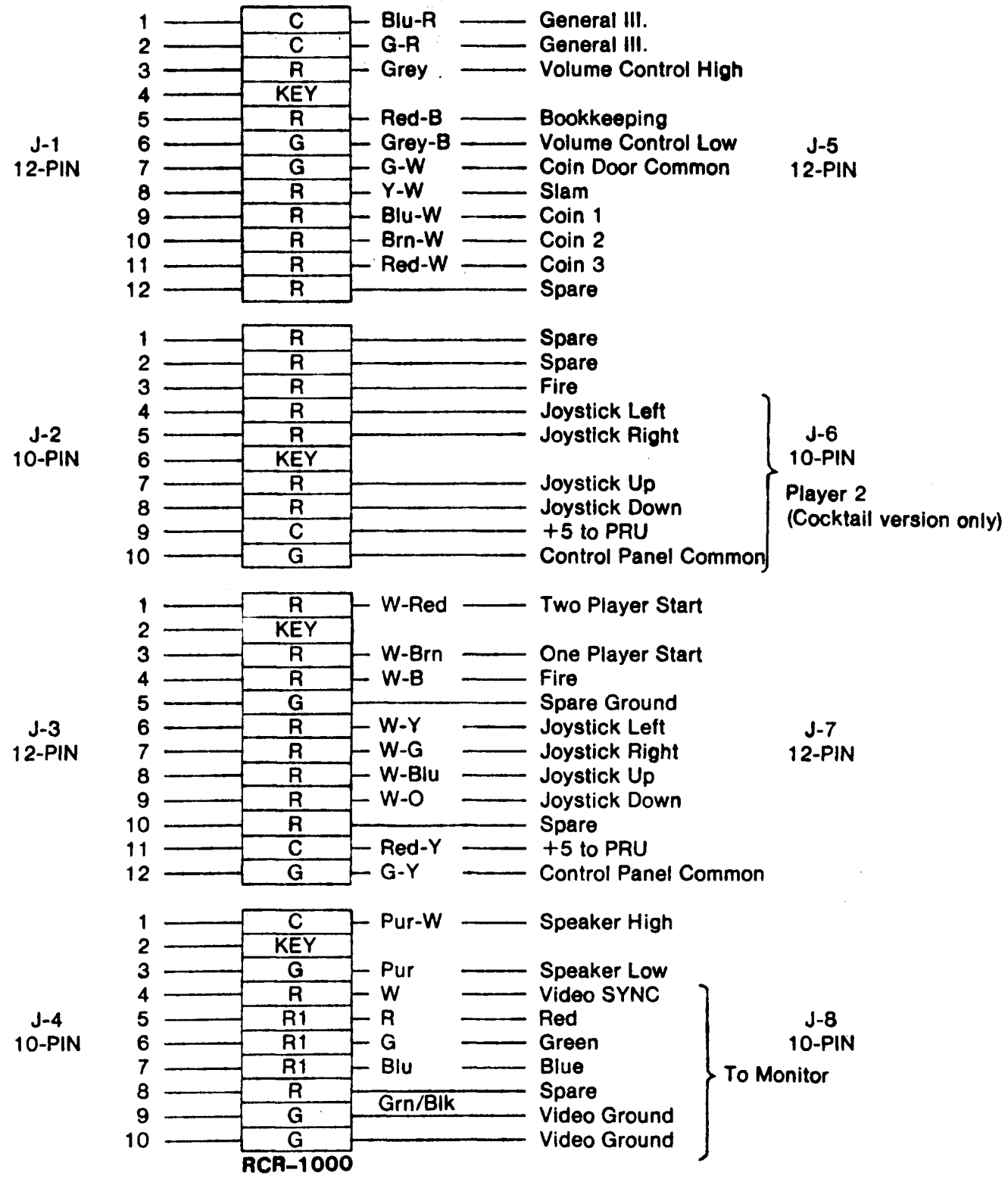


JUMPER

115 VAC
130V VARISTOR
FOR 115 VAC LINE

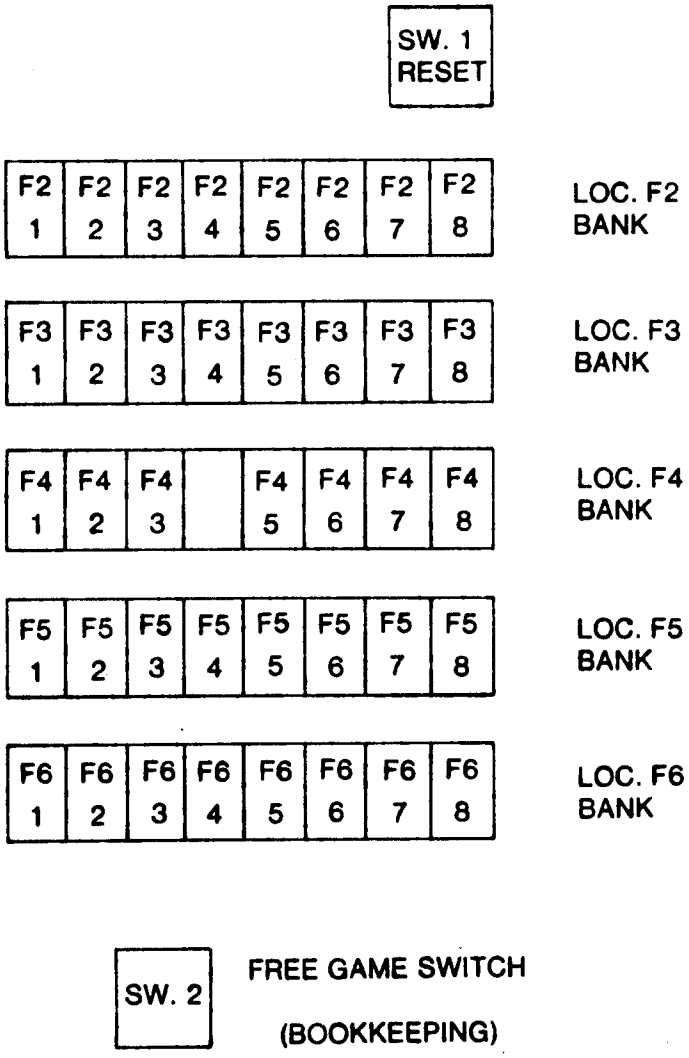


220VAC
250V VARISTOR
FOR 220 VAC LINE


J-1
12-PIN
1 C Blu-R General III.
2 C G-R General III.
3 R Grey Volume Control High
4 KEY
5 R Red-B Bookkeeping
6 G Grey-B Volume Control Low
7 G G-W Coin Door Common
8 R Y-W Slam
9 R Blu-W Coin 1
10 R Brn-W Coin 2
11 R Red-W Coin 3
12 R Spare
J-5
12-PIN
J-2
10-PIN
1 R Spare
2 R Spare
3 R Fire
4 R Joystick Left
5 R Joystick Right
6 KEY
7 R Joystick Up
8 R Joystick Down
9 C +5 to PRU
10 G Control Panel Common
J-6
10-PIN
Player 2
(Cocktail version only)
J-3
12-PIN
1 R W-Red Two Player Start
2 KEY
3 R W-Brn One Player Start
4 R W-B Fire
5 G Spare Ground
6 R W-Y Joystick Left
7 R W-G Joystick Right
8 R W-Blu Joystick Up
9 R W-O Joystick Down
10 R Spare
11 C Red-Y +5 to PRU
12 G G-Y Control Panel Common
J-7
12-PIN
J-4
10-PIN
1 C Pur-W Speaker High
2 KEY
3 G Pur Speaker Low
4 R W Video SYNC
5 R1 R Red
6 R1 G Green
7 R1 Blu Blue
8 R Spare
Grn/Blk
9 G Video Ground
10 G Video Ground
J-8
10-PIN
To Monitor
RCR-1000
R= 10Ω 10Ω .001
C= .001
G=
R1= 10Ω 10Ω 150 pfd

OPERATION

Insert coin for credit. Start game by pressing START button. Object of game is to have Humanoid Intruder shoot as many Robots as possible and escape from room. Humanoid Intruder is controlled by player with control stick. (Eight directions possible). Note: Humanoid Intruder stops moving when shot is fired. Shot is fired in direction Control Stick points to. Bonus Score for each room full of destroyed Robots (even if Robots destroy each other). EVIL OTTO comes out from position Humanoid Intruder started, can be destroyed will go thru walls, and follows Humanoid Intruder with its object to destroy the Humanoid Intruder.



ADDITIONAL SWITCHES

ELECTRONIC BOARDS	SWITCH NO.	PINS	USAGE
BSC	1	1-8	Breaks $\overline{\text{WAIT}}$ line for SIGNATURE ANALYSIS (S.A) MUST BE Closed for game operation
	2	2-7	Adjusts color outputs for the variations in monitor input circuitry
	3	3-6	
	4	4-5	SHOULD BE: OPEN FOR WELLS-GARDNER CLOSED FOR ELECTROHOME
VFB 100	1	1-8	NOT USED
	2	2-7	Breaks $\overline{\text{NMI}}$ line for S.A. MUST BE Closed for game operation
	3	3-6	Breaks $\overline{\text{INT}}$ line for S.A. MUST BE Closed for game operation
	4	4-5	Breaks $\overline{\text{WAIT}}$ line for S.A. MUST BE Closed for game operation
SB 1000	1	1-8	Breaks $\overline{\text{WAIT}}$ line for S.A.
	2	2-7	NOT USED
	3	3-6	NOT USED
	4	4-5	NOT USED

JUMPER OPTIONS

SB 1000: JUMPER W1 MUST BE CONNECTED (W2 OPEN)

VSU 1000: JUMPER W3 MUST BE CONNECTED (W4 OPEN)

ZPU-1001: J8 PINS 2-3 MUST BE CONNECTED TOGETHER

CHIP LOCATION 1E MAY BE POPULATED BY ANY ONE OF 3 DIFFERENT CHIPS

CHIP	STERN PART NO.	CONNECT JUMPER
6513 H	56A-6-S004	W5
6513 L	56A-6-S003	W6
6514	56A-6-S002	W11

FREE GAME SWITCH (SW. #2)

Switch #2 (printed on board "Bookkeeping Clear"), if pressed when HIGH SCORE TO DATE IS DISPLAYED will provide one game without being added on any coin bookkeeping.

MONITOR DIP SWITCH AND GAME SWITCH DISPLAY TEST

Set dip switch 3 on the ZPU board (location F2, See fig. D) to "ON" position, then press the RESET button (SW. #1, located at F1 on the ZPU board).

The monitor will display the OFF (0 on the monitor) ON (□ on the monitor) status of the 40 "ZPU DIP SWITCHES" on the upper chart and the open (0 on the monitor), closed (□ on the monitor) status on all game switches on the lower "VFB SWITCHES" chart.

SEE BELOW FOR ZPU AND VFB SWITCH ASSIGNMENTS. (SEE PAGE 13 FOR DIP SW. DESCRIPTION)

(NOTE: GAME SWITCHES CAN BE TESTED BY CLOSING AND SEEING IF CLOSED DISPLAY SHOWS UP ON MONITOR CHART).

To return to normal operation set dip switch 9 to OFF position and press RESET (SW. #1) button on the ZPU board.

ZPU DIP SWITCH STATUS

1 Normally OFF (On for SA. Tests)	2 Normally OFF (On for SA. Tests)	3 Switch Test	4 Monitor Test	5 N/U	6 N/U	7 N/U	8 N/U	DIP BANK #1 LOC. F2
9	10	11	12	13 N/U	14 N/U	15 Language Adj. SEE PG. 13	16	DIP BANK #2 LOC. F3
EXTRA MAN ADJUSTMENTS SEE PG. 13								
17	18	19	20	21	22	23	24	DIP BANK #3 LOC. F4
COIN ROUTINE COIN SW. 2 SEE PG. 13								
25	26	27	28	29	30	31	32	DIP BANK #4 LOC. F5
COIN ROUTINE COIN SW. 1 SEE PG. 13								
33	34	35	36	37	38	39	40	DIP BANK #5 LOC. F6
SET VALUE FOR CREDIT BUTTON SEE PG. 13								

VFB SWITCHES (SHOWS SETTINGS)

VFB SWITCH STATUS

ON WHEN JOYSTICK AT LEFT	ON WHEN JOYSTICK AT RIGHT	ON WHEN JOYSTICK UP	ON WHEN JOYSTICK DOWN	ON WHEN FIRE PRESSED	•	•	•
ON WHEN START 1 PLAYER IS ON	ON WHEN START 2 PLAYER IS ON	•	•	•	ON IF COIN CHUTE #3 IS CLOSED	ON IF COIN CHUTE #2 IS CLOSED (IF USED)	ON IF COIN CHUTE #1 IS CLOSED
•	•	•	•	•	•	•	•

0 = SWITCH OFF (OPEN)
□ = SWITCH ON (CLOSED)
• = NOT USED

NOTE: Cross hatch pattern is used for Monitor setup pushing Fire Button will cause a red screen to check purity.

ZPU DIP SWITCH

SWITCH NO.	LOCATION	FUNCTION
SW. #1	F2	Signature analysis mode (service only)
SW. #2	F2	Signature analysis mode (service only)
SW. #3	F2	Switch test
SW. #4	F2	Monitor test
SW. #5	F2	N/U
SW. #6	F2	N/U
SW. #7	F2	N/U
SW. #8	F2	N/U
SW. #9	F3	Extra man adjustments (See page 13)
SW.#10	F3	
SW.#11	F3	
SW.#12	F3	
SW.#13	F3	N/U
SW.#14	F3	N/U
SW.#15	F3	Language adjustments
SW.#16	F3	
SW.#17	F4	Coin routine coin switch #2 (See page 13)
SW.#18	F4	
SW.#19	F4	
SW.#20	F4	
SW.#21	F4	
SW.#22	F4	
SW.#23	F4	
SW.#24	F4	
SW.#25	F5	Coin routine coin switch #1 (See page 13)
SW.#26	F5	
SW.#27	F5	
SW.#28	F5	
SW.#29	F5	
SW.#30	F5	
SW.#31	F5	
SW.#32	F5	
SW.#33	F6	Set value for credit button (See page 13)
SW.#34	F6	
SW.#35	F6	
SW.#36	F6	
SW.#37	F6	
SW.#38	F6	
SW.#39	F6	
SW.#40	F6	

NOTE: Cross hatch pattern is used for Monitor setup. Pushing the Fire Button will cause a red screen to check purity. Pushing the Fire Button again will cause a return to the crosshatch pattern, etc.

DIP SWITCH ADJUSTMENTS

CREDIT/COIN ADJUSTMENTS:

The Frenzy Credit System is a programmable system using the Binary number system to set a value to both Coin Chutes and the Credit Button.

This Coin-to-Credit system will allow many different pricing schemes. Every coin is counted as a Dip Setable number of clicks. The Credit Button is also counted as a Dip Setable number of clicks. When enough clicks to make a credit are on hand, a credit is given and the clicks are subtracted from the total on hand when the Credit Button is pushed.

There can be clicks left over in any amount less than the number needed for a credit. The click value for the coins is set to zero whenever the player(s) start a game.

Dip Bank #3 on the Z.P.U. Board sets the value for Coin Switch 2.
Dip Bank #4 on the Z.P.U. Board sets the value for Coin Switch 1.
Dip Bank #5 on the Z.P.U. Board sets the value for the Credit Button.

Dip Switch Number	1	2	3	4	5	6	7	8	ON
Binary Value	1	2	4	8	16	32	64	128	OFF

FOR EXAMPLE: Dip 3 12xxxxxx = Binary Value 3
Dip 4 12xxxxxx = Binary Value 3
Dip 5 x2xxxxxx = Binary Value 2

GIVES: Credit/Coin Ratio of; 1/1, 3/2.

Dropping the first Coin gives you three clicks, if you push the Credit Button now (the Credit Button value is set at two clicks) you will get one credit and have one click left over. If you now drop a second coin, you will get three more clicks plus the one you had left over, giving a new total of four clicks, for two credits.

DIP BANK 1

1	S.A.
2	S.A. MODIFIER
3	SWITCH TEST
4	MONITOR TEST
5	N/U
6	N/U
7	N/U
8	N/U

DIP BANK 2

1	EXTRA MAN LEVEL
2	
3	
4	
5	N/U
6	N/U
7	LANGUAGE
8	

xxxx No Extra Man	x23x 6000	xx34 12,000
1xxx 1000	123x 7000	1x34 13,000
x2xx 2000	xxx4 8000	x234 14,000
12xx 3000	1xx4 9000	1234 15,000
xx3x 4000	x2x4 10,000	
1x3x 5000	12x4 11,000	

0, 0 = English
0, 1 = French
1, 0 = German
1, 1 = Spanish

NOTE: x = OFF
NUMBER = ON

BOOKKEEPING

Inside the coin door is the BMDS (Bookkeeping Monitor Display Switch) - (See Fig. A). Depressing this switch one time initiates this function. The first bookkeeping function to appear on the monitor is number of credits (*Green). To delete from memory press either **Fire Button.** Depressing the BMDS one more time will advance the bookkeeping up (*Blue), and the second bookkeeping function (total coins thru coin chute #1) will be displayed on the botton (*Green). To delete from memory press either **Fire Button.** The previous bookkeeping functions will remain on the screen (*Blue) and the new function will appear on the botton (*Green). Bottom function can be deleted from memory. Following is a complete list of bookeeping functions.

*Color of display if color monitor is used.

	FUNCTION	DESCRIPTION	DIGIT DISPLAY
1)	Credits	Total Credits	00
2)	Chute #1 (Left)	Total Coins	00000000
3)	Chute #2 (Center)	Total Coins	00000000
4)	Chute #3 (Right)	Total Coins	00000000
5)	Plays	Total Number of Plays	000000
6)	Score	Accummulated Score	000000000000
7)	Time Played	Total Amount of Time Played (in seconds)	000000000000
8)	High Score	High Score To Date	000000

COIN INSTRUCTION TRANSLATION (SWS. #15 & 16)

Will say in different language correct coinage

	SW.-#15	SW.-#16
ENGLISH	OFF	OFF
FRENCH	OFF	ON
GERMAN	ON	OFF
SPANISH	ON	ON

TROUBLE SHOOTING BY SELF-TESTS

PERTINENT INFORMATION

1. The following tests occur each time the RESET button is momentarily pressed or when power is removed and re-applied.
2. The self-test indicating LED is on the ZPU-1001 board (CR45) and each indicating flash is accompanied by a tone from the sound system.
3. The LED stops flashing at the malfunction provided all PC boards are connected in the system.

NOTE: If the ZPU-1001 board is not connected to the VFB-1000/BSC-1000 board combination, the self-test program will continuously cycle and counting LED flashes is meaningless. Also, if the SB-1000 board is not connected, or if it is defective, no self-test tone will be generated.

FIRST SELF-TEST

The first of 8 LED flashes occur accompanied by a tone from the speakers. This first test analyzes the ROM circuits on the ZPU board.

ANALYSIS OF FIRST TEST WHEN LED STAYS ON

Continuous illumination of the LED indicates problems in one or more of the following areas:

1. The POWER-ON RESET circuit. Check NAND gate 7G, inverter 8G and associated circuits.
2. Loss of clock signal. Check oscillator transistor Q12, flip flop divider 8A and other associated components.
3. Microprocessor (Z-80) is defective (Chip 7B).
4. Defective Address Bus (shorted or open) or control buffers (chips 6B and 7D, type LS244).
5. Defective ROM chip(s).
6. Defective I/O Decode Circuits. Check chips 5A, 4A, 6A, 7G and decoder 7E.
7. Defective LED latch. Check chips 7G, 3A, and 8G.

Analysis of First Test when LED Flashes Once and stays OFF. This sympton indicates the problem is in one or more of the following areas.

1. Defective PROM circuitry. Check all PROM chips since the malfunction may be in any one chip.
2. Defective Address Decode Circuit. Check chips 6E, 4A, 5A, 6A and 8G.

SECOND SELF-TEST

The second of 8 LED flashes should occur accompanied by a tone from the speaker. This test analyzes the "scratch pad" area of the RAM on the ZPU-1001 board. For the following diagnostics, the LED must flash twice and extinguish.

ANALYSIS OF SECOND TEST

NOTE: All following chips are on the ZPU-1001 Board.

1. Check RAM CHIPS 1E and 2E.
2. Check transistor Q2 and associated components/circuits.
3. Defect in gating chips 2A, 3A and 6A.
4. Check that the jumper used for chip 1E (W5, W6 or W11) is correct for the particular chip part number. See page 10 for jumper options.

THIRD SELF-TEST

The third of 8 LED flashes should occur accompanied by a tone from the speaker. This test analyzes the RAM (screen RAM) located on the VFB-1000 board. For the following diagnostics, the LED must flash three times and extinguish.

NOTE: The following chips are on the VFB-1000 Board.

1. The CRT will display a RAM chip location map which will indicate a defective chip. Mentally rotate the map 90 degrees counterclockwise to properly orient the map with the lower right hand portion of the VFB-1000 board. If the defect is not located, use the following steps:
2. Check the +12V and -5V voltages, specifically to the VFB-1000 board.
3. Check RAM address Multiplexers 6F, 6G, 6H and 6E.
4. Check the RAS* and CAS* circuits: chips 4E, 7E, 1G, 5G and 5F.
5. Check the "RAM write" circuits: chips 5F and 5E.
6. Check the Address/Arbitration circuits, chips 5G, 5F, 7E, 3F, 1F and 2D. Check that switch 2B (contacts 4 & 5) is set to the ON position.
7. Check the "magic" enable circuits of chips 7B and 5C.
8. Check the "write" data path of chips 7A, 8A, 10A, 11A, 12C and 10C.
9. Check the "Read" data path of chips 10D, 11D and 6D.
10. Checks all Bus connectors, especially J1 and J2 on both the VFB-1000 and BSC-1000 boards.

*Denotes negative true logic

FOURTH SELF-TEST

The fourth flash plus a tone test the RAM circuits on the BSC-1000 color board. IF the LED stops on the fourth flash, perform the following listed tests:

NOTE: All following chips will be on the BSC-1000 board.

1. Check RAM chips 3B, 2B, 1B, and 2A.
2. Check the Address Multiplexer chips 4C, 4B and 4A.
3. Check that DIP Switch 2F (pins 4 & 8) is set to the ON position.

FIFTH SELF-TEST

The fifth flash plus tone test the Shifter/Flopper circuits on the VFB-1000 board. If the LED stops on the fifth flash, perform the following tests.

1. Check Shifter/Flopper chips 7A, 8A, 9A, 10A, 11A, 8B, 9B, 10B, 11B.
2. Check ENABLE gates 7B and 5C.
3. Check control latch 6C.
4. Check "OLD DATA" latch 7C.
5. Check Port Decoder 4D.

SIXTH SELF-TEST

The sixth flash plus a tone tests the Arithmetic and Logic Unit (ALU) and the intercept circuits on the VFB-1000 board.

NOTE: All following listed chips are on the VFB-1000 board.

1. Check ALU chips 12C, 10C.
2. Check ENABLE gate 5C.
3. Check the Intercept gates 12A, 12B.
4. Check Flip-Flop 6B and associated gates of 5G and 1H.

SEVENTH SELF-TEST

The seventh flash plus a tone tests the Interrupt and Non Maskable Interrupt (NMI) circuit portions which are on both the ZPU-1001 and VFB-1000 boards. When the LED stops at the seventh flash, perform the following tests:

1. Check that Dip Switch 2B (pins 3-6 and 2-7) is set to on.
2. Z-80 microprocessor.
3. Interrupt generating circuitry 1G, 3D, 2D.
4. Time Gating circuity 1E, 2F, and 2E.
5. NMI ENABLE Latch 1D.
6. NMI generating circuitry 2E, 3E & 2D.

EIGHT SELF-TEST

If the LED indicator and associated tone have occured eight times, the malfunction is either in a circuit that is not within the testing capabilities of this self-test program or the problem is unique such as an intermittent condition that changes with physical movements or temperature.

After eight flashes have been obtained, try the game to see if the problem has been removed by the check-out action. If the game operates properly, it is advisable to attempt to locate the former problem by checking all connectors for tightness. Also lightly tap various areas while viewing the CRT.

If eight flashes have occurred and the game is still inoperable, the following information outlines the circuits that are not part of the self-test routine and must be verified by other test methods:

1. Check the settings of all DIP switches on the ZPU-1001 and VFB-1000 boards by setting switch S9 (on ZPU-1001) to ON and then pressing the RESET* button (on ZPU-1001). The CRT will display the ON/OFF conditions of all switches which must then be checked against the Installation and Operating manual data.
2. Visual analysis of the CRT pattern (when it is available) can provide many clues to circuit operation as described in the following paragraphs. Total loss of the CRT display usually indicates problems in the monitor itself.
3. Malfunctions in the horizontal or vertical address counting circuitry, or SYNC generator circuits will cause "bad" video to be displayed. Vertical or horizontal stripes should give an indication of where the error is. A rolling or flipping picture is an indication of SYNC problems, either in the monitor or on the VFB-1000 board SYNC circuits.
4. Color splotches are an indication of a malfunction in the color gating circuitry, or a monitor problem. Check BSC-1000 board chips 2C, 1C, 2D, 3D, 3E and associated switches and resistors.

SOUND SYSTEM PROBLEMS

1. NO SOUND; Check amplifier 8C on the SB-1000 board. Check VAUDIO (+15V MAX).
2. Voice is normal but there are no sound effects: Check the 6840 chip on the VSU-1000 board. On this board check that Dip Switch 10B (pin 1-8) is in the ON condition. Check the addressing and timing circuitry chips 6A, 8A, 9B, 9A, 9C, 10C, 8A and 10B. Any other malfunction will result in either the loss of a specific sound or, a change in a sound and can thus be identified as a related circuit.
3. Sound effects are normal but there is no voice: Check VSU-1000 chips: CRC ROM chip 3C, PROMs 1C, 2C, clock generator 5A, 6A, decode & control logic 1A, 2A, 3A, 4A, 2B, 5B, 6B, 6C. Also check the -10V supply (on the board). Distorted Noise: check PROM 1C, 2C, CRC ROM chip 3C, filter & amplifier 5C.

RF INTERFERENCE PROBLEMS

Warning: This equipment generates, uses, and can radiate radio frequency energy and if not installed and used in accordance with the instructions manual, may cause interference to radio communications. As temporarily permitted by regulation it has not been tested for compliance with limits for Class A computing devices pursuant to Subpart J of Part 15 of FCC Rules, which are designed to provide reasonable protection against such interference. Operation of this equipment in a residential area is likely to cause interference in which case the user at his own expense will be required to take whatever measures may be required to correct the interfernce.

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Toll Free Service Assistance (800) 621-6424

REVISIONS				
SYM	DESCRIPTION	DFT DATE	CHK DATE	APPD DATE
A	ISSUED E.I. 00922.	6/11/81	6/12/81	

HSA-1200

2N6226

KEY NC

J3 1 2 3 4 5
E B C KEY NC

J2

5 10 VAC 6

6 10 VAC 3

AC

CR1 KBPC6005 BRIDGE

AC

2

F1 4 A. SB

C8 15,000 MFD 16 V.

C1 .01MFD

R8 22Ω 1/2 W

+ 5 V. REG.

TP4

J1

4,5 +5 V. REG.

3

V_{in}

VR1 LM317T

V_{out}

ADJ.

2

1

R1 120Ω

R5 620Ω

R7 100Ω 1/2 W

C2 22 MFD 16 V.

R4 620Ω

R2 1KΩ

6 +12V UNREG

+12V REG

TP2

1 IN OUT 3

GND 2

VR2 7812

C7 6,800MFD 35V

C3 .1MFD

C4 22MFD 16V

GND

TP3

3,8,9,10 GND

7 15 VAC 2

8 CT 4,5,7,8,10

9 15 VAC 1

KEY 9

CR3 IN5391

F2 2A SB

CR5 IN5391

CR4 IN4004

-5V REG

TP1

1

CR2 IN4004

F3 1A SB

R6 75Ω,2W

2 IN OUT 3

GND 1

VR3 7905

C9 1,000MFD 35V

C6 .1MFD

C5 22MFD 16V

R3 1KΩ

2 -5V REG

7 KEY

1 2 3 4

FOR 120V LINE, CONNECT 1 TO 3 AND 2 TO 4.

FOR 240V LINE, CONNECT 2 TO 3, 1 AND 4 SHOULD GO TO LINE.

10 11 6.3 VRMS TO GEN. ILL.

12 13 103 VRMS TO MONITOR

POWER TRANSFORMER 16D-26-1

NOTES:

1. SHOULDER WASHER REQUIRED ON MOUNTING STUD
2. GENERAL INSTRUMENTS.

STERN ELECTRONICS, INC.
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SCHEMATIC, POWER SUPPLY P.C. BOARD

34C-978-S

SH 1 OF 1

34C-978-S

REVISIONS				
SYM	DESCRIPTION	DFT DATE	CHK DATE	APPD DATE
A	ISSUED, E.I. 00265	TH 9/1/10	[illegible]	[illegible]

HEAT SINK & REGULATOR SHOWN FOR REFERENCE ONLY NOT LOCATED ON P.C. BOARD

HSA-1000

SG323

J2
4
3 KEY
2
1

J1
5
6
4
7 14VAC
2 KEY
1
9 14VAC
3
10
6.8 VAC
11

1 START
2
3 START
4

8 VAC

8 GND

TRANSFORMER SHOWN FOR REFERENCE ONLY, NOT MOUNTED ON P.C. BOARD

F3 5A S.B.

CR1 CR2 CR3 CR4 MR500

C1 15000 16V

CR5 IN4004

CR6 IN4004

CR7 IN4004

CR8 IN4004

F1 3A S.B.

F2 3/4A S.B.

C2 6800μF 35V

C3 1000μF 35V

C4 22μF 16V

R1 12Ω

R2 120Ω

R3 1KΩ

TP1

VR1 7812

C5 .01MFD

C6 22μF 16V

R4 5.6Ω 5W

VR2 7815

C7 .01MFD

C8 22μF 16V

R5 25Ω 5W

VR3 7905

C9 .01MFD

C10 22μF 16V

TP4

TP3

TP5

TP2

J3
1 +7.75/ UNREG 43V
2 +5 VDC REG
3 +5 VDC REG
4 +5 VDC REG
5 -5V REG
6 +12V REG
7 +12V REG
8 -5V REG
9 GND
10 GND
11 GND
12 +8/ 45V (AUDIO)
KEY 13 KEY
14 +14.5/ 425V UNREG
15 -14.5/ -25V

J4
1 +7.75/ 12V UNRG
2 +5VDC REG
3 +5VDC REG
4 +5VDC REG
5 -5V REG
6 +12V REG
7 +12V REG
8 -5V REG
9 GND
10 GND
11 GND
12 +8/ 45V (AUDIO)
KEY 13 KEY
14 +14.5/ 425V UNREG
15 -14.5/ 425V UNREG

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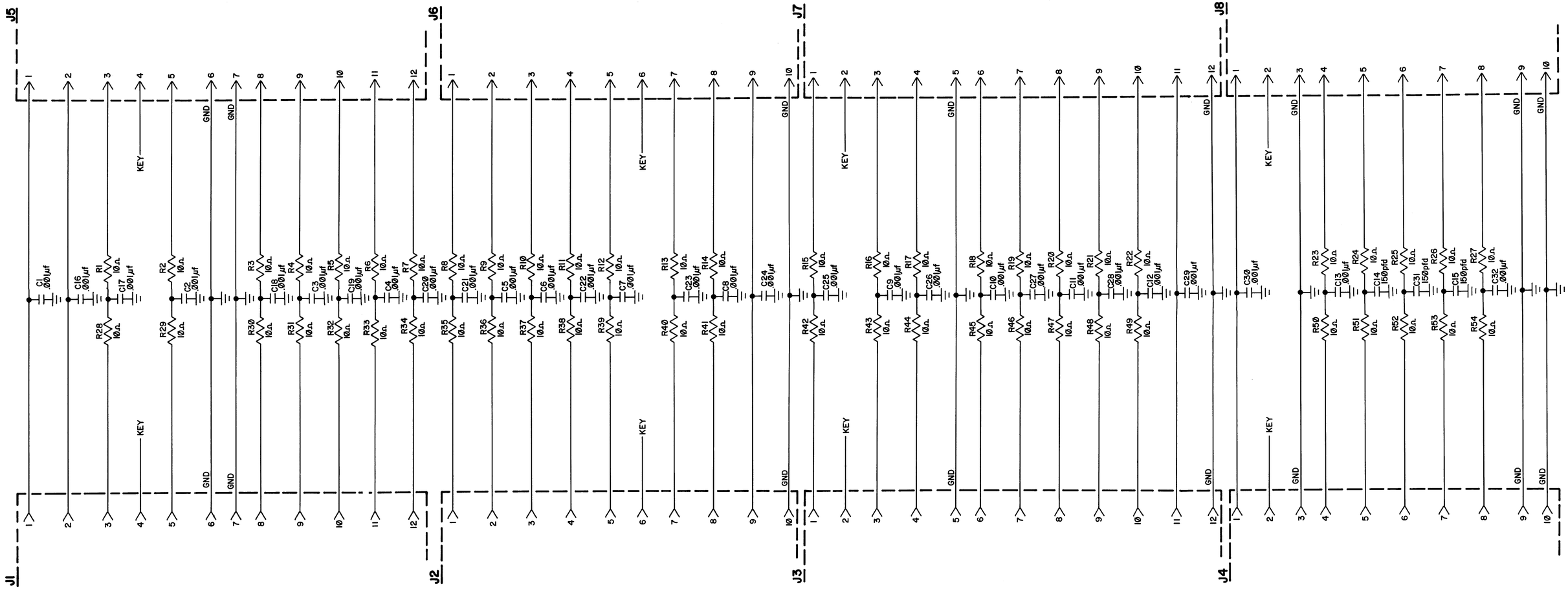
FRENZY
POWER SUPPLY BOARD

12D-668-S

REVISIONS				
SYM	DESCRIPTION	DFT. DATE	CHK DATE	APPD DATE
A	ISSUED E.I. 00389	7/25/80	8/1/80	8/7/80



STERN SYSTEMS OF CHICAGO
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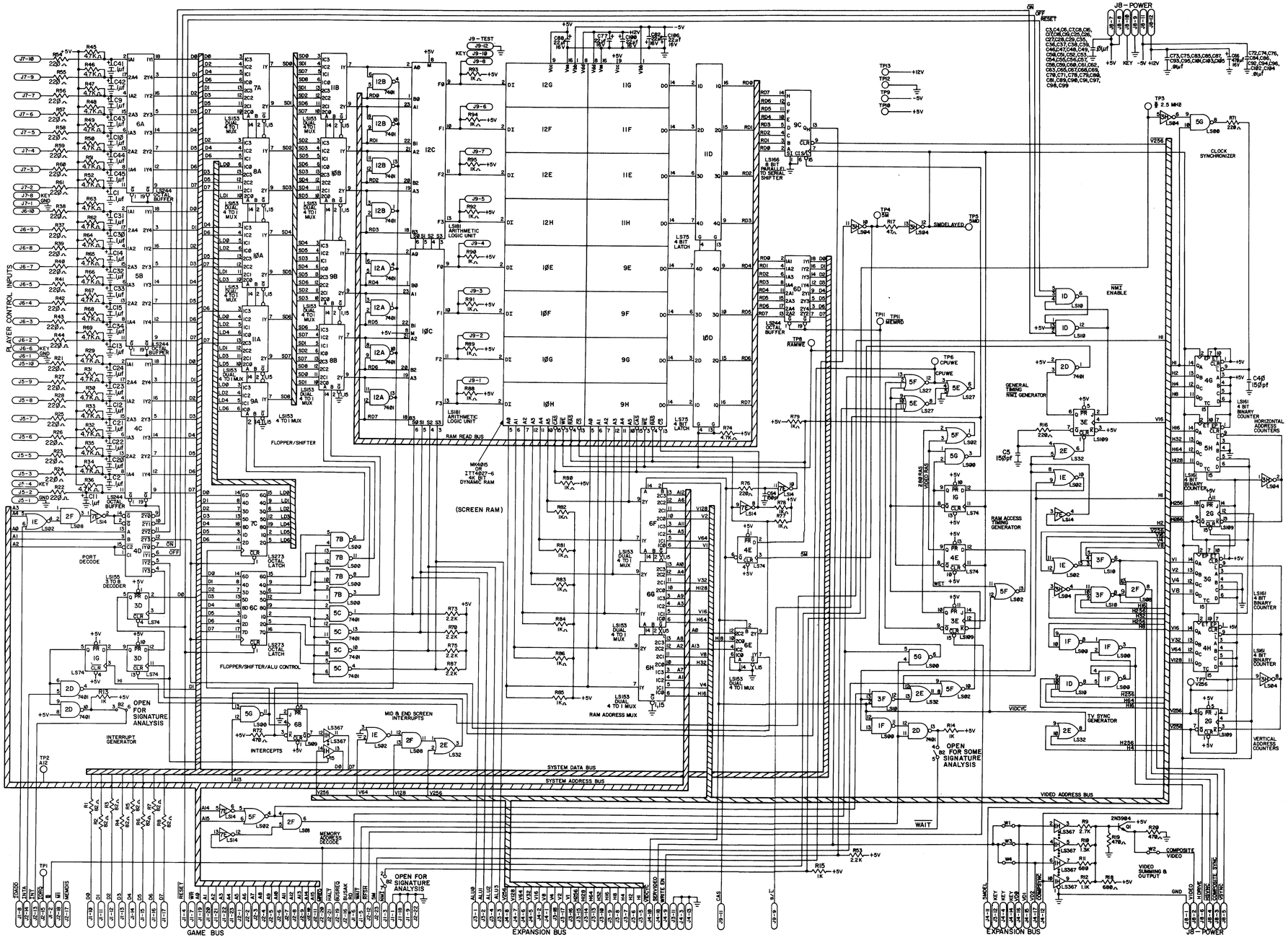
FRENZY RESISTOR, CAPACITOR & RESISTOR BOARD

12D-788-S

REVISIONS				
SYM	DESCRIPTION	DFT DATE	CHK DATE	APPD DATE
A	ISSUED EI 00324	2/4/80		
B	DRAFTING ERROR E.I. 00390	2/4/80		
C	ADDED MISSING INFORMATION E.I. 00441	2/6/80	2/6/80	



LS367	16	8		
LS273	20	10		
LS244	20	10		
LSI81	24	12		
LSI66	16	8		
LSI61	16	8		
LSI55	16	8		
LSI53	16	8		
LSI09	16	8		
LS75	5	12		
LS74	14	7		
LS32	14	7		
LS27	14	7		
LSI4	14	7		
LSI0	14	7		
LS08	14	7		
LS04	14	7		
LS02	14	7		
LS00	14	7		
7401	14	7		
4827-6/MK4815	9	16	8	1
I.C. TYPE	+5V	GND	+12V	-5V
	PIN NO.			

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FRENZY VIDEO FRAME BUFFER BOARD

12D-660-S

REVISIONS				
SYM	DESCRIPTION	DFT DATE	CHK DATE	APPD DATE
B	TO COMPLETE PRODUCTION SCHEMATIC E.I. 00433			

NOTES:
1. DIP SWITCHES F2-2, F2-3, & F2-4 SHOULD BE OPEN WHEN USING WELLS GARDNER MONITOR, CLOSED FOR ELECTROHOME MONITOR.
2. FOR NORMAL OPERATION SWITCH F2-1 SHOULD BE CLOSED.

I.C. TYPE		
	+5V	GND
	PIN NO.	
LS273	20	10
LS257	16	8
LS245	20	10
LS74	14	7
LS27	14	7
LS10	14	7
LS04	14	7
LS00	14	7
7406	14	7
7401	14	7
2114	18	9

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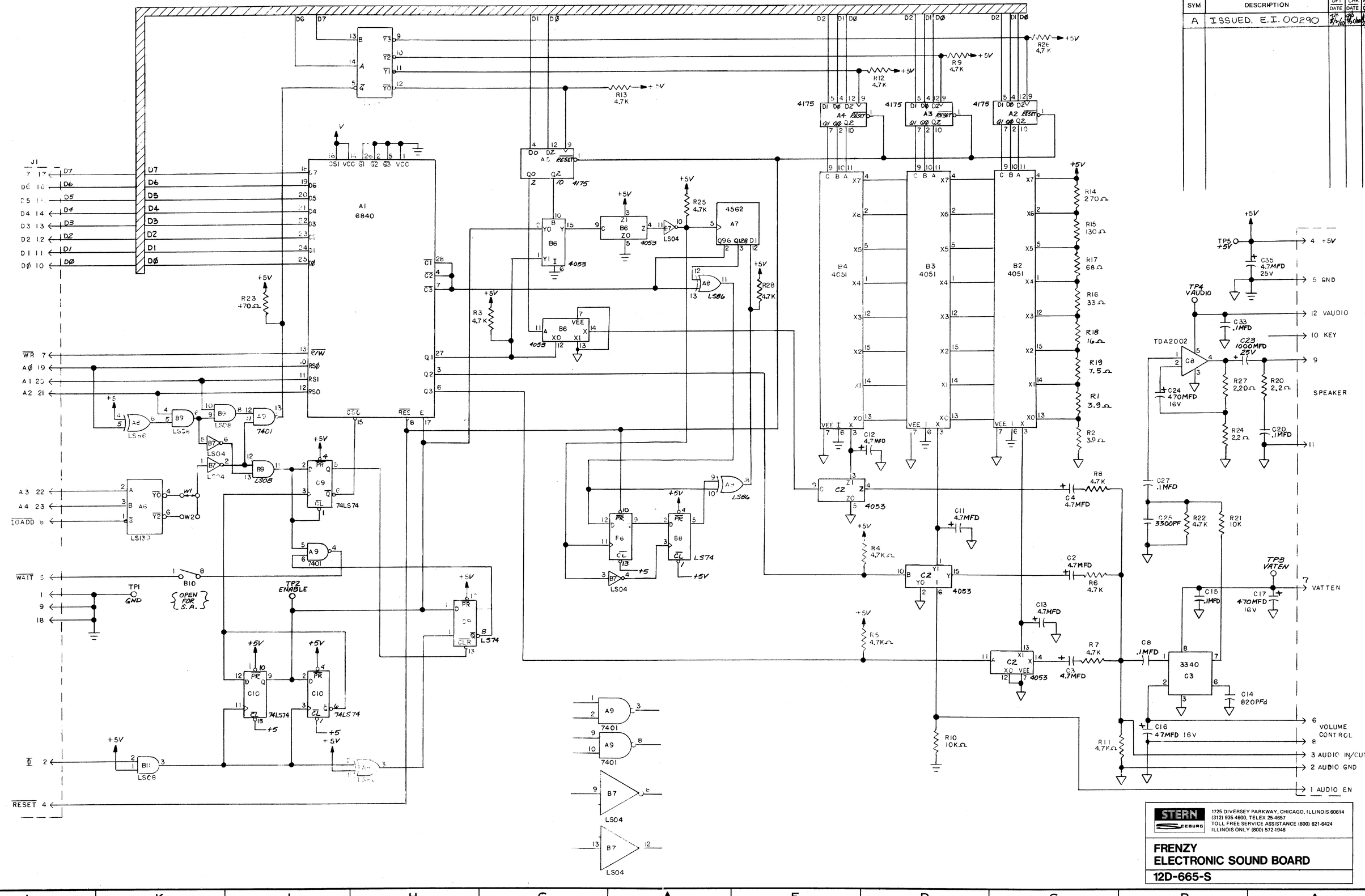
FRENZY BUFFER SYSTEM
COLOR BOARD
12D-766-S

REVISIONS				
SYM	DESCRIPTION	DFT DATE	CHK DATE	APPD DATE
A	ISSUED. E.I. 00290	2/10	2/10	2/10



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FRENZY
ELECTRONIC SOUND BOARD
12D-665-S

12D-665-S

REVISIONS				
SYM	DESCRIPTION	DFT DATE	CHK DATE	APPD DATE
A	ISSUED E.I. 00324	7/1/80		
B	DRAFTING ERROR E.I. 00391	7/9/80		

J1-6 J2-6 RD
J1-8 J2-8 IOADD
J1-7 J2-7 WR
J1-20 J2-20 A1
J1-19 J2-19 A0
J1-22 J2-22 A3
J1-23 J2-23 A4
J1-21 J2-21 A2
A3 LSI39 W4 W3
A4 LS04
A1 LS27
A2 7401
+5V R2 390Ω R3 390Ω
-10V R10 18K
R8 R9 R7 R5 R6 R17 R16 R15 100K Ω D7 D6 D5 D4 D3 D2 D1 D0
C2 C1
W1 W2 +5V
CS PD A10 A9 A8 A7 A6 A5 A4 A3 A2 A1 A0 Vss Vcc Vss Vcc
C3
A11 Vss Vcc Vdd +5V
CUSTOM ROM CONTROLLER
START BUSY CLK AUDIO
CR2 IN4148 CR3 IN4148
RI2 2.2K
J1-4 J2-4 RESET
C4 .1μf
R4 2.2K
B2 MC1455 C5 .01μf
J1-17 J2-17 D7
J1-16 J2-16 D6
J1-15 J2-15 D5
J1-14 J2-14 D4
J1-13 J2-13 D3
J1-12 J2-12 D2
J1-11 J2-11 D1
J1-10 J2-10 D0
B5 B6 14174 CLR
R14 2.2K
RI3 2.2K
J1-1 J2-1
J1-9 J2-9
J1-18 J2-18
J1-3 J2-3 NC
J1-5 J2-5
J1-2 J2-2 Φ
A6 A5 LS161
TP2 CLOCK
RII 2.2K
CI8 .1μf
TPI -10V
R37 240K
C16 .27μf
R30 240K R36 10K R35 10K R34 10K
C24 .022μf C23 150pf
C5 MC1458
R20 100Ω
CI7 .01μf
CI3 470μf 16V
R32 240K R31 270K R28 270K R29 240K
C22 .1μf R33 27K
C5 MC1458
RI8 240K
CI4 4.7μf 25V
RI9 1K
AUDIO IN/OUT J3-6
C6
R27 3K R26 2.2K R21 1.5K R25 1K R22 750Ω R23 560Ω R24 1.3K Ω
X7 X6 X5 X4 X3 X2 X1 X0 Vee
14051
TP4 +5V
KEY J3-2
+5V J3-5
CI5 22μf 16V
CI,C3,C6,C7,C8,C9,CI0, CII,CI2,CI9,C20,C21 .01μf
TP3
AUD GND J3-3
GND J3-4
C2 470μf 16V
CRI IN4740A
RI 200Ω 2W
-12 REG J3-1

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FRENZY
VOICE SYNTHESIZER UNIT
12D-708-S

12D-708-S

10MHZ CLOCK
5 MHZ
2.5 MHZ
10 MHZ
DATA BUS
MICRO — PROCESSOR
DIP JUMPER
7A LS367 CONTROL BUS BUFFER
7B Z80
7C
7D TYP (8)
7E LS155
LS244 ADD BUS BUFFER
LS244 ADD BUS BUFFER
POWER ON RESET
RESET
1K X4 NMOS RAM
1K X4 CMOS RAM
SEE MANUAL FOR W3, W4, & W5 OPTIONS
SPARE GATES
7406
1D 2732 ROM
2D 2732 ROM
3D 2732 ROM
4D 2732 ROM
6D 2732 ROM
4C 2732 ROM
3C 2732 ROM
32 X8 PROM
6E
DECODE IN/OUT ADD
BOOKKEEPING RESET
GAME SETTING SWITCHES
IN4148 (8 PLACES)
LED
POWER CONNECTORS
BUSAK
INTA
RESET
MREQ
RFSH
WR
RD
IORQ
MI
HALT
INT
NMI
BUSREQ
WAIT
5MHZ
IOADD
MEMDIS
ADD11
ADD15

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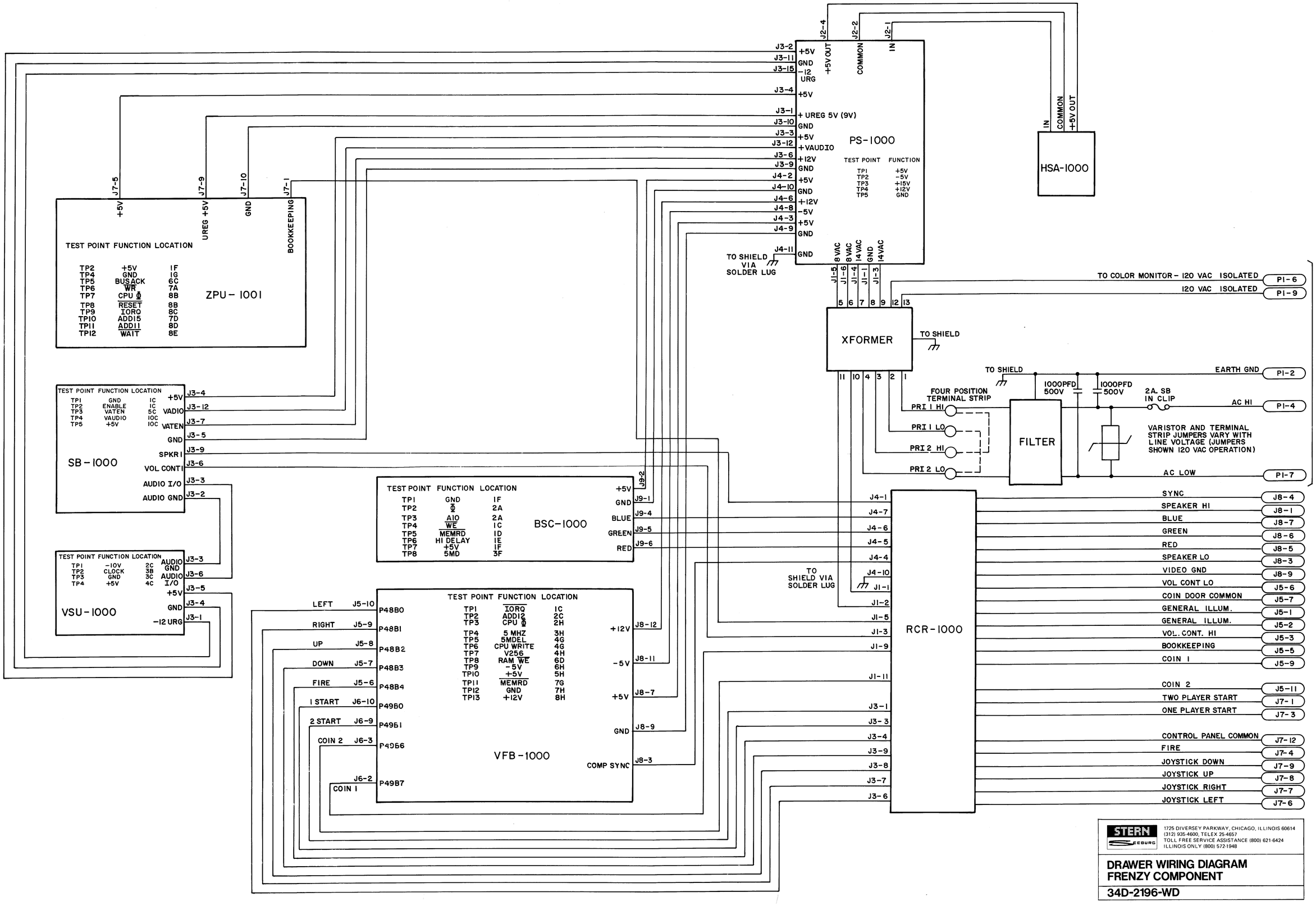
FRENZY
ZPU-1001 UNIT
34C-907-S



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DRAWER WIRING DIAGRAM FRENZY COMPONENT

34D-2196-WD