Serial Camera Control Bus Functional Specification

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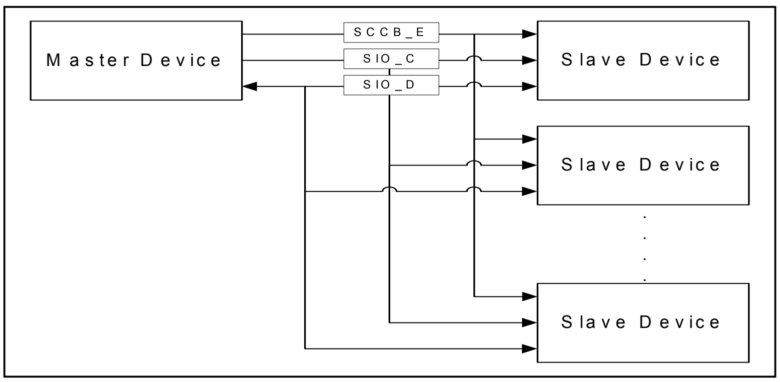
1. General Description

OmniVision Technologies Inc. has defined and deployed the Serial Camera Control Bus (SCCB), a three-wire serial bus, for controlling most of our CameraChip™ parts. In reduced pin package parts (typically 24 pin packages) the SCCB operates in a modified two-wire serial mode.

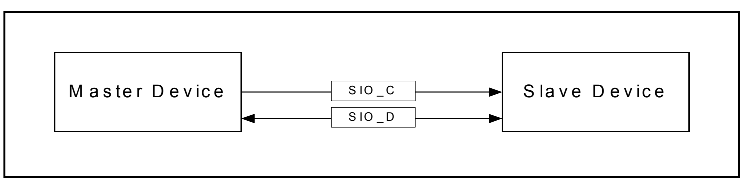
The OmniVision CameraChip devices will only operate as slave devices and the companion back-end interface must assert as the master. One SCCB master device can be connected to the SCCB to control at least one SCCB slave device. An optional suspend-control signal provides the capability for the SCCB master device to power down the SCCB system. The system diagram with three-wire connection is illustrated in Figure 1.

Figure 1. Block Diagram of the 3-Wire Implementation SCCB System



The modified two-wire implementation allows for a SCCB master device to interface with only one slave device. This two-wire application is implemented in the CameraChip™ reduced pin packaged products where the SCCB_E signal is not available externally. In the two-wire application the default for SCCB_E is Enabled and held low. The system diagram with two-wire connection is illustrated in Figure 2.

Figure 2. Block Diagram of the 2-Wire Implementation SCCB System



The two-wire implementation requires one of the following two master control methods in order to facilitate the SCCB communication.

1. In the first instance the master device must be able to support and maintain the data line of the bus in a tri-state mode.
2. The alternate method if the master cannot maintain a tri-state condition of the data line is to drive the data line either high or low and to note the transition there in to assert communications with the slave CameraChip.

1.1 *Terminology*

- **SCCB, Serial Camera Control Bus**
  Typically a three-wire serial bus with an optional suspend-control signal. May be implemented in a two-wire mode where required.
- **SCCB Master Device**
  A SCCB device that can assert SCCB transmissions. Only one master is allowed in the system.
- **SCCB Slave Device(s)**
  SCCB device(s) that can respond to an asserted SCCB transmission.
  At least one slave can be connected to the system.
- **The SCCB System**
  The system consists of one master and at least one slave.
- **SIO_C**
  The serial bus clock signal. Previously depicted as SIO1 and SCL in other documentation.
- **SIO_D**
  The serial bus data signal. Previously depicted as SIO0 and SDA in other documentation.
- **SCCB_E**
  The serial bus enable/disable signal. Previously depicted as SCS_, SCCBB, and IICB in other documentation.
- **SCCB Data Transmissions**
  Transmissions consist of phases. All transmissions initiated by master. Start and stop of a transmission are indicated in the three-wire system by signaling of the SCCB_E. Start and stop of a transmission are indicated in the two-wire system by signaling of the SIO_D.
- **Transmission Cycles**
  Transmission cycles include:
  3-phase write transmission cycle
  2-phase write transmission cycle
  2-phase read transmission cycle
- **Write Transmissions**
  Master-asserted transmissions which write data to slaves
- **Read Transmissions**
  Master=asserted transmissions which read data from slaves
- **Phases**
  A phase contains a total of 9 bits consisting of a sequential transmission of 8-data bits followed by a 9^{th} Don't-Care or NA bit, depending on writes or reads.
  The maximum number of allowable phases per transmission is three.
- **Write Phases**
  Phases that write data to slaves, including ID address, sub-address and actual data.
- **Read phases**
  Phases that read data from slaves.
- **Don't-Care Bit**
  The 9^{th} bit of a write phase
- **NA Bit**
  The 9^{th} bit of a read phase
- **ID address**
  Unique address of each device on the bus. The master asserts the slave ID address to identify transmissions destined for the slave device(s).
- **Sub-Address**
  Within the device address. The master asserts the sub-address to indicate the specific slave function/location to be accessed.
- **Suspend Mode**
  Master-asserted suspend periods of device and/or system suspension.

2. Pin-Outs & Descriptions

Table 1. Pinouts of the Master Device

Signal Name	I/O	Description
SCCB_E*	O	Serial Chip Select Output. The master drives SCCB_E at logical 1 when the bus is idle. Drives at logical 0 when the master asserts transmissions or the system is in Suspend mode.
SIO_C	O	Serial I/O Signal 1 Output. The master drives SIO_C at logical 1 when the bus is idle. Drives at logical 0 and 1 when SCCB Enable is driven at 0. Drives at logical 0 when the system is in Suspend mode.
SIO_D	I/O	Serial I/O Signal 0 Input and Output. Remains floating when the bus is idle, and drives to logical 0 when the system is in Suspend mode.
PWDN_	O	Power-Down Output

Table 2. Pinouts of Slave Device(s)

Signal Name	I/O	Description
SCCB_E*	I	Serial Chip Select Input. The input pad can be shut down when the system is in Suspend mode.
SIO_C	I	Serial I/O Signal 1 Input. The input pad can be shut down when the system is in Suspend mode.
SIO_D	I/O	Serial I/O Signal 0 Input and Output. The input pad can be shut down when the system is in Suspend mode.
PWDN	I	Power-Down Input

* Where SCCB_E is not present on the CameraChip™, this signal is by default enabled and held high.

3. Timing Diagram

This section defines the characteristics of SCCB for:

- SCCB_E
- SIO_C
- SIO_D
- Three-Wire Data Transmission
- Two-Wire Data Transmission
- Transmission Cycles
- Phases
- Suspend Mode

3.1 *SCCB_E*

SCCB_E is a single-directional, low-active control signal that must be driven by the master. It indicates the start of data transmission or stop of data transmission. A high-to-low transition of SCCB_E indicates a start of transmission, while a low-to-high transition of SCCB_E indicates a stop of transmission. SCCB_E must remain at logical 0 during a data transmission. A logical 1 of SCCB_E indicates that the bus is idle.

3.2 *SIO_C*

SIO_C is a single-directional, high-active control signal that must be driven by the master. It indicates each transmitted bit. The master must drive SIO_C at logical 1 when the bus is idle. A data transmission starts when SIO_C is driven at logical 0 after the start of transmission. A logical 1 of SIO_C during a data transmission indicates a single transmitted bit. Thus, SIO_D can occur only when SIO_C is driven at 0. The period of a single transmitted bit is defined as t_{cyc} in Figure 16. The minimum of t_{cyc} is 10μs.

3.3 *SIO_D – Three-Wire*

SIO_D is a bi-directional data signal that can be driven by either the master or slave devices. It remains floating, or tri-state, when the bus is idle. Maintenance of the signal is the responsibility of both the master and slave devices in order to avoid propagating an unknown bus state.

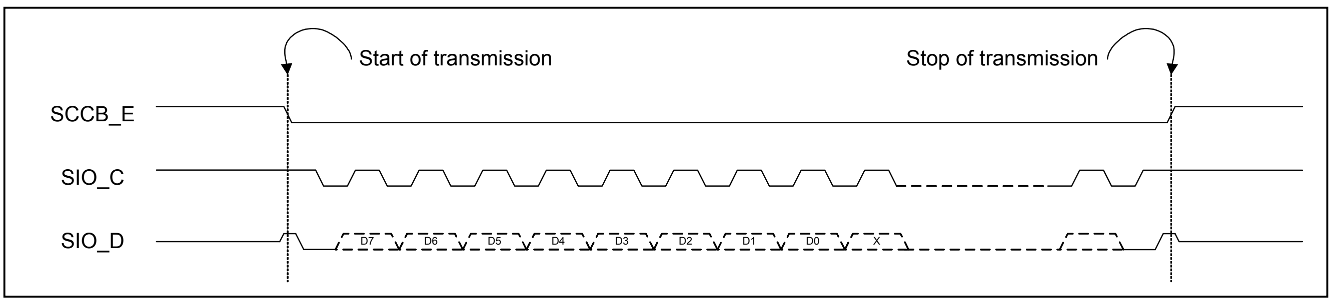
Bus float and contention are allowed during transmissions of Don't-Care or NA bit. The definition of the Don't-Care bit is described in section 3.7.4. The master must avoid propagating an unknown bus state condition when the bus is floating or conflicting. A conflict-protection resistor is required to reduce static current when the bus conflicts. The connection of the conflict-protection resistor is illustrated in Figure 23.

A single-bit transmission is indicated by a logical 1 of SIO_C. SIO_D can occur only when SIO_C is driven at logical 0. However, an exception is allowed at the beginning and the end of a data transmission. During the period that SCCB_E is asserted and before SIO_C goes to 0, SIO_D can be driven at 0. During the period that SIO_C goes to 1 and before SCCB_E is de-asserted, SIO_D can also be driven at 0.

3.4 *Three-Wire Data Transmission*

A graphic overview of SCCB three-wire data transmission is illustrated in Figure 3. The SCCB protocol allows for bus float and contention during data transmissions. Writing data to slaves is defined as a write transmission, while reading data from slaves is defined as a read transmission.

Figure 3. Timing Diagram of a Three-Wire Data Transmission

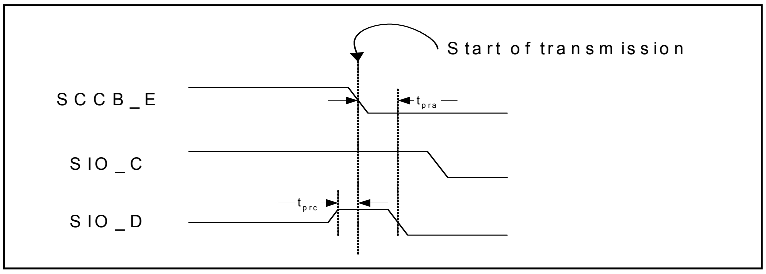


3.4.1 Three-Wire Start of Data Transmission

The start of data transmission in the three-wire implementation is indicated by a high-to-low transition of SCCB_E. Before asserting SCCB_E, the master must drive SIO_D at logical 1. This will avoid propagating an unknown bus state before the transmission of data. After de-asserting SCCB_E, the master must drive SIO_D at 1 for a defined period again to avoid unknown bus state propagation. This period, T_{psa} is defined as the post-active time of SCCB_E, and has a minimum value of 0 μs.

Two timing parameters are defined for start of transmission, t_{prc} and t_{pra}. The t_{prc} is defined as the pre-charge time of SIO_D. This indicates the period that SIO_D must be driven at logical 1 prior to assertion of SCCB_E. The minimum value of t_{prc} is 15ns. The t_{pra} is defined as the pre-active time of SCCB_E. This indicates the period that SCCB_E must be asserted before SIO_D is driven at logical 0. The minimum value of t_{pra} is 1.25μs. The three-wire start of transmission is illustrated in Figure 4.

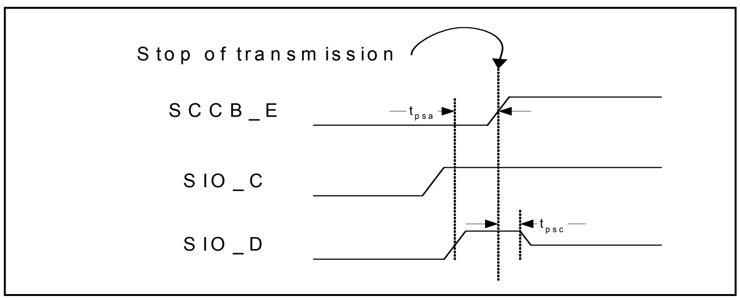
Figure 4. Three-Wire Start of Transmission



3.4.2 Three-Wire Stop of Data Transmission

A stop of data transmission is indicated by a low-to-high transition of SCCB_E. Two timing parameters are defined for stop of transmission: t_{psc} and t_{psa}. The t_{psc} is defined as the post-charge time of SIO_D. It indicates the period that SIO_D must remain at logical 1 after SCCB_E is de-asserted. The minimum value of t_{psc} is 15ns. The t_{psa} is defined as the post-active time of SCCB_E. It indicates the period that SCCB_E must remain at logical 0 after SIO_D is de-asserted. The minimum value of t_{psa} is 0ns. The three-wire stop of transmission is illustrated in Figure 5.

Figure 5. Three-Wire Stop of Transmission



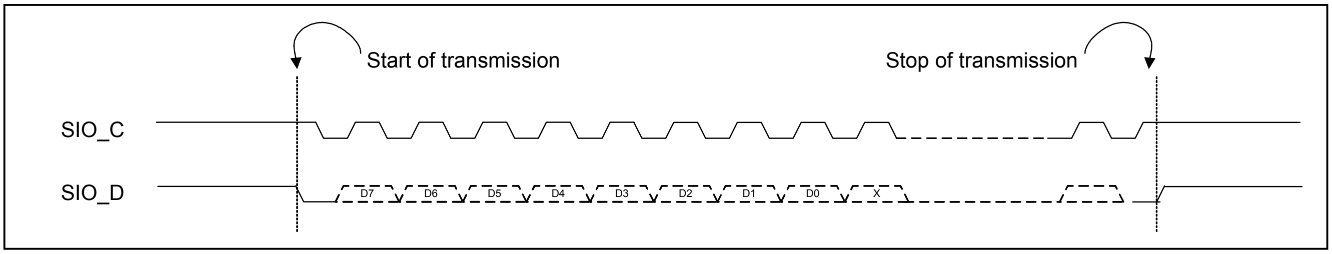
3.5 *Two-Wire Data Transmission*

As previously outlined herein, the two-wire data transmission is required in select 24-pin CameraChip packages. By default the SCCB_E is Enabled and held low. As is the case in the three-wire transmissions it is the responsibility of the companion back-end ASIC as the master to generate and supply the SIO_C signal, and to initiate and terminate data transfers to the slave. In the two-wire mode a system reset will transition the data line from tri-state to either high or low and will be used to indicate the start and stop transitions in place of the SCCB_E toggle.

A graphic overview of SCCB two-wire data transmission where the master can maintain the data line in a tri-state condition is illustrated in Figure 6. The SCCB two-wire transmission where the master is unable to maintain the data line in tri-state mode is illustrated in Figure 7. Again, in all instances writing data to the slave is defined as a write transmission, while reading data from the slave is defined as a read transmission.

Figure 6. Timing Diagram of a Two-Wire Data Transmission, Tri-State Supported

Figure 7. Timing Diagram of a Two-Wire Data Transmission, Tri-State Not Supported



3.5.1 Two-Wire Start of Data Transmission

The start of data transmission in the two-wire, tri-state-supported implementation is indicated by a transition from tri-state (floating) to high or "1" in the SIO_D signal followed by an assertion of the signal to low or "0". The SIO_C must be high or "1" during the assertion by of the SIO_D signal to low or "0". All transactions on the SIO_D signal can only occur when the SIO_C is low or "0". The tri-state supported start condition is illustrated in Figure 8.

The start of the data transmission in the two-wire, tri-state-not-supported implementation is slightly different from that of the tri-state-supported model. The master will drive the SIO_D signal high or "1" when the bus is idle. The start of data transmission will occur when the SIO_D is driven to low or "0" and SIO_C is high or "1". The non-tri-state supported start condition is illustrated in Figure 9.

A write or read operation will always be initiated by the master and only after the occurrence of the start condition. The write operation is completed only when the master asserts the stop condition or another start condition. Similarly, the read operation is completed only when the master asserts a stop condition or another start condition.

Figure 8. Two-Wire Start of Transmission – Tri-State Supported

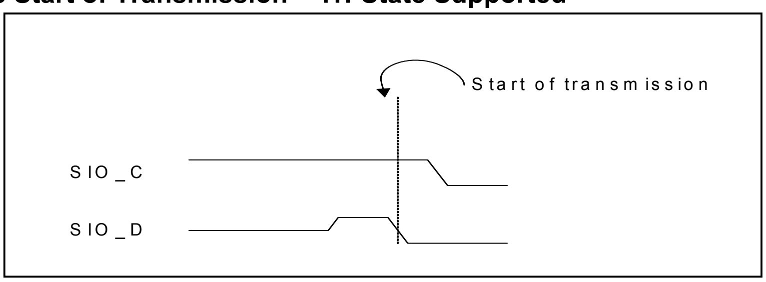
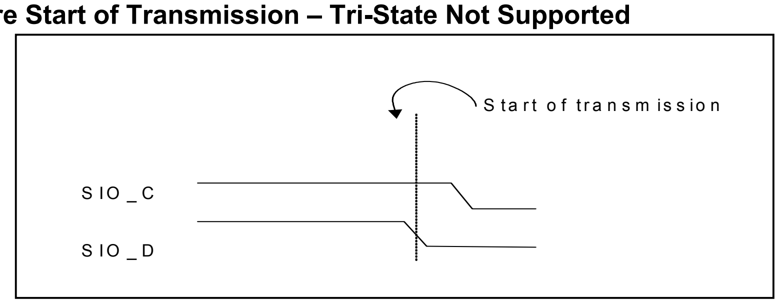


Figure 9. Two-Wire Start of Transmission – Tri-State Not Supported



3.5.2 Two-Wire Stop of Data Transmission

A stop of data transmission in the two-wire tri-state-supported implementation is indicated by a transition of the SIO_D signal from low or “0” to high or “1” while the SIO_C signal is high or “1”. Once SIO_D has transitioned to high and the stop transmission has occurred (a minimum time of 15ns) the master may then return the SIO_D signal to tri-state or floating condition. The tri-state-supported stop condition is illustrated in Figure 10.

The stop of data transmission in the two-wire tri-state-not-supported implementation is similar to the tri-state-supported model. The key difference will be that the master will not return the SIO_D to tri-state. The master will hold SIO_D high as well as maintain the SIO_C signal at high or “1”. The tri-state-not-supported stop condition is illustrated in Figure 11.

Figure 10. Two-Wire Stop of Transmission – Tri-State Supported

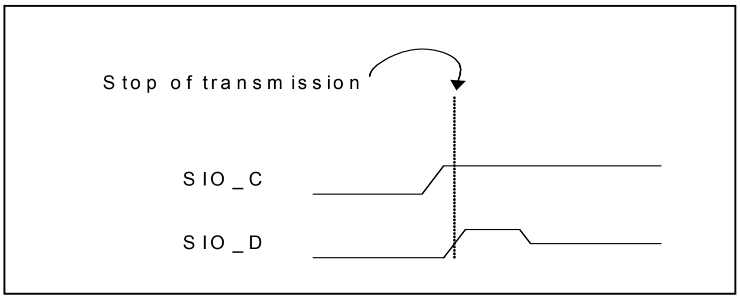
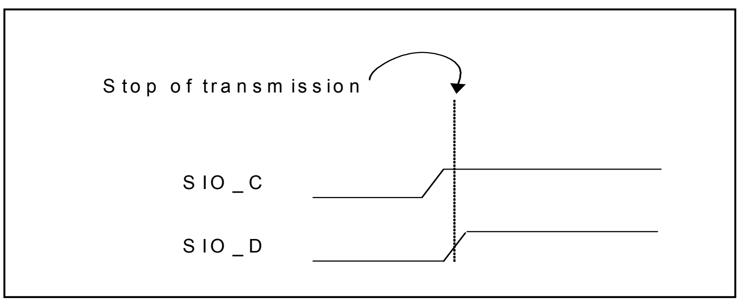


Figure 11. Two-Wire Stop of Transmission – Tri-State Not Supported



3.6 *Transmission Cycles*

A basic element of a data transmission is called a phase. This section describes the 3 kinds of transmissions:

3-phase write transmission cycle

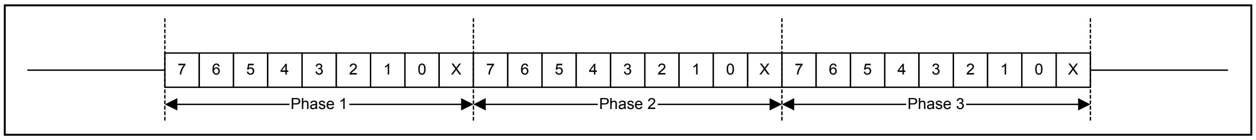
2-phase write transmission cycle

2-phase read transmission cycle

3.6.1 Phases of Transmissions

A phase contains a total of 9 bits. The 9 bits consist of an 8-bit sequential data transmission followed by a 9th bit. The 9th bit is a Don’t-Care bit or an NA bit, depending on whether the data transmission is write or read. The maximum number of phases that can be included in a transmission is three. The Most Significant Bit (MSB) is always asserted first for each phase.

Figure 12. Phases of Transmission

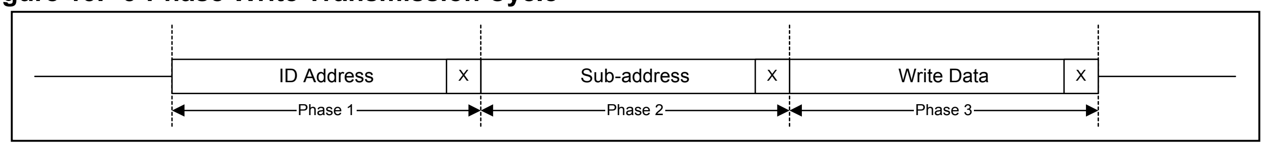


Phase 1: ID Address
Phase 2: Sub-address / Read data
Phase 3: Write Data

3.6.2 3-Phase Write Transmission Cycle

The 3-phase write transmission cycle is a full write cycle such that the master can write one byte of data to a specific slave(s). The ID address identifies the specific slave that the master intends to access. The sub-address identifies the register location of the specified. The write data contains 8-bit data that the master intends to overwrite the content of this specific address. The 9th bit of the three phases will be Don't-Care bits.

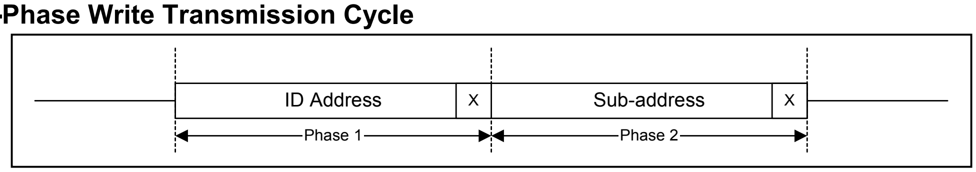
Figure 13. 3-Phase Write Transmission Cycle



3.6.3 2-Phase Write Transmission Cycle

The 2-phase write transmission cycle is followed by a 2-phase read transmission cycle. The purpose of issuing a 2-phase write transmission cycle is to identify the sub-address of some specific slave from which the master intends to read data for the following 2-phase read transmission cycle. The 9th bit of the two write transmission phases will be Don't-Care bits.

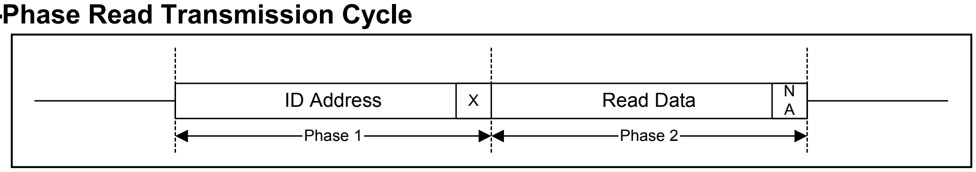
Figure 14. 2-Phase Write Transmission Cycle



3.6.4 2-Phase Read Transmission Cycle

There must be either a 3-phase or a 2-phase write transmission cycle asserted ahead of a 2-phase read transmission cycle. The 2-phase read transmission cycle has no ability to identify the sub-address. The 2-phase write transmission cycle contains read data of 8 bits and a 9th, NA bit. The master must drive the NA bit at logical 1.

Figure 15. 2-Phase Read Transmission Cycle



3.7 *Phase Descriptions*

This section describes the individual phases found in the various transmission cycles

3.7.1 Phase 1

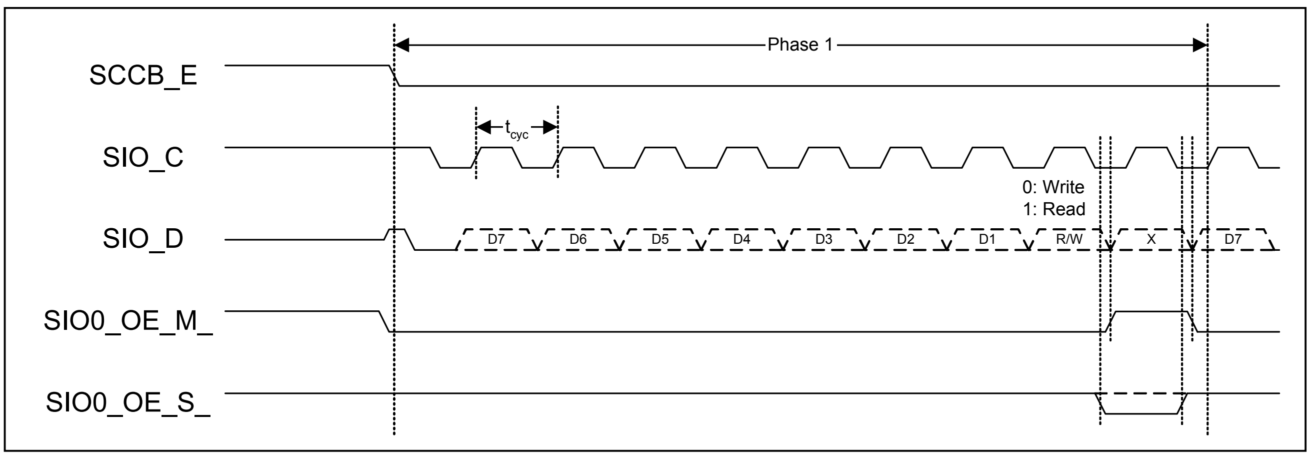
Phase 1 is asserted by the master to identify the selected slave to which data is read or written. Each slave has a unique ID address. The ID address is comprised of 7 bits, ordered from bit 7 to bit 1, and can identify up to 128 slaves. The 8^{th,} bit, bit 0, is the read/write selector bit that specifies the transmission direction of the current cycle. A logical 0 represents a write cycle and a logical 1 represents a read cycle.

The 9th bit of the phase 1 must be a Don't-Care bit. SIO_D_OE_M_ and SIO_D_OE_S_ shown in Figure 9 are internal low-active I/O enabled signals in the master and slave(s) respectively. SIO_D_OE_S_ transaction occurs before the transition of SIO_D_OE_M_, as shown in Figure 16. The master asserts the ID address, but de-asserts the 9th bit, the Don't-Care bit. The master must mask the input of SIO_D during the period of the Don't-Care bit and force the input to 0 to avoid propagating an unknown bus state. The master continues asserting the following phases regardless of the response to the Don't-Care bit by the slave(s).

The SIO_OE_S is controlled by the slave(s) and may remain at logical 1, or be driven at logical 0. The bus may be in a floating or conflicting status during the transmission of the Don't-Care bit. In this case, it is the slaves' responsibility to avoid propagating an unknown bus state.

A detailed description of the Don't-Care bit is described in section 3.7.4.

Figure 16. Phase 1 – ID Address

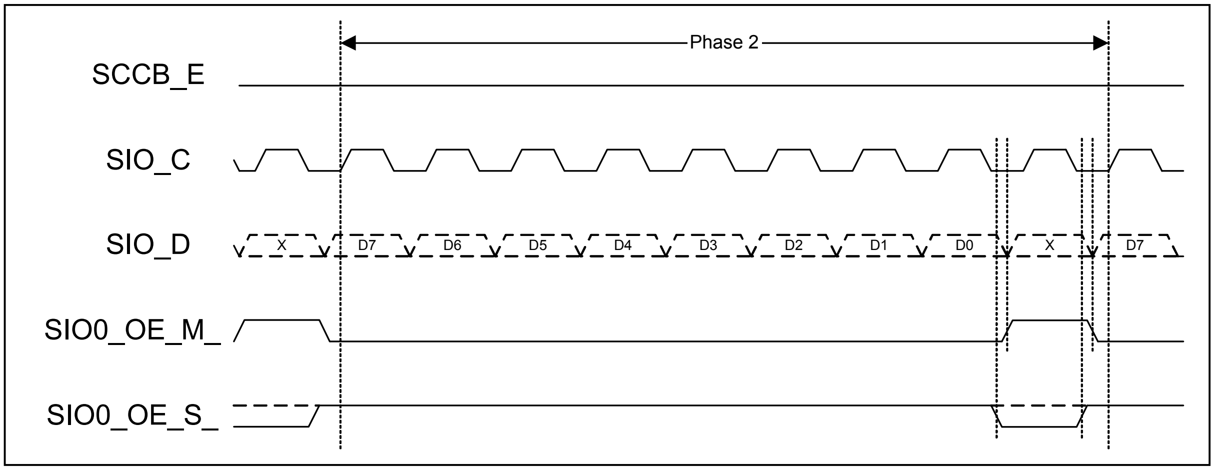


3.7.2 Phase 2

Either the master or the slave(s) may assert a phase 2 transmission. A phase 2 transmission asserted by the master identifies the sub-address of the slave(s) the master intends to access. A phase 2 transmission asserted by the slave(s) indicates the read data that the master will receive. The slave(s) recognize the sub-address of this read data according to previous 3-phase or 2-phase write transmission cycles.

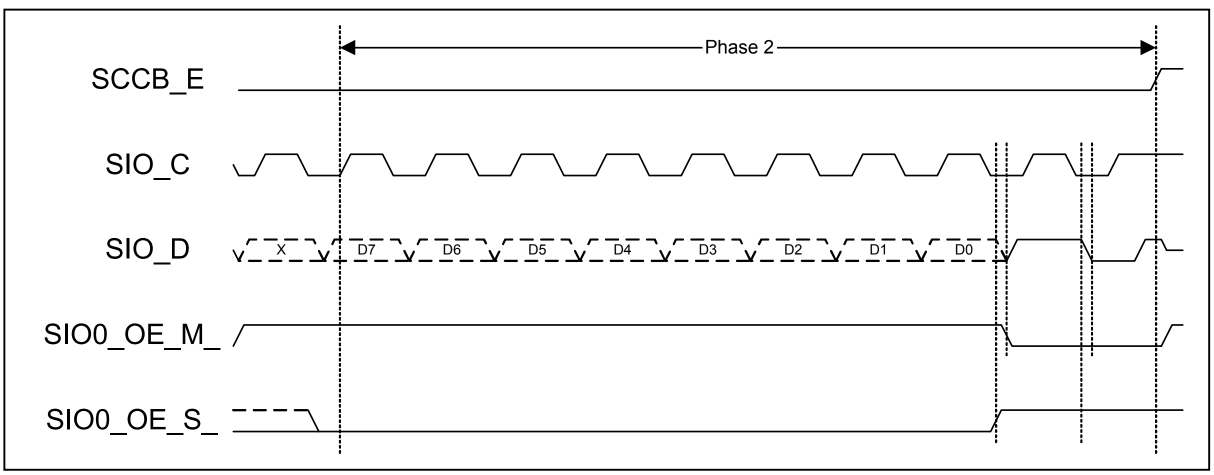
The 9th bit is defined as a Don't-Care bit when the master asserts the phase 2. SIO_D_OE_M_ and SIO_D_OE_S_ are the same as those defined in section 3.7.1. The detailed timing is illustrated in Figure 17.

Figure 17. Phase 2 – Sub-address (3-Phase Write Transmission)



The 9th bit is defined as an NA bit when the slave(s) assert the phase 2 transmission. SIO_D_OE_M_ is de-asserted from the 9th bit of phase 1 and is re-asserted for the NA bit. The master is responsible for driving SIO_D at logical 1 during the period of the NA bit. Concurrently, SIO_D_OE_S_ is asserted. The selected slave is responsible to drive SIO_D during the read data period. Since SIO_D_OE_S_ is de-asserted before SIO_D_OE_M_ is asserted during the period of the NA bit, bus float of SIO_D occurs when the master tries to drive the NA bit. The detailed timing is illustrated in Figure 18.

Figure 18. Phase 2 – Read Data (2 Phase Read Transmission)

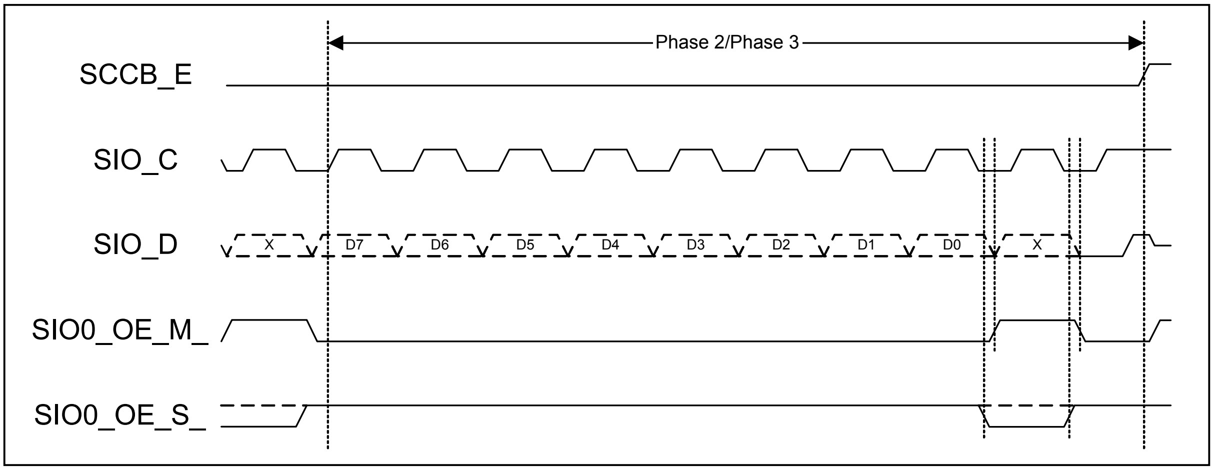


3.7.3 Phase 3

Only the master may assert the phase 3 transmission. The phase 3 transmission contains the actual data the master intends to write to the slave(s). The timing diagram shown in Figure 19 is for both the Phase 2 sub-address write transmission and the Phase 3 write data transmission.

The 9th bit of the phase 3 transmission is defined as a Don't-Care bit since the master is asserting the transmission. SIO_D_OE_M_ and SIO_D_OE_S_ are the same as those defined for a phase 1 transmission.

Figure 19. Phase 2/3 – Phase 2 Sub-address Write Transmission, Phase 3 Write Data Transmission



3.7.4 Don't-Care Bit

The Don't-Care bit is the 9^{th} bit of a master-issued transmission; ID address, sub-address and write data. The master will continue to assert transmission phases until the transmission cycle is complete. The master also assumes that there is no transmission error during data transmissions. The purpose of the Don't-Care 9^{th} bit is to indicate the completion of the transmission.

When there is more than one slave on the bus, the slave(s) may respond to the Don't-Care bit in one of two ways. If slave 1 is selected and data is written to this specific slave, slave 1 will drive SIO_D to logical 0 for the Don't-Care bit. In this case, the SIO_D signal may conflict at the beginning of the Don't-Care bit, while it may be floating at the end of the Don't-Care bit.

Alternately, it is possible that the slave(s) do not respond to the Don't-Care bit of the current phase. In this situation, the SIO_D bus remains at float for the whole Don't-Care bit.

The master does not check for transmission errors during data transmissions. There is a provision for the slave(s) to record the status of the Don't-Care bit in an internal register, as shown in the following example:

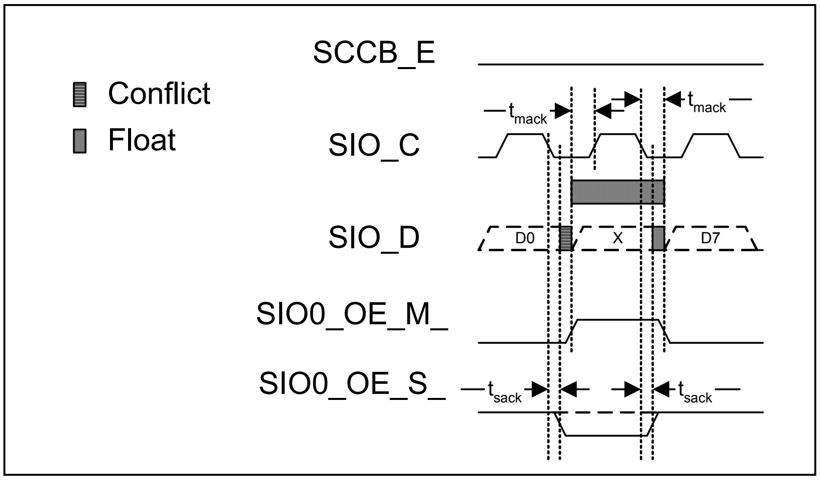
> *A slave(s) has defined a one-byte register as the Don't-Care Status Register. The default value of the Don't-Care Status Register is defined as 55. Assuming there are no errors during the data transmission, this register value will remain unchanged. If the slave does not receive the Don't-Care bit, the register value will change to 54.*

The master may query the Don't-Care Status Register to determine if there has been a transmission or data. The master will issue an additional read transmission to the Don't-Care Status Register in the target slave to check the value and subsequently determine if an error has occurred. This scheme will not determine an error if the entire SCCB circuit has been corrupted.

SIO_D_OE_M_ can be de-asserted and re-asserted during the Don't-Care bit transmission only when SIO_C is driven to logical 0. The t_{mack} is defined as the period of de-assertion of SIO_D_OE_M_ prior to the low to high transition of SIO_C during the Don't-Care bit transmission. The period of re-assertion of SIO_D_OE_M_ after the high-to-low transition is also defined as t_{mack}. The minimum value of t_{mack} is 1.25μs.

If a slave intends to respond to the Don't-Care bit, SIO_D_OE_S_ can be asserted and de-asserted during the Don't-Care bit transmission only when SIO_C is driven to logical 0. The t_{sack} is defined as the period of assertion of SIO_D_OE_S_ occurring after the high-to-low transition of SIO_C at the beginning of the Don't-Care bit transmission. The period of de-assertion of SIO_D_OE_S_ occurring after the high-to-low transition at the end of the Don't-Care bit transmission is also defined as t_{sack}. The minimum value of t_{sack} is 370ns.

Figure 20. Don't-Care Bit

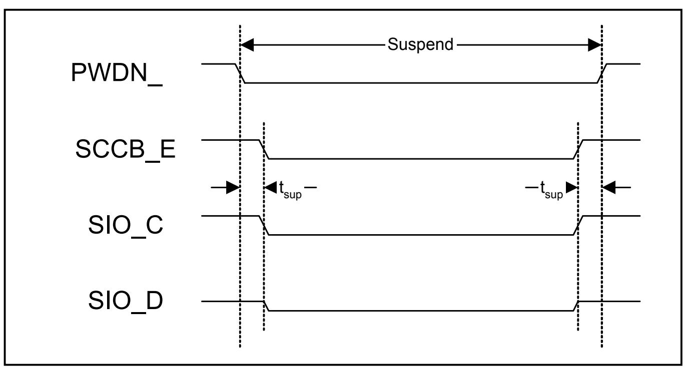


3.8 *Suspend Mode*

Suspend mode is determined by the dedicated PWDN_ pin of the master. This is achieved by the low-active output signal that specifies the suspension period as the master attempts to power-down the system. During the suspension period, SCCB_E, SIO_C and SIO_D are all driven to logical 0 by the master in order to avoid current leakage. There must be some time for PWDN_ to be asserted prior to and be de-asserted after the assertion of SCCB_E, SIO_D and SIO_C. This parameter is defined as t_{sup}. The minimum value of t_{sup} is 50ns. This scheme can prevent logical errors from occurring in SCCB slaves.

The PWDN pin in slaves has the opposite polarity of the PWDN_ pin of the master. Two control schemes for suspending the slave(s) are described in section 5.4.

Figure 21. Suspend Mode



4. Electrical Characteristics

Table 3. SCCB Electrical Characteristics

Symbol	Parameter	Condition	Min	Max	Unit
t_{cyc}	Single bit transmission cycle time	~	10	~	μs
t_{prc}	Pre-charge time of SIO_D	~	15	~	ns
t_{pra}	Pre-active time of SCCB_E	~	1.25	~	μs
t_{psc}	Post-charge time of SIO_D	~	15	~	ns
t_{psa}	Post-active time of SCCB ENABLE	~	0	~	μs
t_{mack}	SIO_D_OE_M_ transition time	~	1.25	~	μs
t_{sack}	SIO_D_OE_S_ transition time	~	370	~	ns
t_{sup}	PWDN_ pre/post-charge time	~	50	~	ns

5. Structure

The structure of the SCCB system is shown in Figure 15. This diagram illustrates the connection of one master with one slave. Multiple slaves may be connected on the same bus. A conflict-protection resistor of SIO_D is required for each slave. Connection of conflict-protection resistors for multiple slaves is illustrated in Figure 24.

Figure 22. Block Diagram of the Master and Slaves

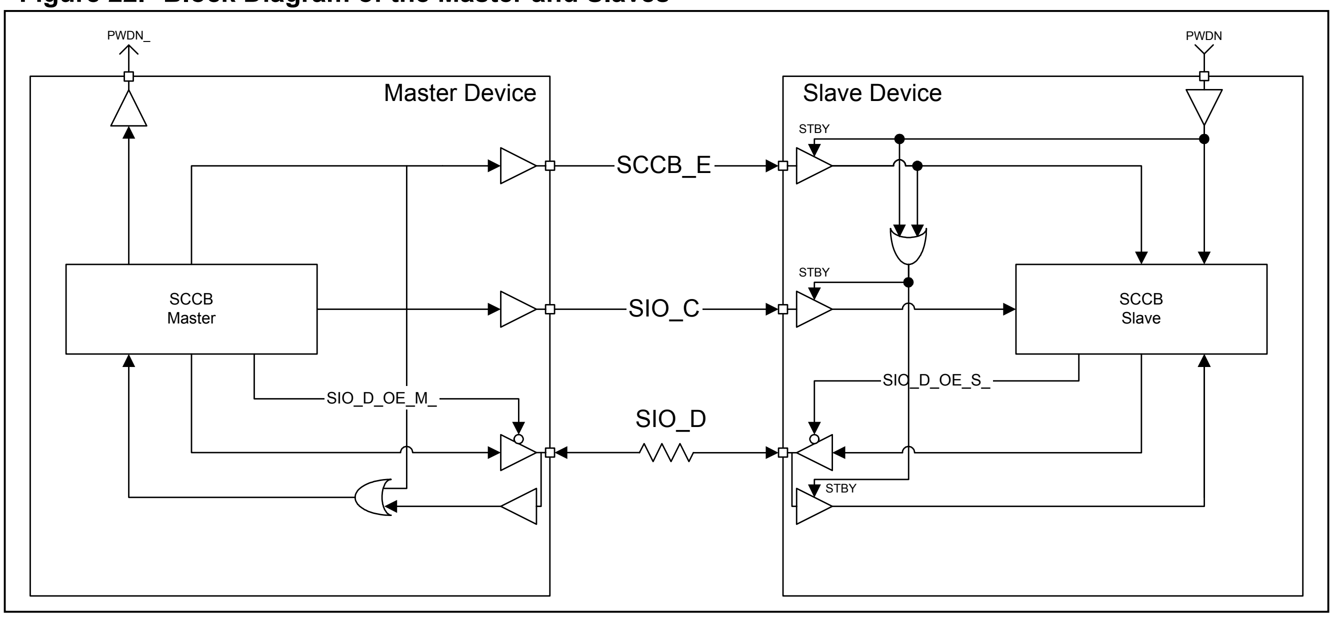
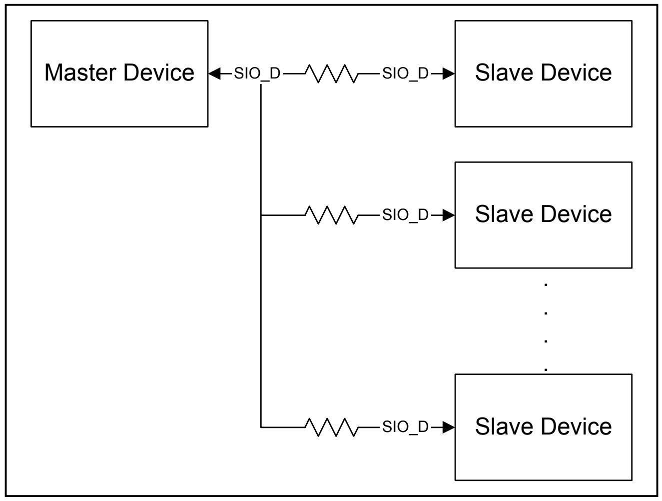


Figure 23. Connection of conflict-protection resistors



5.1 *The Master Device*

The master device drives both SCCB_E and SIO_C signals, while either the master or slave(s) can drive the SIO_D signal. During the de-assertion of SCCB_E, the master must block the SIO_D input to avoid propagating unknown bus conditions due to bus float. During the Don't-Care bit transmission, the master must ignore the status of SIO_D and keep asserting the subsequent phases.

The PWDN_ is driven by the master to indicate the suspend mode cycle. As noted in section 5.4, there are two different ways to implement suspension circuits within the system.

5.2 *Slave Devices*

The slave(s) receive the SCCB_E and SIO_C signals from the master, while either the master or the slave(s) can drive SIO_D. Input pads of the SCCB_E, SIO_C and SIO_D signals contain the standby (STBY) control terminal for reducing leakage current when the inputs are floating. Output terminals of those input pads are driven at logical 1 when STBY is asserted. This can avoid logical errors during suspend cycles.

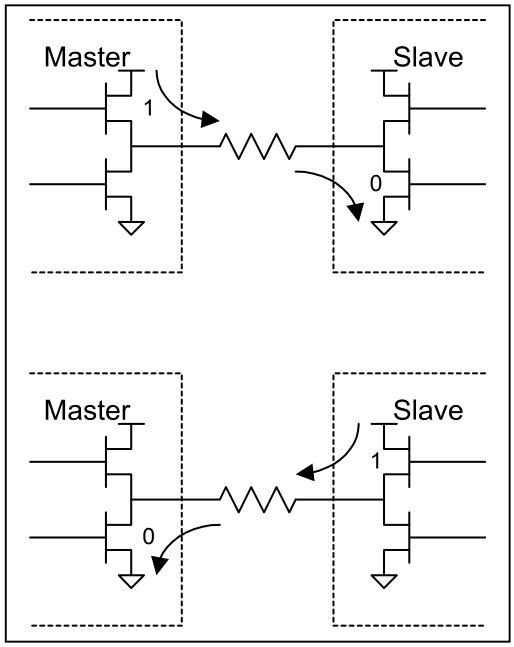
PWDN controls STBY of SCCB_E. This means the output terminal of the SCCB_E input pad is driven at logical 1 during suspend mode cycles even though the master drives the input of SCCB_E at 0.

The STBY control terminals of both SIO_C and SIO_D are controlled by PWDN and SCCB_E. During suspend mode cycles and the de-assertion of SCCB_E, the output terminals of SIO_C and SIO_D input pads are both driven at logical 1. During the Don't-Care bit transmission, the slave(s) must avoid propagating unknown bus conditions.

5.3 *Conflict-Protection Resistors*

Incorporating series resistors between the SIO_D output of the master and the SIO_D input of the slave(s) can avoid short circuits when bus contention occurs.

Figure 24. Conflict-protection Resistors



5.4 *Suspend Circuits*

There is two methods for issuance of a bus suspend cycle: using the PWDN mode or the Switch mode as noted herein.

5.4.1 PWDN Mode

The power pads of the slave(s) are always connected to VDD. The PWDN_ signal from the master device need to be inverted prior to connection to the slave(s) and the slave(s) circuit has an opposite polarity. During normal operations, PWDN_ of the master is driven at logical 1 and the NPN transistor is ON. In normal operation the PWDN of the slave(s) is driven at logical 0. During the suspend mode cycle, PWDN_ is driven at 0 and the NPN transistor is OFF. During suspend mode operation the PWDN of the slave(s) is driven at 1. There is no leakage current during the suspend cycle.

5.4.2 Switch Mode

The PWDN circuit of the slave(s) is always connected to logical 0. A power switch circuit is required for each slave. The power of each slave is OFF during suspend mode cycles. In suspend mode operation there is no leakage current present as no power is provided to the slave(s).

Figure 25. Suspend Circuit – PWDN Mode

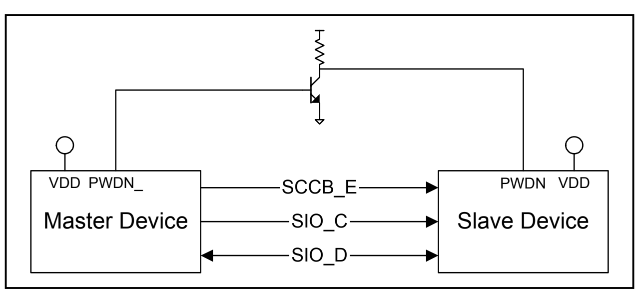
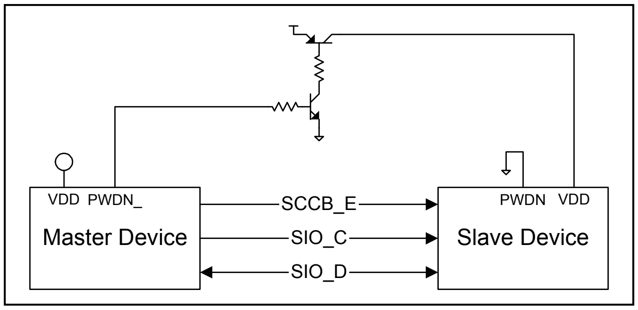


Figure 26. Suspend Circuit – Switch Mode



6. Revision History

Revision	Comment
1.01	Nomenclature change entire document – SIO1 change to SIO_C, SIO0 change to SIO_D, SCS_ change to SCCB Enable
2.0	Inclusion of section 3.5 documenting the two-wire master/slave implementation where SCCB_E is not available in the CameraChip™.