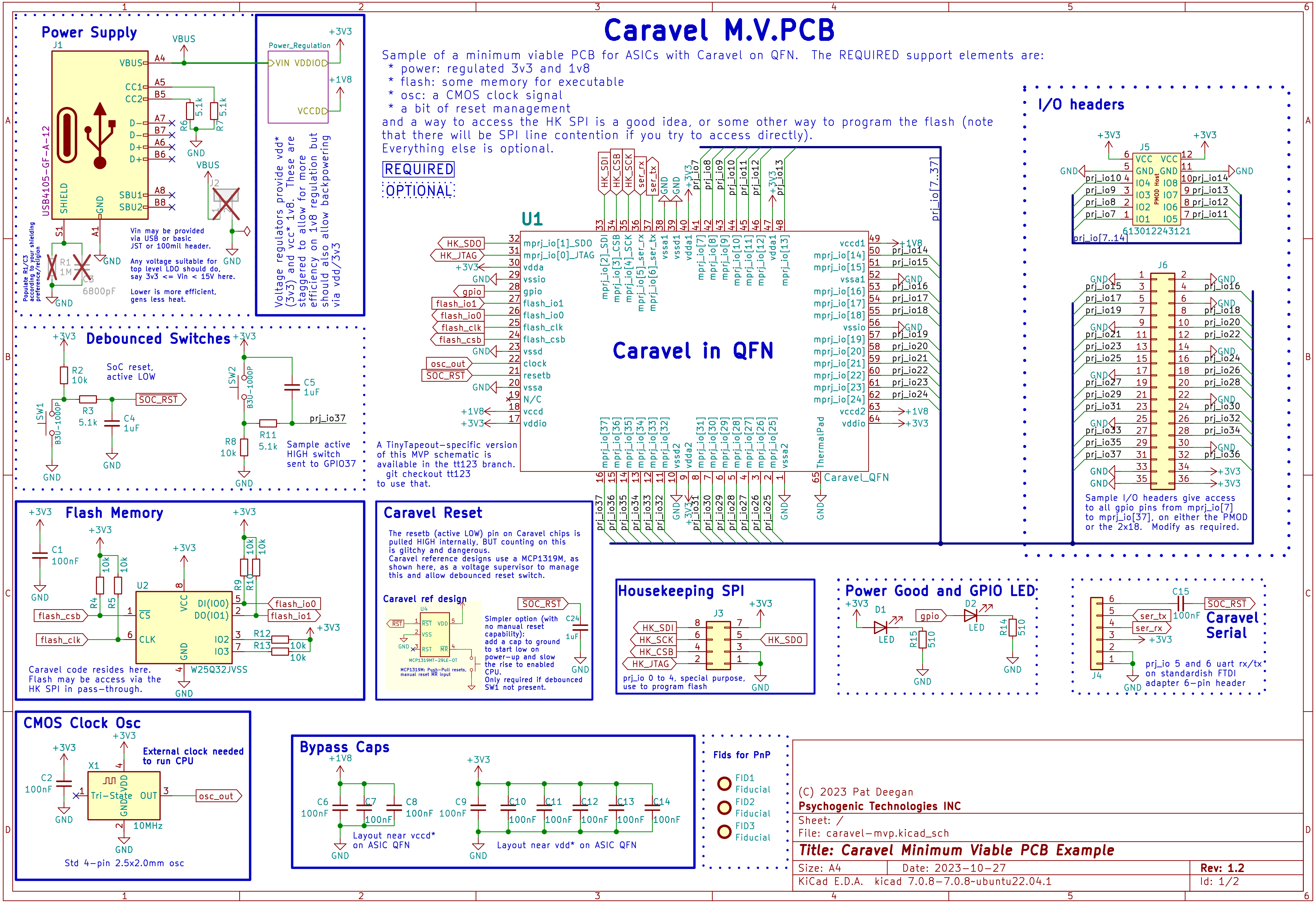
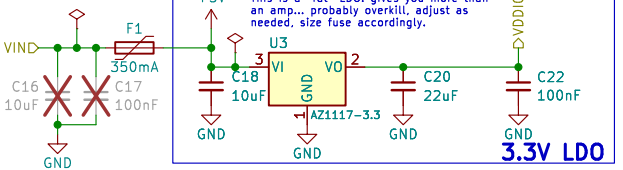
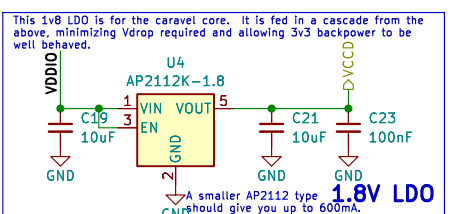

Caravel M.V.PCB
Sample of a minimum viable PCB for ASICs with Caravel on QFN. The REQUIRED support elements are:
* power: regulated 3v3 and 1v8
* flash: some memory for executable
* osc: a CMOS clock signal
* a bit of reset management
and a way to access the HK SPI is a good idea, or some other way to program the flash (note that there will be SPI line contention if you try to access directly).
Everything else is optional.
REQUIRED
OPTIONAL
Power Supply
Power_Regulation
Voltage regulators provide vdd* (3v3) and vcc* 1v8. These are staggered to allow for more efficiency on 1v8 regulation but should also allow backpowering via vdd/3v3
Vin may be provided via USB or basic JST or 100mil header.
Any voltage suitable for top level LDO should do, say 3v3 <= Vin < 15V here.
Lower is more efficient, gens less heat.
Populate R1/C3 according to your shielding preference/religion
Debounced Switches
SoC reset, active LOW
Sample active HIGH switch sent to GPIO37
U1
Caravel in QFN
Caravel_QFN
A TinyTapeout-specific version of this MVP schematic is available in the tt123 branch.
git checkout tt123
to use that.
I/O headers
Sample I/O headers give access to all gpio pins from mprj_io[7] to mprj_io[37], on either the PMOD or the 2x18. Modify as required.
Flash Memory
Caravel code resides here. Flash may be access via the HK SPI in pass-through.
W25Q32JVSS
Caravel Reset
The resetb (active LOW) pin on Caravel chips is pulled HIGH internally, BUT counting on this is glitchy and dangerous.
Caravel reference designs use a MCP1319M, as shown here, as a voltage supervisor to manage this and allow debounced reset switch.
Caravel ref design
Simpler option (with no manual reset capability): add a cap to ground to start low on power-up and slow the rise to enabled CPU.
Only required if debounced SW1 not present.
Housekeeping SPI
prj_io 0 to 4, special purpose, use to program flash
Power Good and GPIO LED
Caravel Serial
prj_io 5 and 6 uart rx/tx on standardish FTDI adapter 6-pin header
CMOS Clock Osc
External clock needed to run CPU
10MHz
Std 4-pin 2.5x2.0mm osc
Bypass Caps
Layout near vccd* on ASIC QFN
Layout near vdd* on ASIC QFN
Fids for PnP
FID1 Fiducial
FID2 Fiducial
FID3 Fiducial
(C) 2023 Pat Deegan
Psychogenic Technologies INC
Sheet: /
File: caravel-mvp.kicad_sch
Title: Caravel Minimum Viable PCB Example
Size: A4
Date: 2023-10-27
Rev: 1.2
KiCad E.D.A. kicad 7.0.8-7.0.8~ubuntu22.04.1
Id: 1/2

Voltage Regulators

Simple voltage regulation for logic and core. In a distinct sheet to allow you to easily do fancy stuff, like use switchers or whatever is needed.





Psychogenic Technologies INC

Sheet: /Power_Regulation/
File: power_reg.kicad_sch

Title: Voltage Regulation

Size: User	Date: 2023-09-30	**Rev: 1.1**
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