Caravel M.V.PCB: TinyTapeout Variant

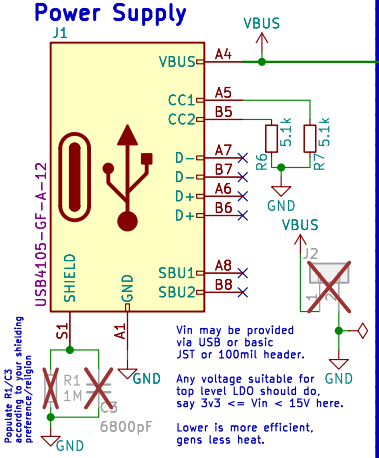
Sample of a minimum viable PCB for ASICs with Caravel on QFN. The REQUIRED support elements are:
* power: regulated 3v3 and 1v8
* flash: some memory for executable
* osc: a CMOS clock signal

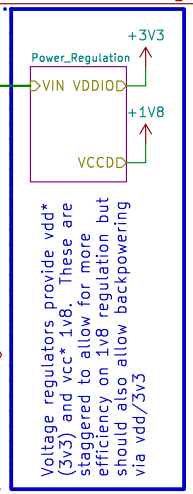
REQUIRED / OPTIONAL

and a way to access the HK SPI is a good idea. Everything else is optional.

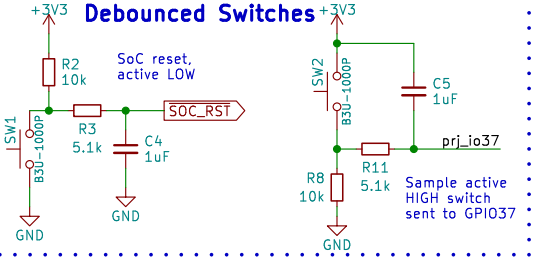
This version has a symbol and net names to match TinyTapeout function assignments.

Power Supply

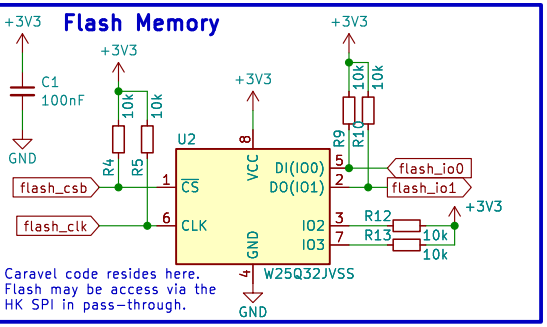




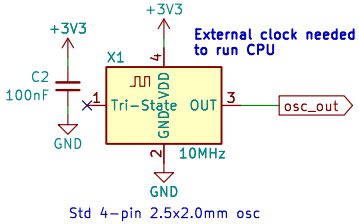
Debounced Switches



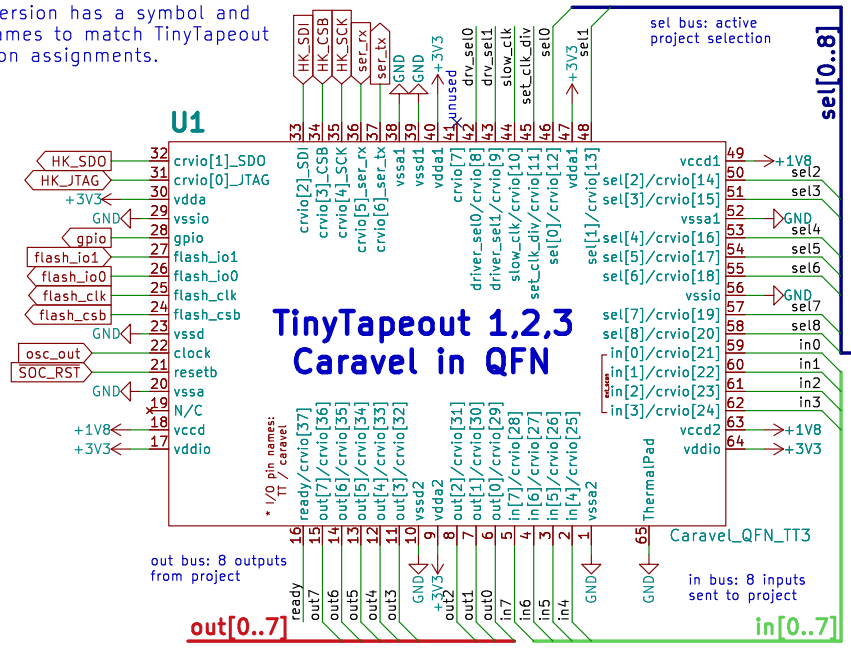
Flash Memory



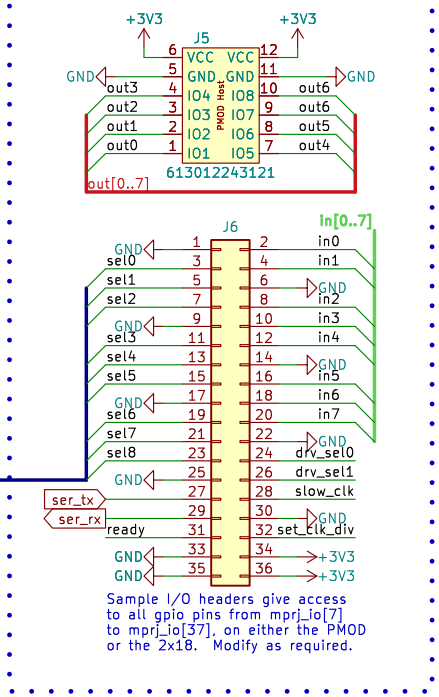
CMOS Clock Osc



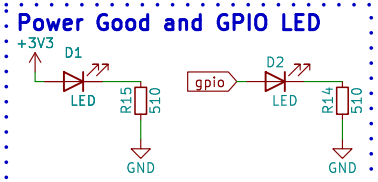
TinyTapeout 1,2,3 Caravel in QFN



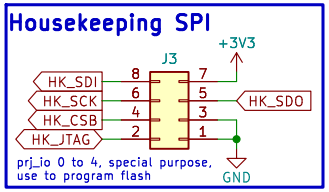
I/O headers

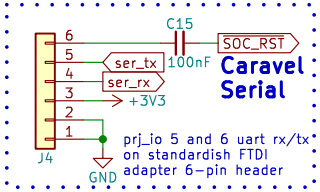


Power Good and GPIO LED

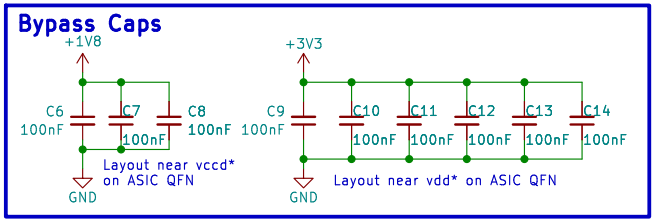


Housekeeping SPI





Bypass Caps



Fids for PnP

FID1 Fiducial
FID2 Fiducial
FID3 Fiducial

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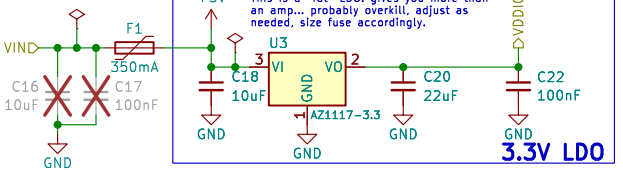
Sheet: /
File: caravel-mvp.kicad_sch

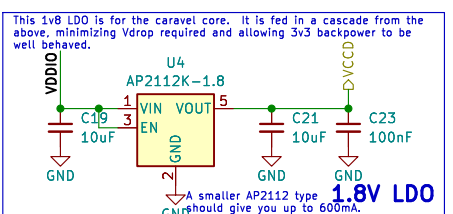
Title: Caravel Minimum Viable PCB Example: TinyTapeout Version

Size: A4	Date: 2023-09-30	**Rev: 1.0**
KiCad E.D.A. kicad 7.0.8-7.0.8~ubuntu22.04.1		Id: 1/2

Voltage Regulators

Simple voltage regulation for logic and core. In a distinct sheet to allow you to easily do fancy stuff, like use switchers or whatever is needed.



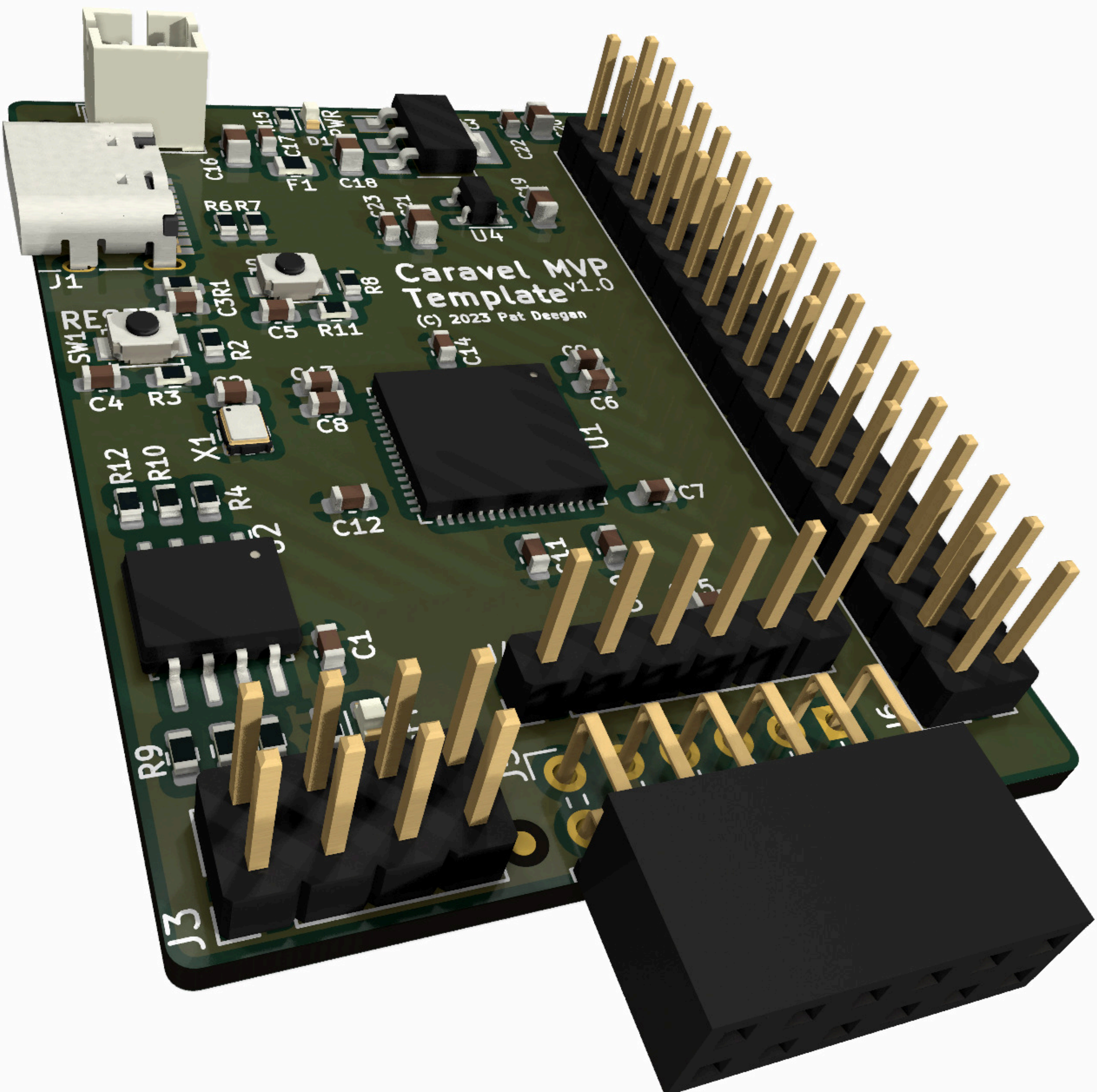


Psychogenic Technologies INC

Sheet: /Power_Regulation/
File: power_reg.kicad_sch

Title: Voltage Regulation

Size: User	Date: 2023-09-30	**Rev: 1.0**
KiCad E.D.A. kicad 7.0.8-7.0.8~ubuntu22.04.1		Id: 2/2


Caravel MVP
Template V1.0
(C) 2023 Pat Deegan
J1
J2
J3
SW1
C1
C3
C4
C5
C6
C7
C8
C11
C12
C14
C15
C16
C17
C18
C19
C21
C22
C23
D1
PWR
F1
R1
R2
R3
R4
R6
R7
R8
R9
R10
R11
R12
U1
U3
U4
X1