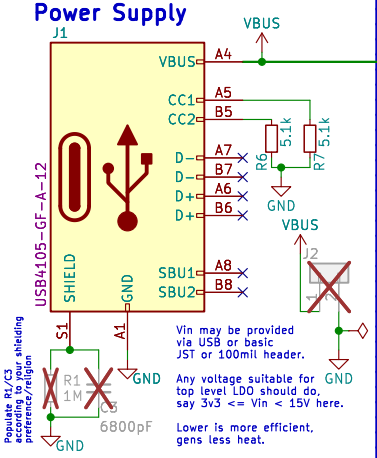
Caravel M.V.PCB

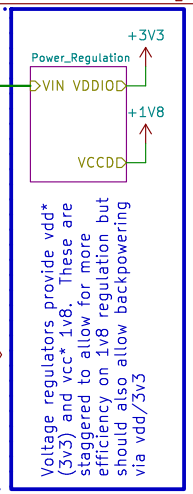
Sample of a minimum viable PCB for ASICs with Caravel on QFN. The REQUIRED support elements are:
* power: regulated 3v3 and 1v8
* flash: some memory for executable
* osc: a CMOS clock signal

REQUIRED / OPTIONAL

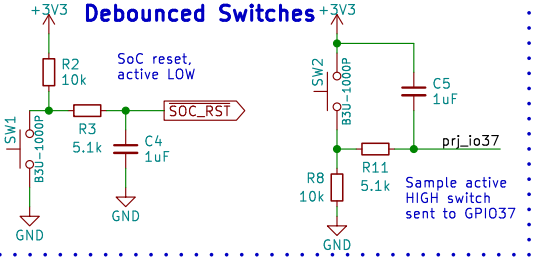
and a way to access the HK SPI is a good idea. Everything else is optional.

Power Supply

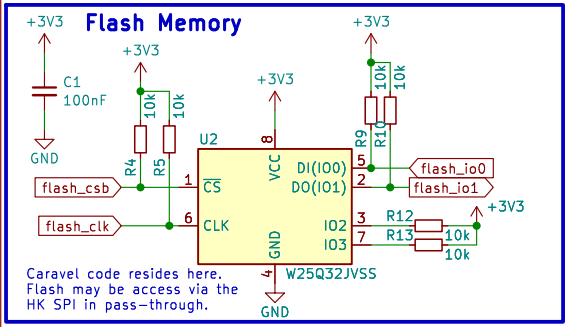




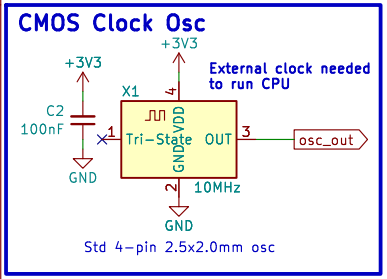
Debounced Switches



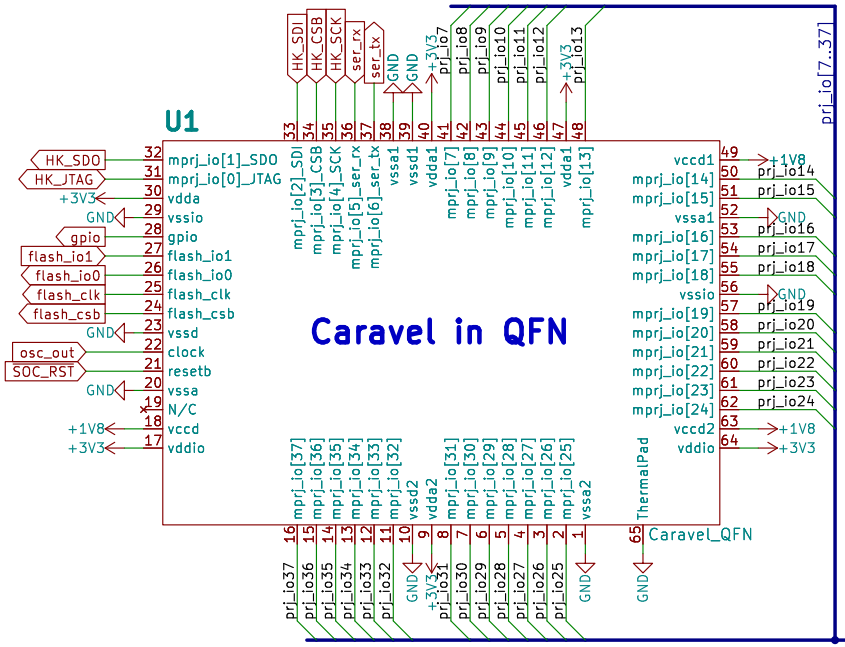
Flash Memory



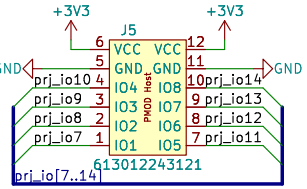
CMOS Clock Osc

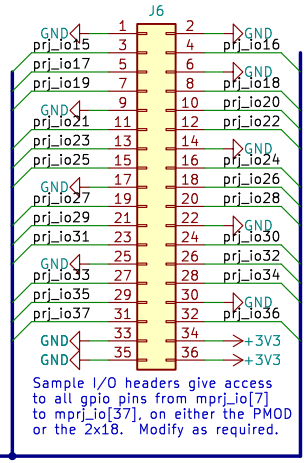


U1 — Caravel in QFN

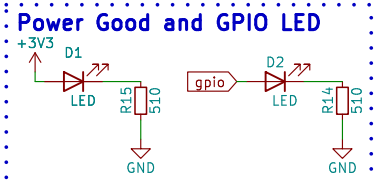


I/O headers

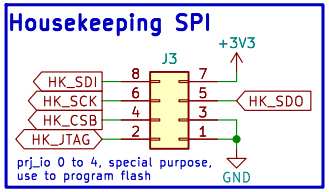


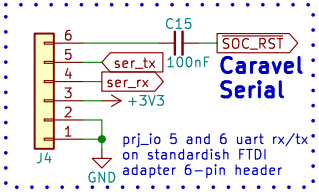


Power Good and GPIO LED

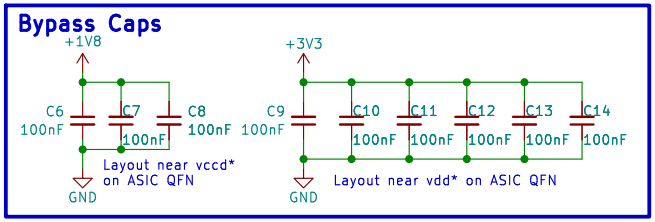


Housekeeping SPI





Bypass Caps



Fids for PnP

FID1 Fiducial
FID2 Fiducial
FID3 Fiducial

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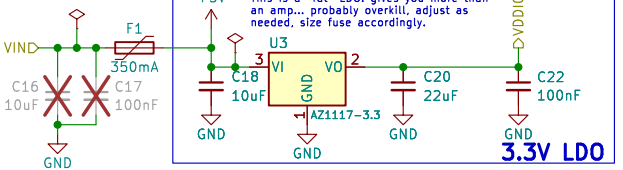
Sheet: /
File: caravel-mvp.kicad_sch

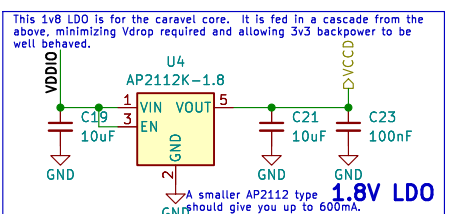
Title: Caravel Minimum Viable PCB Example

Size: A4	Date: 2023-09-30	Rev: 1.0
KiCad E.D.A. kicad 7.0.8-7.0.8~ubuntu22.04.1		Id: 1/2

Voltage Regulators

Simple voltage regulation for logic and core. In a distinct sheet to allow you to easily do fancy stuff, like use switchers or whatever is needed.





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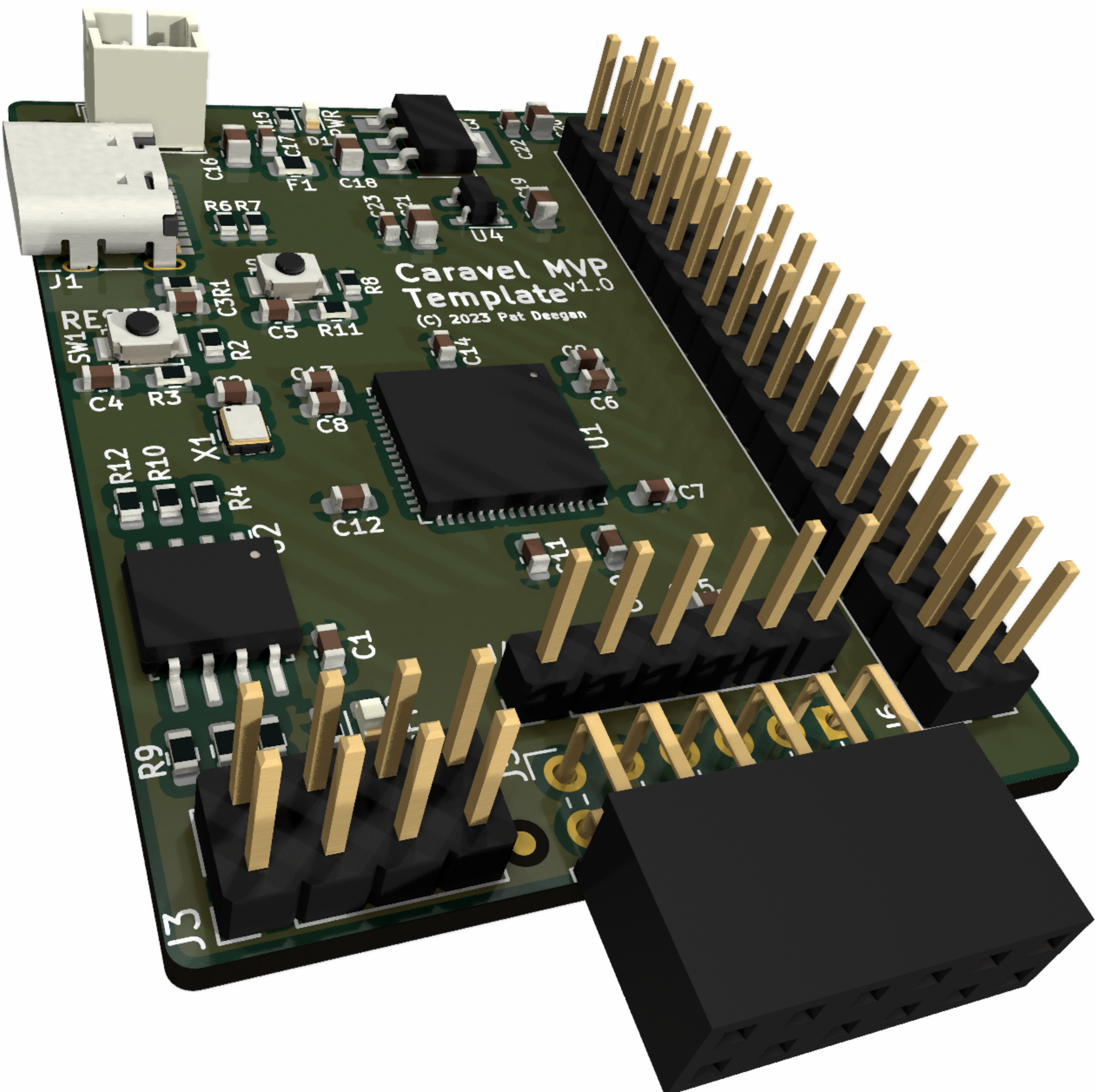
Sheet: /Power_Regulation/
File: power_reg.kicad_sch

Title: Voltage Regulation

Size: User	Date: 2023-09-30	**Rev: 1.0**
KiCad E.D.A. kicad 7.0.8-7.0.8~ubuntu22.04.1		Id: 2/2


Caravel MVP
Template V1.0
(C) 2023 Pat Deegen
SW1
C4
R3
R2
C3
R1
C5
R11
R8
C16
C15
C17
D1
PWR
F1
C18
R6
R7
U4
C22
C19
C14
C6
U1
C8
X1
R12
R10
R4
C12
C7
C11
C1
R9
J3
J4