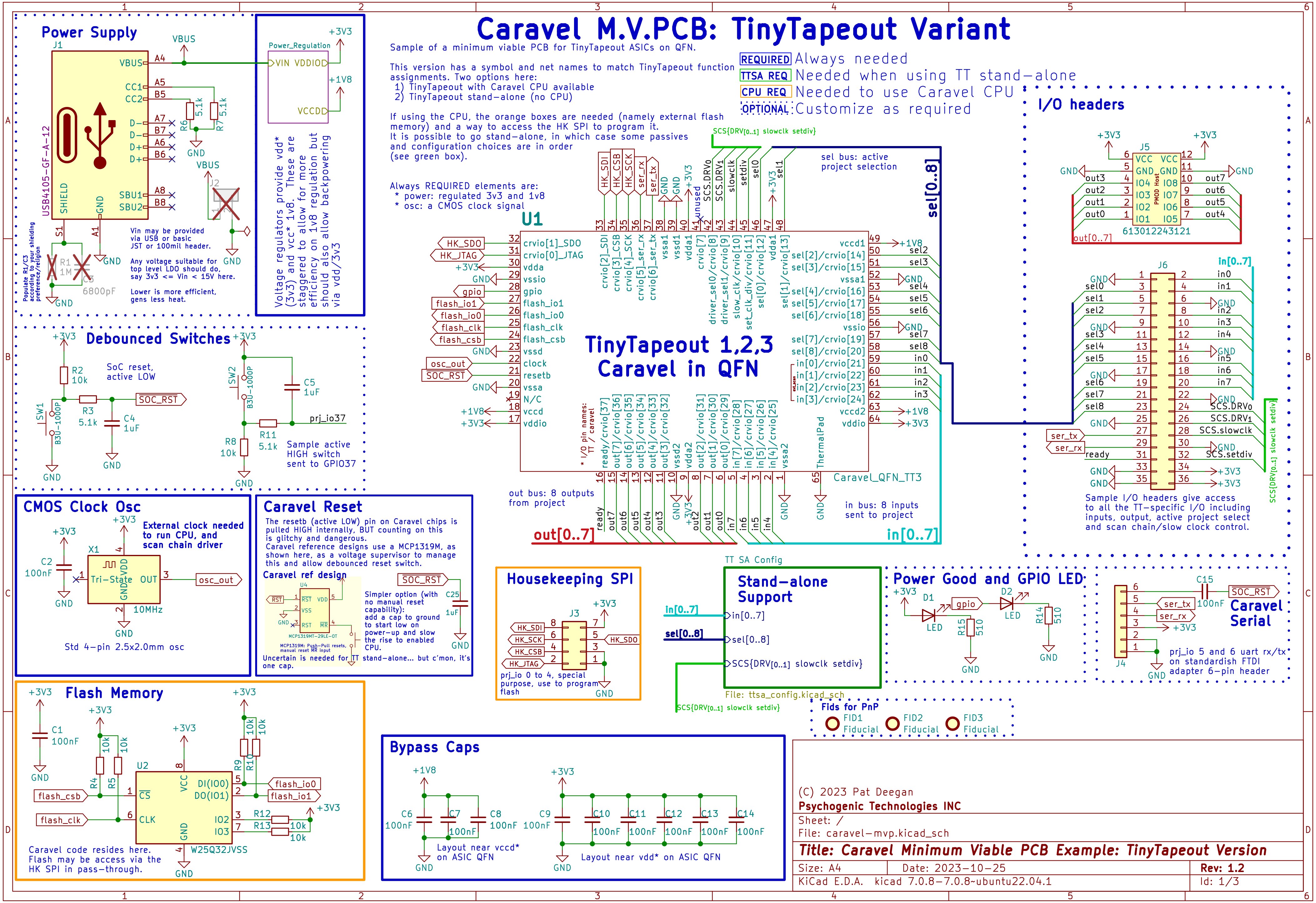
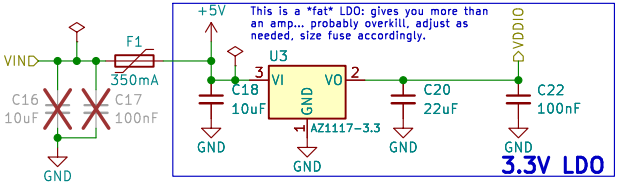


Caravel M.V.PCB: TinyTapeout Variant
Sample of a minimum viable PCB for TinyTapeout ASICs on QFN.
This version has a symbol and net names to match TinyTapeout function assignments. Two options here:
1) TinyTapeout with Caravel CPU available
2) TinyTapeout stand-alone (no CPU)
If using the CPU, the orange boxes are needed (namely external flash memory) and a way to access the HK SPI to program it.
It is possible to go stand-alone, in which case some passives and configuration choices are in order (see green box).
Always REQUIRED elements are:
* power: regulated 3v3 and 1v8
* osc: a CMOS clock signal
REQUIRED Always needed
TTSA REQ Needed when using TT stand-alone
CPU REQ Needed to use Caravel CPU
OPTIONAL Customize as required
Power Supply
J1
USB4105-GF-A-12
VBUS
Vin may be provided via USB or basic JST or 100mil header.
Any voltage suitable for top level LDO should do, say 3v3 <= Vin < 15V here.
Lower is more efficient, gens less heat.
Populate R1/C3 according to your shielding preference/religion
Power_Regulation
VIN VDDIO
VCCD
+3V3
+1V8
Voltage regulators provide vdd* (3v3) and vcc* 1v8. These are staggered to allow for more efficiency on 1v8 regulation but should also allow backpowering via vdd/3v3
Debounced Switches
SoC reset, active LOW
SOC_RST
Sample active HIGH switch sent to GPIO37
prj_io37
U1
TinyTapeout 1,2,3
Caravel in QFN
Caravel_QFN_TT3
sel bus: active project selection
sel[0..8]
out bus: 8 outputs from project
out[0..7]
in bus: 8 inputs sent to project
in[0..7]
SCS{DRV[0..1] slowclk setdiv}
I/O headers
J5
613012243121
J6
Sample I/O headers give access to all the TT-specific I/O including inputs, output, active project select and scan chain/slow clock control.
CMOS Clock Osc
External clock needed to run CPU, and scan chain driver
X1
10MHz
osc_out
Std 4-pin 2.5x2.0mm osc
Caravel Reset
The resetb (active LOW) pin on Caravel chips is pulled HIGH internally, BUT counting on this is glitchy and dangerous.
Caravel reference designs use a MCP1319M, as shown here, as a voltage supervisor to manage this and allow debounced reset switch.
Caravel ref design
Simpler option (with no manual reset capability): add a cap to ground to start low on power-up and slow the rise to enabled CPU.
Uncertain is needed for TT stand-alone... but c'mon, it's one cap.
Housekeeping SPI
J3
prj_io 0 to 4, special purpose, use to program flash
TT SA Config
Stand-alone Support
in[0..7]
sel[0..8]
SCS{DRV[0..1] slowclk setdiv}
File: ttsa_config.kicad_sch
Power Good and GPIO LED
Caravel Serial
J4
prj_io 5 and 6 uart rx/tx on standardish FTDI adapter 6-pin header
Fids for PnP
FID1 Fiducial
FID2 Fiducial
FID3 Fiducial
Flash Memory
U2
W25Q32JVSS
Caravel code resides here. Flash may be access via the HK SPI in pass-through.
Bypass Caps
Layout near vccd* on ASIC QFN
Layout near vdd* on ASIC QFN
(C) 2023 Pat Deegan
Psychogenic Technologies INC
Sheet: /
File: caravel-mvp.kicad_sch
Title: Caravel Minimum Viable PCB Example: TinyTapeout Version
Size: A4
Date: 2023-10-25
Rev: 1.2
KiCad E.D.A. kicad 7.0.8-7.0.8~ubuntu22.04.1
Id: 1/3

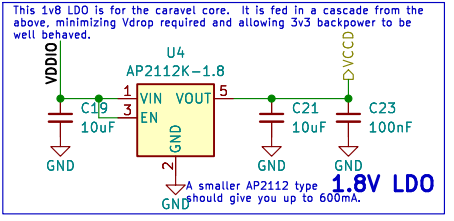
Voltage Regulators

Simple voltage regulation for logic and core. In a distinct sheet to allow you to easily do fancy stuff, like use switchers or whatever is needed.



NOTE: On our simple TinyTapeout demo boards, with power good LEDs and everything, idle draw on the 3v3 supply was below 40mA, so both the 3v3 and the 1v8 LDOs have more than a little margin.

Chances are you could get away with much (much) smaller regulators and maybe even a zener diode shunt type thing for the 1v8 core.



Psychogenic Technologies INC

Sheet: /Power_Regulation/

File: power_reg.kicad_sch

Title: Voltage Regulation

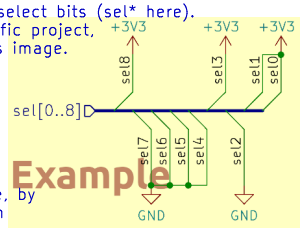
Size: User	Date: 2023-09-30	**Rev: 1.2**
KiCad E.D.A. kicad 7.0.8-7.0.8~ubuntu22.04.1		Id: 2/3

Stand-Alone TinyTapeout Reqs and Knobs

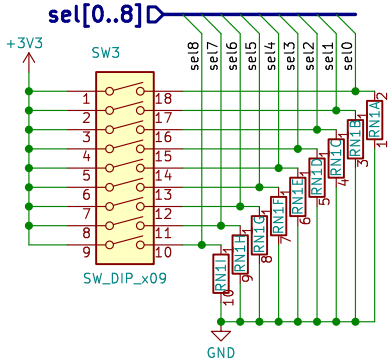
If not using the Caravel CPU, you can save space and cost by dumping its support components but that means you need to handle a bit of its work externally. Here are the related components and configs.

Project Selection

Projects are selected using the 9 active_select bits (sel* here).
If you're only interested in a single specific project, you can hardwire it here as shown in this image.
For example, I want project #267,
which in binary (MSB) is:
1 0000 1011
Bringing every '1' bit high and
tying ever '0' to ground,
will select this value.



Or we can make things more configurable, by using switches or other means. The main thing to consider is always ensuring the signals are in a defined state (pulled high or low, not floating).



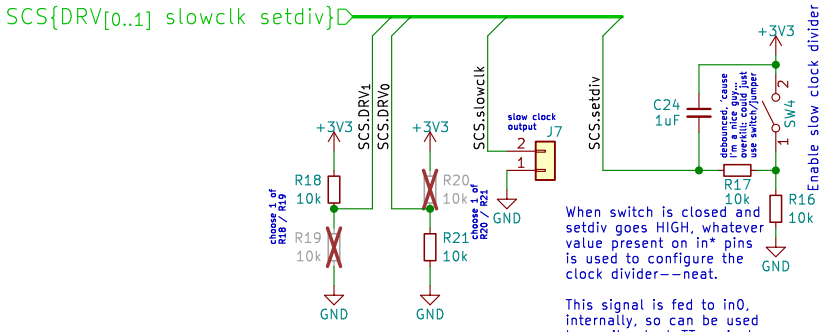
Rather than hard-wiring a selection, here is one scheme to allow any of the projects to be active using a DIP switch and resistor network.

When a switch is open, the line is pulled low. When it is closed, that bit goes high.

The pull down resistors on each sel* isn't required when you have everything you need to run the Caravel CPU because, as part of the running firmware, it is trivial to enable pull-up or -down on any of the I/O pins.

Scan Chain Driver And Clocking

The scan chain stuff is a little involved... best to refer to the TinyTapeout documentation.
Still, notes here should be somewhat helpful.



When switch is closed and setdiv goes HIGH, whatever value present on in* pins is used to configure the clock divider--neat.

This signal is fed to in0, internally, so can be used to easily clock TT projects.

The scan chain driver selection is done through these two pins.

DRV_1	DRV_0	setting
0	0	external
0	1	logic an.
1	X	internal

You mostly likely want internal, here, so populating as shown using DNPs.

Or you can use jumpers, such as in the TT demo board here: TinyTapeout 123 Demo PCB schematic

Input State

Depending on your use case, it might be worth ensuring the state of the input pins is always valid--i.e. using pull-ups or pull-downs. This is highly application specific but digital doesn't like floaties so much... worst case maybe just sit all the in* on some weak (high value) resistors to ground.

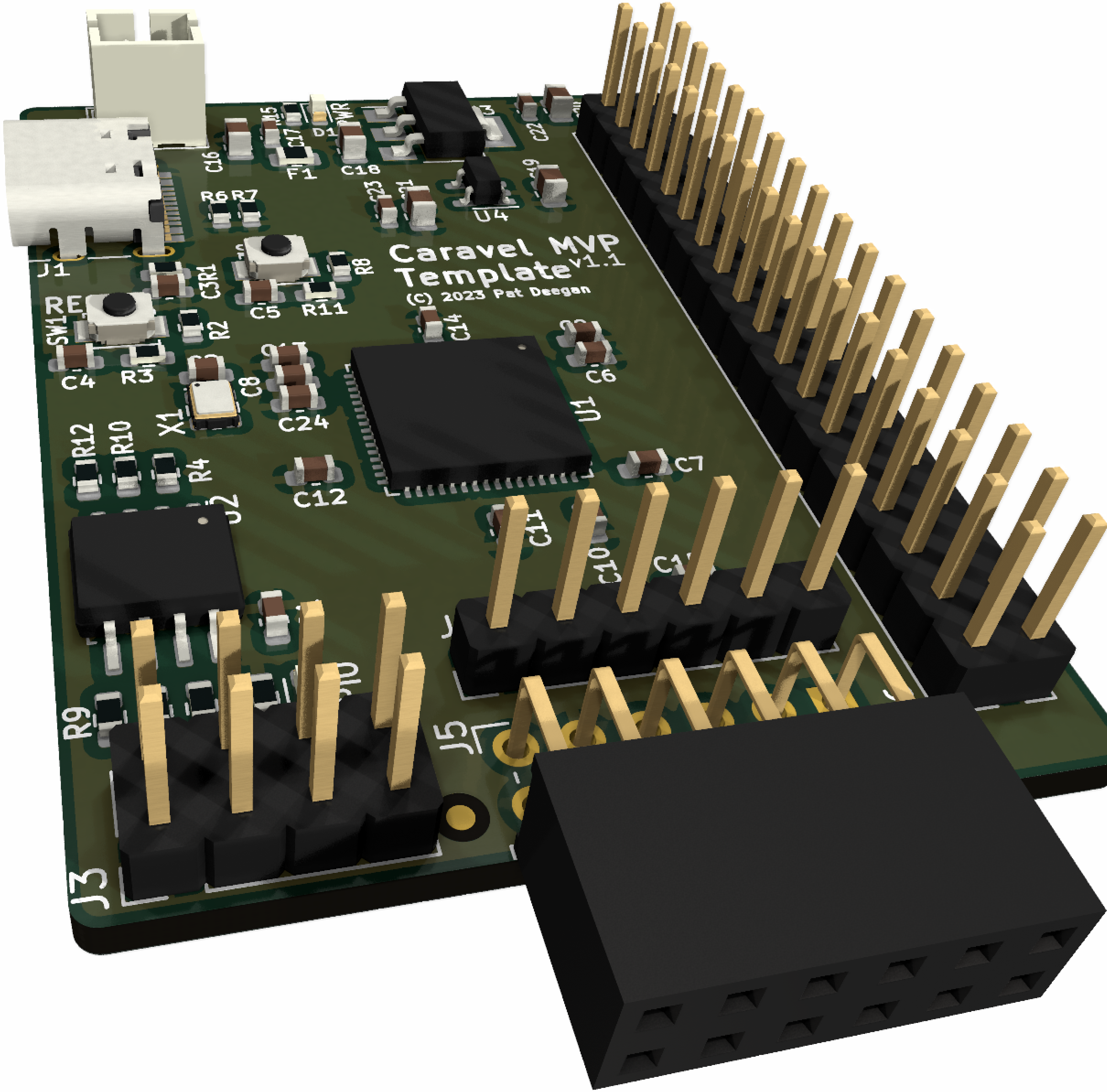
Note: none of these components are in the sample layout. This allows you to delete this sheet from the top level and not muck about, if you aren't going stand-alone.

Psychogenic Technologies INC

Sheet: /TT SA Config/
File: ttsa_config.kicad_sch

Title: Stand-Alone TinyTapeout Requirements and Config

Size: A4	Date: 2023-10-24	**Rev: 1.2**
KiCad E.D.A. kicad 7.0.8-7.0.8~ubuntu22.04.1		Id: 3/3



Caravel MVP
Template v1.1
(C) 2023 Pat Deegan
J1
RE
SW1
C4
R3
R2
C3R1
C5
R11
R8
R6 R7
C16
F1
C17
D1
PWR
C18
C23
U4
C22
C19
C14
C6
U1
C8
C24
X1
R12
R10
R4
C12
C7
U2
C11
C10
J5
J3
R9