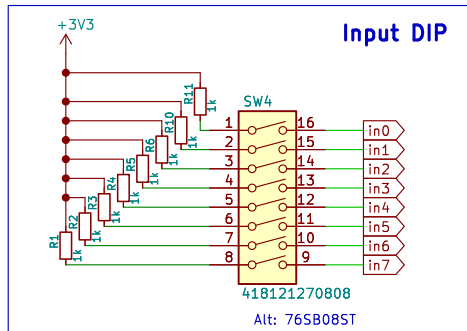
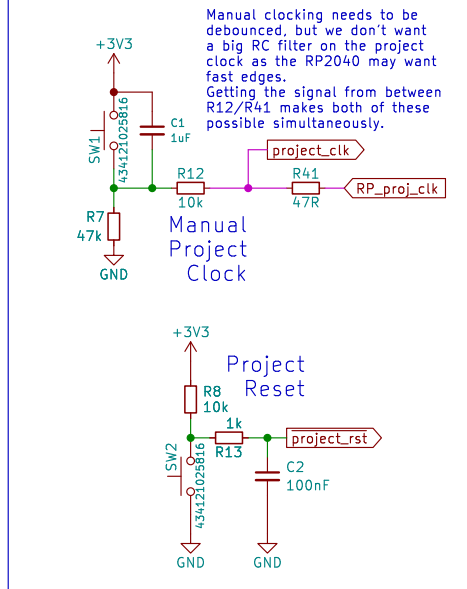


Tiny Tapeout 4/5 Demo Board

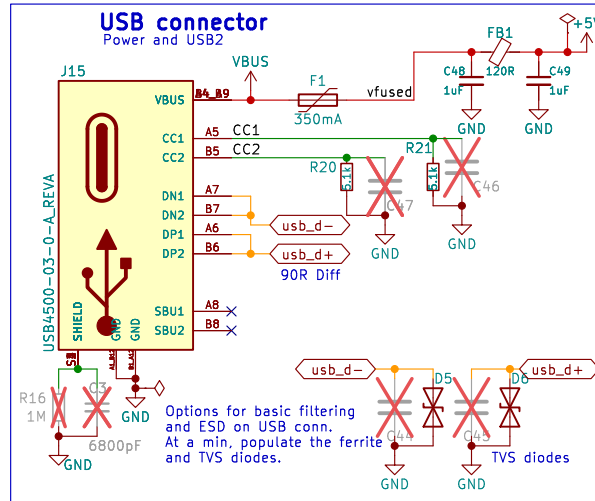
User Input + Config



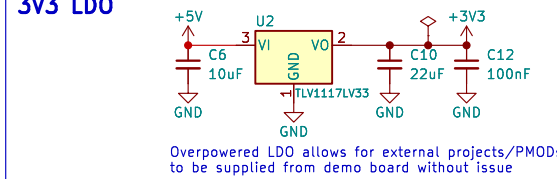
Momentary Switches (debounced)



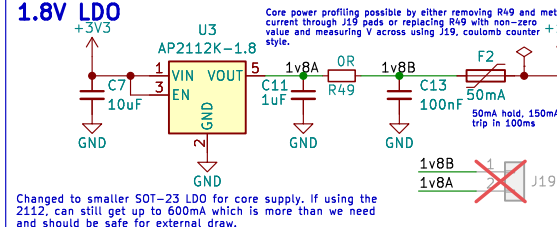
Power



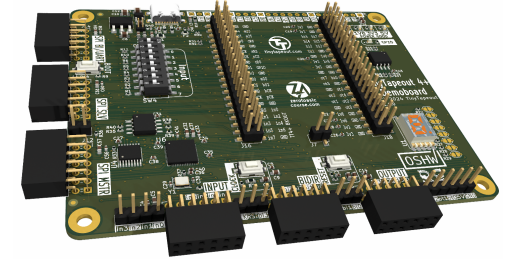
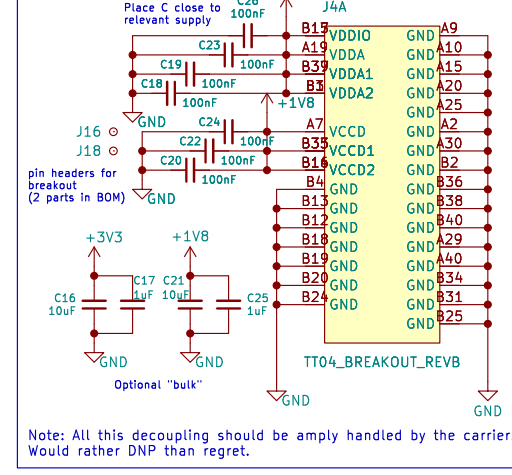
3V3 LDO



1.8V LDO



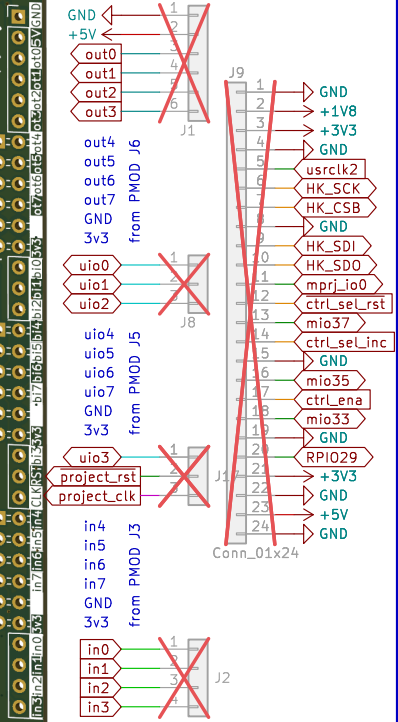
TT Carrier Power



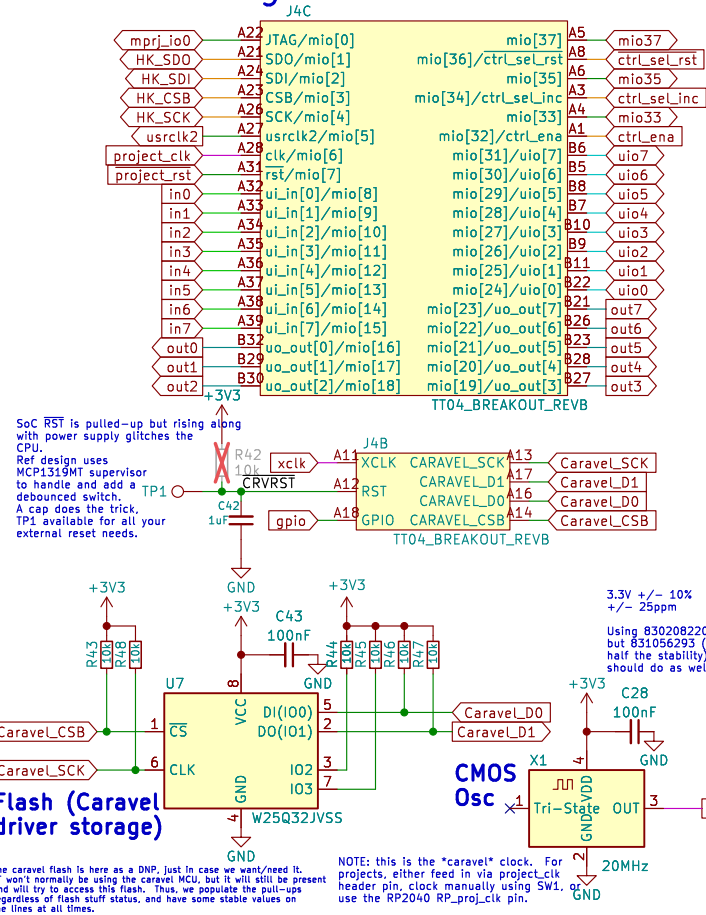
Extensive labelling, designed for TT4+ with new MUX, RP2040 on board, accessed via USB.
Project clock from RP2040, external or manual, DIP switches for inputs, 7-segment display (remappable with jumpers) on outputs, full access to 8 in, out and bidirectionals via PMODs, all pins broken out in headers.

Power via +5V USB, or 5V breakout pin. On-board regulation to 3v3 and 1v8. VDDIO is 3v3, including on PMODs. <https://github.com/TinyTapeout/tt-demo-pcb>

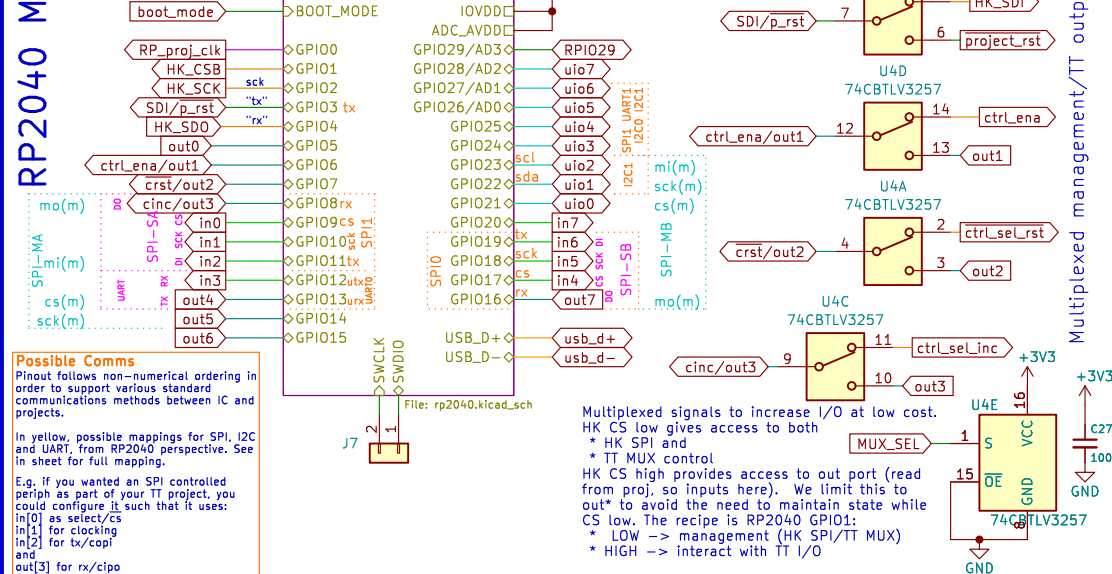
Board edge connectors (pinheaders)



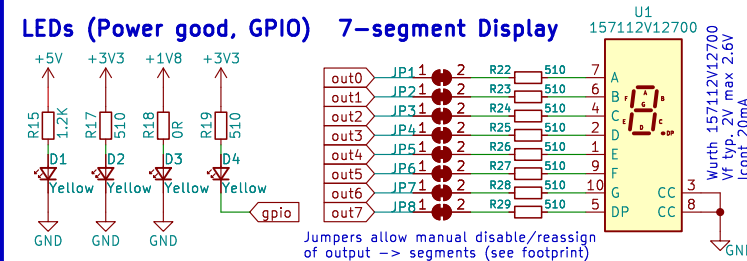
TT Carrier Logic



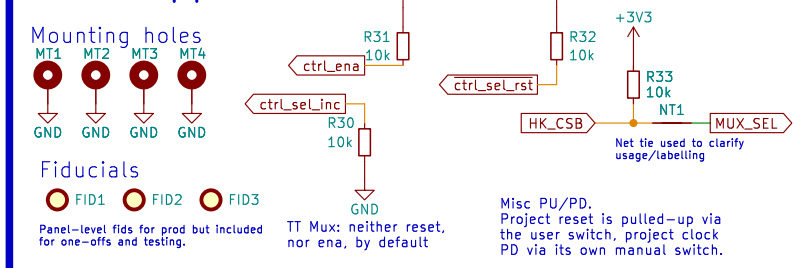
RP2040 MCU



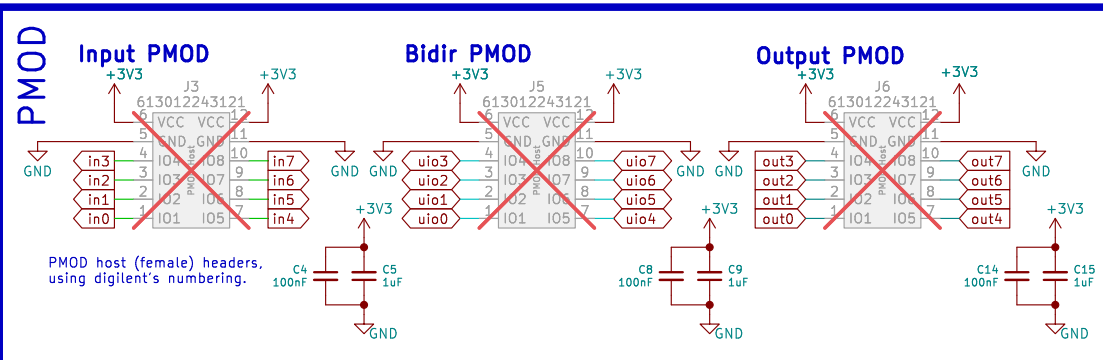
Indication



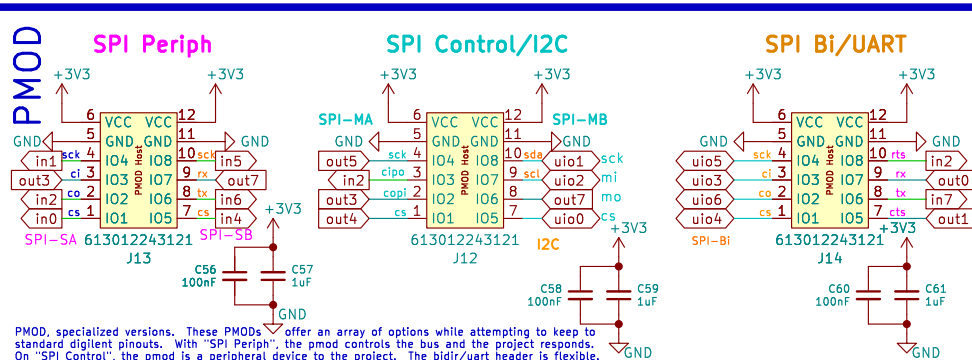
Misc Support



PMOD



PMOD



RP2040 Basic Support

IOVDD □ IOVDD

Logic supply, nominally 3v3.

BOOT_MODE □ QSPL_SS

When held low on powerup, flash SS determines boot mode
(HIGH == flash boot, LOW == USB device)

USB_VDD supplies USB PHY, nominal 3v3. If IOVDD is 3v3, can share supply.

In fact, in this and many applications, IOVDD, USB_VDD and ADC_AVDD are all powered directly from a single 3v3 supply, with the 1v1 digital core being handle by on-board regulator.

VREG_VOUT: Int core regulator, 1.1V
Can supply DVDD
Place 1uF in/out bypass near pin.

J10 Short to hold in reset
RUN

J11
QSPL_SS → +3V3
QSPL_CLK
QSPL_SD0
QSPL_SD1
GND

Flash program header
Note: should we replace 3v3 with RUN, to be able to reset/hold while updating flash?

Rule of thumb
 $C1, C2 = 2 * CL - 2 * C_{stray}$
Using a stray cap of 5pF, gives $C_n = 6pF$
Into:
 $CL = (C1 * C2) / (C1 + C2) + C_{stray}$
These $C_n = 6pF$ give
 $CL = 8pF$ -- just what we need.

WE 830108206909:
CFPX-180 model
10 ppm tol, 20ppm stab
CL 8pF

SWCLKD 24
SWDIO 25

TESTEN 19

Factory test mode: GND

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