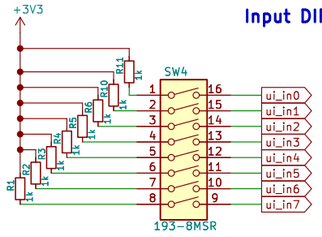
Tiny Tapeout 06+ Demo Board

User Input + Config

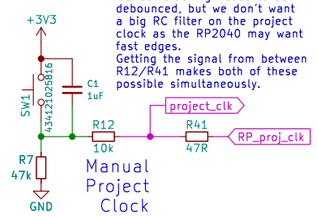
Input DIP

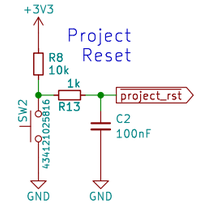


Alt: 76SB08ST

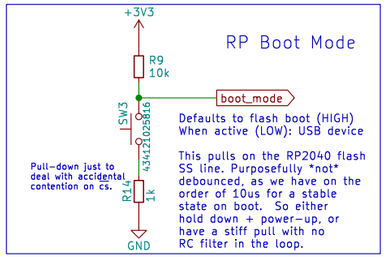
Momentary Switches (debounced)

Manual clocking needs to be debounced, but we don't want a big RC filter on the project clock as the RP2040 may want fast edges.
Getting the signal from between R12/R41 makes both of these possible simultaneously.



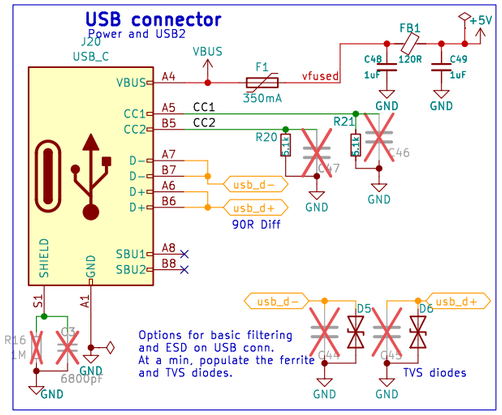


RP Boot Mode

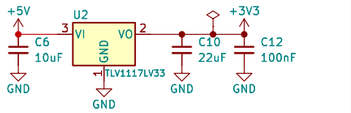


Power

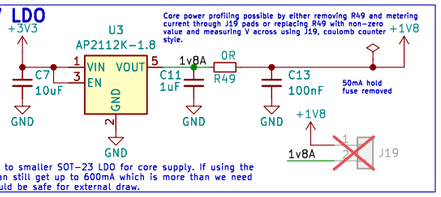
USB connector



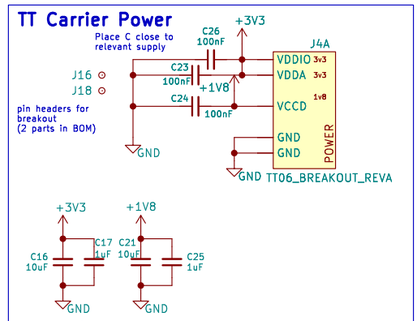
3V3 LDO

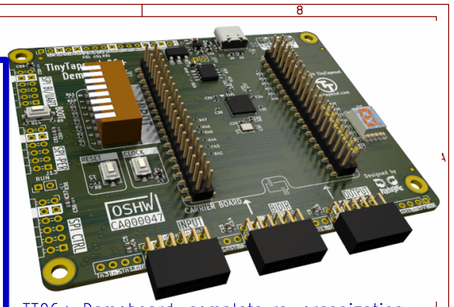


1.8V LDO



TT Carrier Power

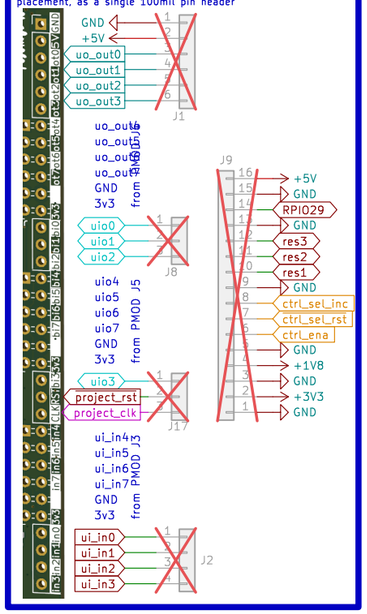




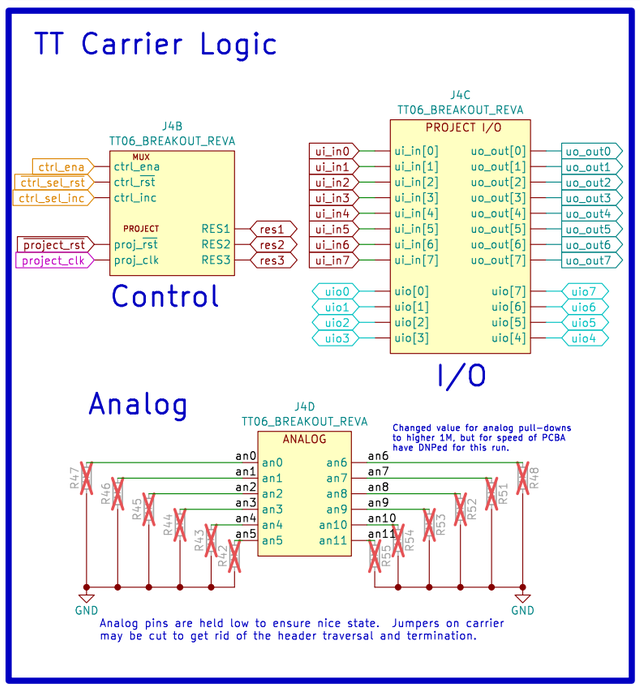
TT06+ Demoboard: complete re-organization, support for TT06+ new carrier pinout.
For users, main difference is the new piano DIP input and the fact no MUX is in the way on demoboards.
https://github.com/TinyTapeout/tt-demo-pcb

Board edge connectors (pinheaders)

I/O is available through standard PMODs or, with judicious placement, as a single 100mil pin header

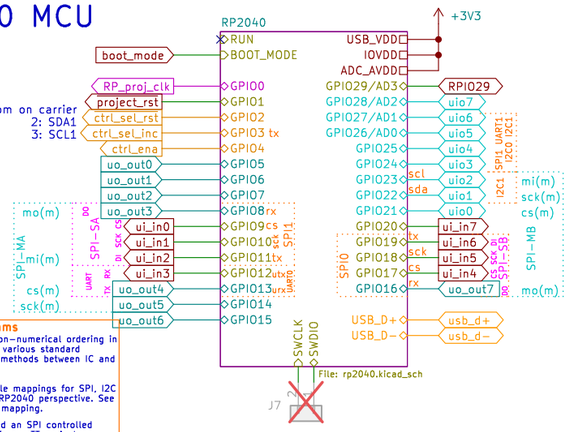


TT Carrier Logic



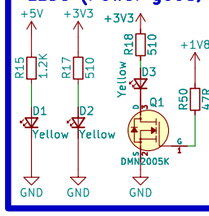
Analog

RP2040 MCU

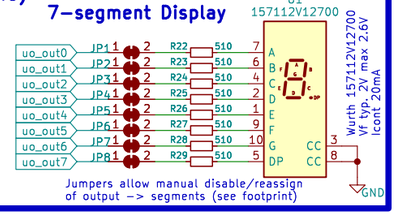


Indication

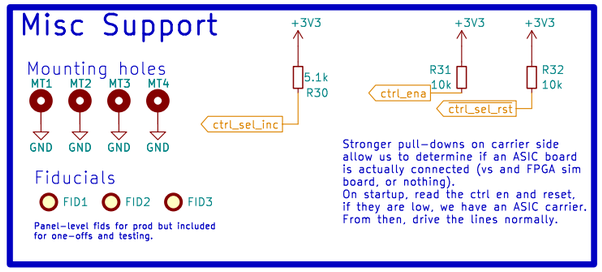
LEDs (Power good, GPIO)



7-segment Display

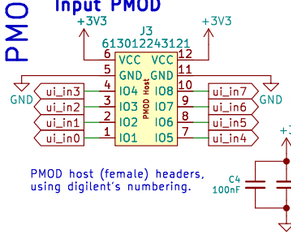


Misc Support

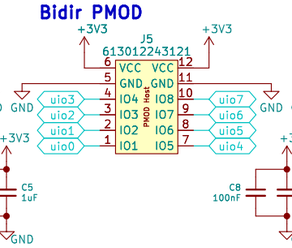


PMOD

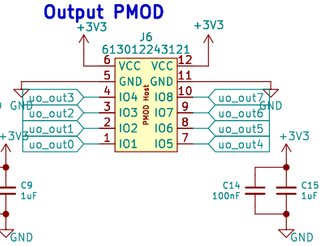
Input PMOD



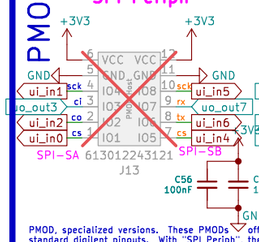
Bidir PMOD



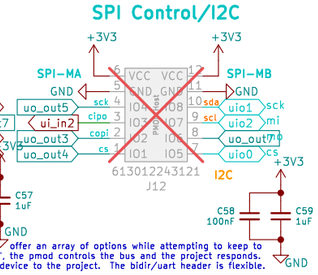
Output PMOD



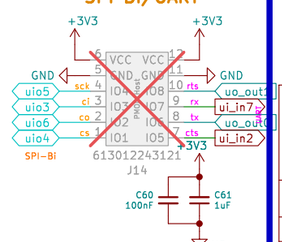
SPI Periph



SPI Control/I2C



SPI Bi/UART



PMOD, specialized versions. These PMODs offer an array of options while attempting to keep to standard digilent pinouts. With "SPI Periph", the pmod controls the bus and the project responds. On "SPI Control", the pmod is a peripheral device to the project. The bidir/uart header is flexible.

(C) 2024 Pat Deegan

Psychogenic Technologies

Sheet: /
File: tinytapeout-demo.kicad_sch

Title: Tiny Tapeout 06+ Demo Board

Size: A3	Date: 2024-12-10	**Rev: 2.1.0**
KiCad E.D.A. 8.0.8		Id: 1/2

RP2040 Basic Support

IOVDD — Logic supply, nominally 3v3.

BOOT_MODE — QSPI_SS: When held low on powerup, flash SS determines boot mode (HIGH == flash boot, LOW == USB device)

USB_VDD supplies USB PHY, nominal 3v3. If IOVDD is 3v3, can share supply.

In fact, in this and many applications, IOVDD, USB_VDD and ADC_AVDD are all powered directly from a single 3v3 supply, with the 1v1 digital core being handle by on-board regulator.

VREG_VOUT: Int core regulator, 1.1V. Can supply DVDD. Place 1uF in/out bypass near pin.

J10: Short to hold in reset — RUN

J11: QSPI_SS, QSPI_CLK, QSPI_SD0, QSPI_SD1, +3V3

Flash program header. Note: should we replace 3v3 with RUN, to be able to reset/hold while updating flash?

WE 830108206909: CFPX-180 model, 10 ppm tol, 20ppm stab, CL 8pF

C29 6pF, C30 6pF, Y1 12.0MHz, R37 1k

Rule of thumb: C1, C2 = 2 * CL - 2 * Cstray. Using a stray cap of 5pF, gives Cn = 6pF.

Into: CL = (C1 * C2) / (C1 + C2) + Cstray. These Cn = 6p give CL = 8pF -- just what we need.

U6 RP2040

GPIO0 2 GPIO0
GPIO1 3 GPIO1
GPIO2 4 GPIO2
GPIO3 5 GPIO3
GPIO4 6 GPIO4
GPIO5 7 GPIO5
GPIO6 8 GPIO6
GPIO7 9 GPIO7
GPIO8 11 GPIO8
GPIO9 12 GPIO9
GPIO10 13 GPIO10
GPIO11 14 GPIO11
GPIO12 15 GPIO12
GPIO13 16 GPIO13
GPIO14 17 GPIO14
GPIO15 18 GPIO15
GPIO16 27 GPIO16
GPIO17 28 GPIO17
GPIO18 29 GPIO18
GPIO19 30 GPIO19
GPIO20 31 GPIO20
GPIO21 32 GPIO21
GPIO22 34 GPIO22
GPIO23 35 GPIO23
GPIO24 36 GPIO24
GPIO25 37 GPIO25
GPIO26_ADC0 38 GPIO26/AD0
GPIO27_ADC1 39 GPIO27/AD1
GPIO28_ADC2 40 GPIO28/AD2
GPIO29_ADC3 41 GPIO29/AD3

RUN 26 — R36 10k to IOVDD — async reset
USB_D+ 47 USB_DP
USB_D- 46 USB_DM
QSPI_SS 56
QSPI_SD0 53
QSPI_SD1 55
QSPI_SD2 54
QSPI_SD3 51
QSPI_CLK 52
XIN 20
XOUT 21
SWCLK 24
SWDIO 25 SWD
TESTEN 19 — Factory test mode: GND

C32 1uF 1v1, C37 1uF

Flash

U5 W25Q32JVSS

Note: SS pulled-up externally, from bootmode switch

R34 10k, C31 100nF, R35 10k, R38 10k, R39 10k, R40 10k

QSPI_SS, QSPI_CLK, QSPI_SD0, QSPI_SD1, QSPI_SD2, QSPI_SD3

Quad SPI requires QE bit in status register-2 to be set. In this case, WP becomes IO2 and HOLD becomes IO3.

Supply bypass, place near 1, 10, 22, 33, 42, 49

C33 100nF, C35 100nF, C38 100nF, C34 100nF, C36 100nF, C39 100nF

Supply bypass, near 23, 50

C40 100nF, C41 100nF

	Function								
GPIO	F1	F2	F3	F4	F5	F6	F7	F8	F9
0	SPI0 RX	UART0 TX	I2C0 SDA	PWM0 A	SIO	PIO0	PIO1		USB OVCUR DET
1	SPI0 CSn	UART0 RX	I2C0 SCL	PWM0 B	SIO	PIO0	PIO1		USB VBUS DET
2	SPI0 SCK	UART0 CTS	I2C1 SDA	PWM1 A	SIO	PIO0	PIO1		USB VBUS EN
3	SPI0 TX	UART0 RTS	I2C1 SCL	PWM1 B	SIO	PIO0	PIO1		USB OVCUR DET
4	SPI0 RX	UART1 TX	I2C0 SDA	PWM2 A	SIO	PIO0	PIO1		USB VBUS DET
5	SPI0 CSn	UART1 RX	I2C0 SCL	PWM2 B	SIO	PIO0	PIO1		USB VBUS EN
6	SPI0 SCK	UART1 CTS	I2C1 SDA	PWM3 A	SIO	PIO0	PIO1		USB OVCUR DET
7	SPI0 TX	UART1 RTS	I2C1 SCL	PWM3 B	SIO	PIO0	PIO1		USB VBUS DET
8	SPI1 RX	UART1 TX	I2C0 SDA	PWM4 A	SIO	PIO0	PIO1		USB VBUS EN
9	SPI1 CSn	UART1 RX	I2C0 SCL	PWM4 B	SIO	PIO0	PIO1		USB OVCUR DET
10	SPI1 SCK	UART1 CTS	I2C1 SDA	PWM5 A	SIO	PIO0	PIO1		USB VBUS DET
11	SPI1 TX	UART1 RTS	I2C1 SCL	PWM5 B	SIO	PIO0	PIO1		USB VBUS EN
12	SPI1 RX	UART0 TX	I2C0 SDA	PWM6 A	SIO	PIO0	PIO1		USB OVCUR DET
13	SPI1 CSn	UART0 RX	I2C0 SCL	PWM6 B	SIO	PIO0	PIO1		USB VBUS DET
14	SPI1 SCK	UART0 CTS	I2C1 SDA	PWM7 A	SIO	PIO0	PIO1		USB VBUS EN
15	SPI1 TX	UART0 RTS	I2C1 SCL	PWM7 B	SIO	PIO0	PIO1		USB OVCUR DET
16	SPI0 RX	UART0 TX	I2C0 SDA	PWM0 A	SIO	PIO0	PIO1		USB VBUS DET
17	SPI0 CSn	UART0 RX	I2C0 SCL	PWM0 B	SIO	PIO0	PIO1		USB VBUS EN
18	SPI0 SCK	UART0 CTS	I2C1 SDA	PWM1 A	SIO	PIO0	PIO1		USB OVCUR DET
19	SPI0 TX	UART0 RTS	I2C1 SCL	PWM1 B	SIO	PIO0	PIO1		USB VBUS DET
20	SPI0 RX	UART1 TX	I2C0 SDA	PWM2 A	SIO	PIO0	PIO1	CLOCK GPIN0	USB VBUS EN
21	SPI0 CSn	UART1 RX	I2C0 SCL	PWM2 B	SIO	PIO0	PIO1	CLOCK GPOUT0	USB OVCUR DET
22	SPI0 SCK	UART1 CTS	I2C1 SDA	PWM3 A	SIO	PIO0	PIO1	CLOCK GPIN1	USB VBUS DET
23	SPI0 TX	UART1 RTS	I2C1 SCL	PWM3 B	SIO	PIO0	PIO1	CLOCK GPOUT1	USB VBUS EN
24	SPI1 RX	UART1 TX	I2C0 SDA	PWM4 A	SIO	PIO0	PIO1	CLOCK GPOUT2	USB OVCUR DET
25	SPI1 CSn	UART1 RX	I2C0 SCL	PWM4 B	SIO	PIO0	PIO1	CLOCK GPOUT3	USB VBUS DET
26	SPI1 SCK	UART1 CTS	I2C1 SDA	PWM5 A	SIO	PIO0	PIO1		USB VBUS EN
27	SPI1 TX	UART1 RTS	I2C1 SCL	PWM5 B	SIO	PIO0	PIO1		USB OVCUR DET
28	SPI1 RX	UART0 TX	I2C0 SDA	PWM6 A	SIO	PIO0	PIO1		USB VBUS DET
29	SPI1 CSn	UART0 RX	I2C0 SCL	PWM6 B	SIO	PIO0	PIO1		USB VBUS EN

(C) 2023, 2024 Pat Deegan

Psychogenic Technologies

Sheet: /RP2040/

File: rp2040.kicad_sch

Title: Tiny Tapeout 4/5 Demo Board

Size: A4 | Date: 2024-04-12 | **Rev: 1.2.2**

KiCad E.D.A. 8.0.8 | Id: 2/2