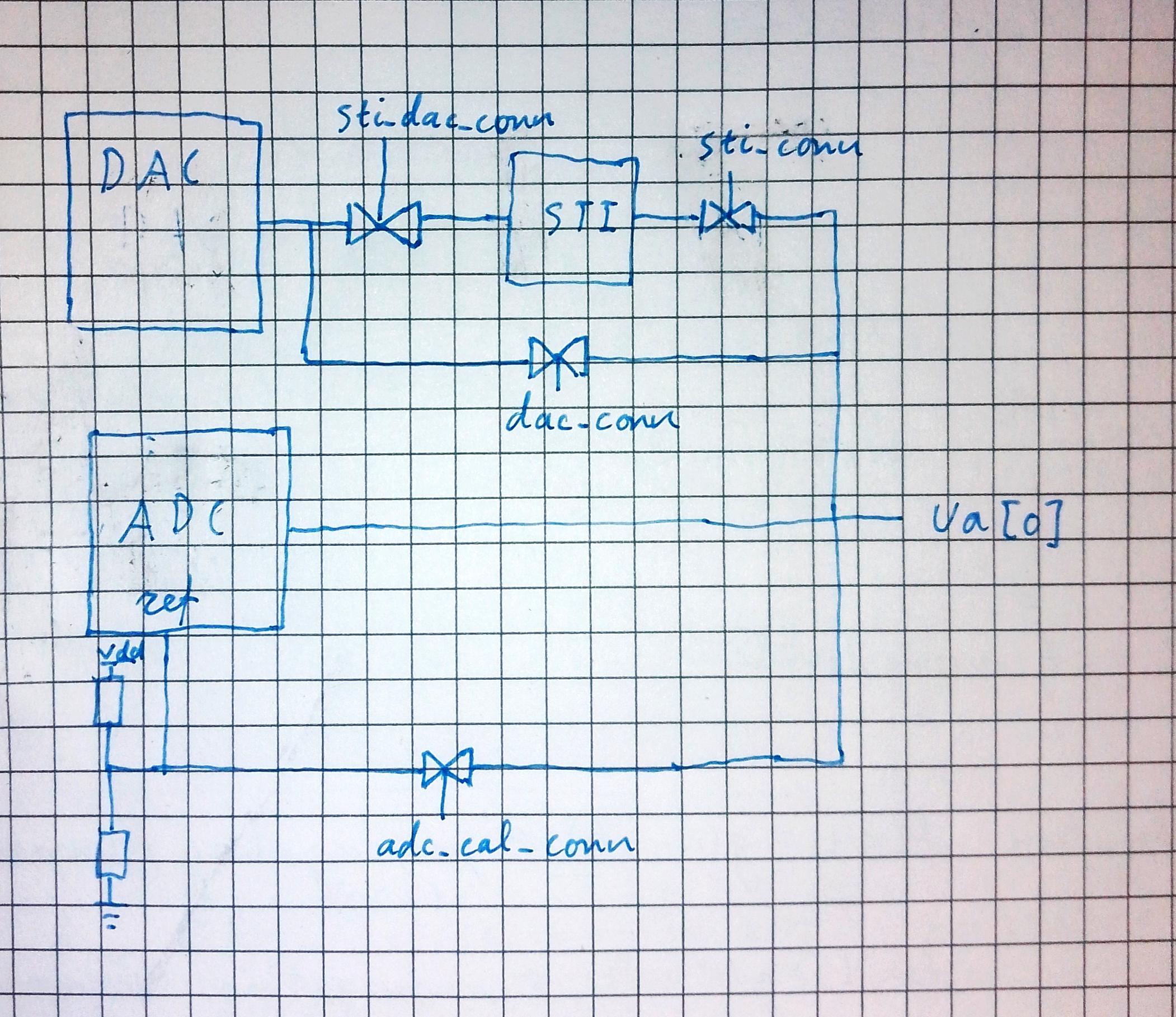
# Tt9 adc dac project

## Pinout

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| ui[0] | dac0 | uo[0] | bus0[0] | uio[0] | bus2[0] |
| ui[1] | dac1 | uo[1] | bus0[1] | uio[1] | bus2[1] |
| ui[2] | dac2 | uo[2] | bus0[2] | uio[2] | bus2[2] |
| ui[3] | dac3 | uo[3] | bus0[3] | uio[3] | bus2[3] |
| ui[4] | dac4 | uo[4] | bus1[0] | uio[4] | dac\_conn |
| ui[5] | dac5 | uo[5] | bus1[1] | uio[5] | adc\_cal\_conn |
| ui[6] | dac6 | uo[6] | bus1[2] | uio[6] | sti\_conn |
| ui[7] | dac7 | uo[7] | bus1[3] | uio[7] | sti\_dac\_conn |

## Block diagram



Transmission gates controlled by the “conn” signals connect different devices together.

## DAC

The dac inputs are directly connected to the dac[] bus. The inputs are active low, so writing FF to them wil result in the dac outputting 0. The output range of the dac is 0 to 1.8v and it uses the supply rails as the reference voltage. It’s a r2r dac and there is no output buffer whatsoever. Its output is connected to transmission gates that can short it to the analog output pin or to the STI.

## ADC

Tis design uses 4 bit flash adc made out of an encoder and 15 comparators. The encoder was in vhdl and syntesis and layout was made by Openlane. The encoder takes in a signal from each of the 15 comarators and a clock, and outputs 3 4 bit busses. The busses are multiplexed so that the frequency on the output pins is 3 times lower than the clock. The comparators compare the analog input voltage with scaled voltages between 0 and 1 made by resistive dividers. The top of this divider can be connected to the output via a transmission gate, this is the max voltage for the comparator. The comparators themselves are copied from Stefans Schippers video <https://www.youtube.com/watch?v=bYbkz8FXnsQ&t=1137s> I just added some more buffering on the output.

## Simulations Et bilde som inneholder skjermbilde, Plottdiagram, line, diagram Automatisk generert beskrivelse

Stefans comparator with extra drive stages before layout

<https://www.youtube.com/watch?v=bYbkz8FXnsQ&t=1133s>

Et bilde som inneholder skjermbilde, rom, line, astronomi

Automatisk generert beskrivelse

Dac and the comparators working post layout the horizontal blue traces on the right are the reference voltages for each comparator, the green plot is the dac voltage and the blue vertical lines are the outputs of every comparator. Ignore the dense population of outputs in the beginning of graph to the right, its due to the dac voltage settling.

Et bilde som inneholder tekst, skjermbilde, Font, Grafikk

Automatisk generert beskrivelse

Sti circuit

Et bilde som inneholder skjermbilde, tekst

Automatisk generert beskrivelse

STI in pre layout simulation. Pmos width was adjusted to get a symmetrical response

Et bilde som inneholder skjermbilde, diagram, Plottdiagram, line

Automatisk generert beskrivelse

STI in post layout simulation (0 to 600nS) It is not symmetrical I’m thinking because of device mismatch, it will be interesting to see what we get in the manufactured chip. The graph after 600nS shows the reference voltage being switched on. its not buffered so it takes some time to discharge line capacitance but it settles down eventually to somewhere around 1v.

Pmos width was adjusted to get a linear response

Sti circuit:

## Digital block layout process

These are just some notes for me since I found it a bit tricky to do the digital layout but its really not complicated if you know the commands

Et bilde som inneholder tekst, skjermbilde, Font

Automatisk generert beskrivelse

Use ghdl to convert vhdl project to Verilog code, and then just follow this openlane example:

<https://openlane2.readthedocs.io/en/latest/getting_started/newcomers/index.html>