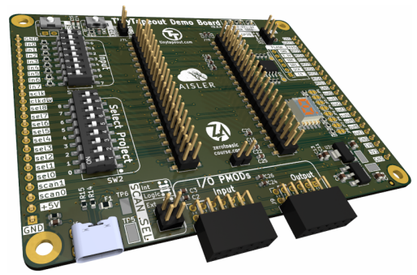
TinyTapeout 1/2/3 Demo Board

Version 2.2.4 Preview

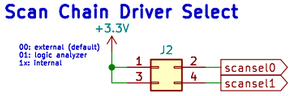


Extensive labelling, jumpers to set scan selection and clock source (on-board oscillator or manual/pico), DIP switches for inputs and selection, 7-segment display (remappable with jumpers) on outputs, full access to 8 in and out via PMODs, all pins broken out in breadboardable headers. Optional Raspberry Pi Pico, pads on underside.

Power via +5V USB, or 5V breakout pin. On-board regulation to 3v3 and 1v8. VDDIO is 3v3, including on PMODs.

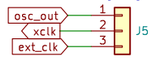
User Input + Config

Scan Chain Driver Select



Caravel Clock Source

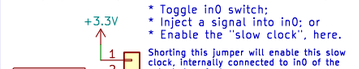
Select oscillator [1–2]
or RPI/Manual [2–3]



TT Project Internal Clock

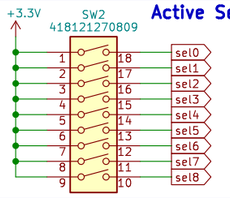
TinyTapeout projects are clocked on in0. You may:

* Toggle in0 switch;
* Inject a signal into in0; or
* Enable the "slow clock", here.

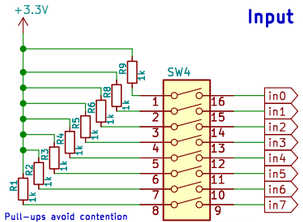


Shorting this jumper will enable this slow clock, internally connected to in0 of the selected project.
It is "slow" because the rate is determined by the settings on in[0..7] (the caravel clock source rate divided by IN value).

Active Select

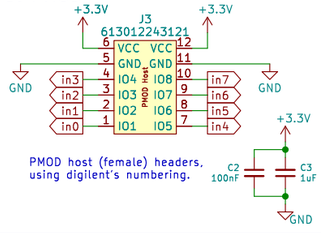


Input DIP



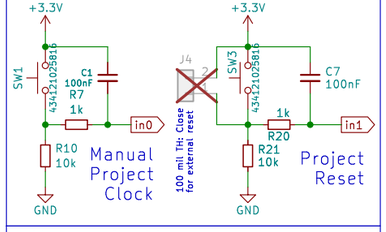
Pull-ups avoid contention if sharing inputs with Pico. Discreets beat array on costing: subject to PCBA pricing struct.

Input PMOD

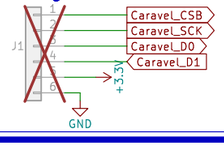


PMOD host (female) headers, using digilent's numbering.

Momentary Switches (debounced)

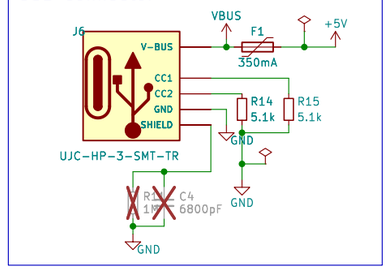


Memory flashing connector

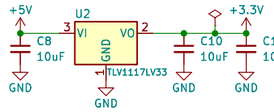


Power

USB connector

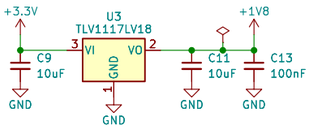


3.3V LDO



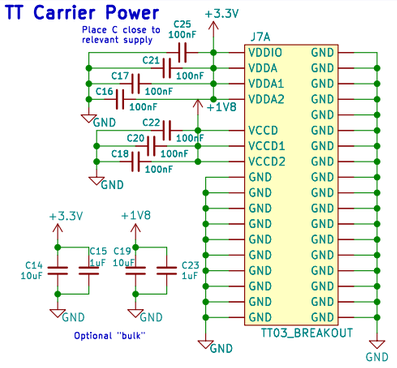
Both of these LDOs are serious overkill, but this means you can safely power much external circuitry using the 3v3 and 1v8 header pins.

1.8V LDO



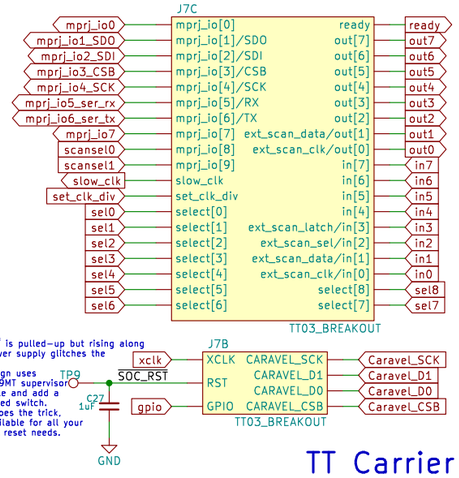
The 1v8 regulator is cascaded on the 3v3, which should allow operation if back-powering 3v3 line, as Matt did in TT2 bringup livestream.

TT Carrier Power



Note: All this decoupling should be amply handled by the carrier. Would rather DNP than regret.

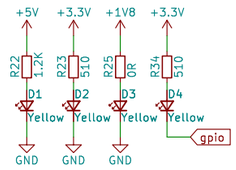
TT Carrier Logic



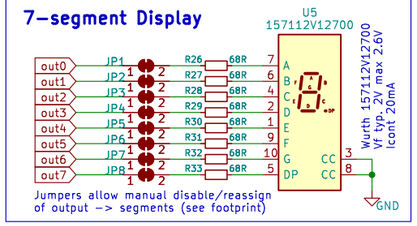
SoC RST is pulled-up but rising along with power supply glitches the CPU.
Ref design uses MCP1319MT supervisor to handle and add a debounced switch. A cap does the trick. TP9 available for all your external reset needs.

Outputs

LEDs (Power good, GPIO)

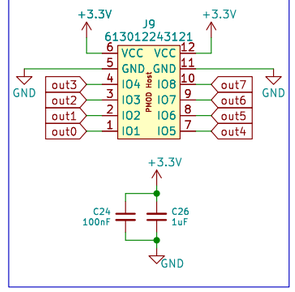


7-segment Display

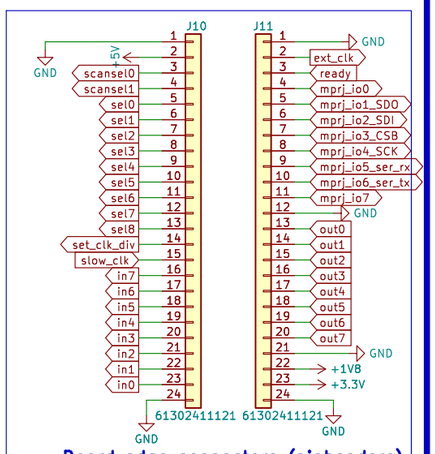


Jumpers allow manual disable/reassign of output -> segments (see footprint)

Output PMOD

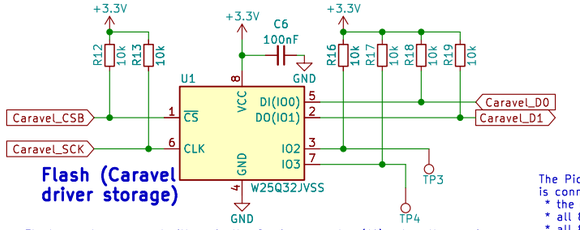


Board edge connectors (pinheaders)



Peripherals

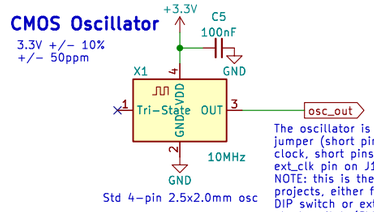
Flash (Caravel driver storage)



Flash may be accessed either via the 6-pin connector (J1), when the carrier is NOT loaded. When populated, it may be read and written to using the Caravel pass-through mode via the HK SPI.

CMOS Oscillator

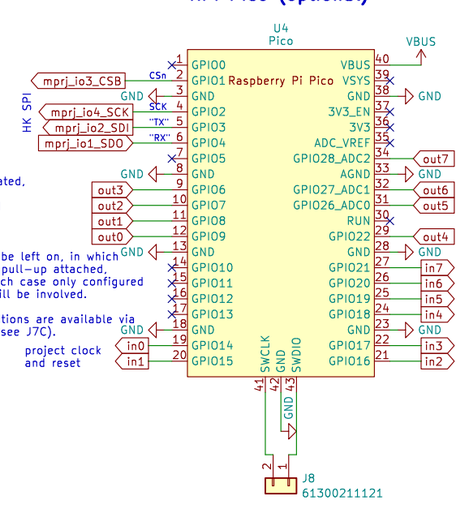
3.3V +/- 10%
+/- 50ppm



Std 4-pin 2.5x2.0mm osc

The oscillator is selected using the J5 jumper (short pins 1–2). To use an external clock, short pins 2–3 instead and feed into ext_clk pin on J11.
NOTE: this is the *caravel* clock. For projects, either feed in via in0 (PMOD or DIP switch or external header) or use the clock switch (SW1).

RPi Pico (optional)



The Pico, when populated, is connected to:
* the caravel HK SPI
* all 8 inputs
* all 8 outputs

Input DIP switch may be left on, in which case signal will have pull-up attached, or switched off in which case only configured caravel pull-downs will be involved.

NOTE: ext_scan_* functions are available via the project I/O pins (see J7C).

project clock and reset

Misc Support

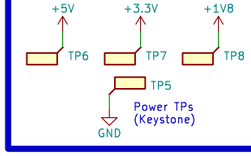
Mounting holes

MT1 MT2 MT3 MT4

Fiducials

FID1 FID2 FID3

Panel-level fids for prod but included for one-offs and testing.

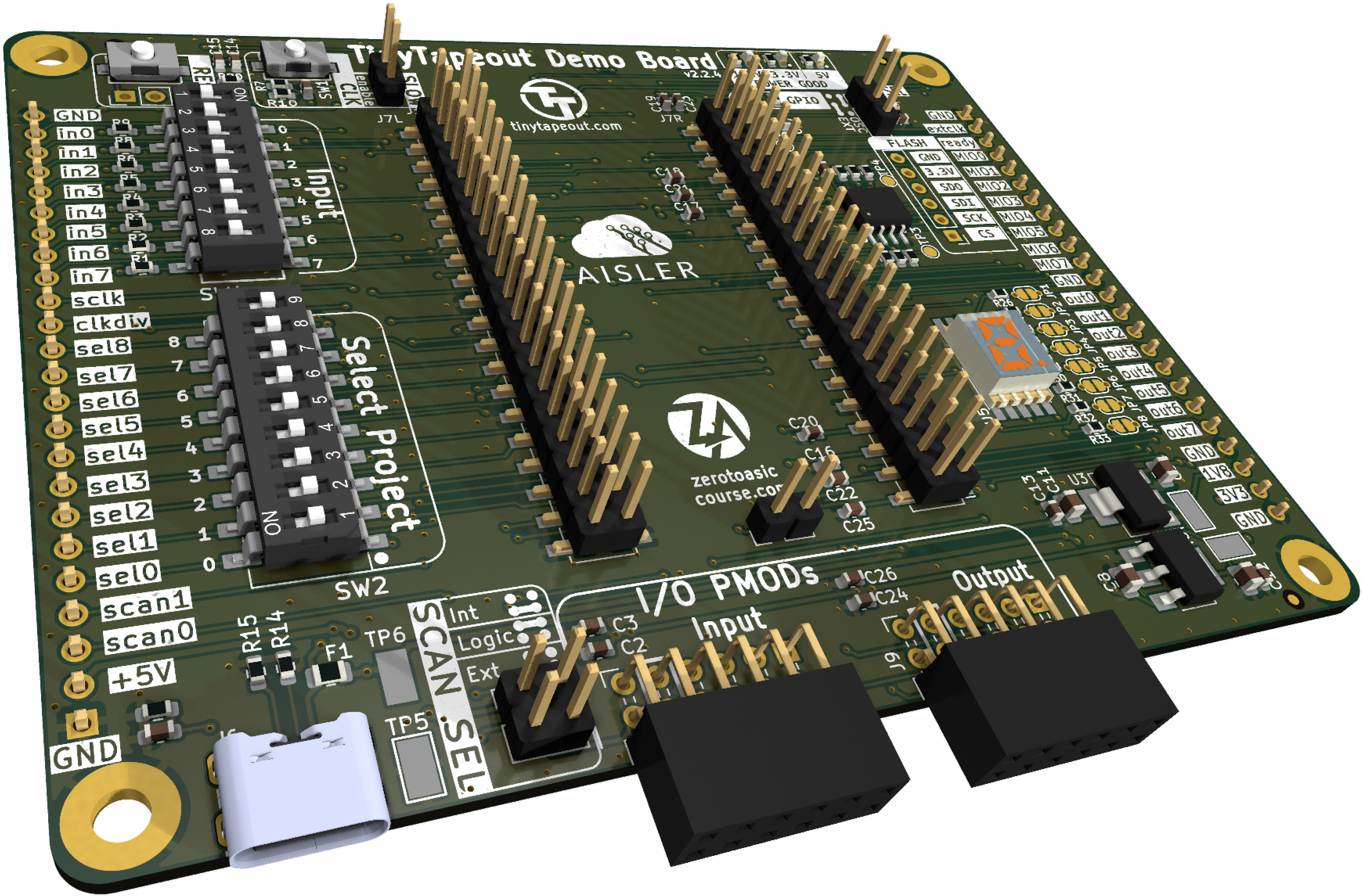


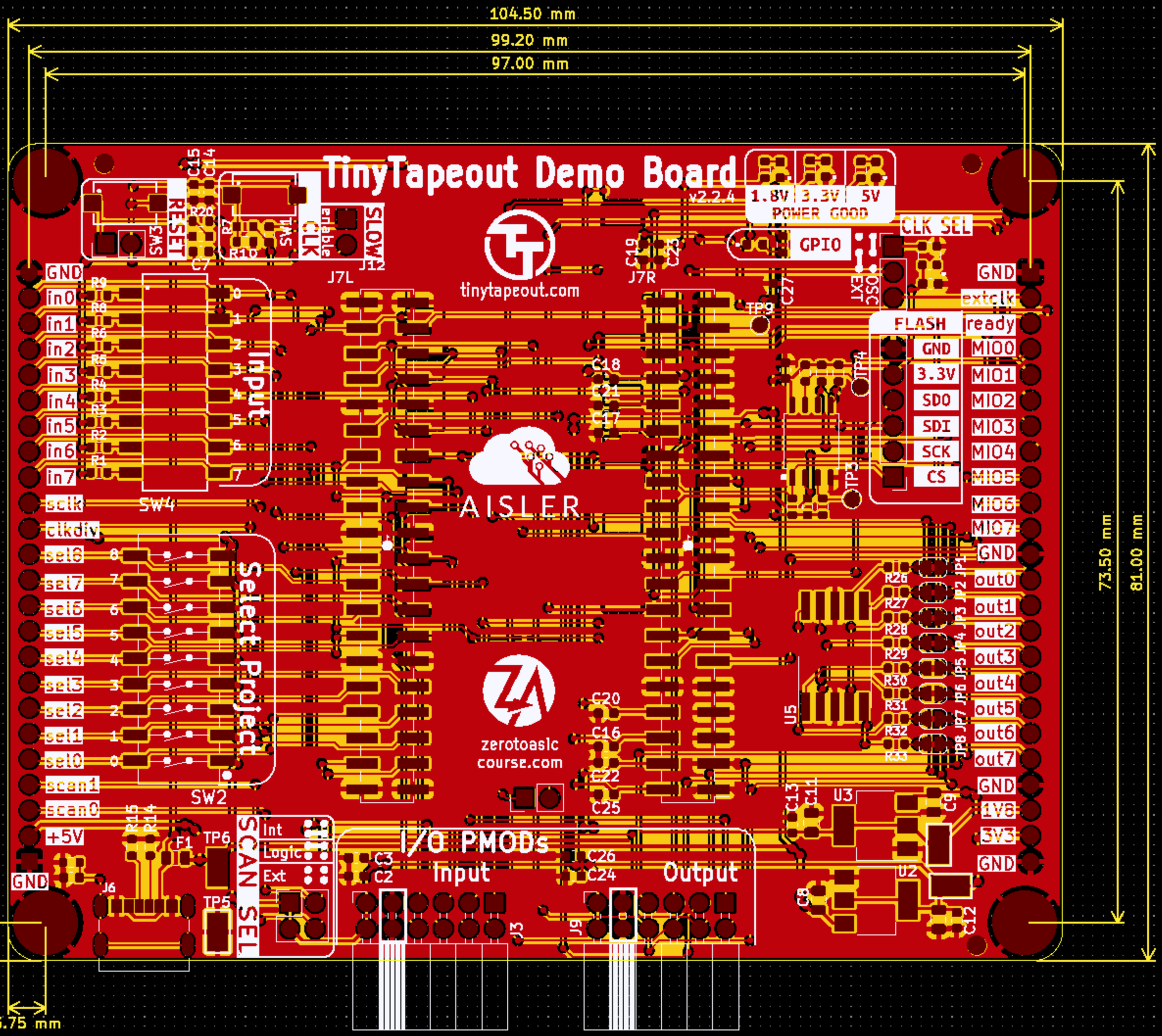
Psychogenic Technologies

Sheet: /
File: mpw-mb1.kicad_sch

Title: TinyTapeout Demo Board

Size: A3	Date: 2023-10-27	**Rev: 2.2.4**
KiCad E.D.A. kicad 7.0.8-7.0.8~ubuntu22.04.1		Id: 1/1


v2.2.4
tinytapeout.com
AISLER
zerotoasic
GND
in0
in1
in2
in3
in4
in5
in6
in7
sclk
clkdiv
sel8
sel7
sel6
sel5
sel4
sel3
sel2
sel1
sel0
scan1
scan0
+5V
GND
Input
Select Project
SW2
SCAN SEL
Int
Logic
Ext
I/O PMODs
Input
Output
TP5
TP6
F1
R15
R14
J7L
J7R
POWER GOOD
GPIO
FLASH
GND
3.3V
SDO
SDI
SCK
CS
GND
extclk
ready
MIO0
MIO1
MIO2
MIO3
MIO4
MIO5
MIO6
MIO7
GND
out0
out1
out2
out3
out4
out5
out6
out7
GND
1V8
3V3
GND


104.50 mm
99.20 mm
97.00 mm
73.50 mm
81.00 mm
3.75 mm
3.75 mm
TinyTapeout Demo Board
v2.2.4
tinytapeout.com
1.8V
3.3V
5V
POWER GOOD
GPIO
CLK SEL
RESET
CLK
SLOW
J7L
J7R
GND
in0
in1
in2
in3
in4
in5
in6
in7
sclk
clkdiv
sel6
sel7
sel6
sel5
sel4
sel3
sel2
sel1
sel0
scan1
scan0
+5V
Input
Select Project
SW4
SW2
SCAN SEL
Int
Logic
Ext
I/O PMODs
Input
Output
AISLER
zerotoasic
course.com
FLASH
GND
3.3V
SDO
SDI
SCK
CS
extclk
ready
MIO0
MIO1
MIO2
MIO3
MIO4
MIO5
MIO6
MIO7
out0
out1
out2
out3
out4
out5
out6
out7
1V8
3V3
U5
U3
U2