

# Design of a Configurable Logic Block (CLB)

Using CMOS Logic Family



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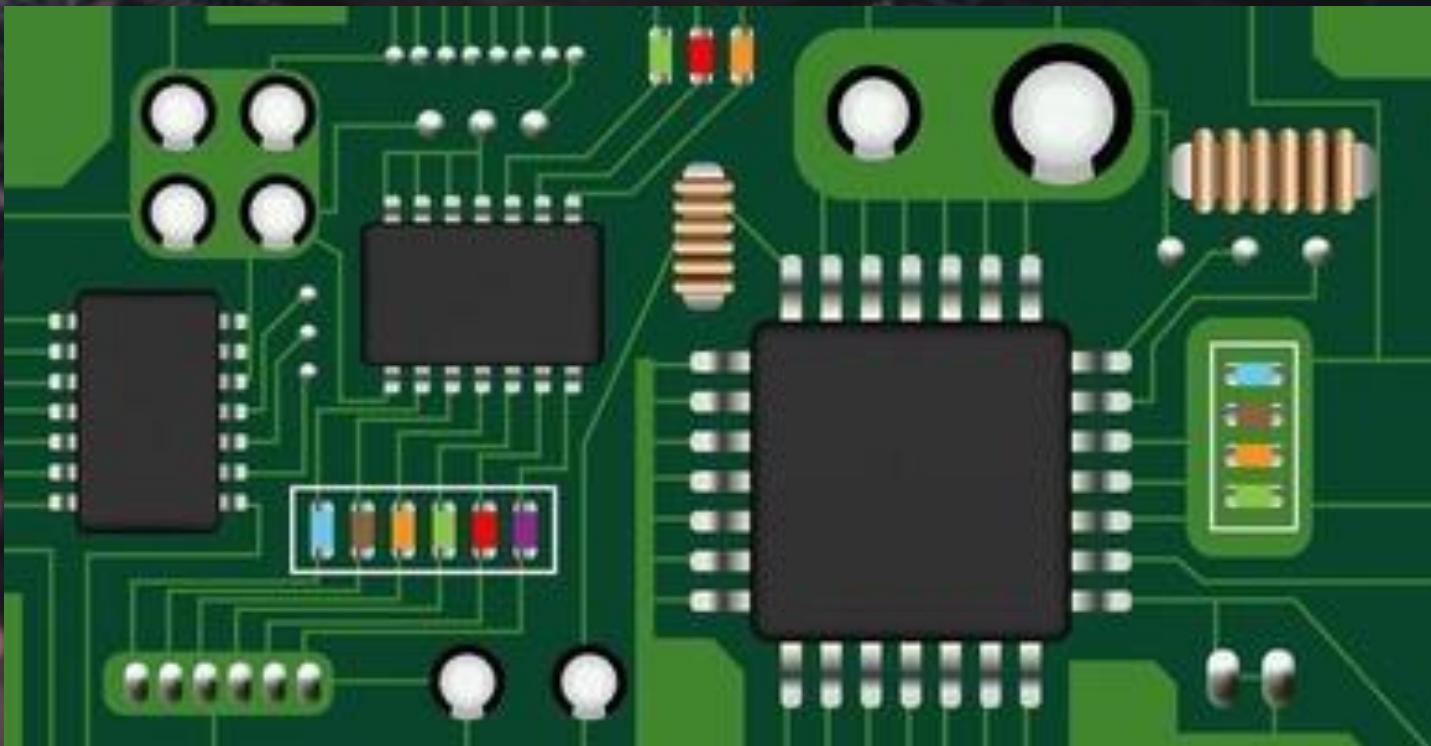
**UG Students**  
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# Outline

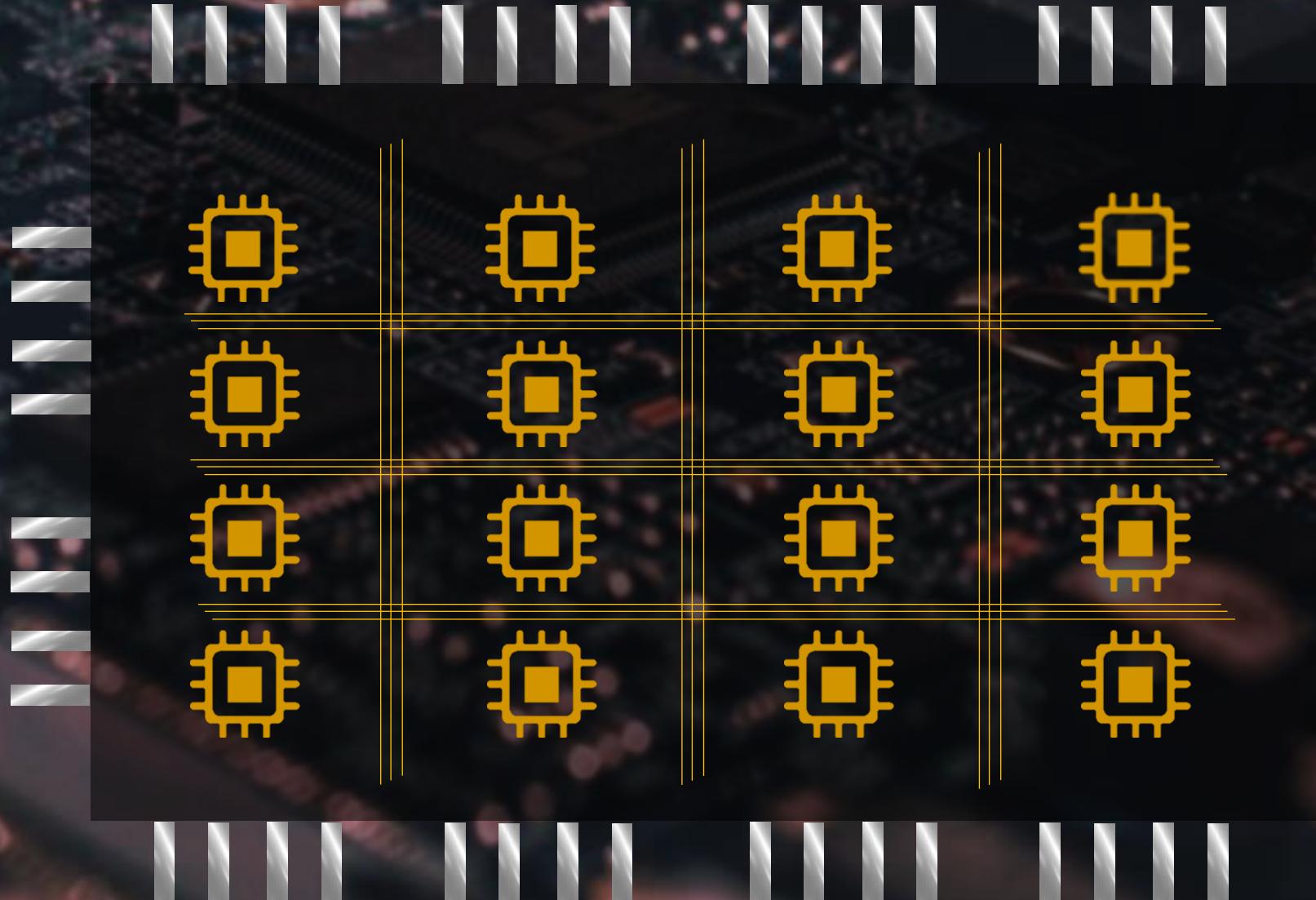
- Background
- Proposed Design
- Schematics
- Functionality Test
- Layout
- Circuit Performance Analysis
- Conclusion
- References

# Background

FPGA Board

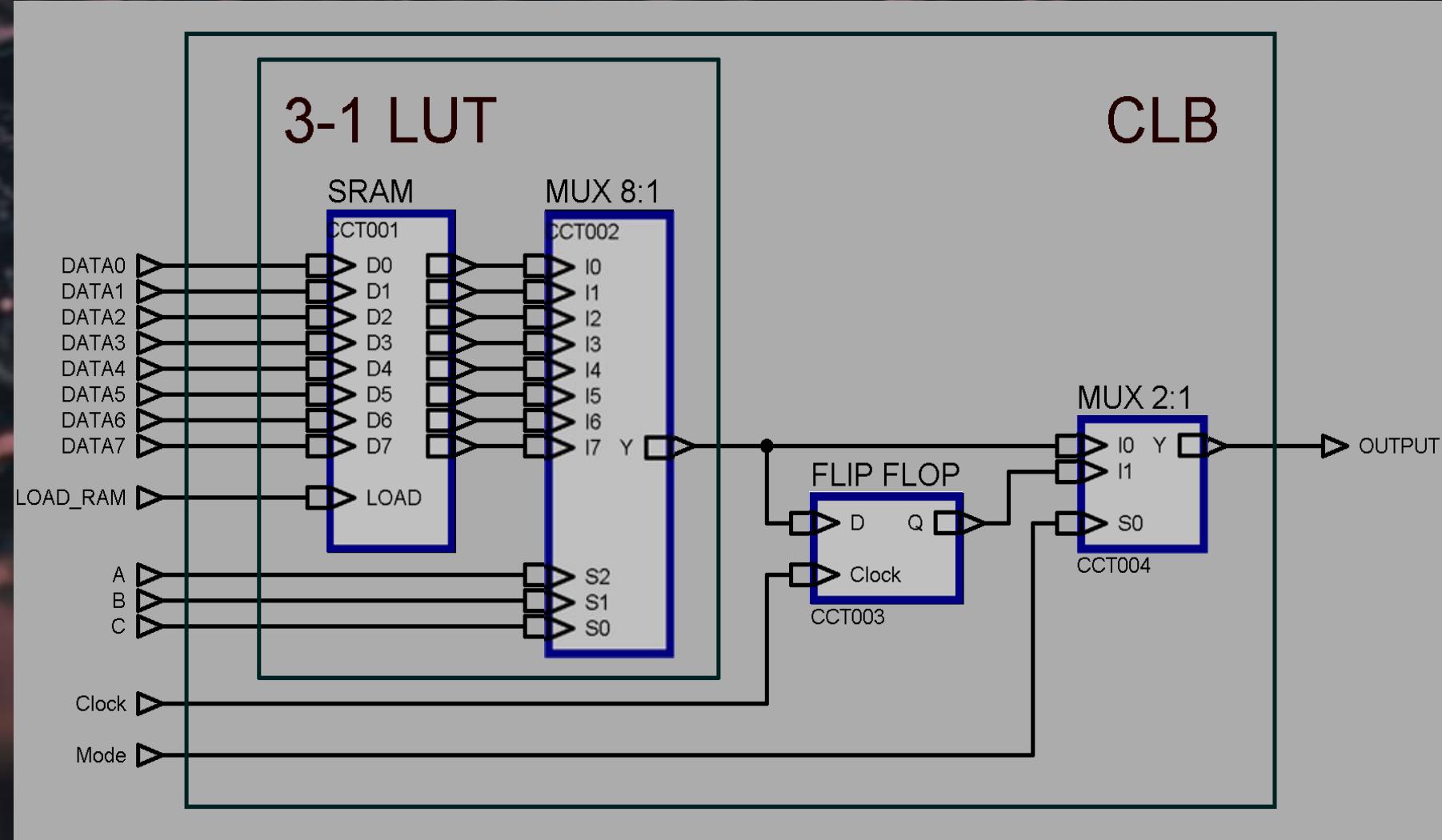


# Inside an FPGA



Group 3

# Proposed Design[1]



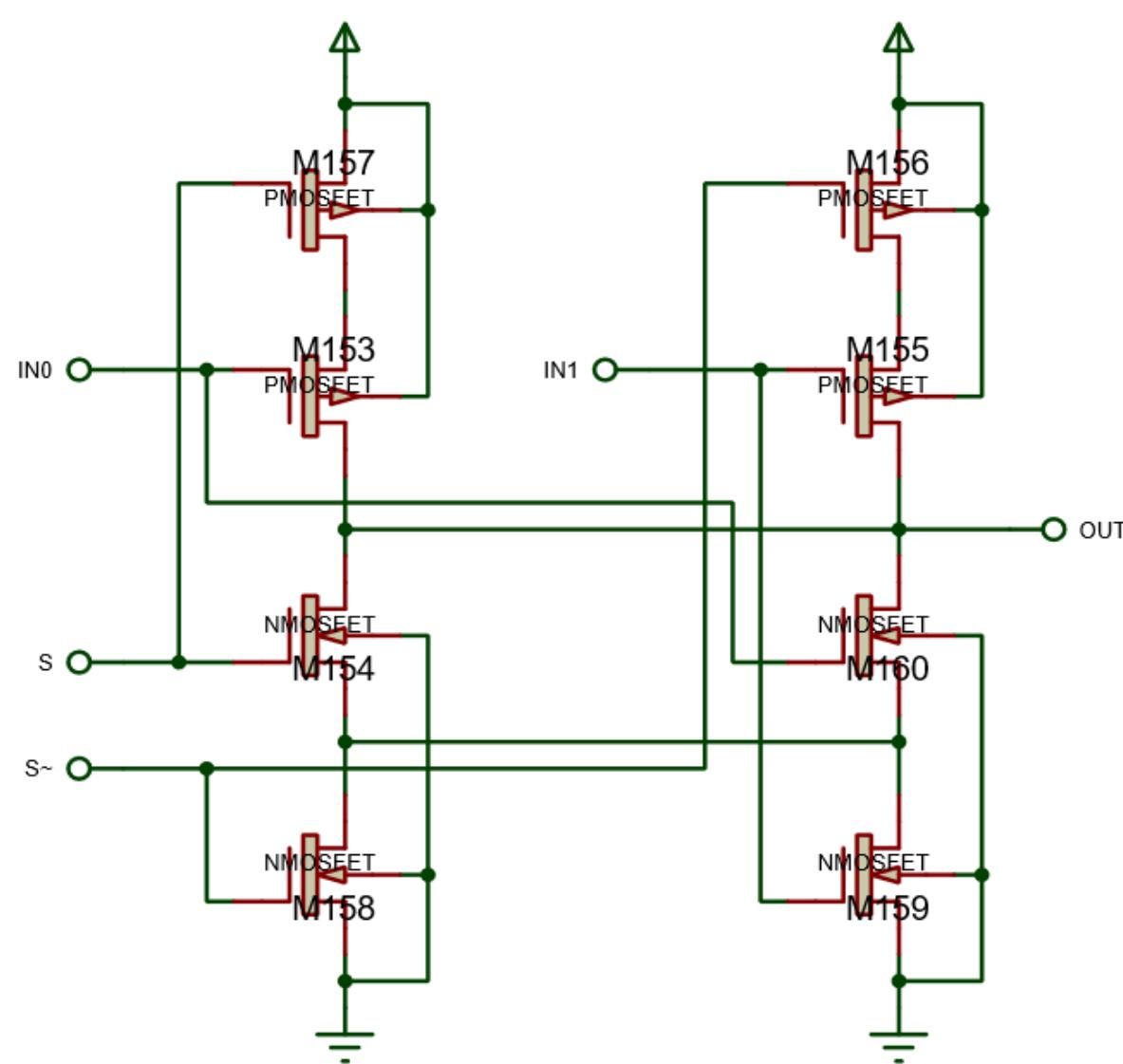
## Design Requirements

- Logic Family
  - Standard CMOS
- Logic Function
  - AB+C

## CLB Block Components

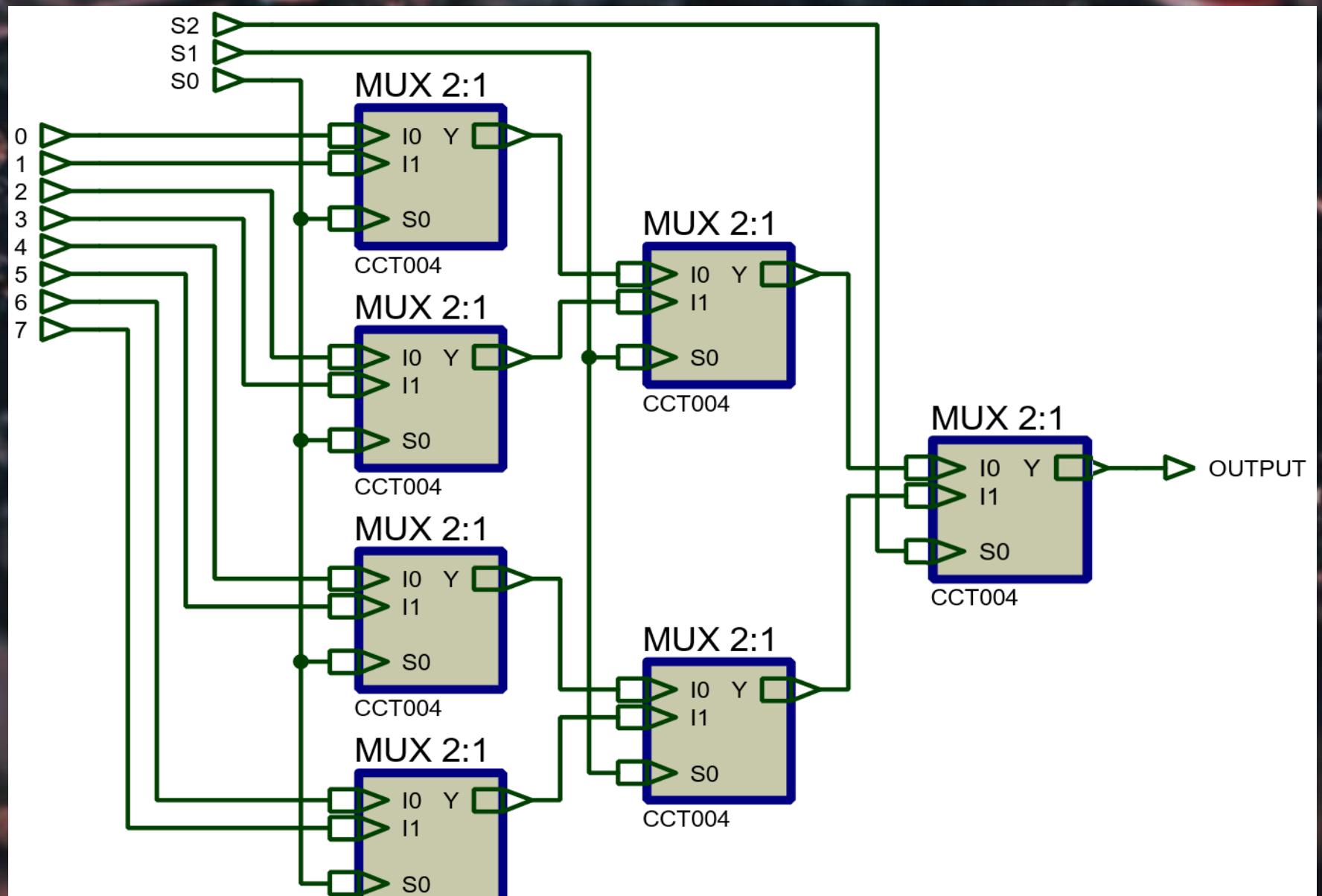
- **3-1 LUT**
  - 8bit SRAM
  - MUX 8:1
- Positive Edge Triggered D FLIP-FLOP
- MUX 2:1

# MUX 2:1



[3]

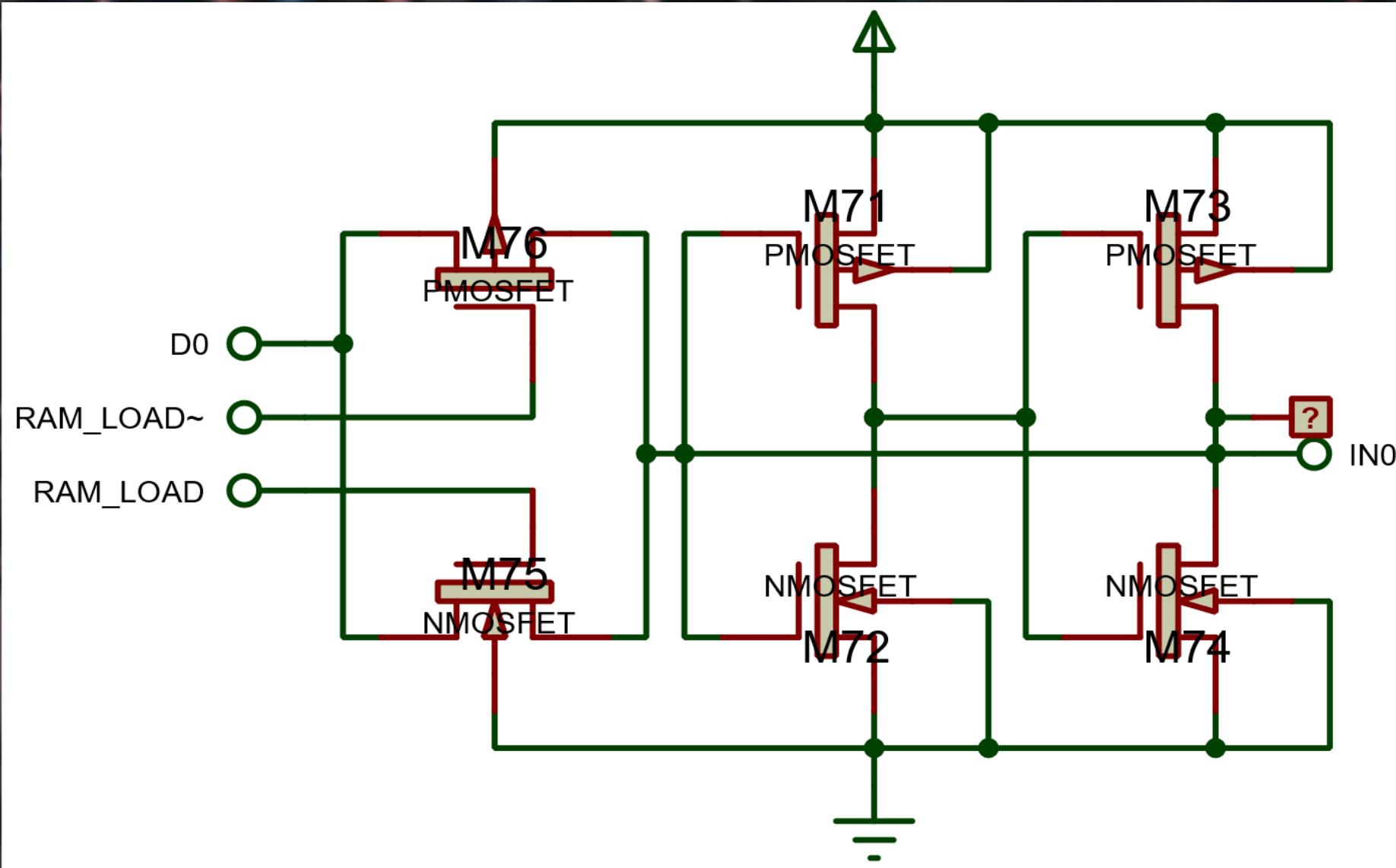
# MUX 8:1



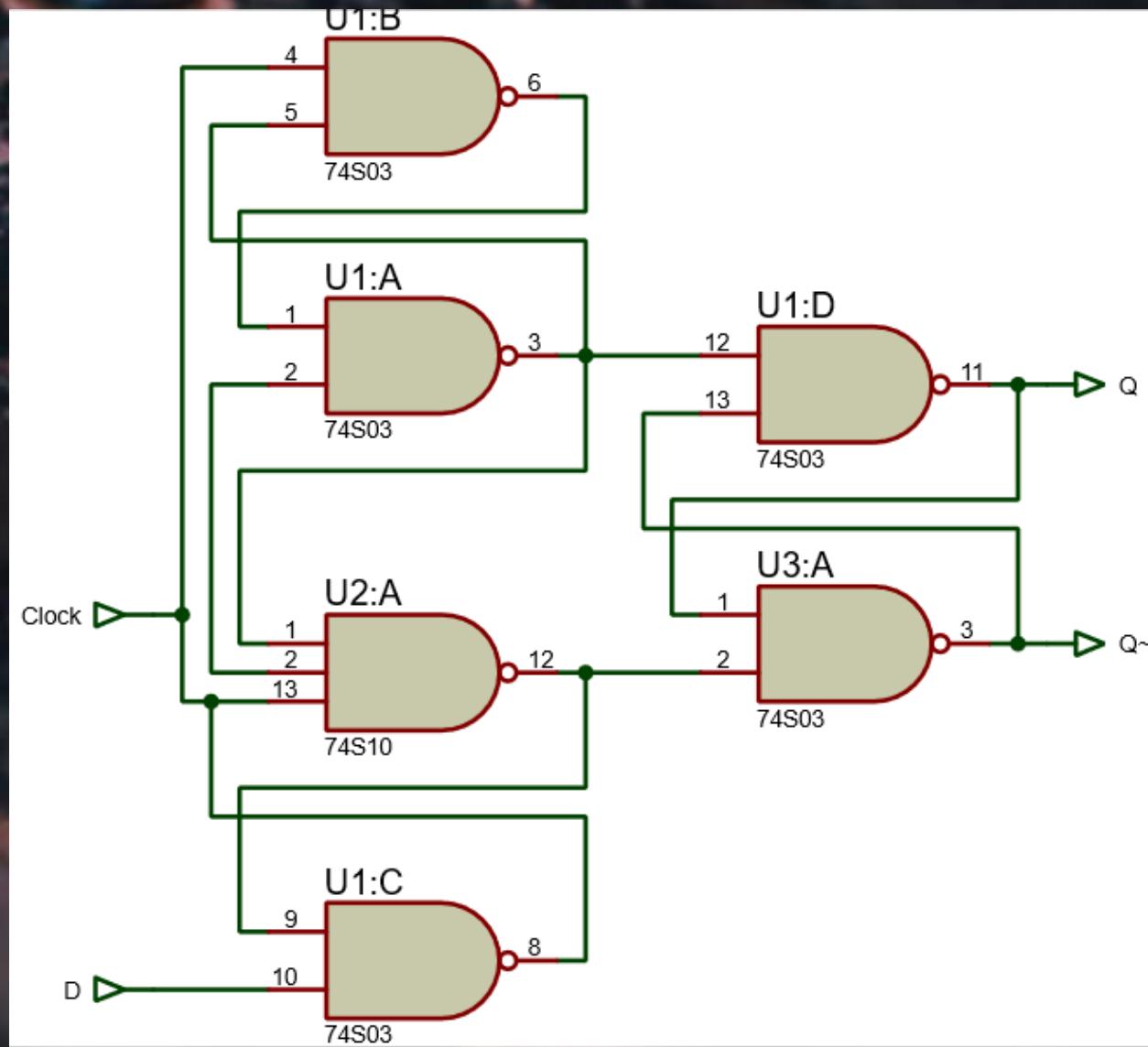
[3]

# SRAM UNIT CELL

[2]



# POSITIVE EDGE TRIGGERED D FLIP-FLOP

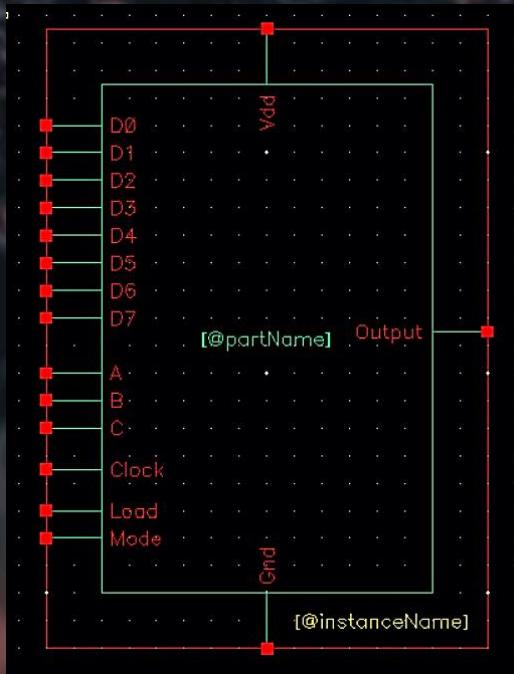


[4]

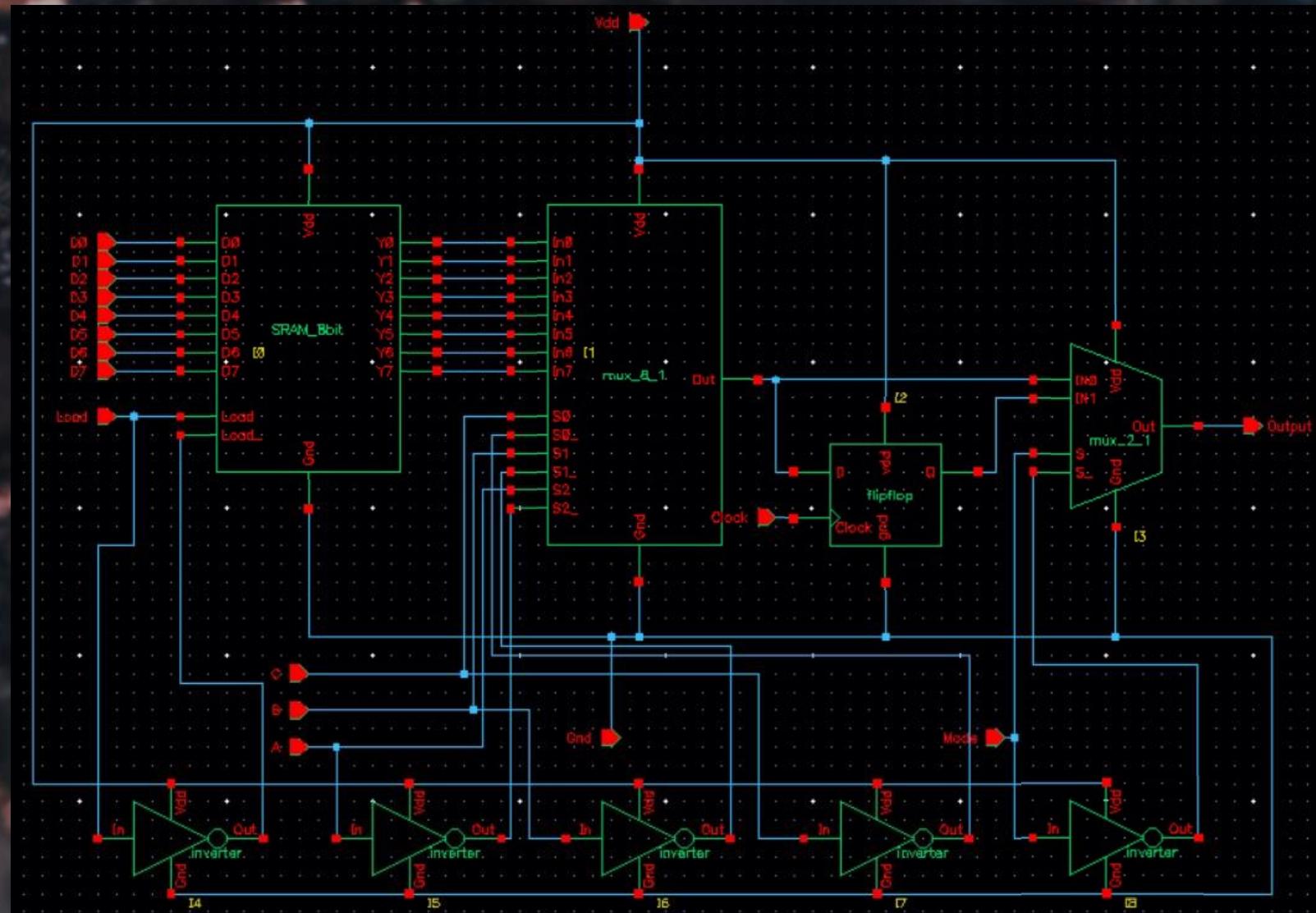
Group 3

# Schematics

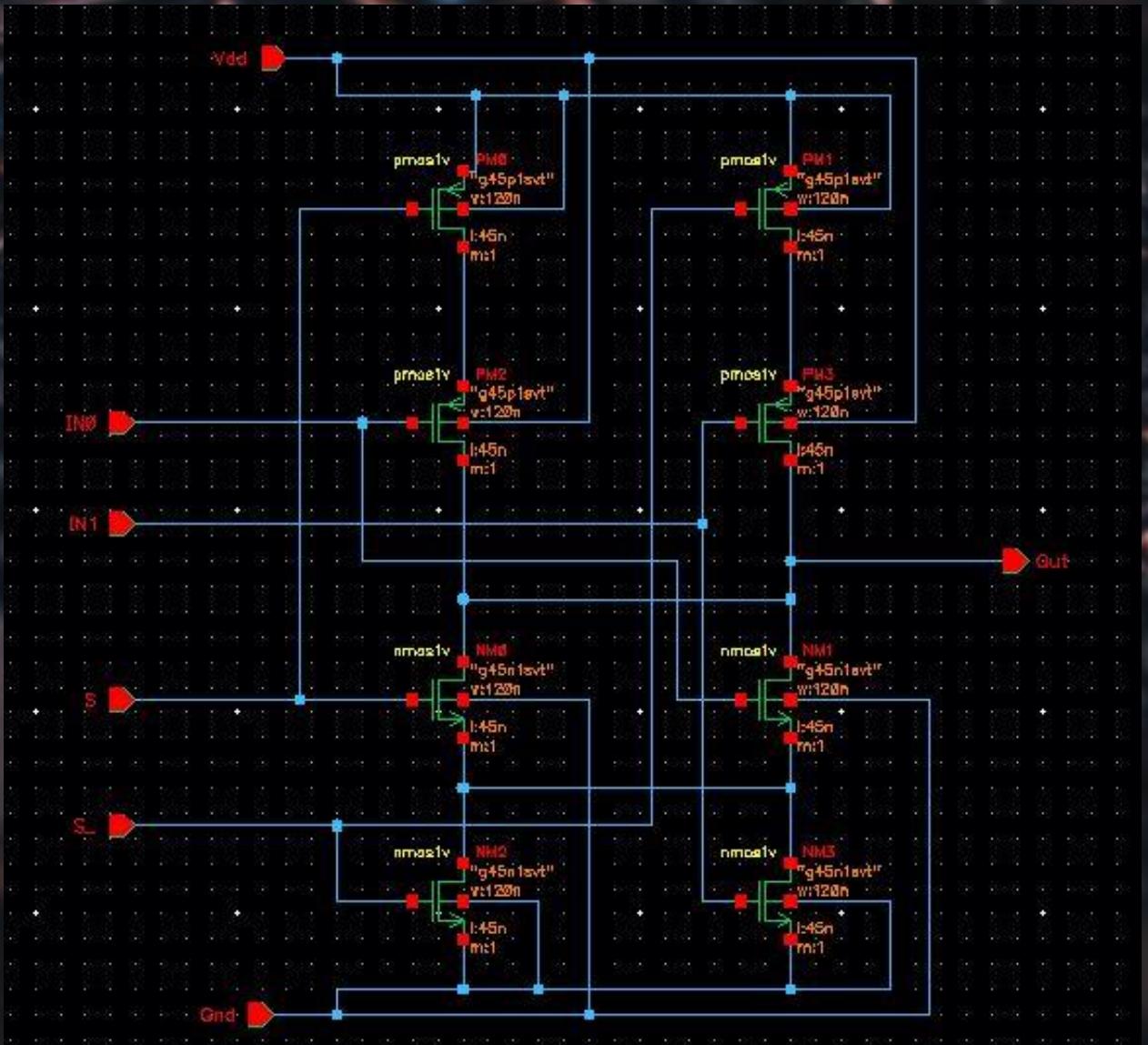
CLB SYMBOL



CLB SCHEMATIC

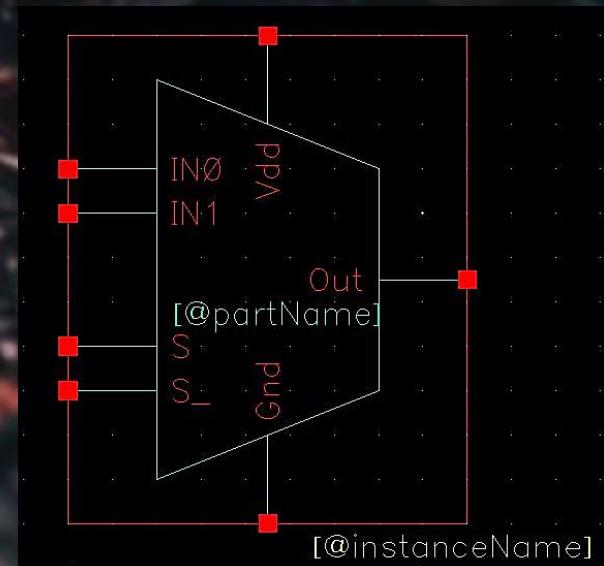


# MUX 2:1 SCHEMATIC

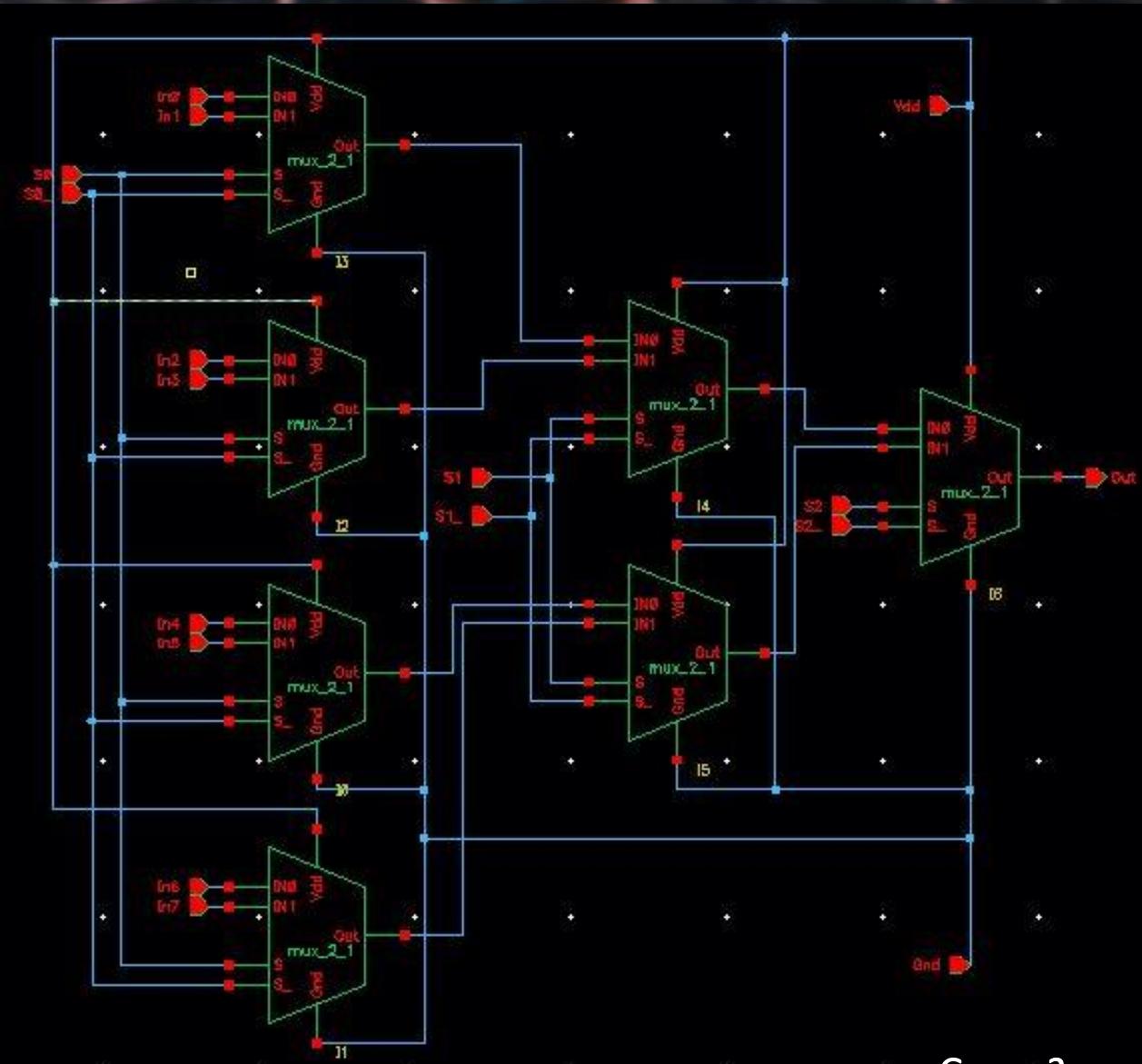


Group 3

SYMBOL



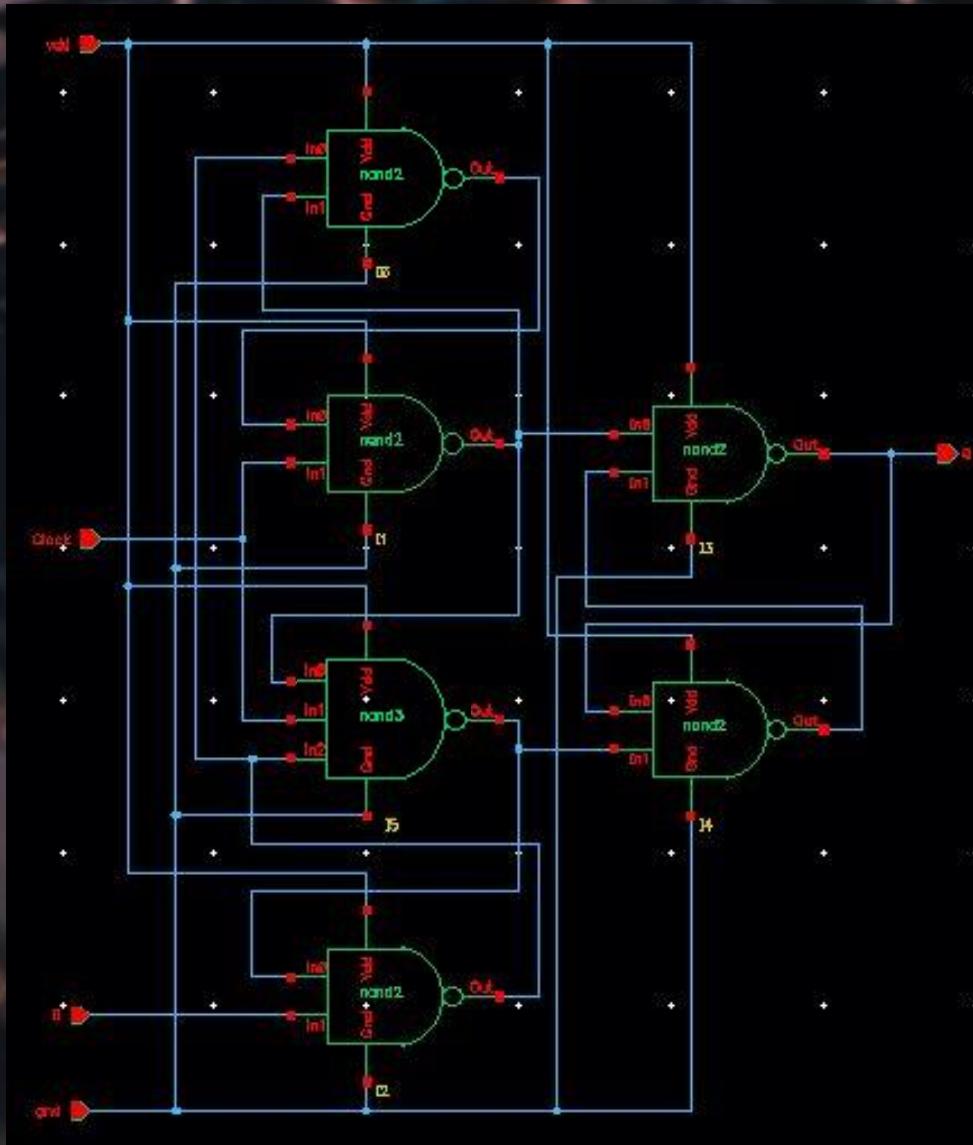
# MUX 8:1 SCHEMATIC



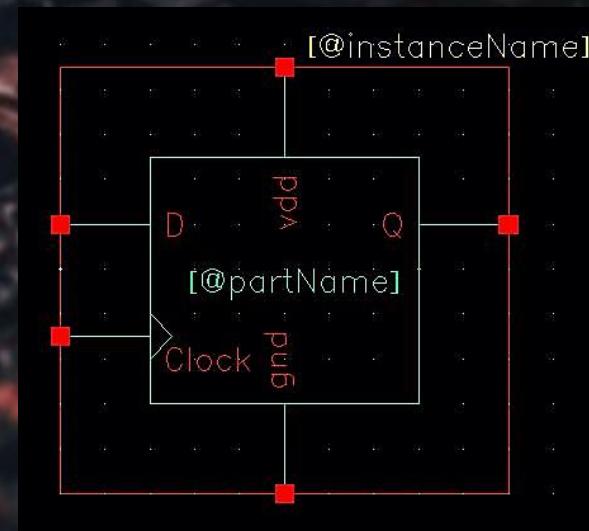
SYMBOL



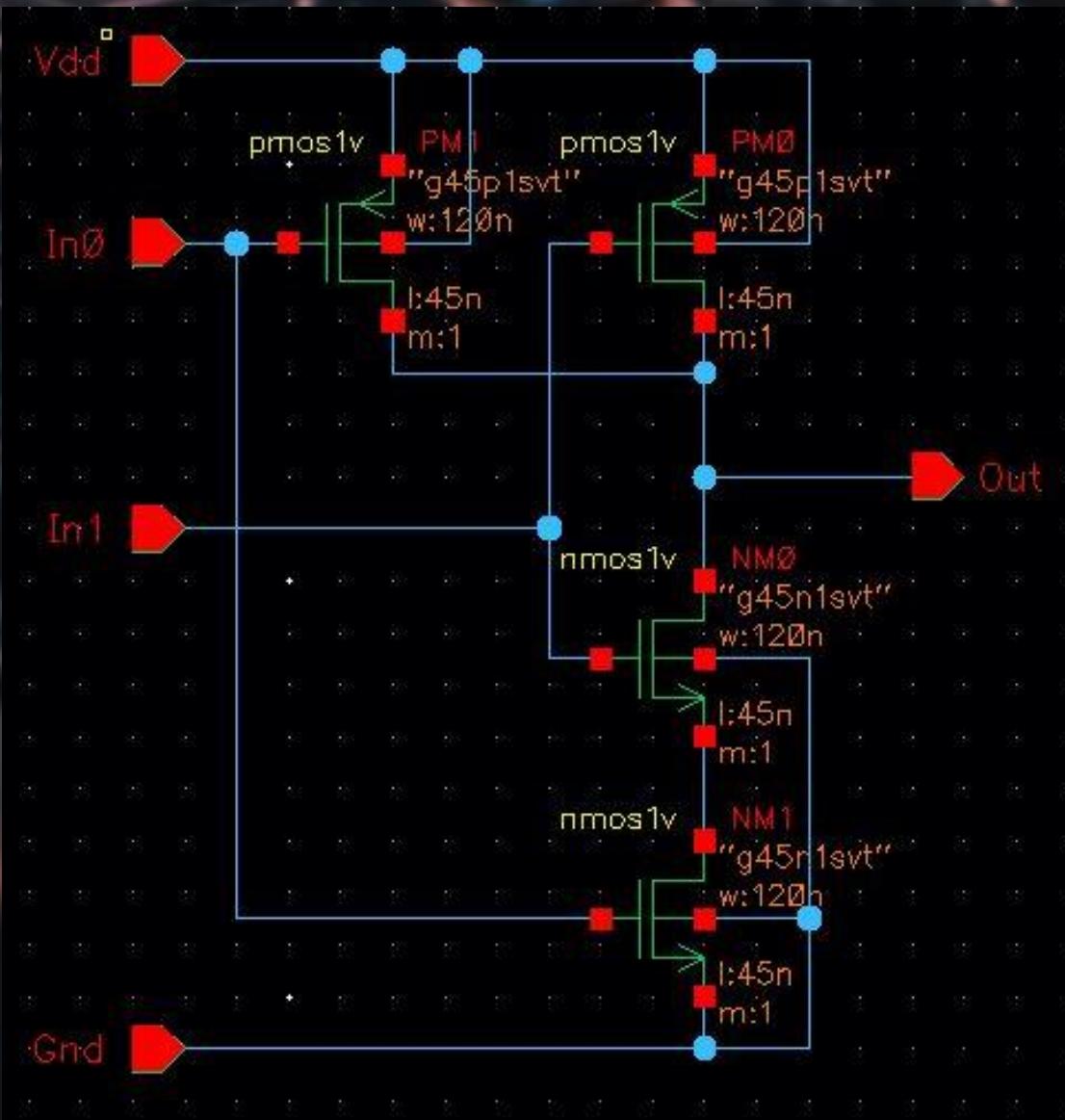
# D FLIP-FLOP SCHEMATIC



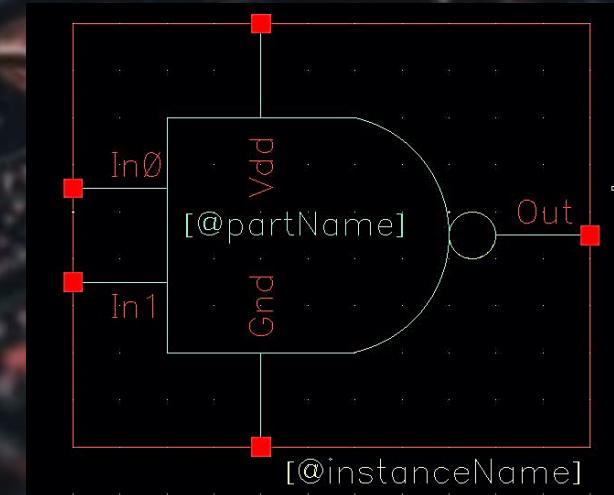
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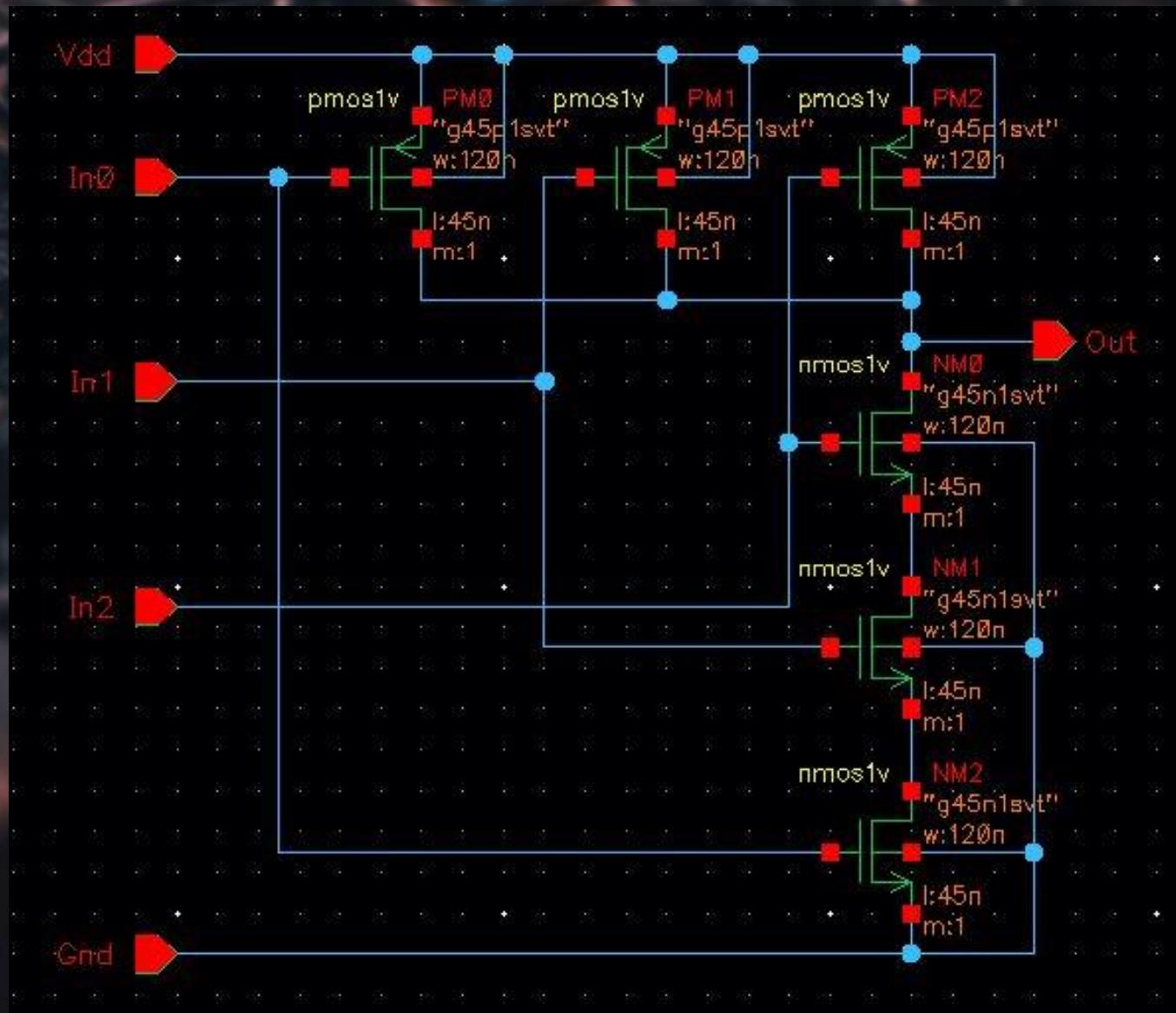
# 2 INPUT NAND SCHEMATIC



SYMBOL

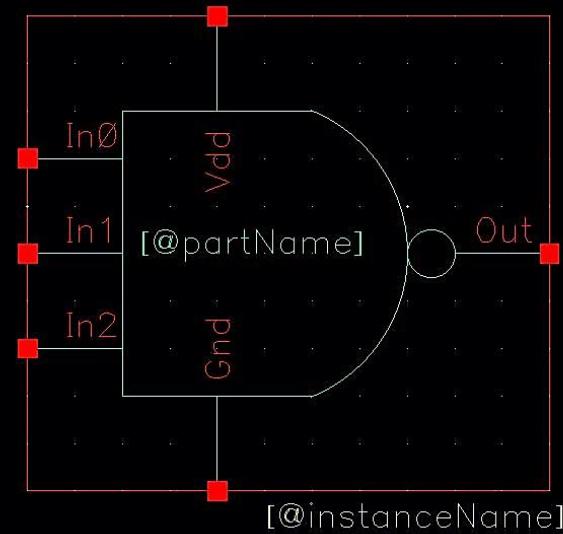


# 3 INPUT NAND SCHEMATIC

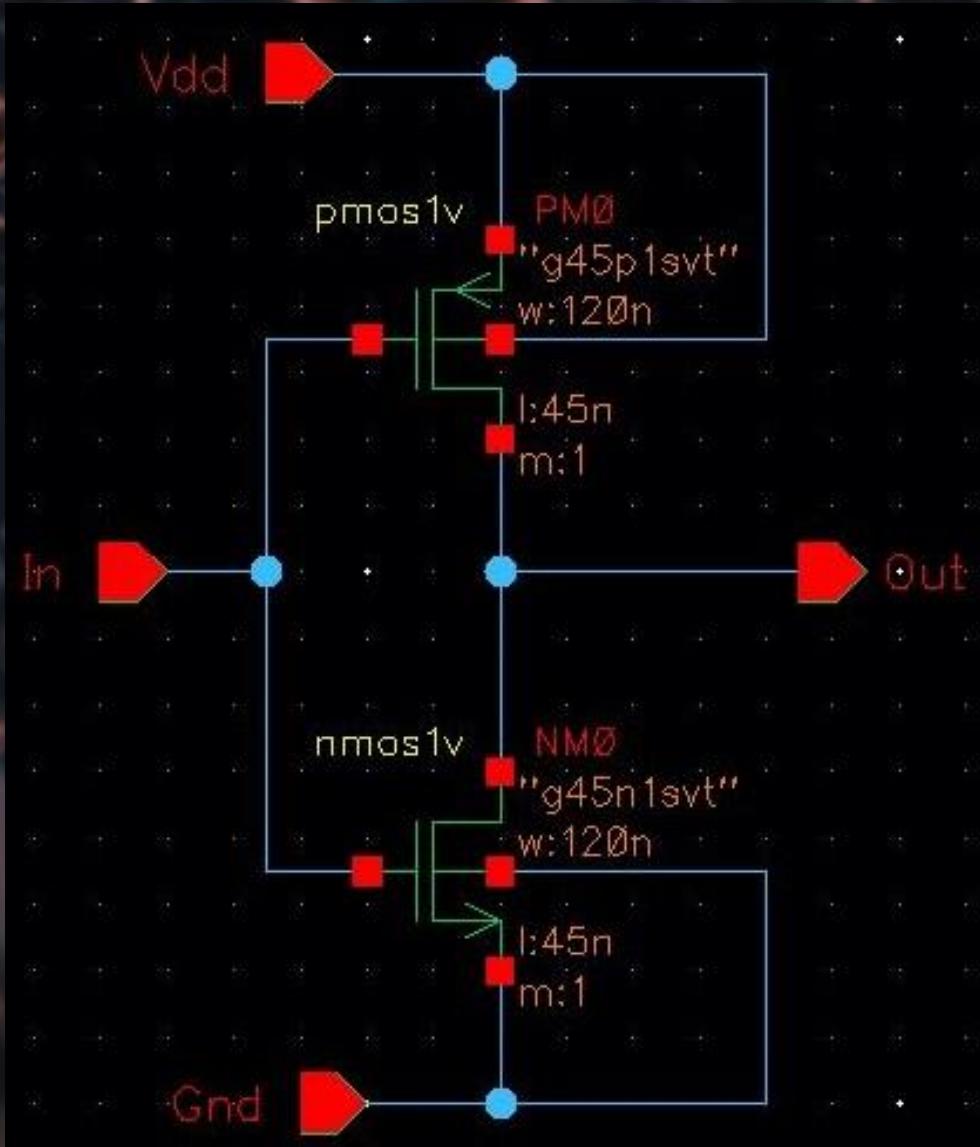


Group 3

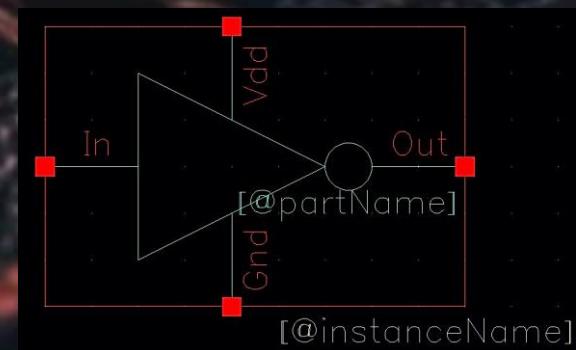
SYMBOL



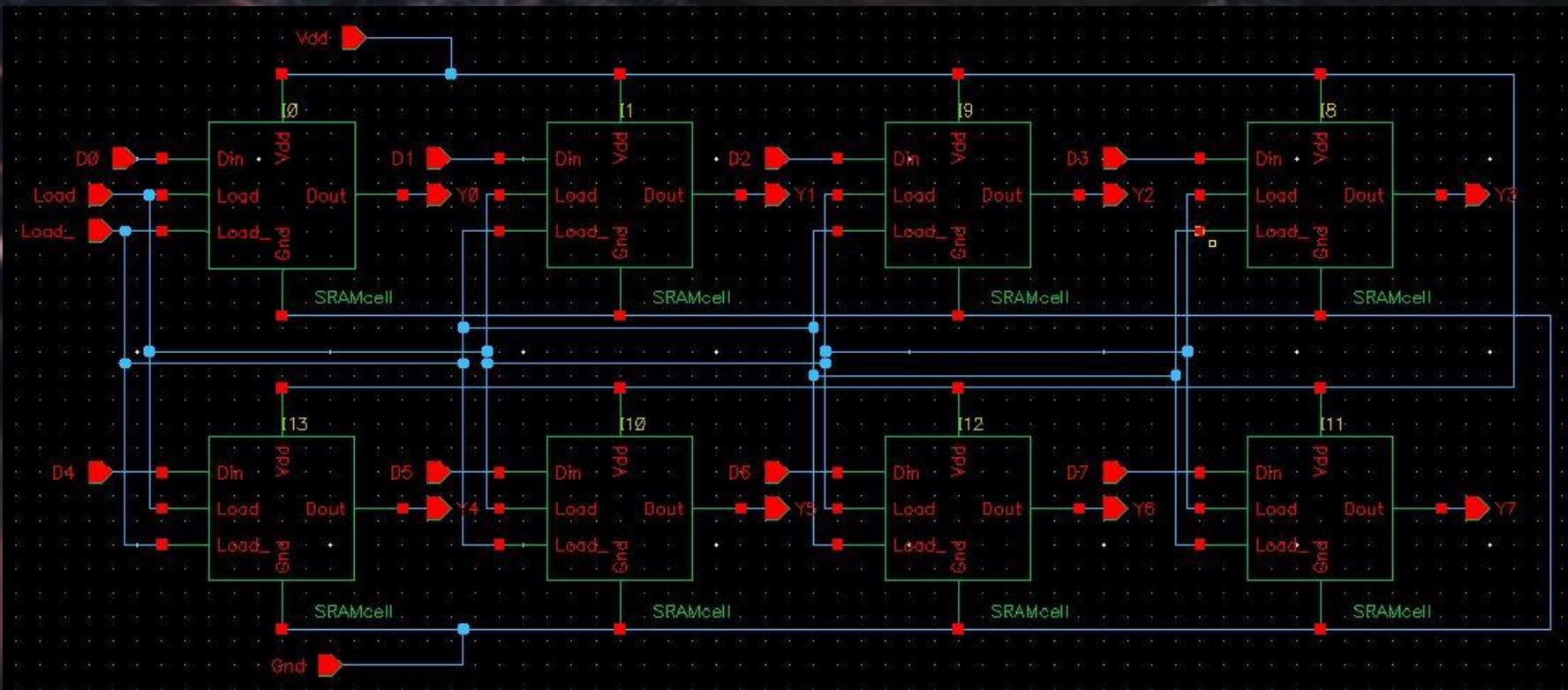
# INVERTER SCHEMATIC



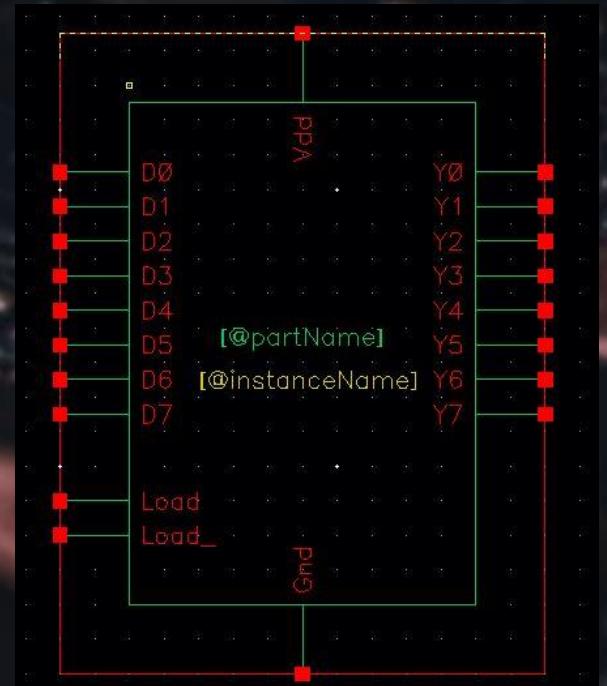
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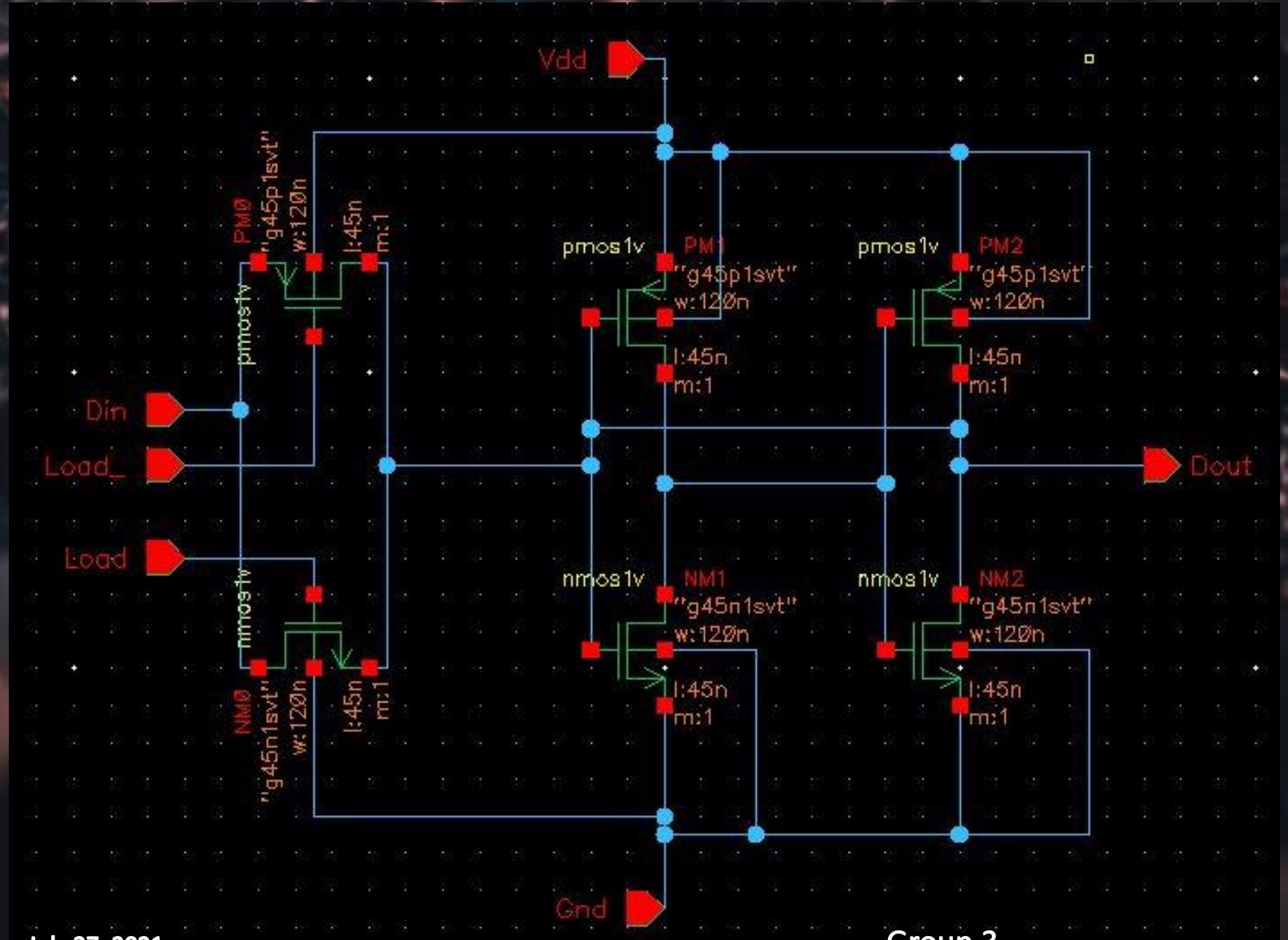
# SRAM SCHEMATIC



SYMBOL

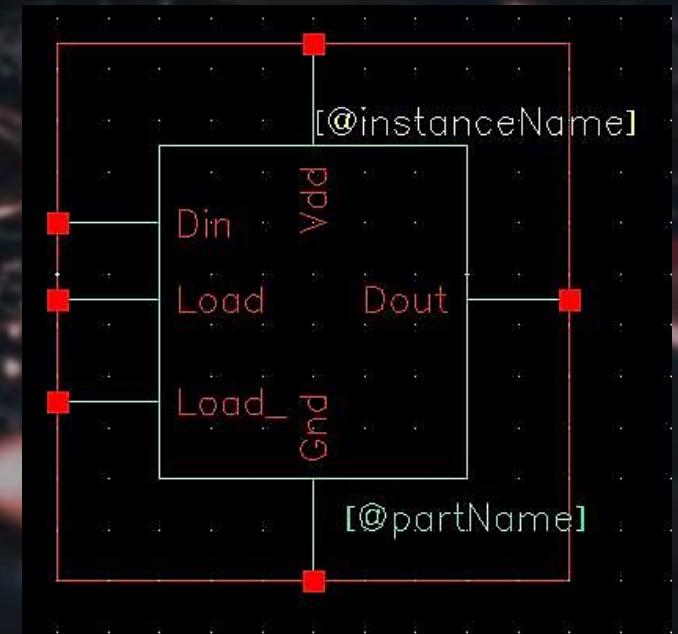


# SRAM CELL SCHEMATIC



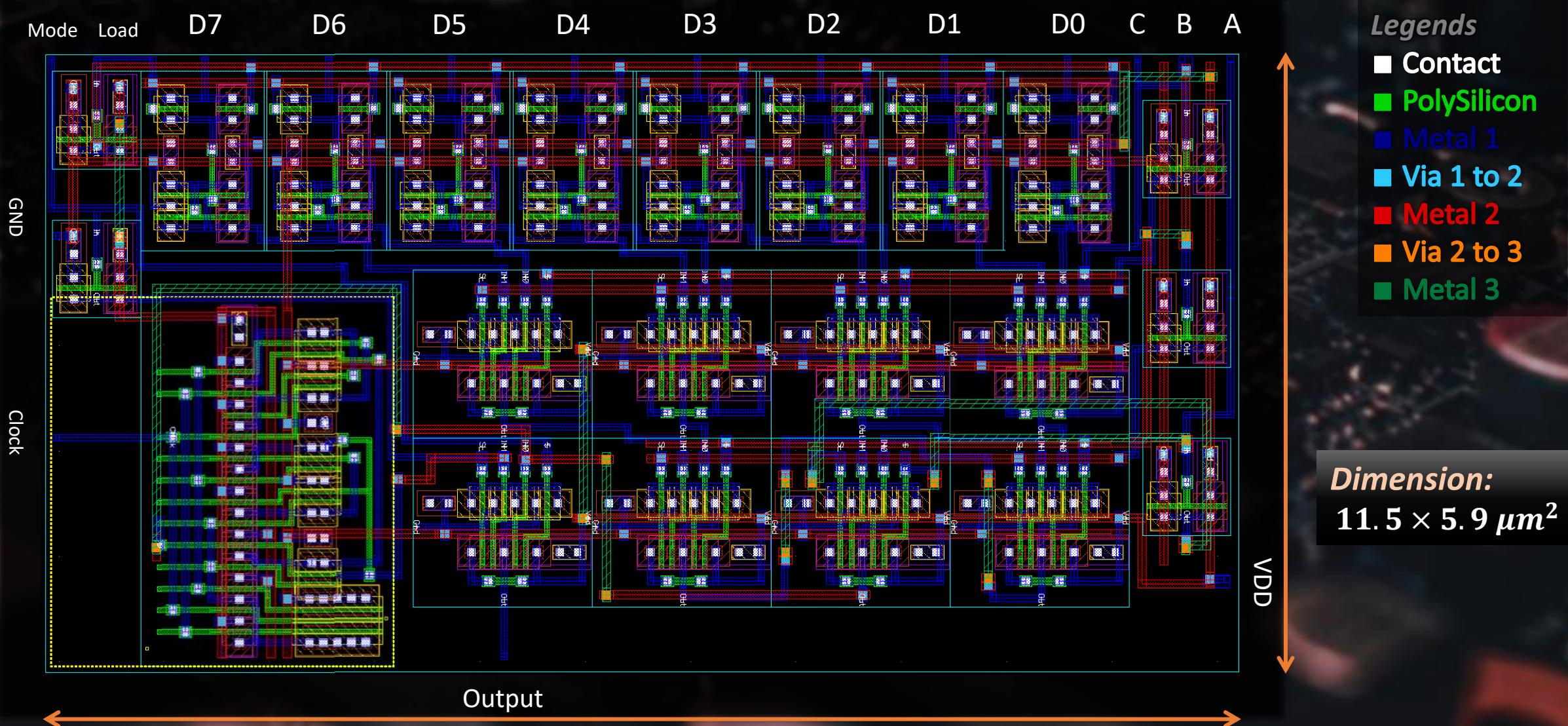
Group 3

## SYMBOL

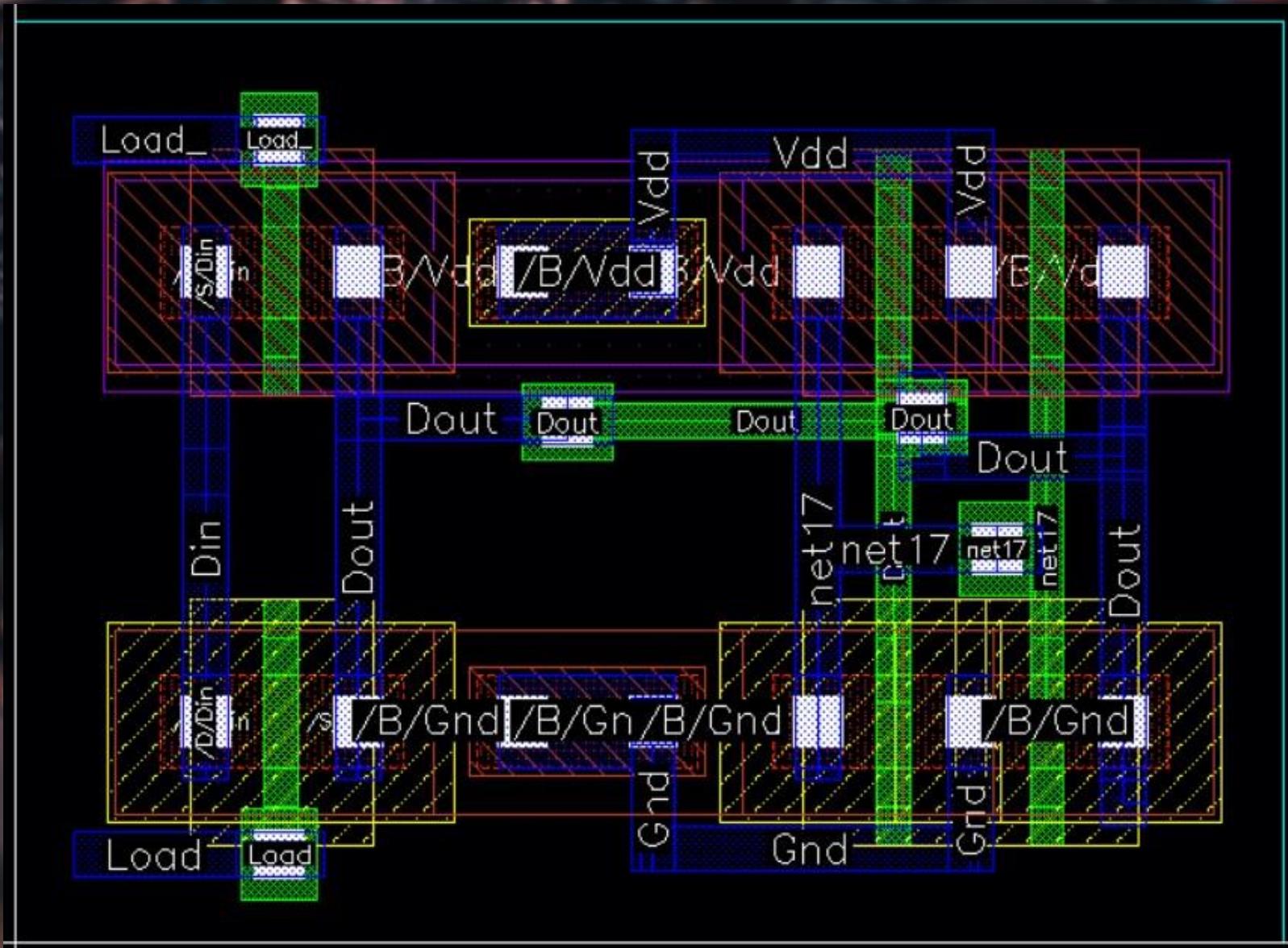


# Layout

## CLB LAYOUT

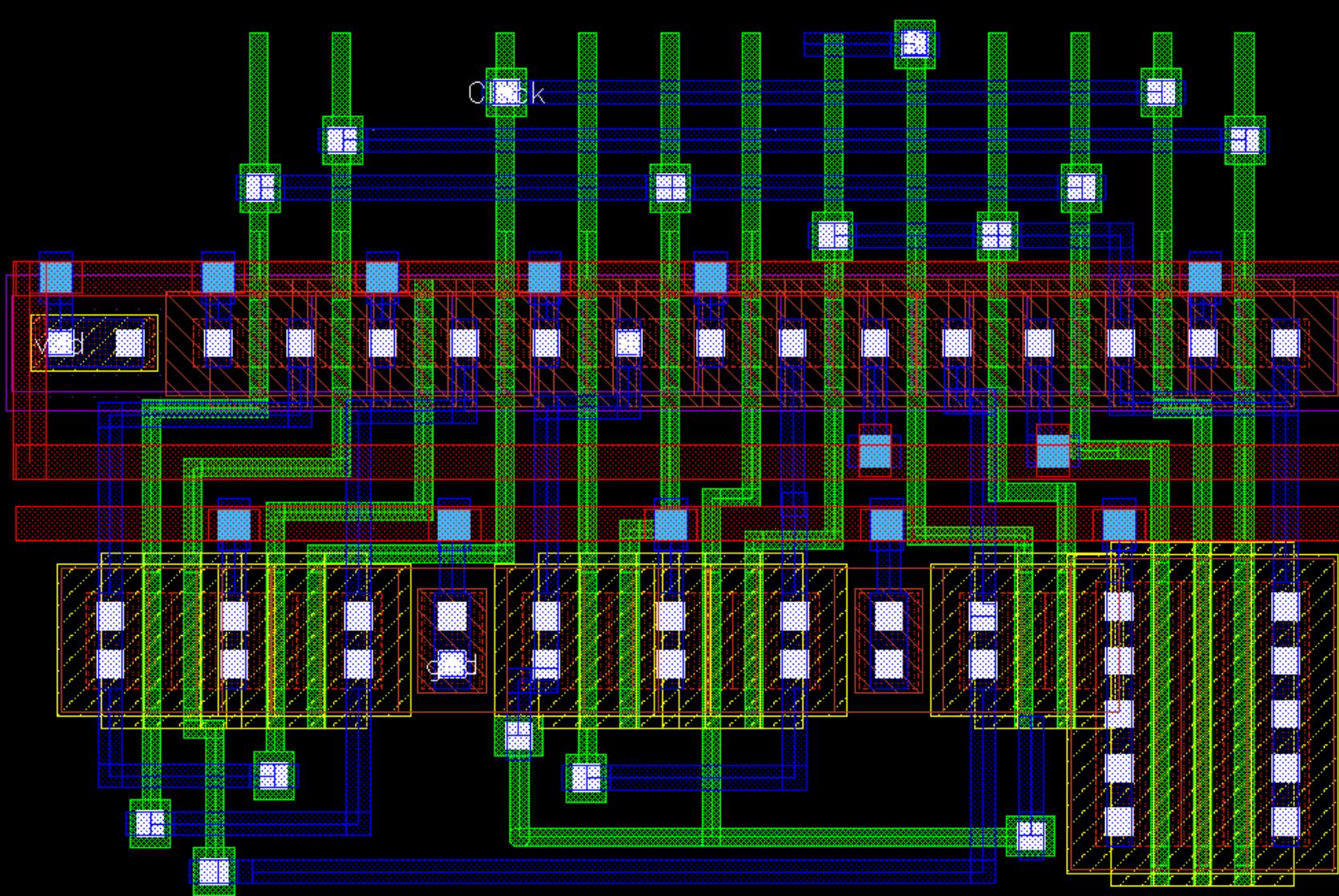


# SRAM CELL Layout



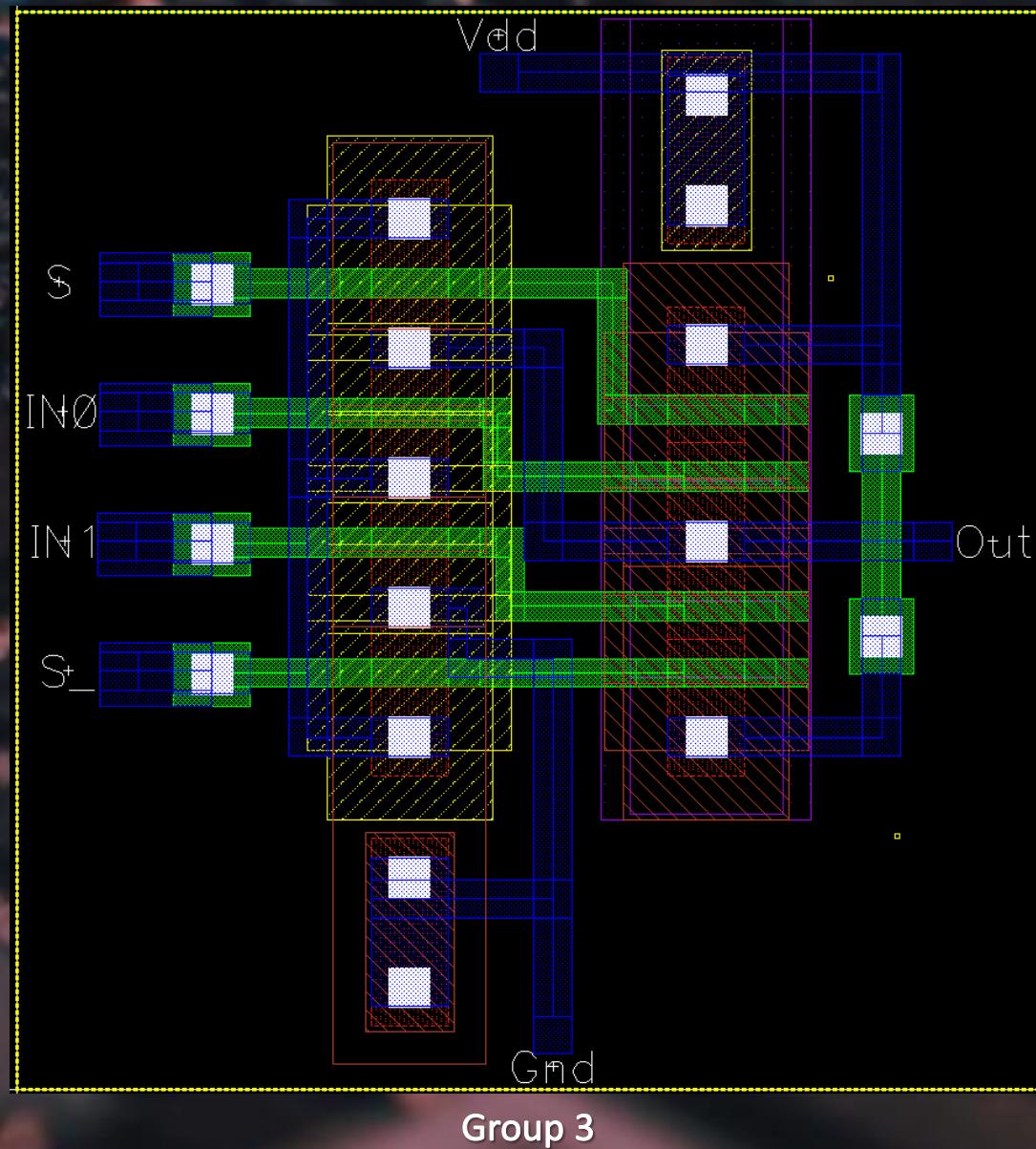
Group 3

# D FLIP-FLOP Layout

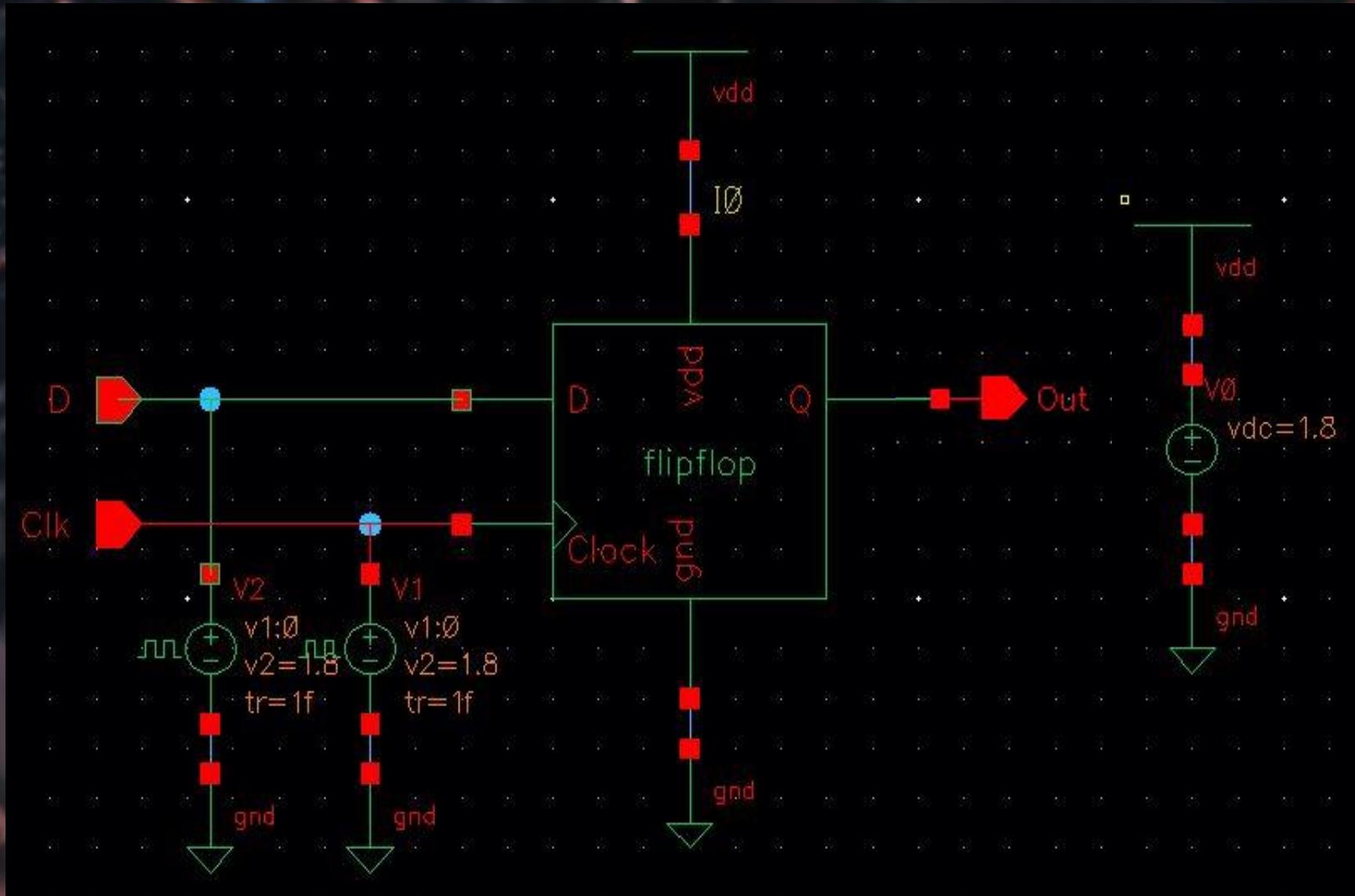


Group 3

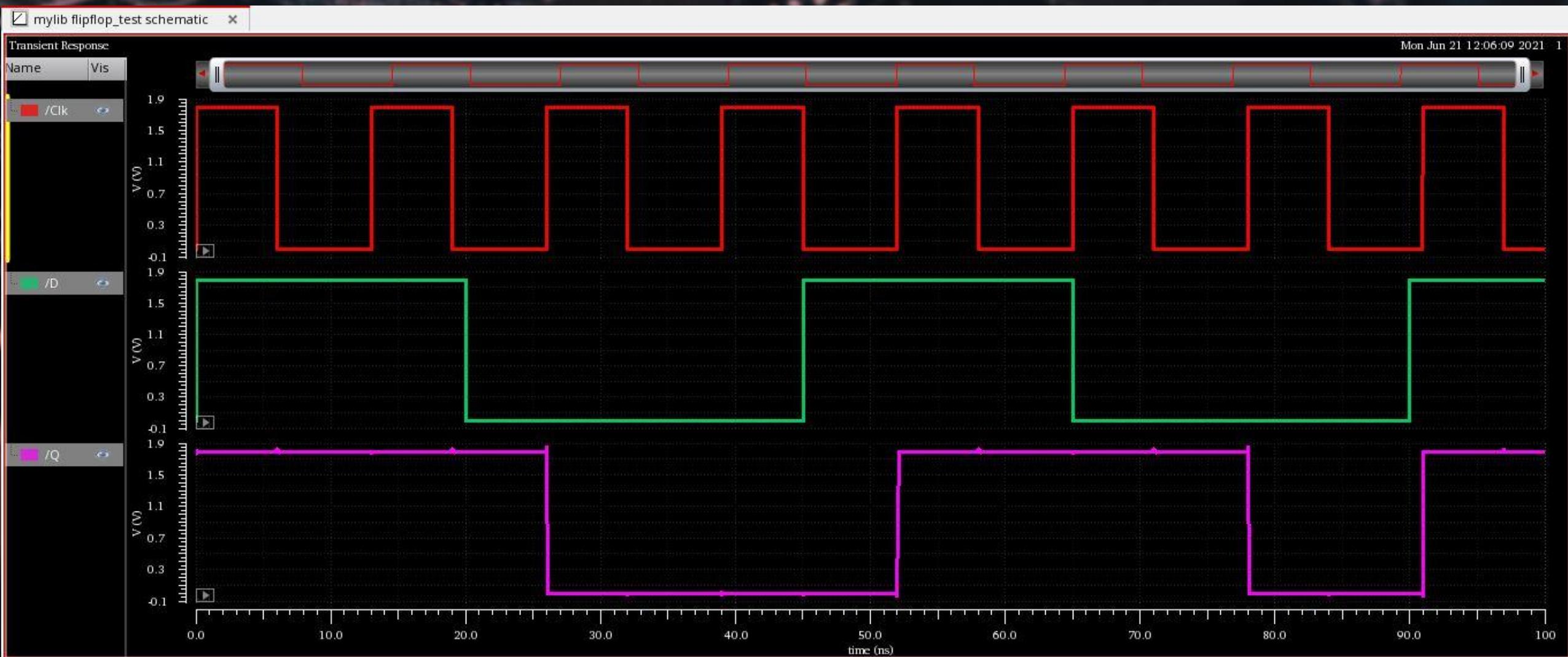
# MUX 2:1 Layout



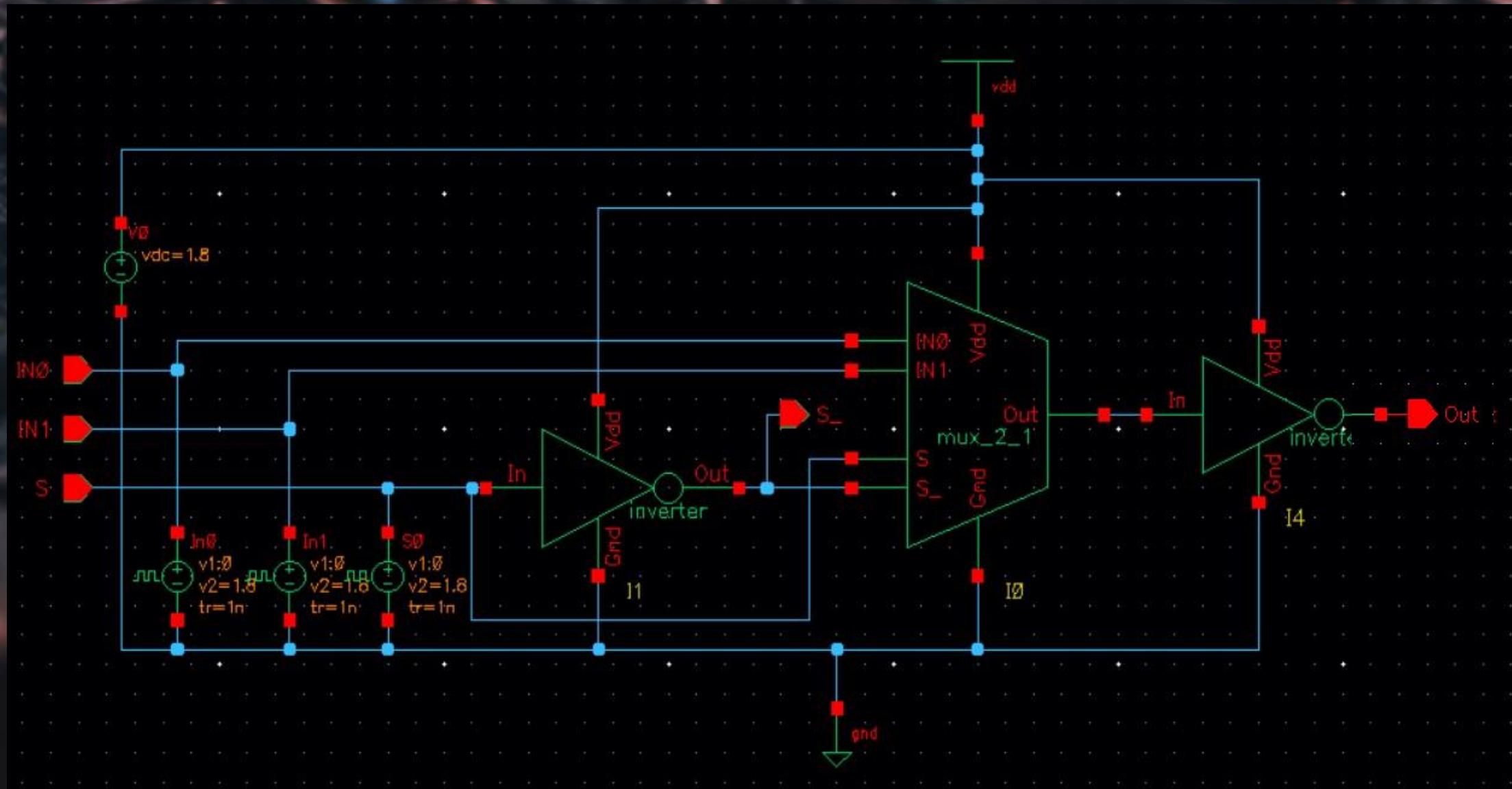
# Functionality Test (D FLIP-FLOP)



# OUTPUT (D FLIP-FLOP)



# Functionality Test (MUX 2:1)

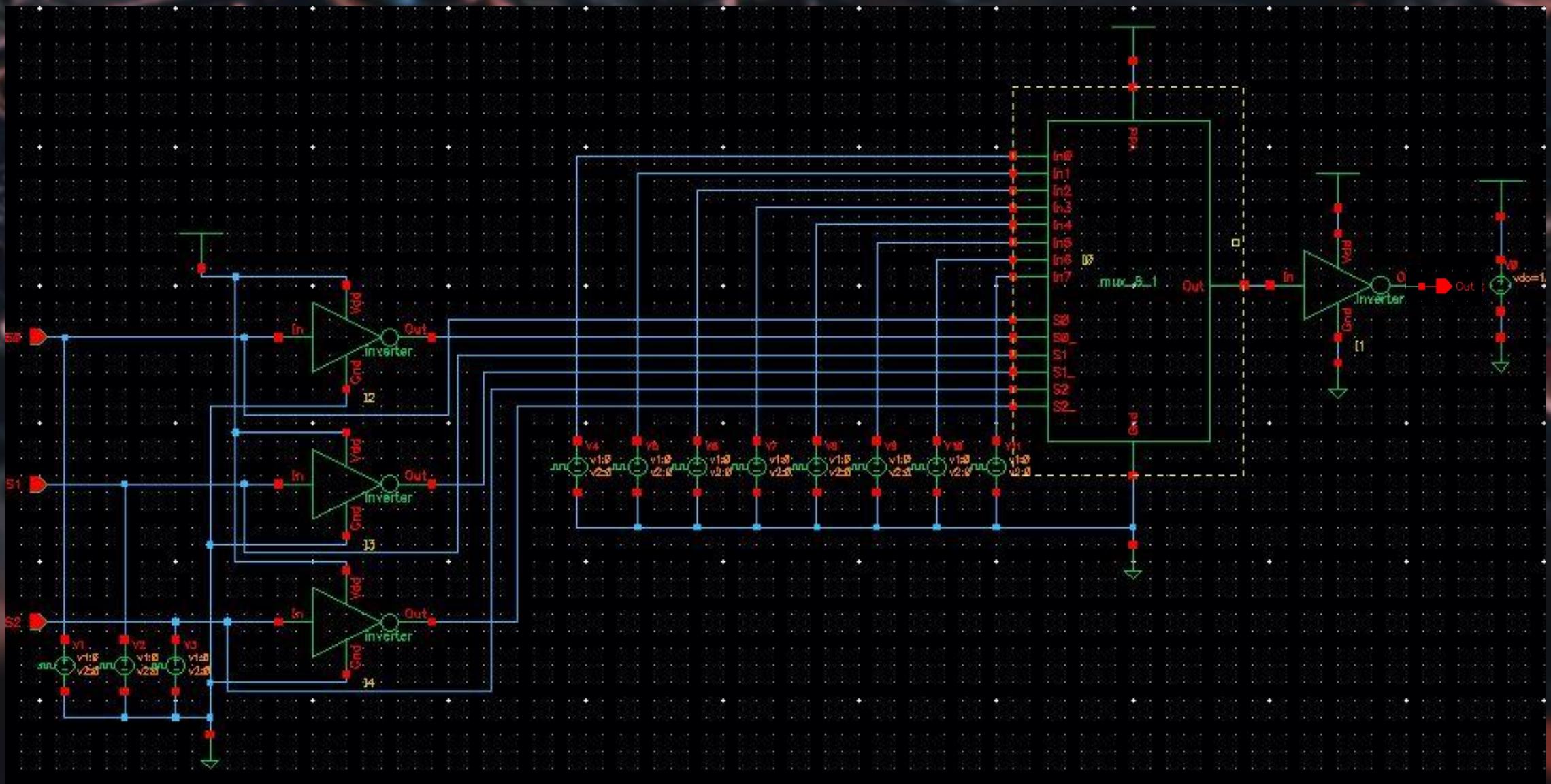


Group 3

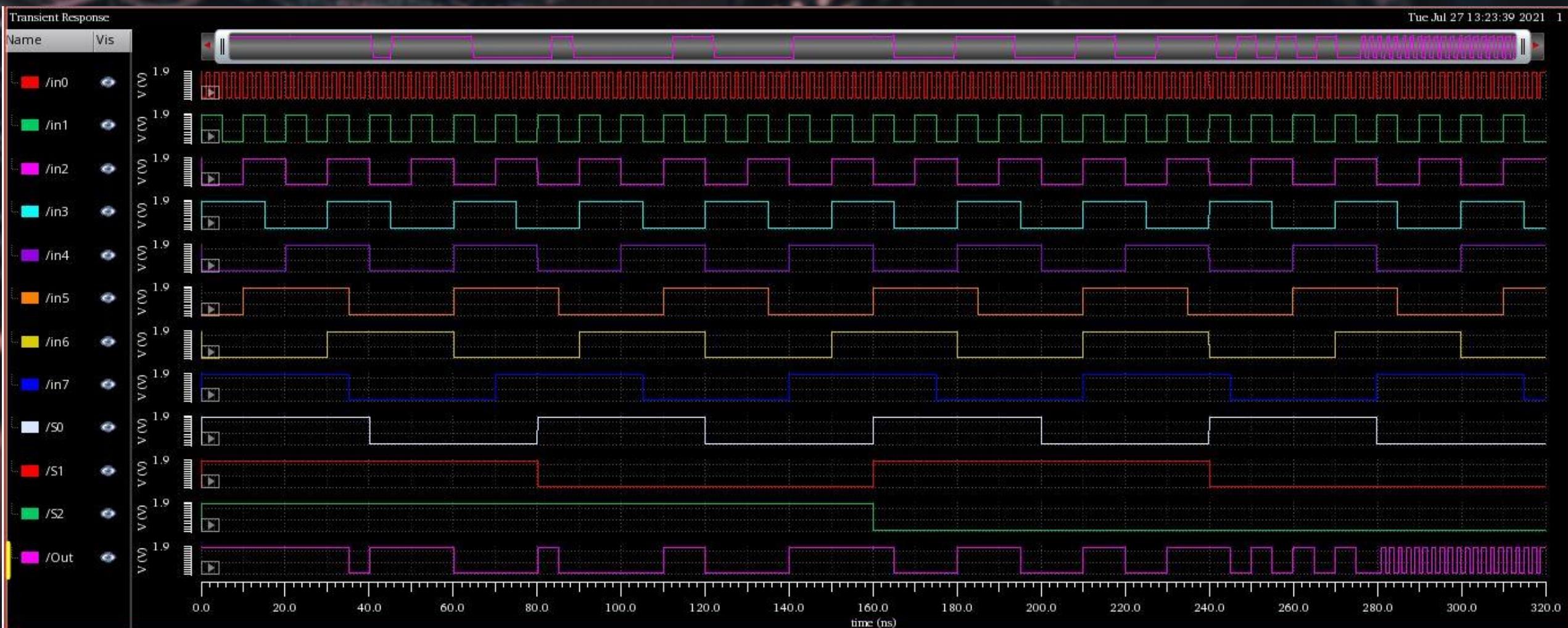
# OUTPUT (MUX 2:1)



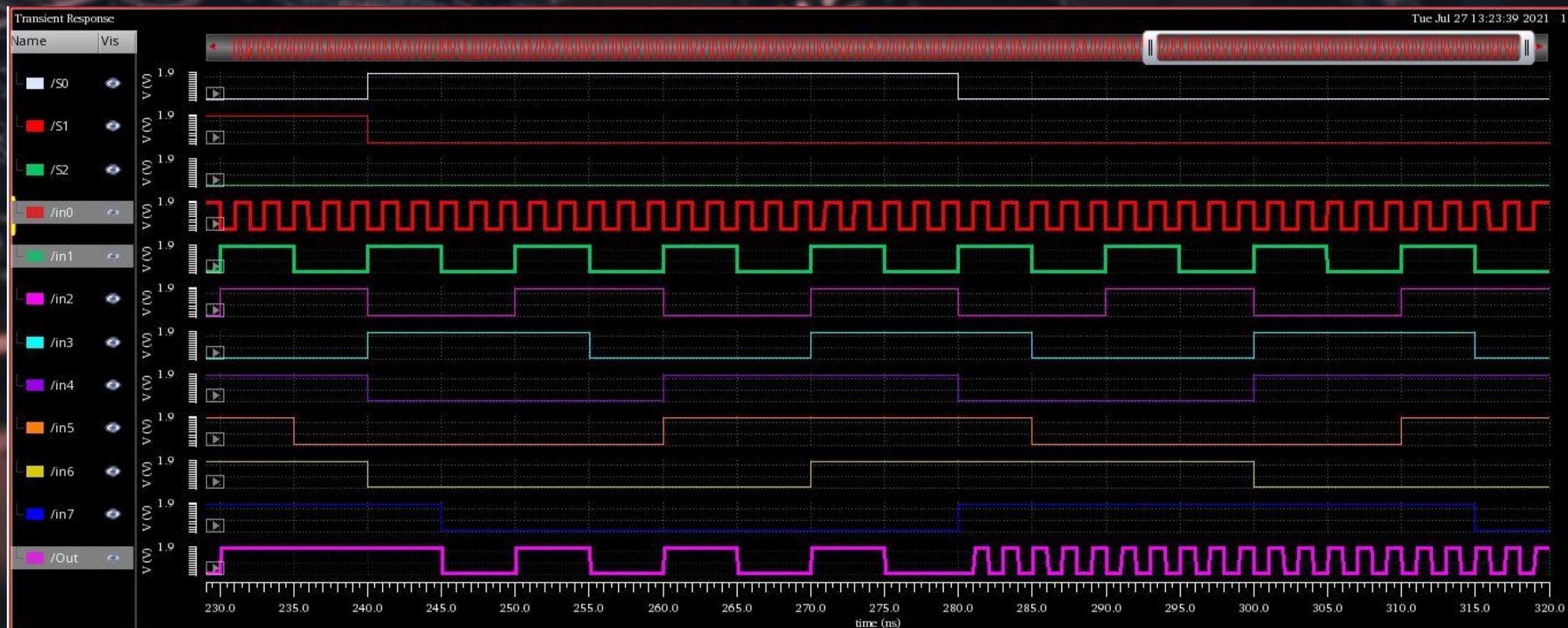
# Functionality Test (MUX 8:1)



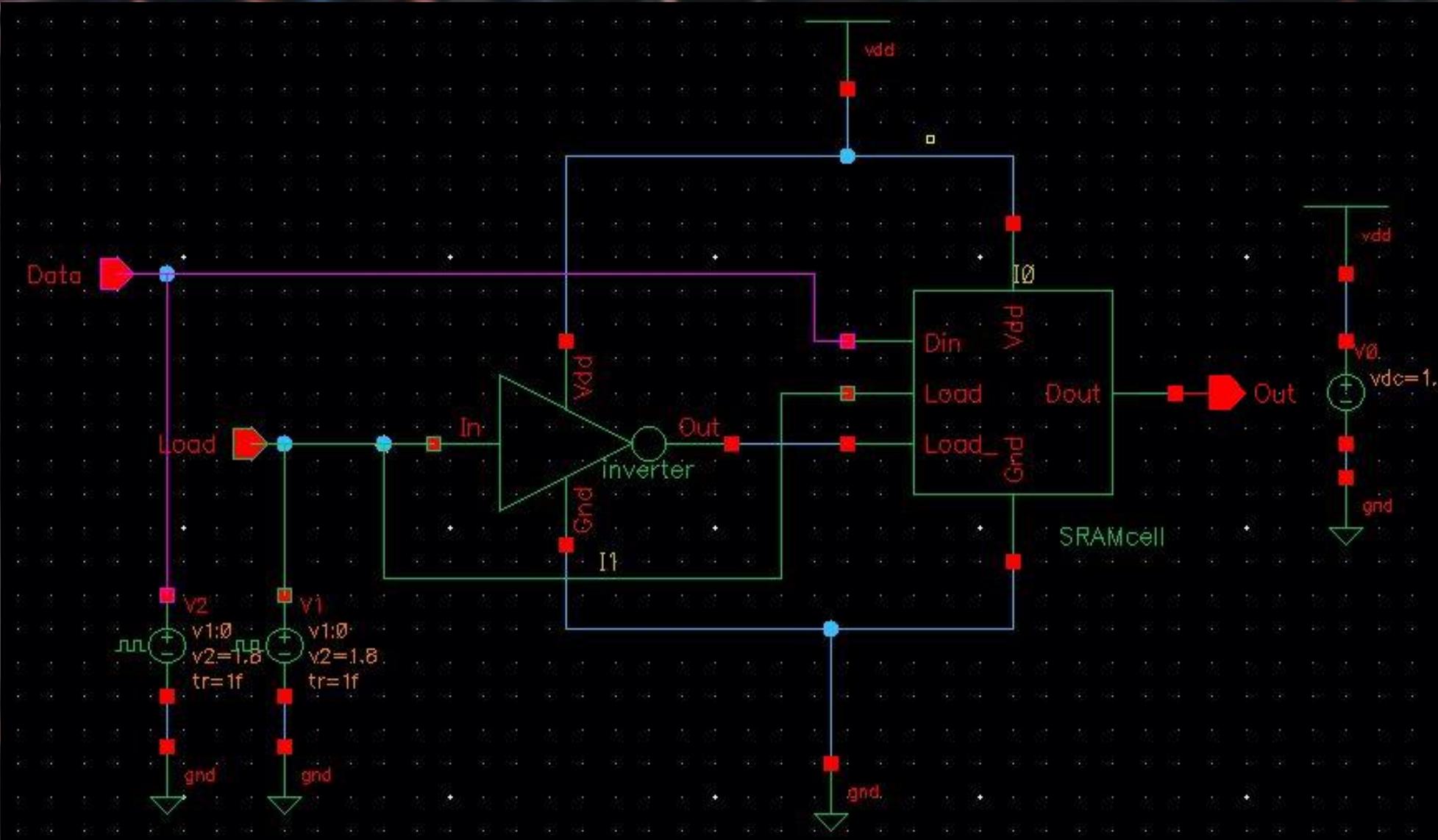
# OUTPUT (MUX 8:1)



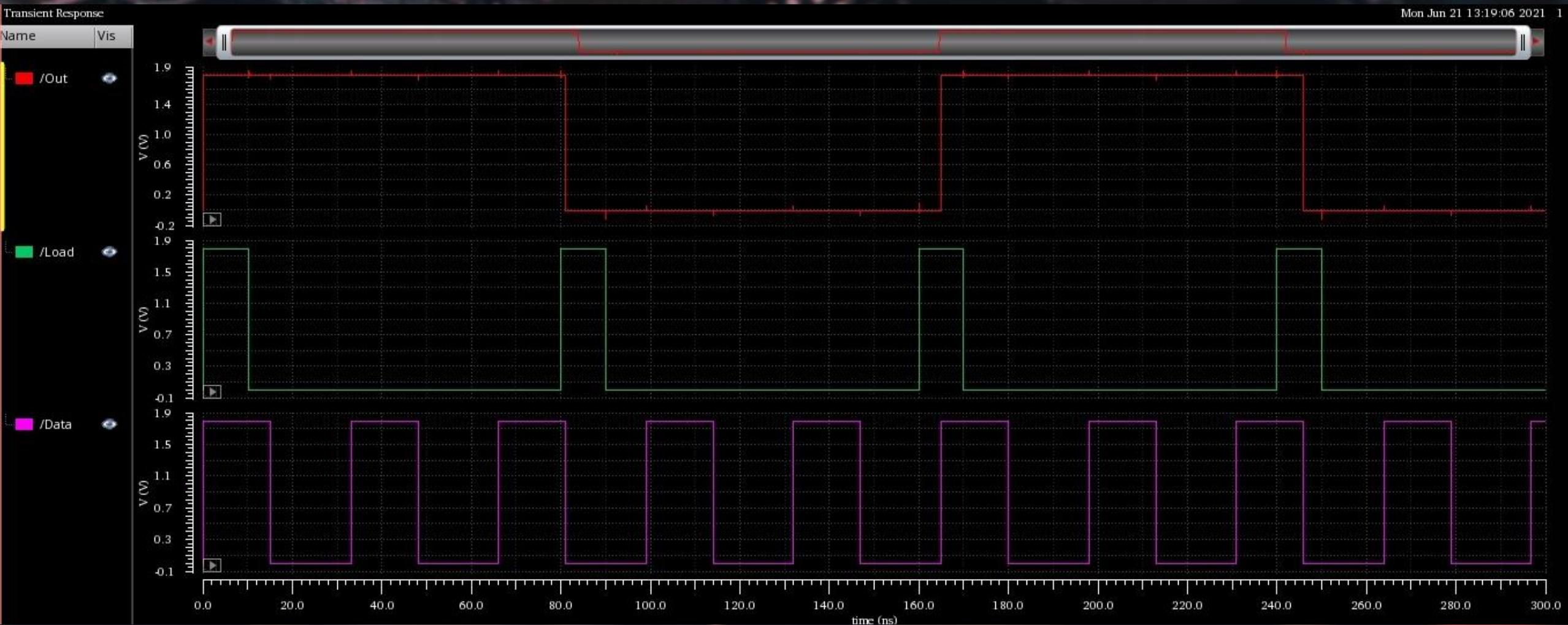
# OUTPUT (MUX 8:1) [ZOOMED]



# Functionality Test (SRAM CELL)



# OUTPUT (SRAM CELL)



# Circuit Analysis

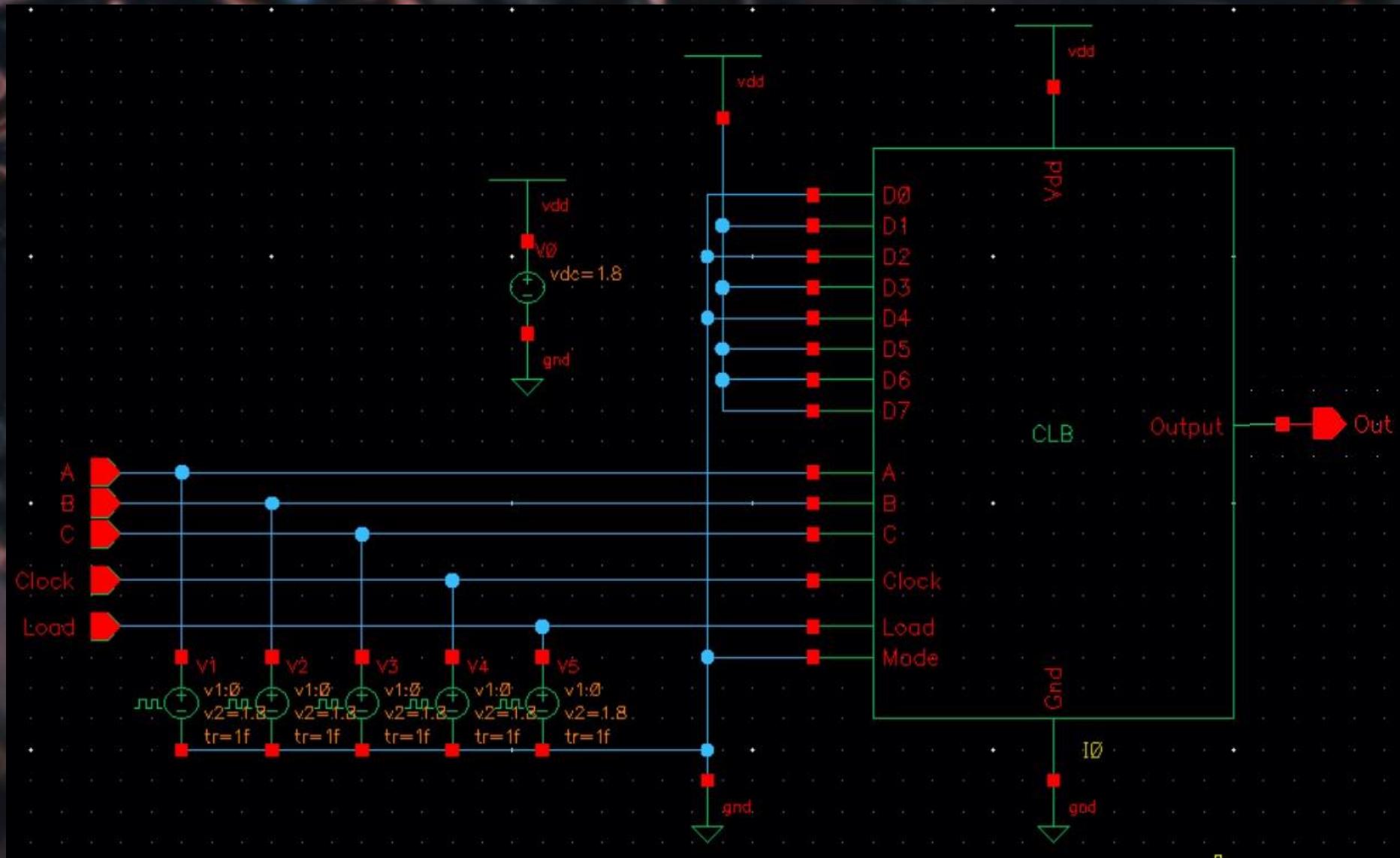
Function

$$F = AB + C$$

Truth Table

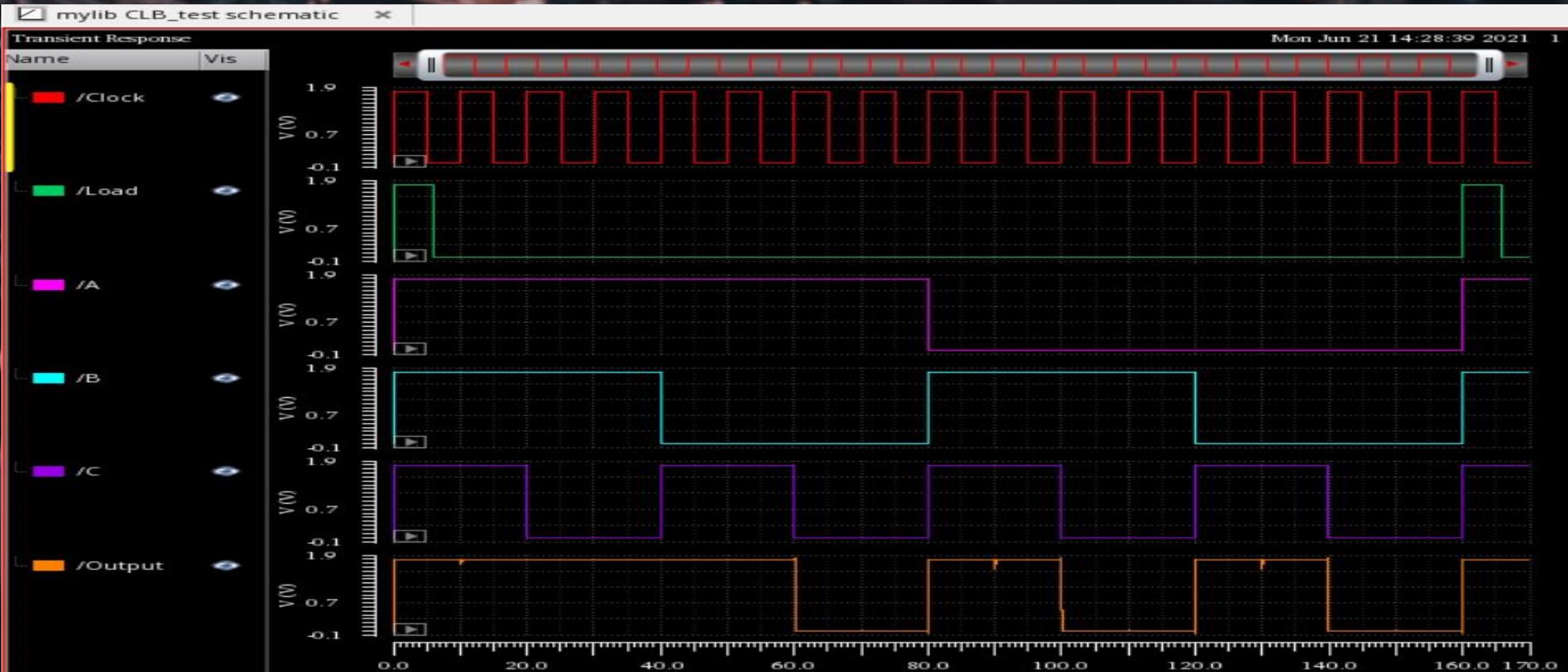
States	A	B	C	AB + C
state0	0	0	0	0
state1	0	0	1	1
state2	0	1	0	0
state3	0	1	1	1
state4	1	0	0	0
state5	1	0	1	1
state6	1	1	0	1
state7	1	1	1	1

# Functionality Test (CLB) [Combinatorial]

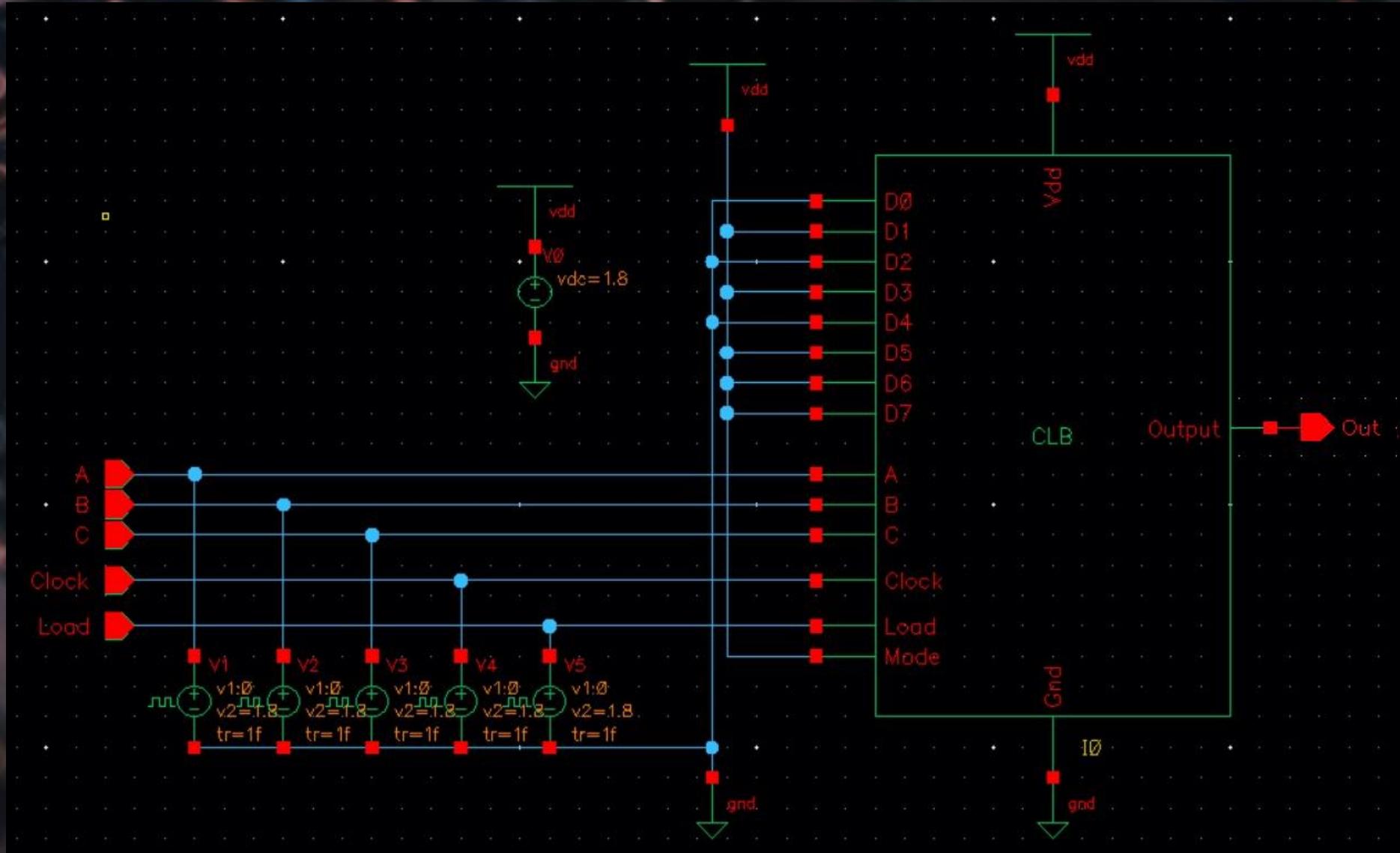


Group 3

# OUTPUT (CLB) [Combinatorial]

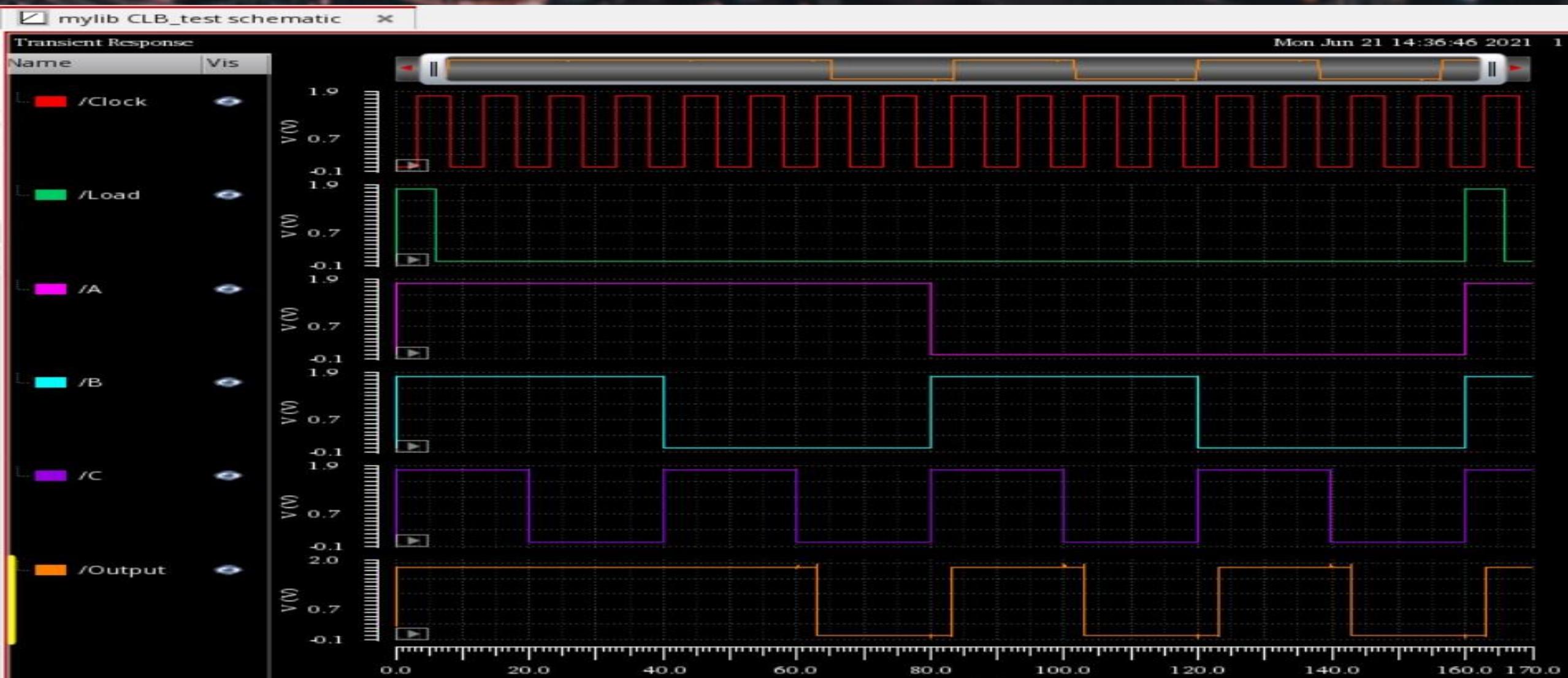


# Functionality Test (CLB) [Sequential]



Group 3

# OUTPUT (CLB ) [Sequential]

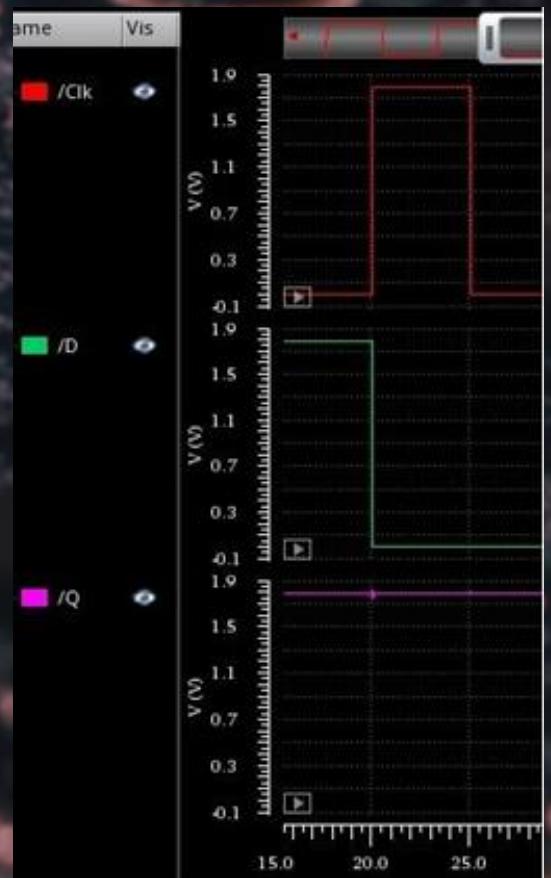


# Circuit Analysis

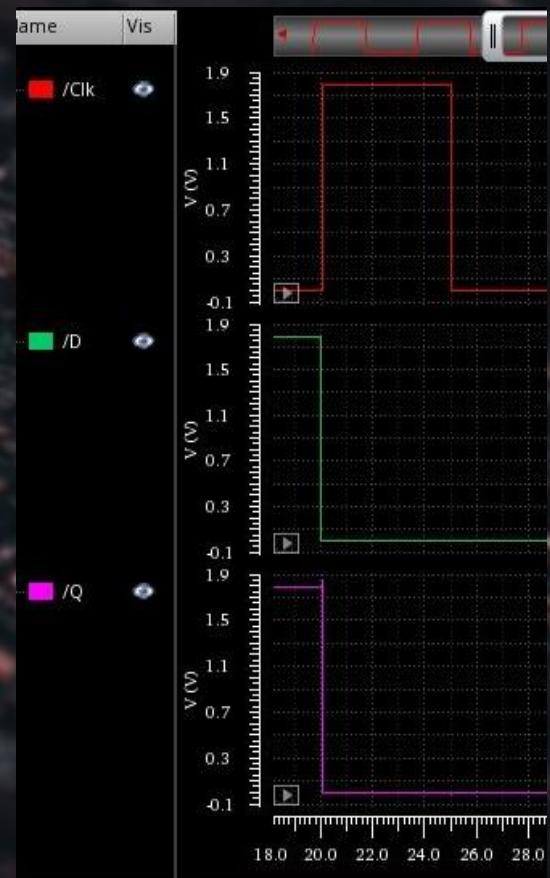
*Minimum clock period = Total combinatorial delay + Clock to Q delay + Setup time*

Time period and maximum frequency calculation

	Time (ps)
<b>Setup Time (Flip Flop)</b>	11 
<b>Clock to Q Delay (Flip Flop)</b>	20.38
<b>Combinatorial Delay</b>	51.25 
<b>Optimal Period</b>	82.63 ~ 82
<b>Critical Period</b>	65 



Failed setup (clock lags D by 10ps)



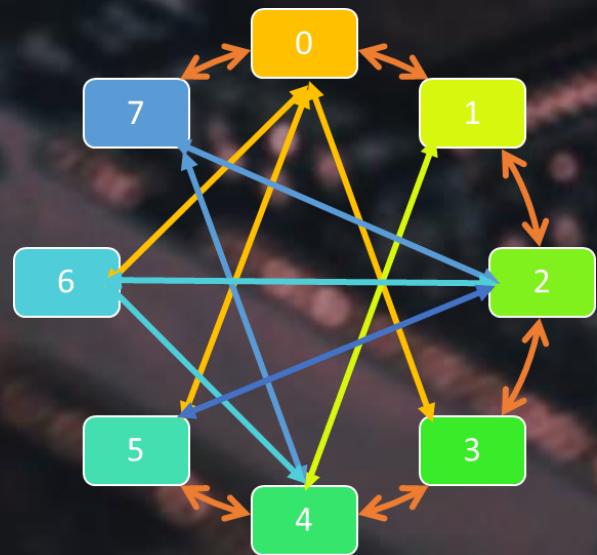
Setup Success (clock lags D by 11ps)

# Circuit Analysis

Truth Table

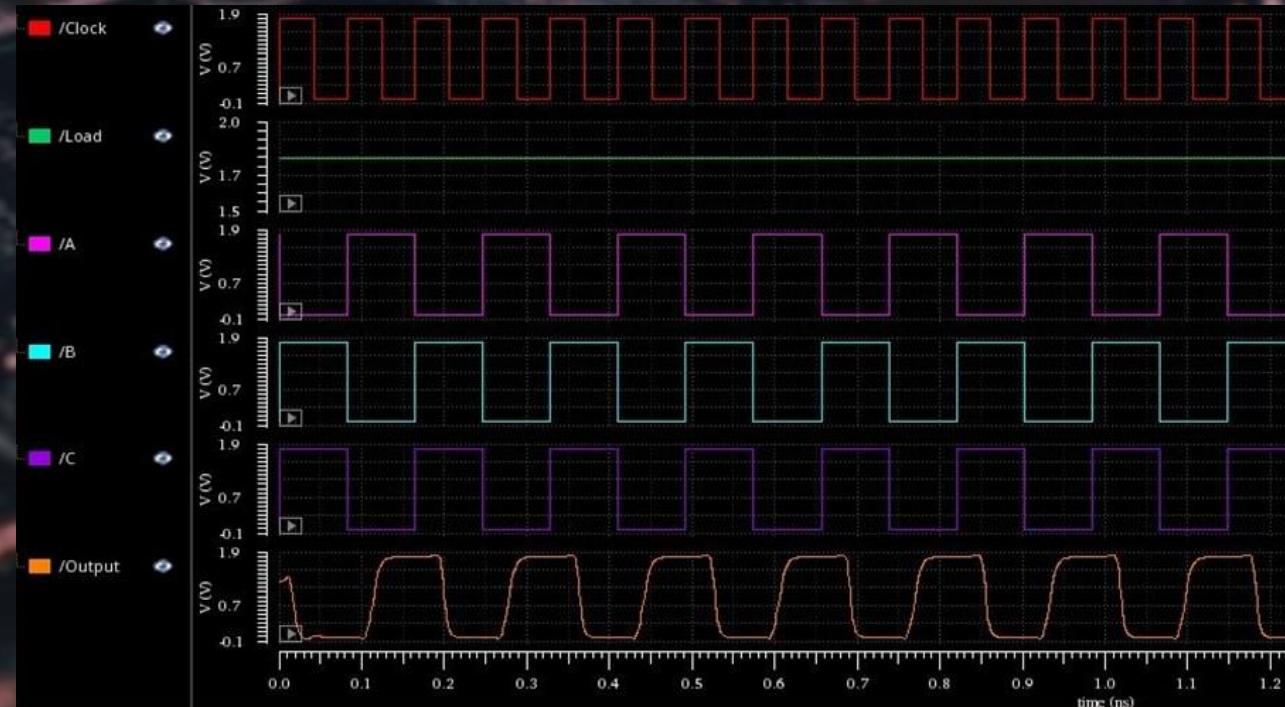
States	A	B	C	AB + C
state0	0	0	0	0
state1	0	0	1	1
state2	0	1	0	0
state3	0	1	1	1
state4	1	0	0	0
state5	1	0	1	1
state6	1	1	0	1
state7	1	1	1	1

State Transition Graph

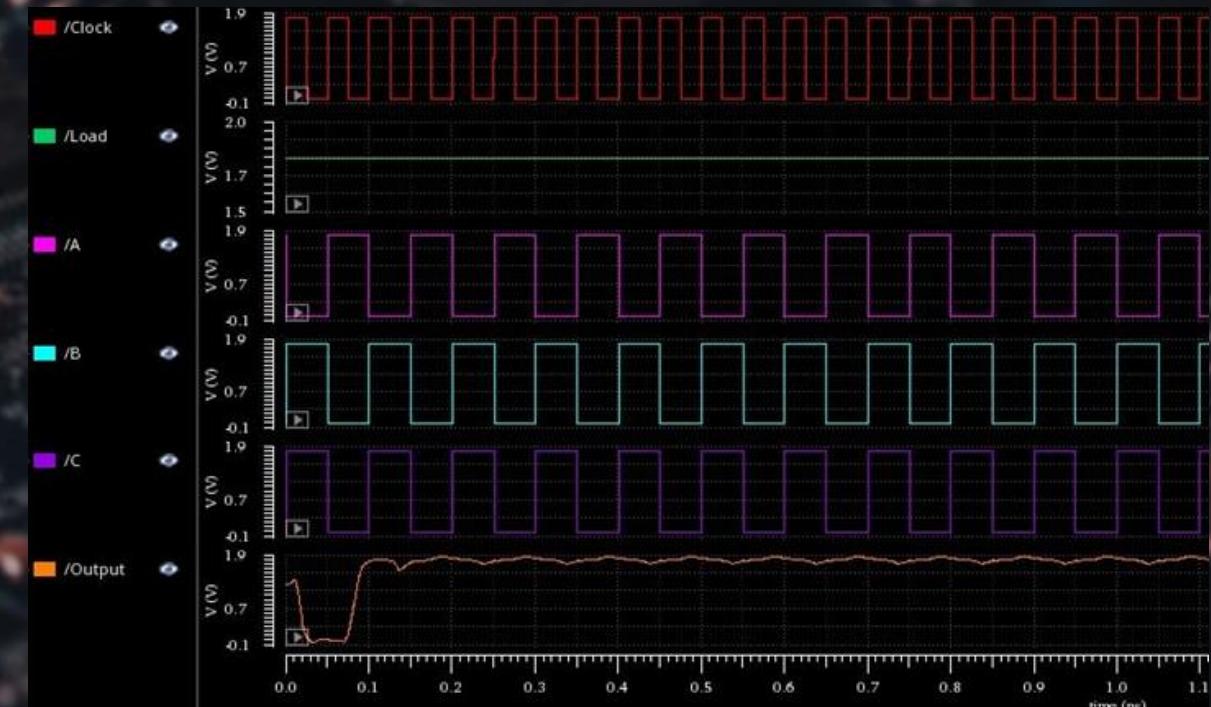


CLB circuit combinatorial delay data

State transition	Rise Time (ps)	Fall Time (ps)
0 to 1	35.74	41.08
0 to 3	41.32	37.83
0 to 5	37.77	40.77
0 to 6	42.61	23.33
0 to 7	40.52	41.49
2 to 1	33.69	41.39
2 to 3	40.83	44.28
2 to 5	18.49	41.44
2 to 6	18.33	23.73
2 to 7	18.47	44.34
4 to 1	36.08	50.11
4 to 3	42.19	51.25
4 to 5	39.32	46.3
4 to 6	44.33	43.15
4 to 7	41.93	47.46



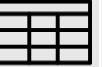
Output barely follows input with 82ps period (optimal) in sequential mode



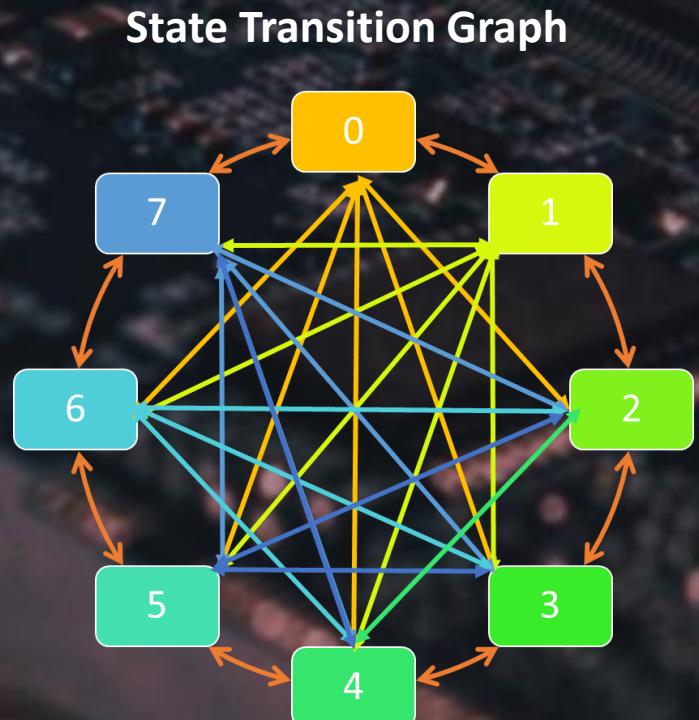
Output failure at 50ps period in sequential mode for worst input condition (state4 to state3 in table-2)

# Circuit Performance

## SUMMARY

Design Metric	CLB test circuit	Raw logic implementation
Worst Case Delay (ps)	51.25	8.055
Maximum Frequency (GHz)	12.195 (Optimal) 15.385 (Critical)	33.333 (Critical)
Active Energy (J/transition)	$12.011 \times 10^{-15}$	 $2.223 \times 10^{-15}$
Leakage Energy (J/transition)	$5.429 \times 10^{-15}$	 $19.592 \times 10^{-21}$
Loading Energy (J/transition)	$278.3 \times 10^{-21}$	
Average Energy (J/transition)	$6.006 \times 10^{-15}$	
Layout Area ( $m^2$ )	$67.85 \times 10^{-12}$	
Figure of Merit ( $Jsm^2$ )	<b><math>3.34 \times 10^{-35}</math></b>	

# Circuit Analysis



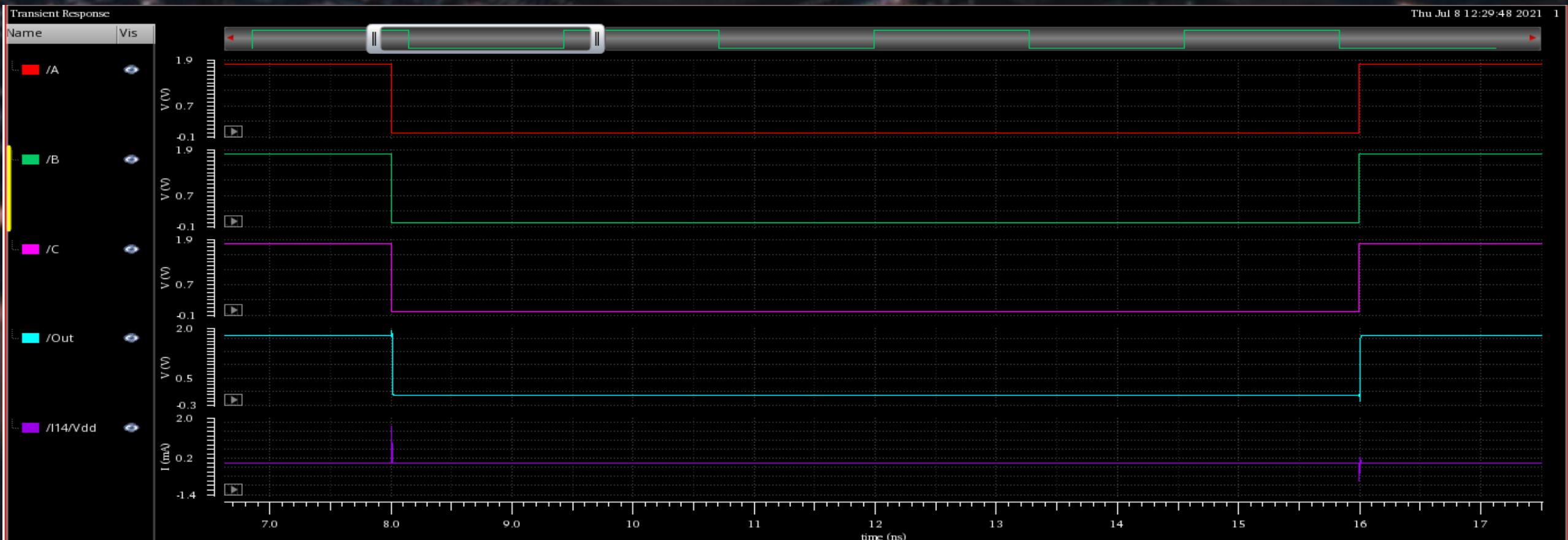
Switching energy for all state transitions (CLB)

State (A to B)	Switching energy A to B, fJ	Switching energy B to A, fJ	State (A to B)	Switching energy A to B, fJ	Switching energy B to A, fJ
0 to 1	17.2	16.7	2 to 4	3.65	11.01
0 to 2	4.48	2.93	2 to 5	18.47	18.43
0 to 3	19.63	19.17	2 to 6	8.925	12.92
0 to 4	2.1	2.81	2 to 7	17.04	17.8
0 to 5	18.59	17.84	3 to 4	21.25	20.13
0 to 6	13.26	13.28	3 to 5	6.079	3.796
0 to 7	20.39	19.06	3 to 6	10.21	10.03
1 to 2	17.28	17.69	3 to 7	2.878	1.97
1 to 3	4.121	4.953	4 to 5	17.78	17.26
1 to 4	19.26	18.72	4 to 6	12.4	12.59
1 to 5	3.239	2.159	4 to 7	21.24	18.37
1 to 6	11.3	12.5	5 to 6	8.354	11.89
1 to 7	5.876	5.44	5 to 7	3.856	4.517
2 to 3	15.39	16	6 to 7	9.93	8.507

# Circuit Analysis

$$\text{Switching Energy} = \frac{1}{\text{Total State Transitions}} \sum_{\text{State transition}} \int_{t \text{ start}}^{t \text{ end}} i(vdd) * 1.8 dt$$

Switching Current



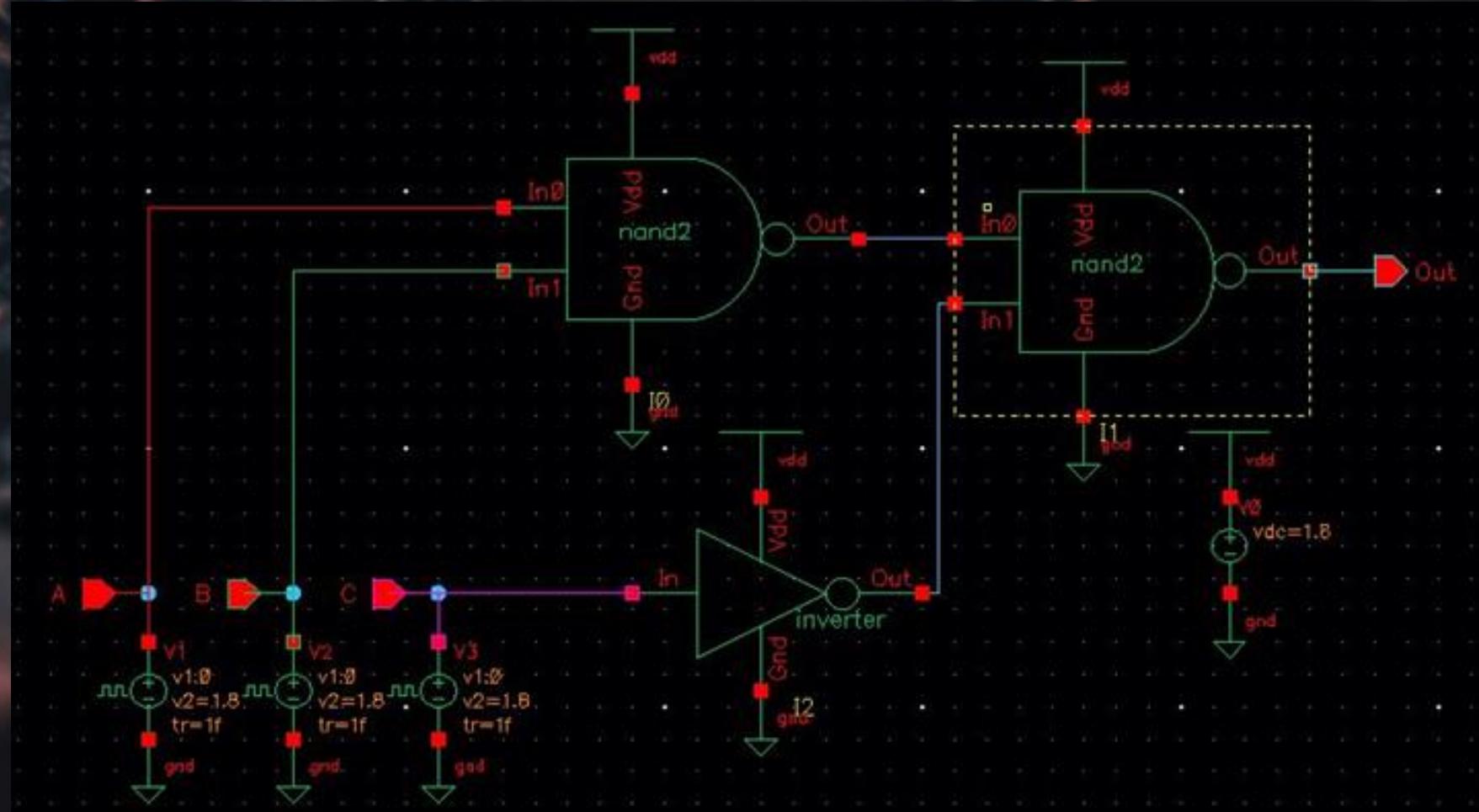
# Circuit Analysis

$$\text{Leakage Energy} = \frac{1}{\text{Total States} * 2} \sum_{\text{State}} \int_0^{2 * \text{critical period}} i(vdd) * 1.8 dt$$

Leakage Energy

State	Leakage Energy for two cycles in CLB circuit ( $\times 10^{-15}$ J)	Leakage Energy for two cycles in raw logic circuit ( $\times 10^{-21}$ J)
0	9.472	52.05
1	11.69	52.59
2	9.47	33.21
3	11.69	33.75
4	9.47	50.9
5	11.69	51.44
6	11.69	15.95
7	11.69	23.58
SUM	86.862	313.47

# Raw Logic Implementation



Function

$$F = AB + C$$

# Conclusion

- CLB fully implemented in **45nm** CMOS technology.
- Parallel loading of 8bit SRAM, combinatorial and sequential mode of operation.
- FOM  $3.34 \times 10^{-35}$  achieved with frequency of **12.195 GHz**, average energy  $6.006 \times 10^{-15}$  J & area of **67.85  $\mu\text{m}^2$** .

## Limitations & Future Prospects:

- CLB array performance not observed.
- Advanced CLB features (Adder/ Multiplier) not implemented.
- LUT programming peripherals not included.

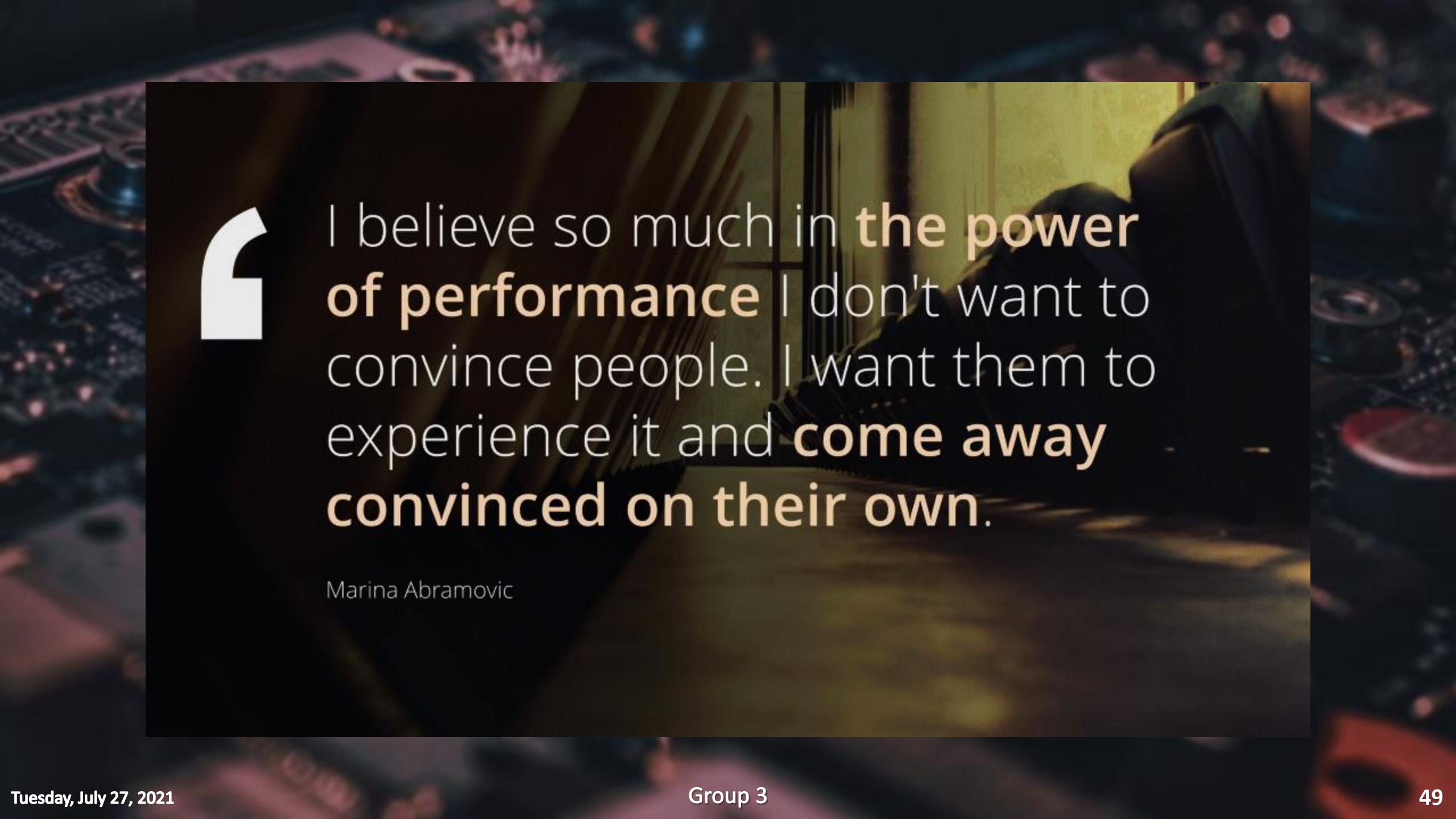
# Software Used

- Cadence Virtuoso
- Proteus

# References

- [1] ALTERA Cyclone II Device Family Data Sheet
- [2] O. Thomas, M. Vinet, O. Rozeau, P. Batude and A. Valentian, "Compact 6T SRAM cell with robust read/write stabilizing design in 45nm Monolithic 3D IC technology," *2009 IEEE International Conference on IC Design and Technology*, 2009, pp. 195-198, doi: 10.1109/ICICDT.2009.5166294.
- [3] Pant, Diwaker & Pandey, Ankita & Mehra, Dr. Rajesh. (2012). CMOS Design of 2:1 Multiplexer Using Complementary Pass Transistor Logic.
- [4] Fundamentals of Digital Logic with Verilog Design by Stephen Brown and Zvonko Vranesic

Video Demonstration: [EEE 454 Project Group 3 Demonstration](#)

A blurred background image showing a person in a dark room. The person is wearing a dark jacket and has their hands clasped in front of them. The room is filled with colorful, out-of-focus lights, possibly from stage equipment or stage lighting.

“

I believe so much in **the power of performance** I don't want to convince people. I want them to experience it and **come away convinced on their own.**

Marina Abramovic