MILITARY INSTITUTE OF SCIENCE & TECHNOLOGY

Department of Electrical Electronic and Communication Engineering

Subject: VLSI II Laboratory (**EECE – 457)**

PROJECT REPORT

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Course Code	**EECE – 457**
Batch	EECE-20
Section	A
Date of submission	August 10, 2025

MIST | Technology for Advancement
Military Institute of Science and Technology

Project Title: Design, Layout, and Performance Analysis of a Configurable Logic Block (CLB) Using 90nm Technology

Introduction:

Field-Programmable Gate Arrays (FPGAs) rely on Configurable Logic Blocks (CLBs) as their primary reconfigurable logic elements. A CLB integrates a Look-Up Table (LUT), multiplexers, SRAM cells, and sequential elements such as flip-flops to implement custom logic functions. This work presents the complete design, schematic verification, layout, and performance evaluation of a 3:1 CLB implemented in 90nm CMOS technology using Cadence Virtuoso. The selected function for implementation is **A + BC**, realized through an 8-bit LUT with SRAM-based configuration storage. Key design metrics including worst-case delay, critical frequency, area, and average energy consumption were obtained through post-layout simulations. The proposed design achieves functional correctness in both combinational and sequential modes, adhering to design verification rules (DRC/LVS) and optimizing the Figure of Merit (FOM) for performance and efficiency.

Schematic, Layouts and Test Outputs:

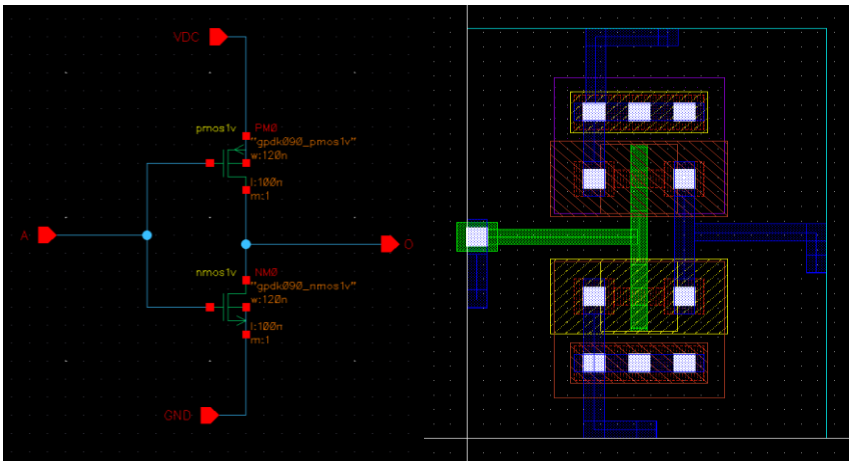

Figure 1: Inverter Schematic and Layout

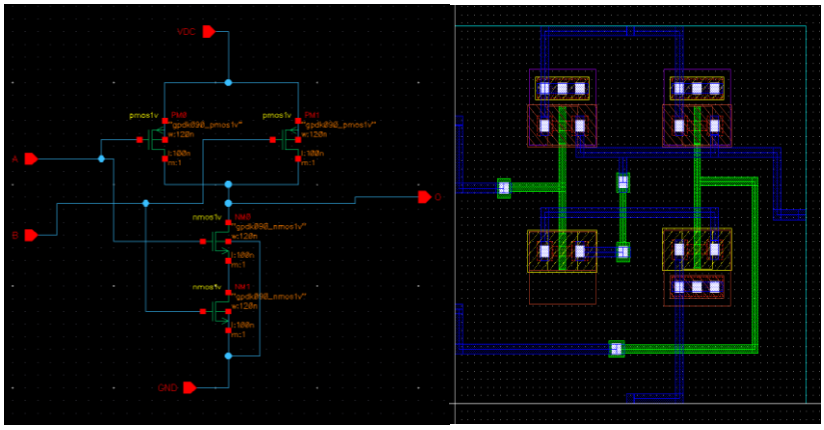

Figure 2: 2 input NAND Schematic and Layout

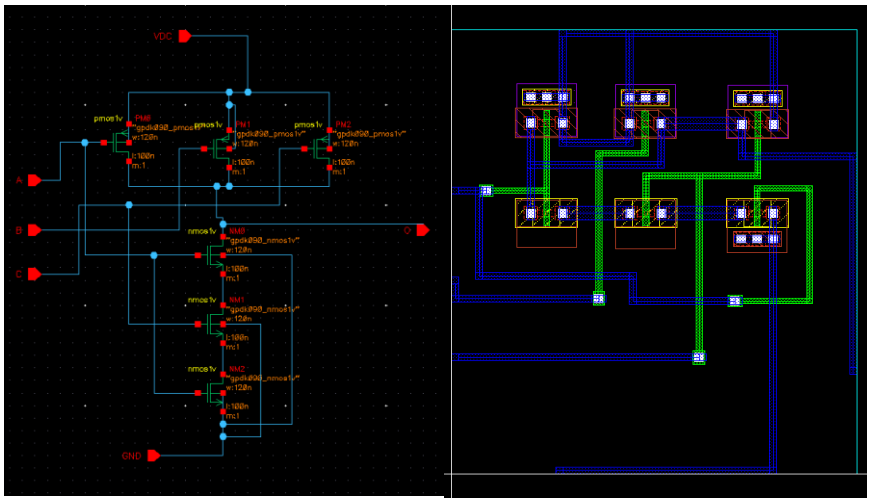

Figure 3: 3 Input NAND Schematic and Layout

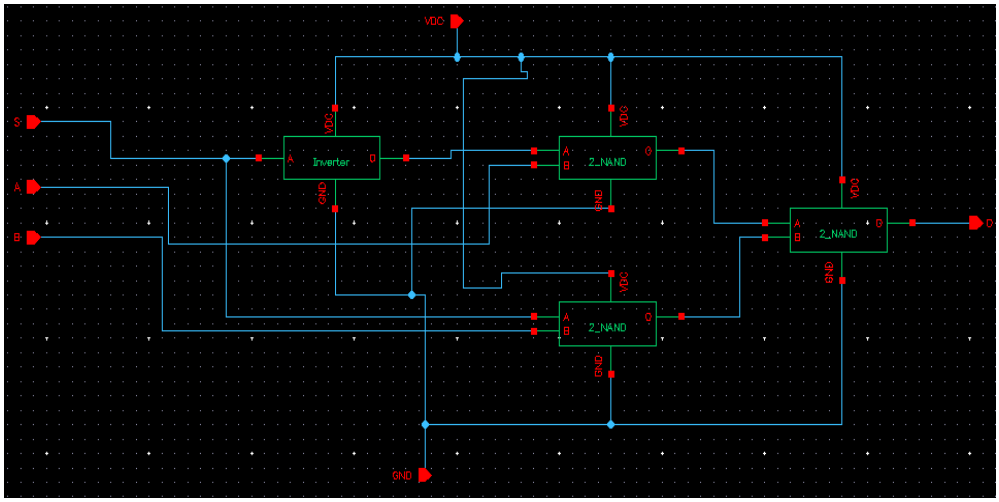

Figure 4: 2x1 MUX Schematic

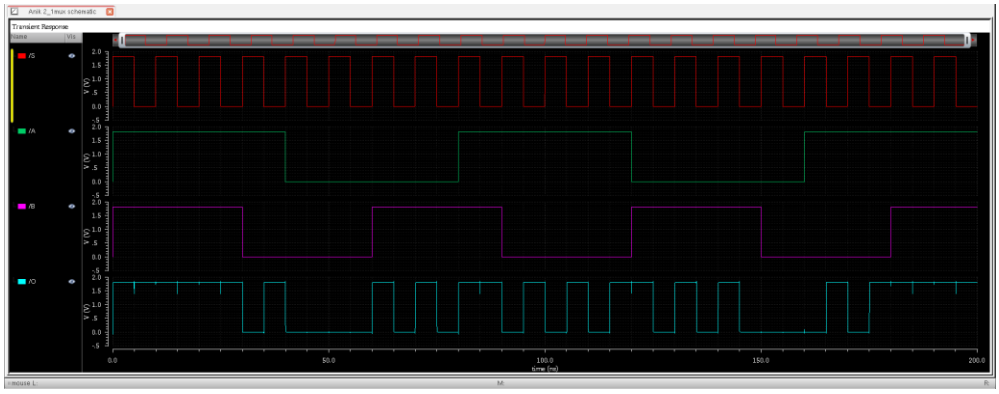

Figure 5: 2x1 MUX Output curve check

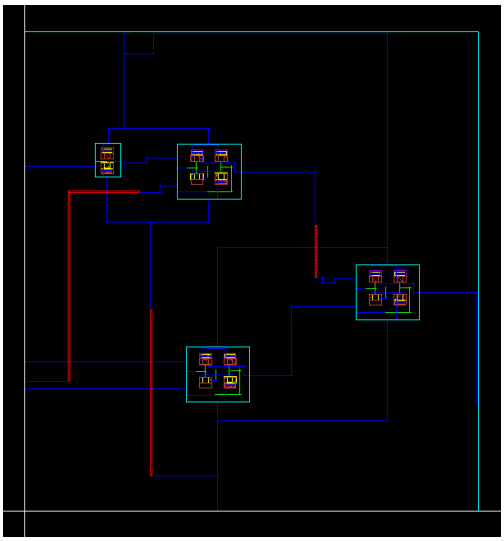

Figure 6: 2x1 Mux Layout

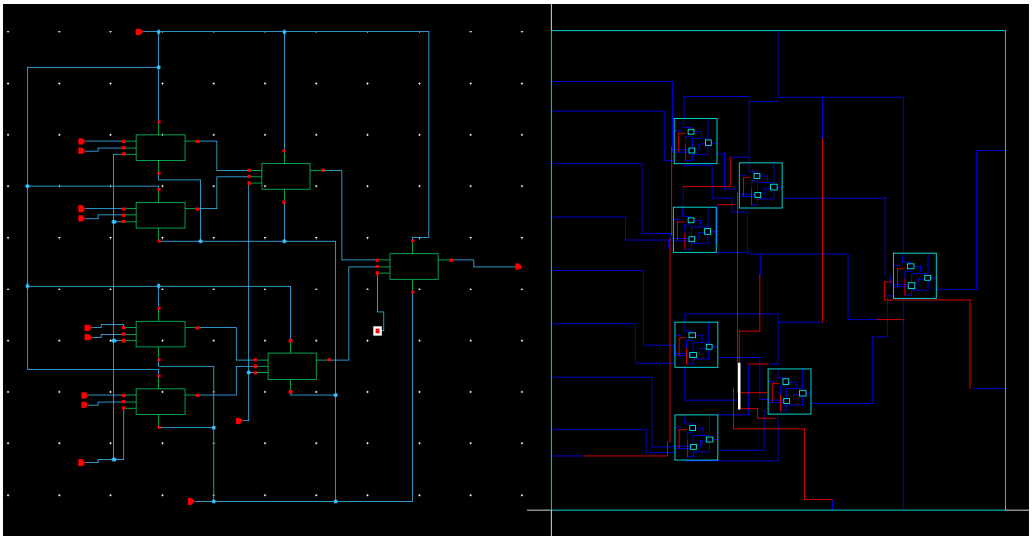

Figure 7: 8x1 MUX Schematic and Layout

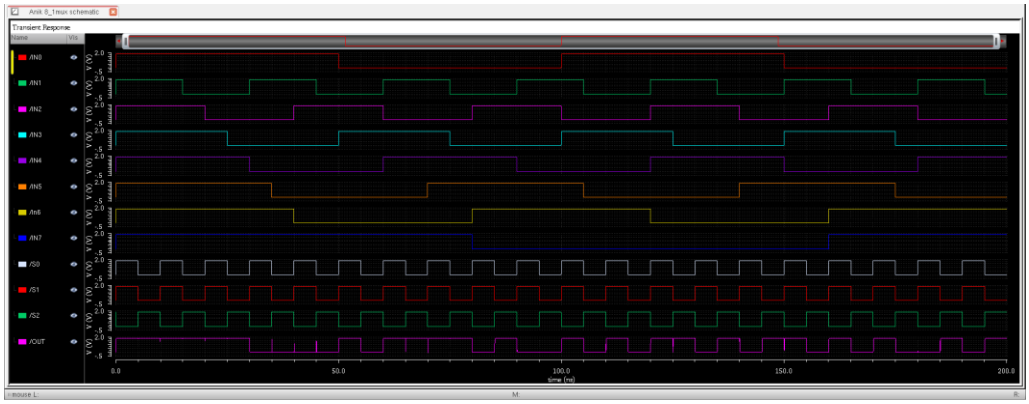

Figure 8: 8x1 MUX Output

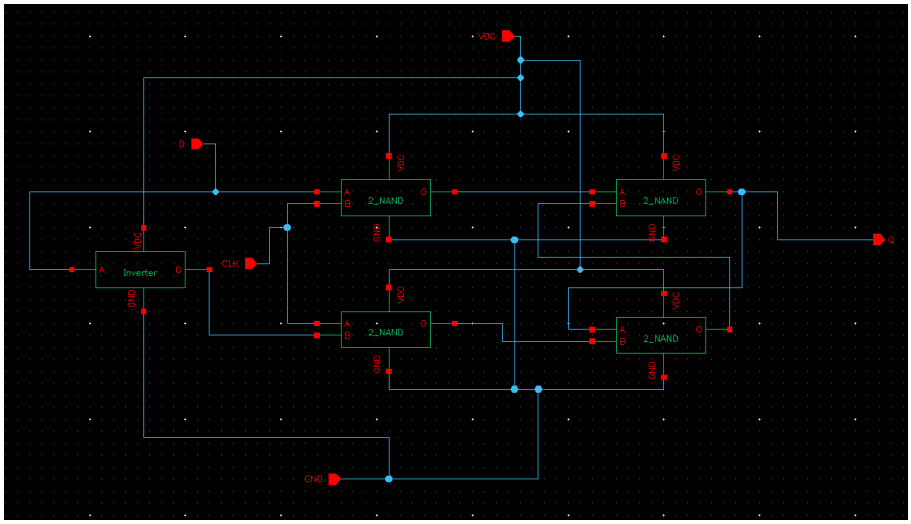

Figure 9:D Flipflop Schematic

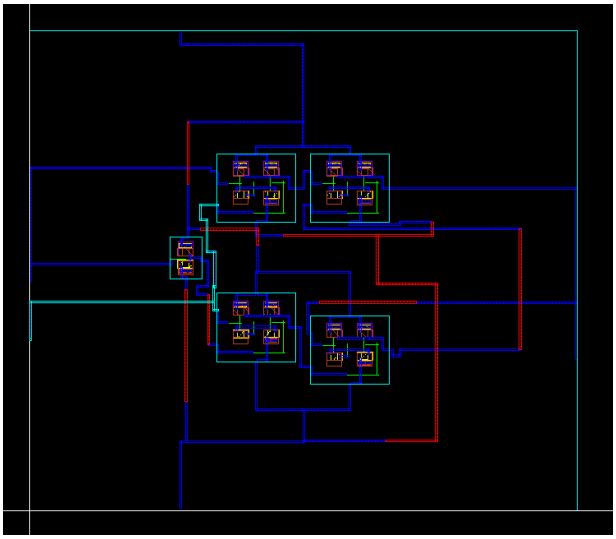

Figure 10: D Flipflop Layout

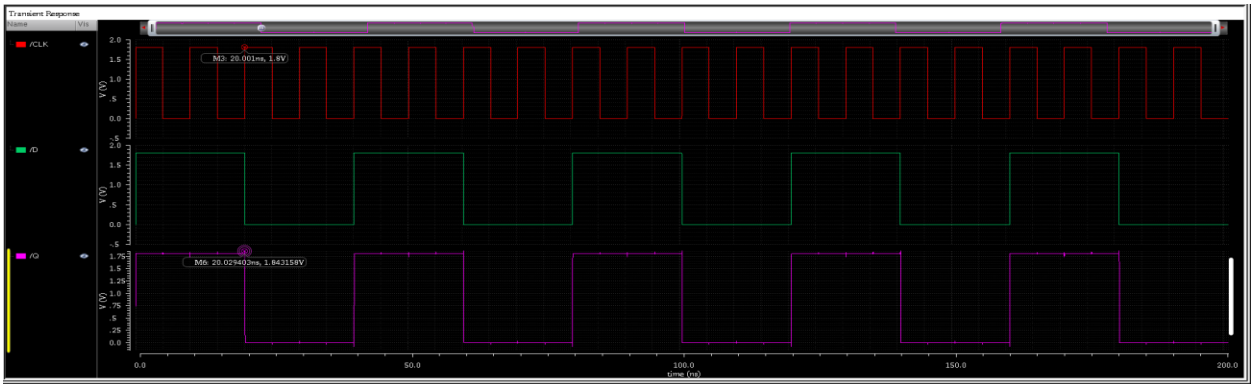

Figure 11: D Flipflop Output

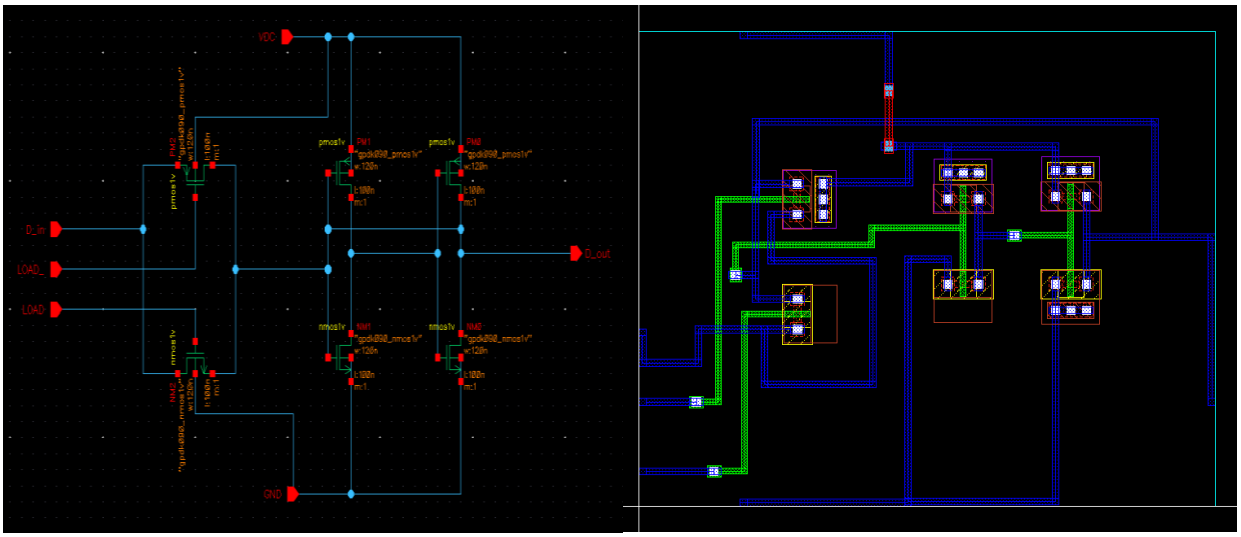

Figure 12: SRAM CELL Schematic and Layout

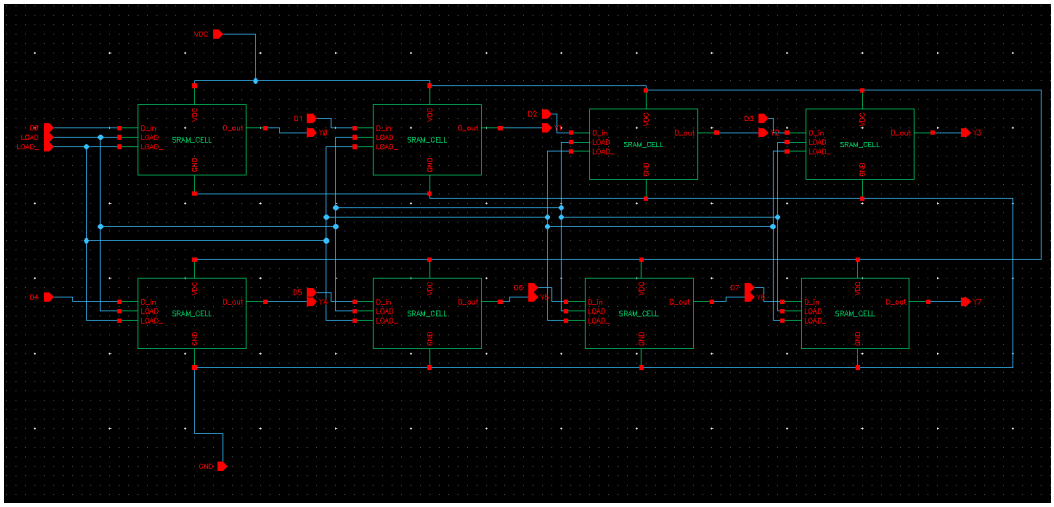

Figure 13: 8-bit SRAM Schematic

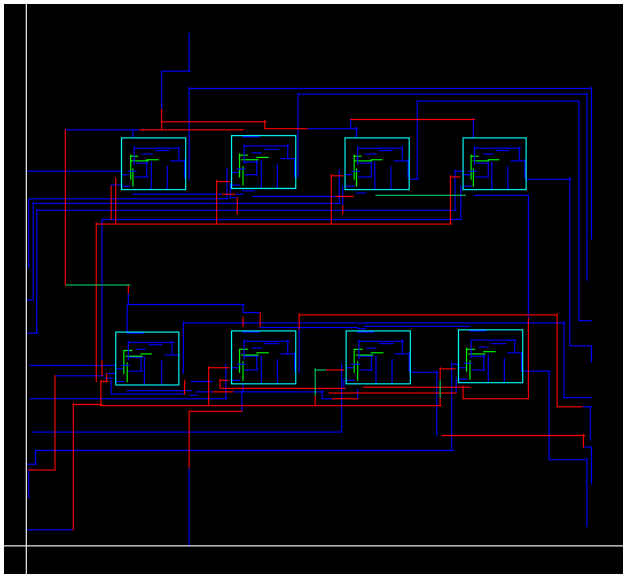

Figure 14: 8-bit SRAM Layout

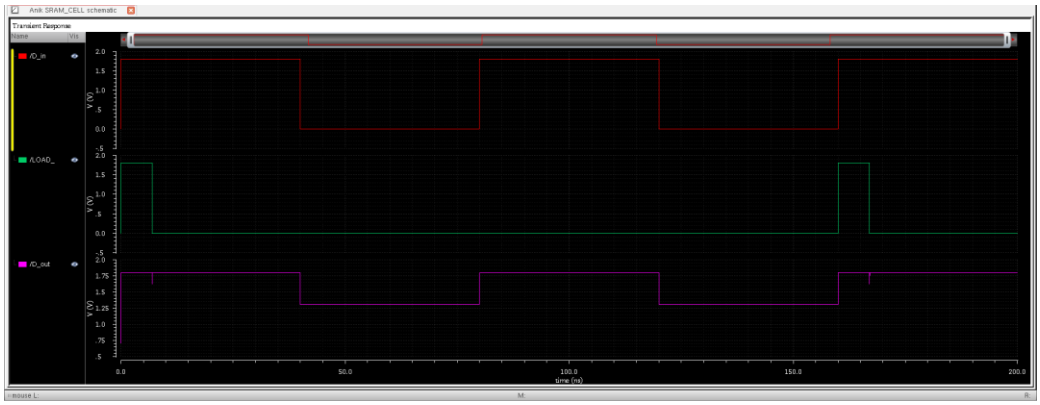

Figure 15: SRAM CELL Output

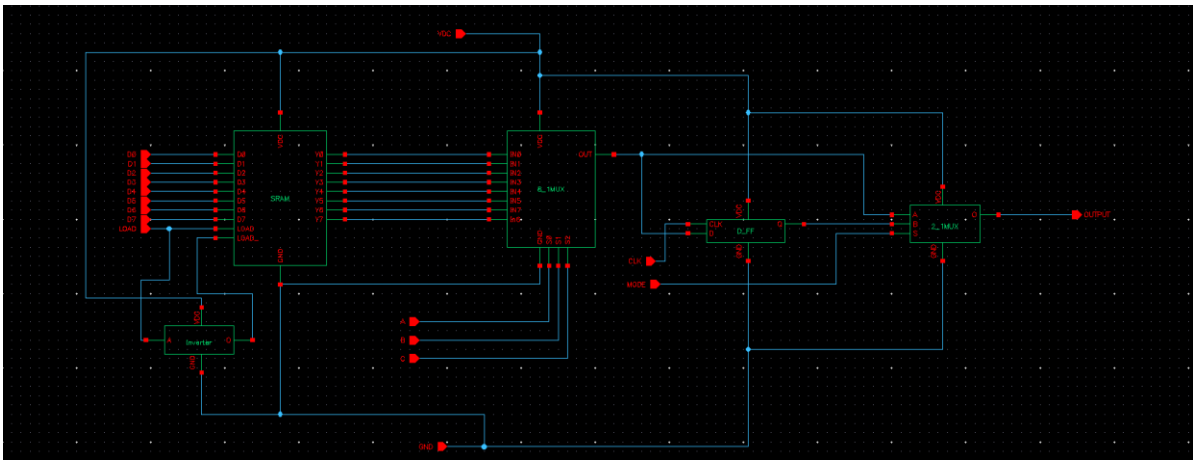

Figure 16: CLB Schematic

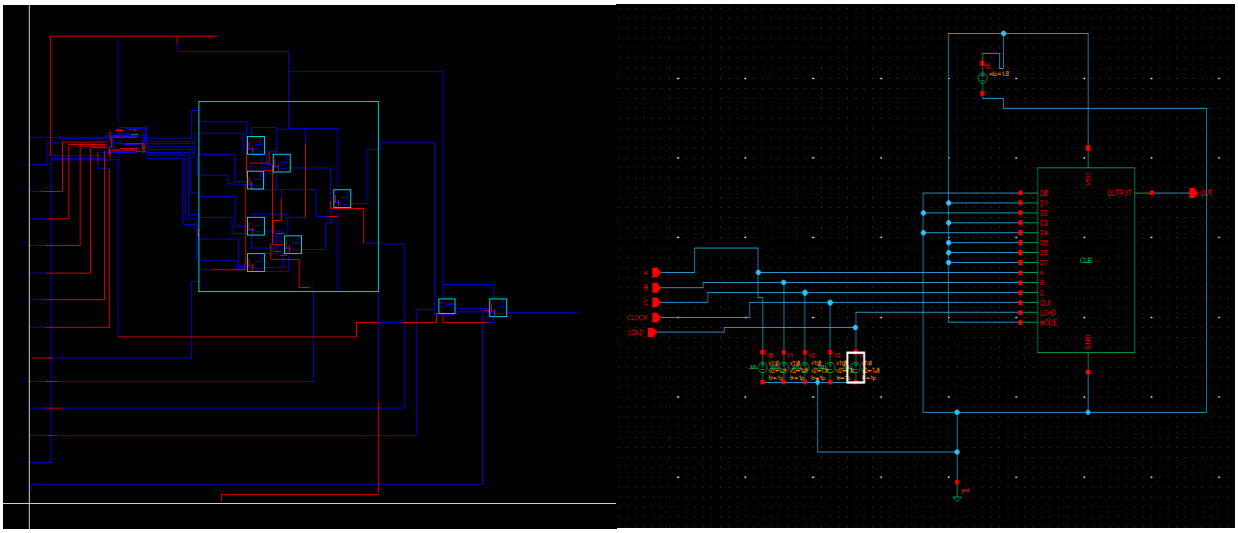

Figure 17: CLB Layout and CLB Testing Circuit

States	C	B	A	A + BC
state0	0	0	0	0
state1	0	0	1	1
state2	0	1	0	0
state3	0	1	1	1
state4	1	0	0	0
state5	1	0	1	1
state6	1	1	0	1
state7	1	1	1	1

Table 1: Truth Table For A+BC (which has been taken as the function for CLB)

Figure 18: Functionality Test (CLB) [Combinational](For MODE=0)

Figure 19: Functionality Test (CLB) [Sequential] (For MODE=1)

For Both Case Sequential and Combinational my output curve is similar due to there is no set reset pin in my d flipflop which does not create additional delay in sequential output as per reference.

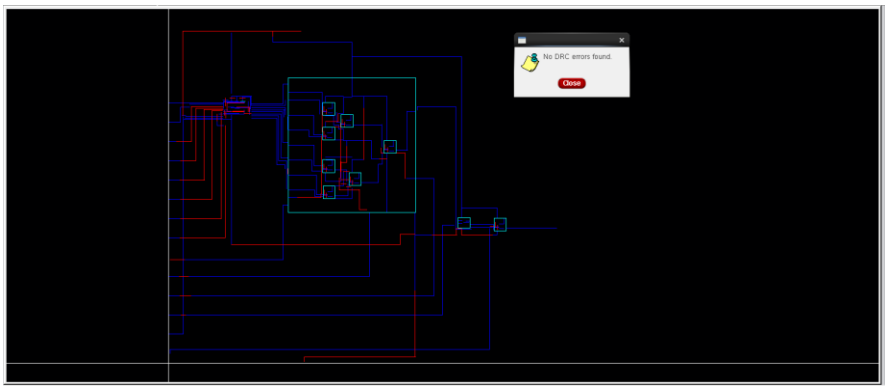

Figure 20: Final CLB Layout DRC check

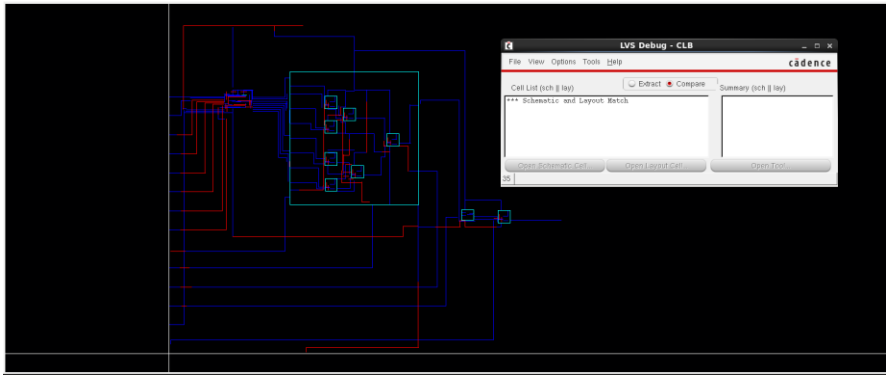

Figure 21: Final CLB Layout LVS check

According to Figure 20 and 21 it is clear that CLB layout is verified by DRC and LVS check rule.

Design Metrics:

Delay Calculation:

1.Clock to Q delay:

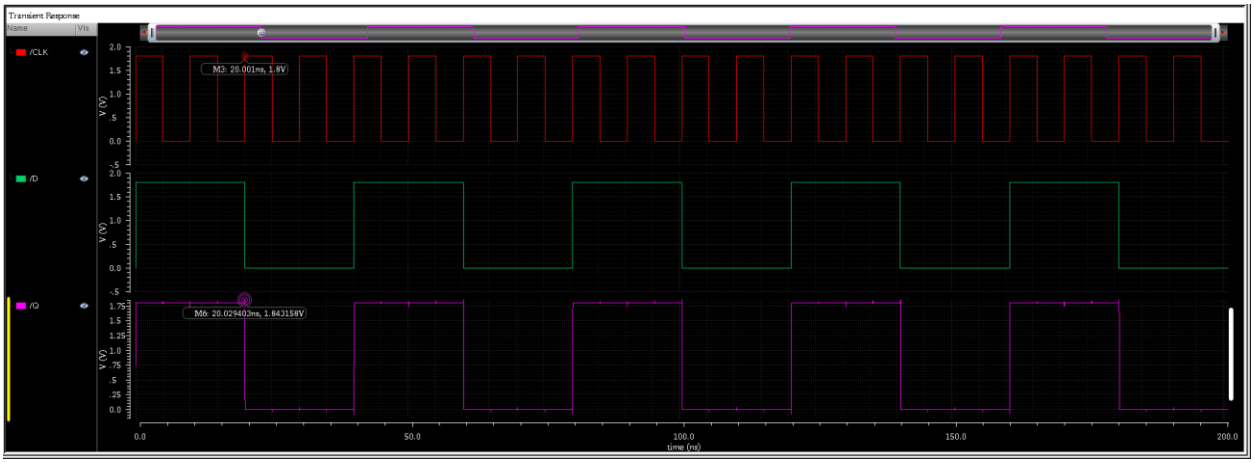

Figure 22: Clock to Q Delay

Clock-to-Q delay, in a flipflop, is the time it takes for the output (Q) to change to its new state after the active edge of the clock signal. From, Fig. 22 the Q changes at **28.403ps** after the active clock edge.

2. Worst Case Delay Finding and calculation:

We were required to determine the state delay for each combination in which the output changes concurrently with a change in the input. Accordingly, the state diagram is constructed based on the custom-designed truth table.

States	C	B	A	A + BC
state0	0	0	0	0
state1	0	0	1	1
state2	0	1	0	0
state3	0	1	1	1
state4	1	0	0	0
state5	1	0	1	1
state6	1	1	0	1
state7	1	1	1	1

Subsequently, we designed circuits that transition between states and calculated the rise time and fall time delays by subtracting the lower-level time from the upper-level time. For this measurement, we considered only the first cycle in which the output changes with respect to the input. This approach was adopted to avoid the cumulative delay that occurs in subsequent cycles,

which would make it difficult to determine the exact rise and fall delays. As a result, we obtained the following table, from which it was observed that the worst-case delay occurs during the state transition from State 2 to State 3.

Rise and Fall time delay when transition between certain states:

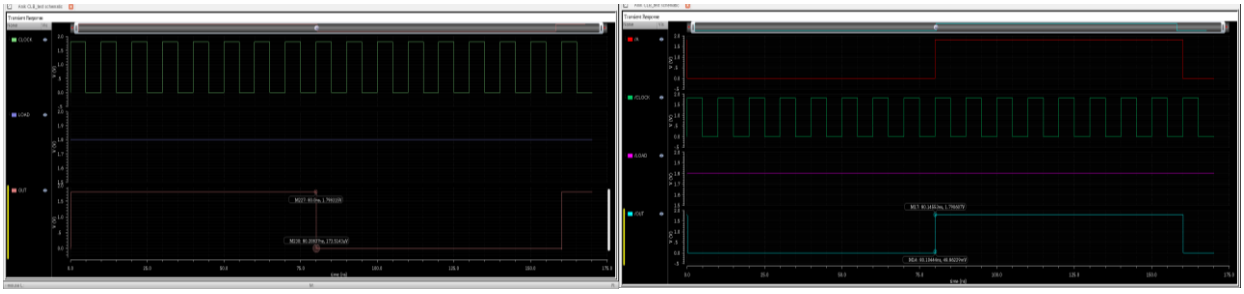

Figure 23: FALL AND RISE TIME DELAY FOR STATE TRANSITION 0 TO 1

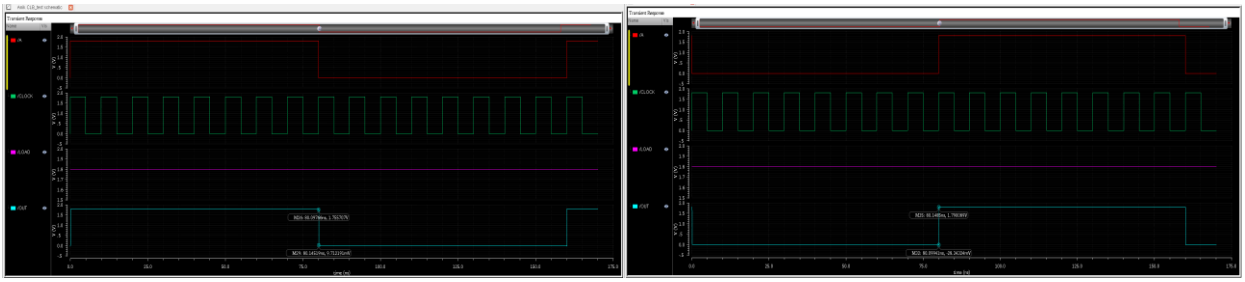

Figure 24: FALL AND RISE TIME DELAY FOR STATE TRANSITION 0 TO 3

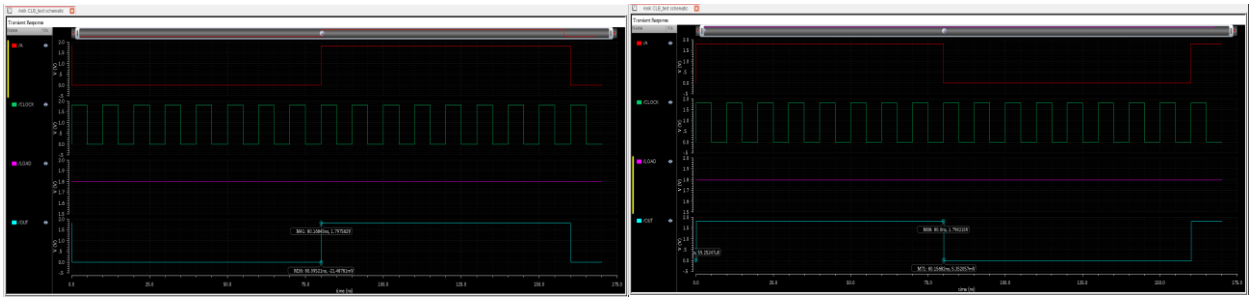

Figure 24: RISE AND FALL TIME DELAY FOR STATE TRANSITION 0 TO 5

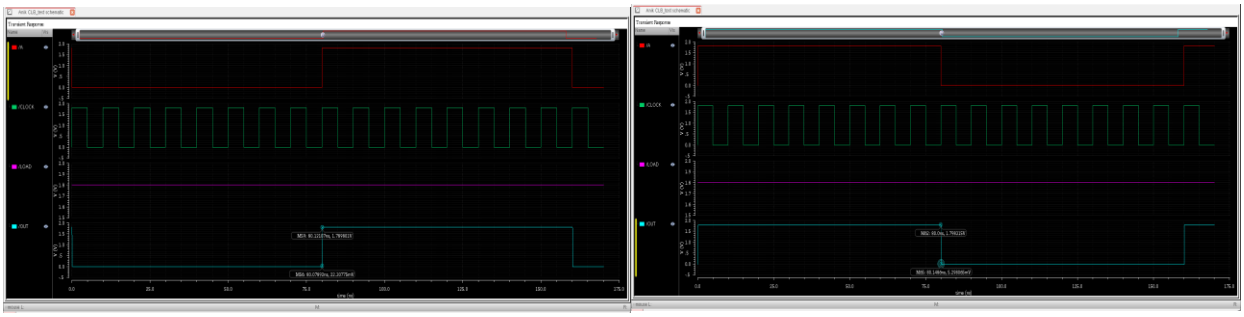

Figure 25: RISE AND FALL TIME DELAY FOR STATE TRANSITION 0 TO 7

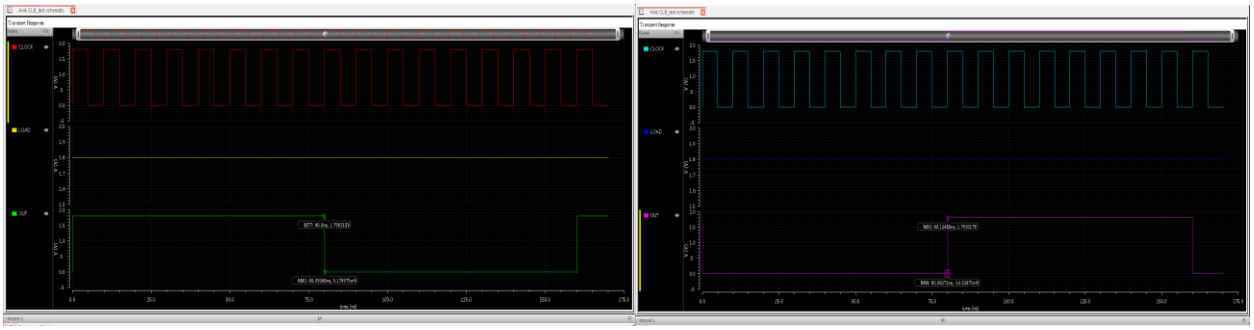

Figure 26: FALL AND RISE TIME DELAY FOR STATE TRANSITION 0 TO 6

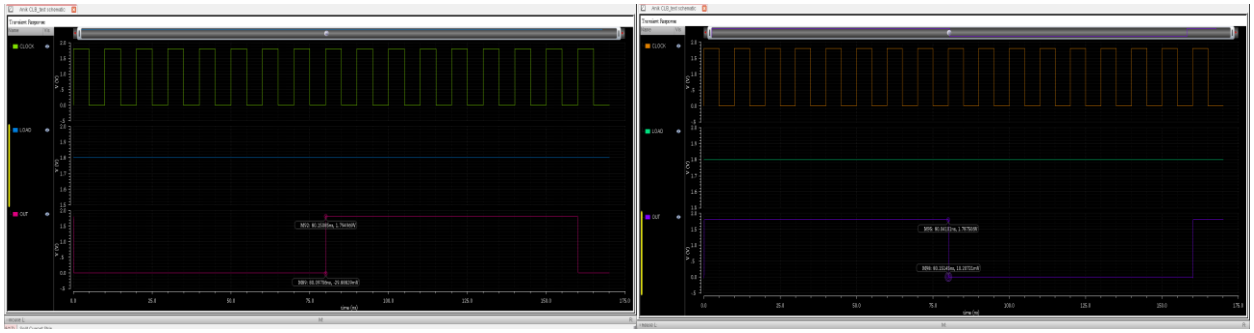

Figure 28: RISE AND FALL TIME DELAY FOR STATE TRANSITION 2 TO 1

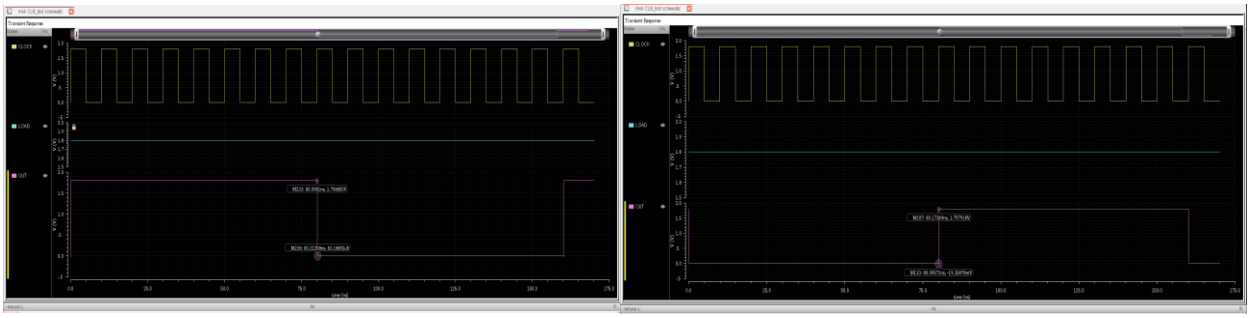

Figure 29: FALL AND RISE TIME DELAY FOR STATE TRANSITION 2 TO 3

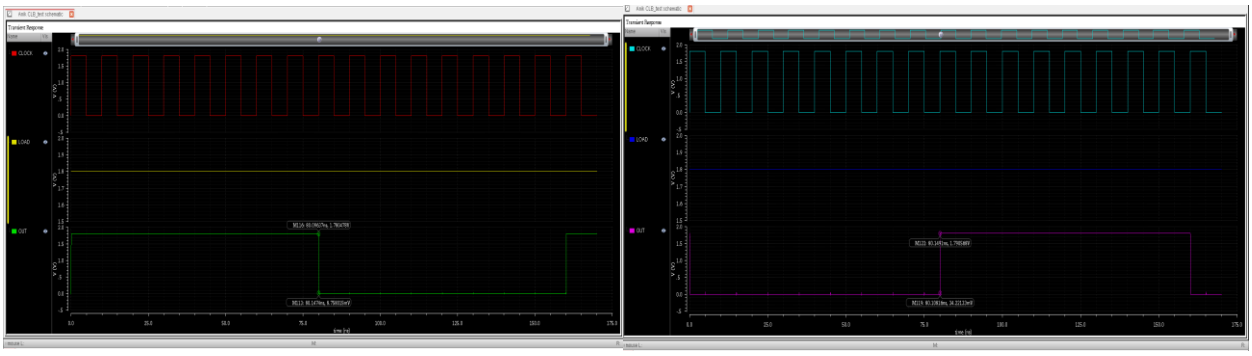

Figure 30: FALL AND RISE TIME DELAY FOR STATE TRANSITION 2 TO 5

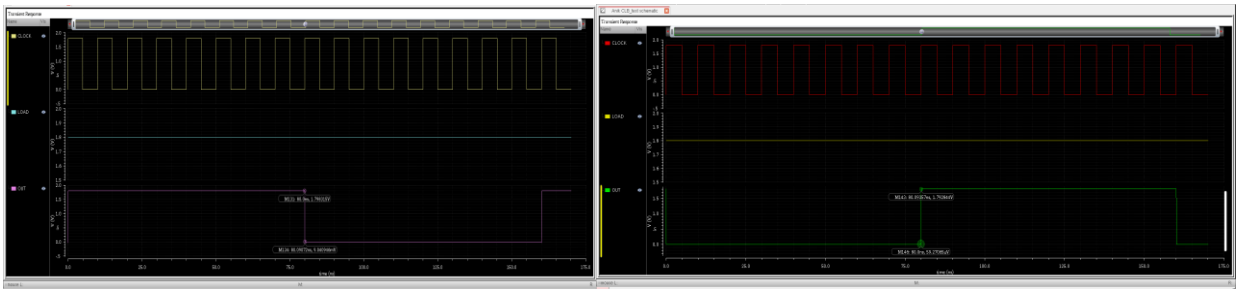

Figure 31: FALL AND RISE TIME DELAY FOR STATE TRANSITION 2 TO 6

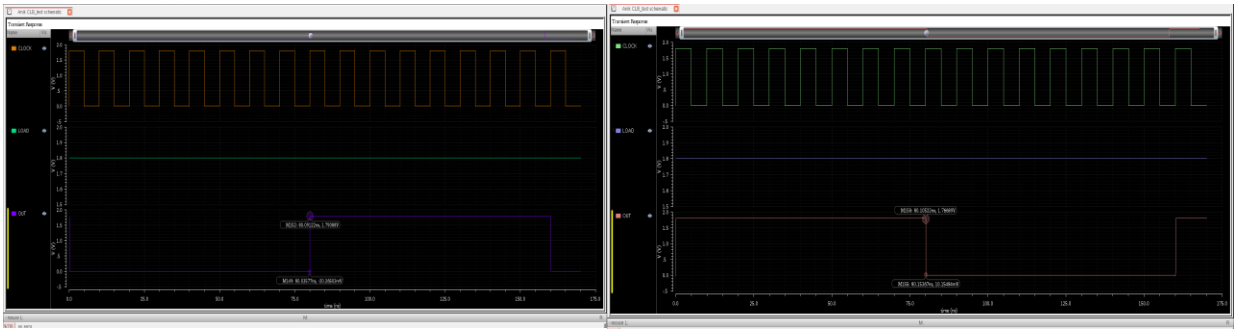

Figure 32: RISE AND FALL TIME DELAY FOR STATE TRANSITION 2 TO 7

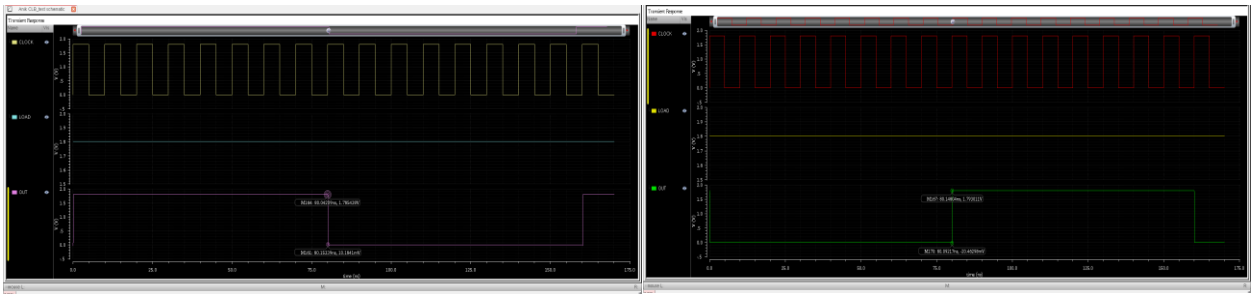

Figure 33: FALL AND RISE TIME DELAY FOR STATE TRANSITION 4 TO 1

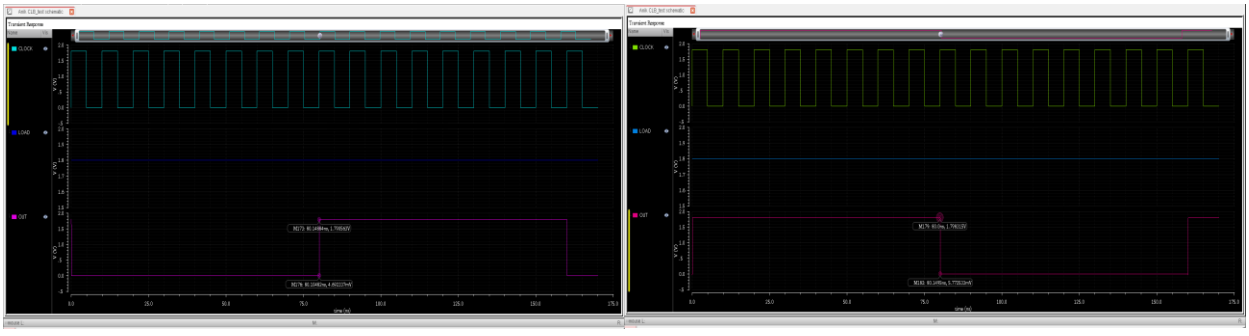

Figure 34: RISE AND FALL TIME DELAY FOR STATE TRANSITION 4 TO 3

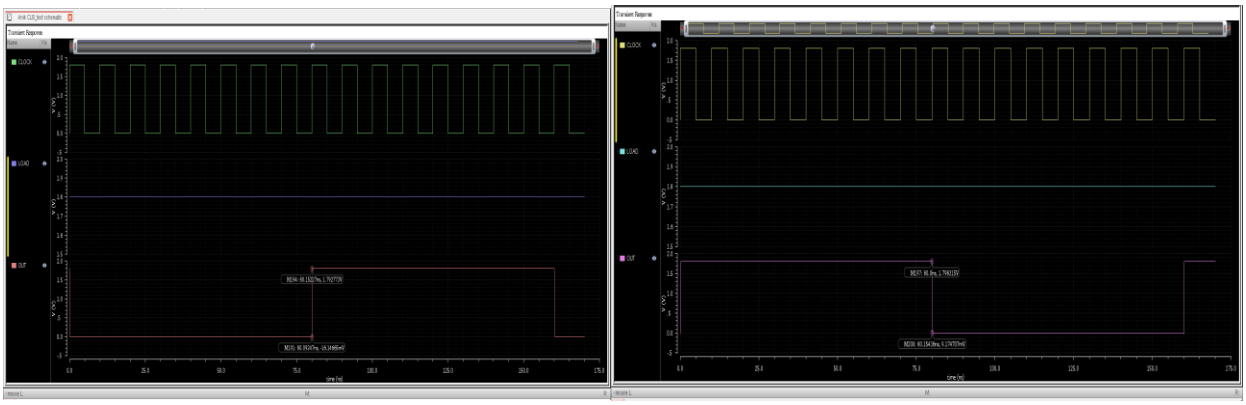

Figure 35: RISE AND FALL TIME DELAY FOR STATE TRANSITION 4 TO 5

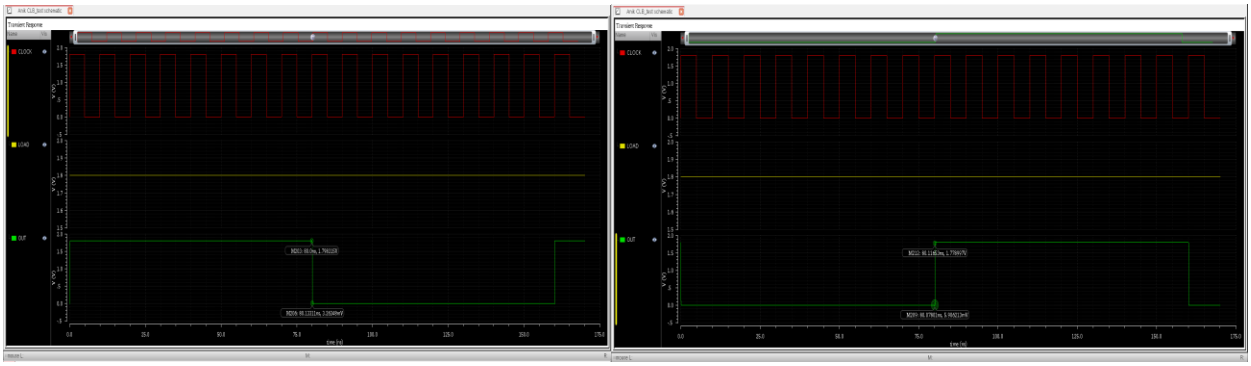

Figure 36: FALL AND RISE TIME DELAY FOR STATE TRANSITION 4 TO 6

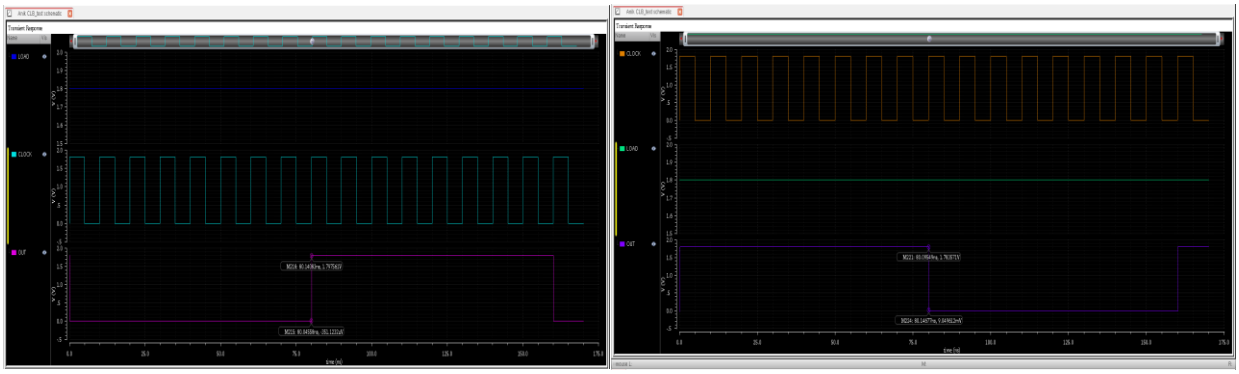

Figure 37: RISE AND FALL TIME DELAY FOR STATE TRANSITION 4 TO 7

Analyzing all the rise and fall time delays it is to be seen that the worst-case delay is about 214.46ps in State 2 to State 3 transition.

State transition	Rise Time(ps)	Fall Time(ps)
0 to 1	41.09	208.37
0 to 3	49.09	47.53
0 to 5	73.24	156.82
0 to 6	60.94	90.65
0 to 7	42.15	148.6
2 to 1	53.85	110.44
2 to 3	77.78	214.46
2 to 5	40.94	51.03
2 to 6	93.57	90.72
2 to 7	55.45	48.45
4 to 1	55.87	111.3
4 to 3	44.02	149.5
4 to 5	59.8	154.36
4 to 6	38.52	133.11
4 to 7	95.25	51.28

Table 2: RISE AND FALL TIME FOR WORST CASE DELAY IN STATE TRANSITION

There for we get,

Minimum clock period = Total combinatorial delay + Clock to Q delay + Setup time

= (214.46 + 28.403 + 0)

= 242.863ps

≈243 ps

Critical Frequency:

The *critical frequency* is the highest clock frequency at which a sequential circuit can operate correctly, determined by the minimum clock period that still produces an accurate output. If the frequency exceeds this limit, timing errors and output distortion occur.

Determination of Critical Frequency for the CLB (Sequential Mode):
Simulations were performed with clock periods ranging from 243ps down to 93ps. In this range, the output barely followed the input.

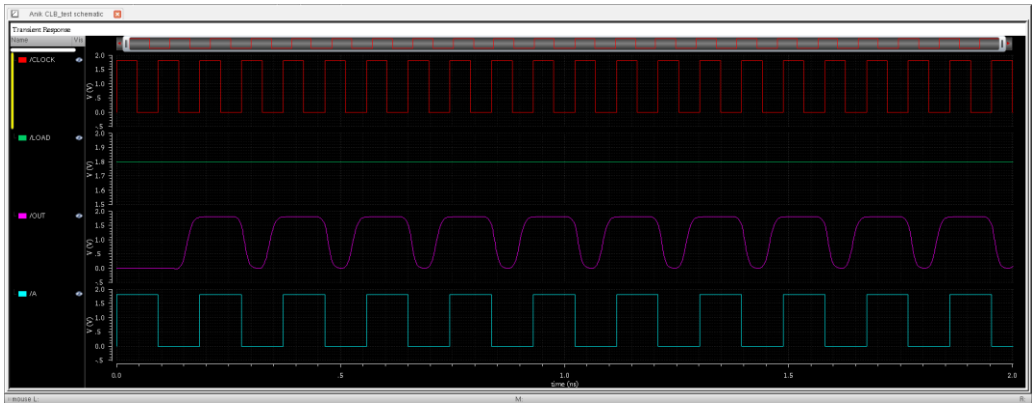

Figure 38: Clock periods ranging from 243ps down to 93ps. In this range, the output barely followed the input.

When the clock period was set to 93ps, the output became distorted, indicating the circuit had reached its operational limit. After multiple simulations, 93ps was identified as the minimum clock period.

giving a critical frequency of:

$$f_{critical} = \frac{1}{93\ \text{ps}} \approx 10.75\ \text{GHz}$$

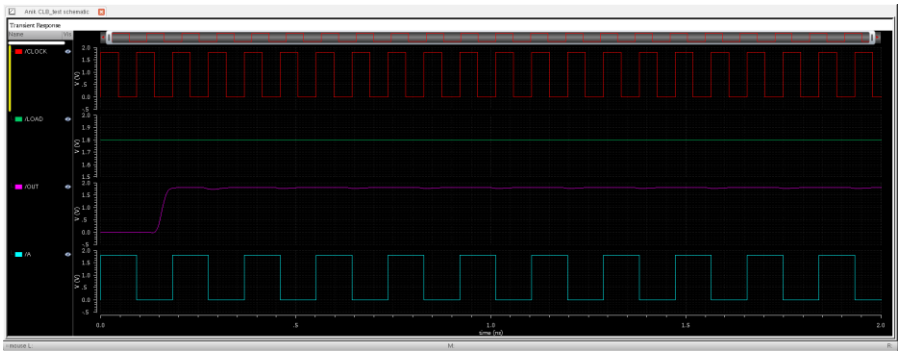

Figure 39: When the clock period was set to 93ps, the output became distorted

Area Calculation:

To determine this, we use SKILL IDE and measured the CLB layout in m^2. After creating the .il file we open the CIW window to load that file and call the function. But before all this we must run the layout so that CIW can fetch it from the cache memory. The code and the outputs are given below. The area of the CLB layout is **$1.33418 \times 10^{-6}\ m^2$.**

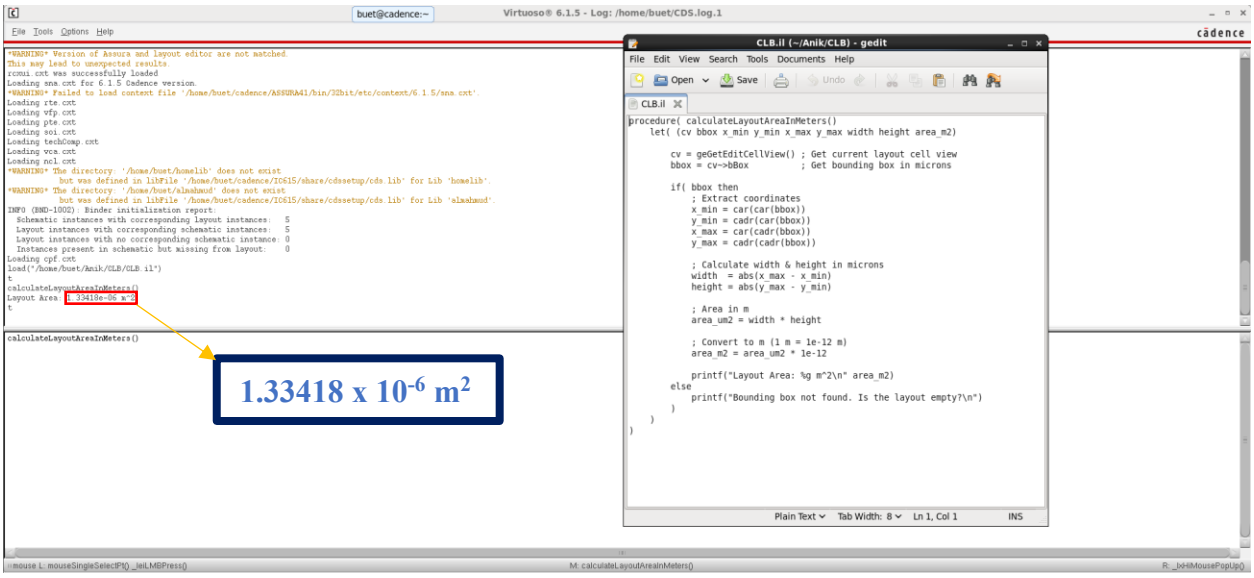

Figure 40: Area Calculation.

Average Energy Calculation:

The average energy consumption was determined by integrating the instantaneous power over the simulation time and dividing by the total duration. Instantaneous power was computed as the product of the supply voltage and the measured current through the circuit. In Cadence Virtuoso, the built-in calculator tool was used to evaluate:

$$E_{\text{avg}} = \frac{\int_{t_0}^{t_f} V(t) \cdot I(t)\, dt}{t_f - t_0}$$

where t_0 and t_f are the start and end times of the measurement window. We can see our CLB consumes 167.7fJ of average energy.

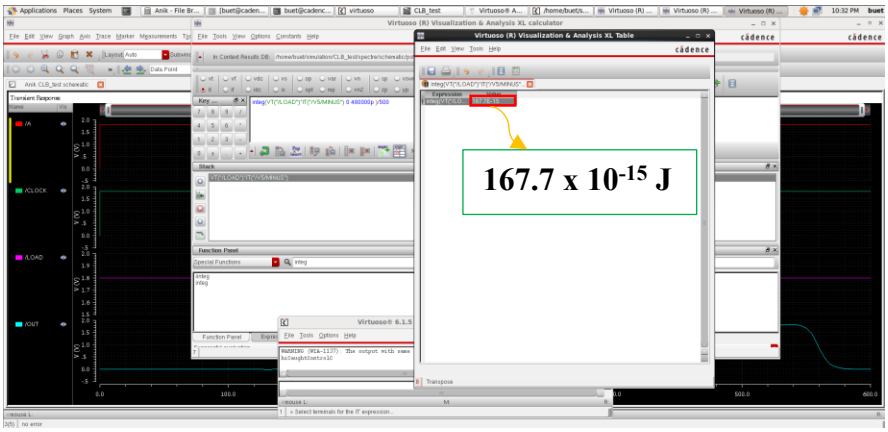

Figure 41: Avg. Energy Calculation

FOM Calculation:

We know the equation of FOM is:

$FOM = E_{avg} \times t_{delay} \times Area$

From our previous calculation we have,

$E_{avg} = 167.7 \times 10^{-15}$ J

$t_{delay} = 243 \times 10^{-12}$ s

$Area = 1.33418 \times 10^{-6}$ m^2

Therefore, our FOM is,

$FOM = E_{avg} \times t_{delay} \times Area$

$= 167.7 \times 10^{-15} \times 243 \times 10^{-12} \times 1.33418 \times 10^{-6}$

$= 5.43693026 \times 10^{-29}$ J·s·m²

Conclusion:

A 3:1 Configurable Logic Block (CLB) was designed, implemented, and evaluated in 90 nm CMOS technology, integrating a Look-Up Table (LUT), multiplexer (MUX), Static Random-Access Memory (SRAM), and D-type flip-flop into a compact, functionally complete architecture. The selected logic function, **A + BC**, exhibited correct operation in both combinational and sequential modes. Post-layout analysis determined a worst-case delay of **214.46ps**, yielding a theoretical minimum clock period of **243ps** and a corresponding critical frequency of approximately **4.12 GHz**. Additional high-speed simulations indicated that the CLB could sustain correct operation down to a clock period of **93ps**, corresponding to a maximum achievable critical frequency of approximately **10.75 GHz** before output distortion occurred. The final layout occupied **1.33418×10^{-6} m²** and demonstrated an average energy consumption of **167.7 fJ**, resulting in a Figure of Merit (FOM) of **5.43×10^{-29} J·s·m²**. These results confirm that the design meets functional and performance specifications, achieving a favorable balance between speed, area, and power efficiency, and providing a solid foundation for future FPGA CLB performance optimization.