Project 2: 1-bit Full Adder

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1. Introduction and Motivation

This project focuses on designing a 1-bit full adder with propagation delays (TpLH and TpHL) as close as possible. The primary aim is to investigate the design intricacies of this full adder and evaluate its performance under various conditions, including corner simulations, Monte Carlo analysis for local mismatch, and post-layout simulations. Furthermore, the report includes circuit design, transistor sizing, functional and post-layout simulations, and analyze worst-case delay and power consumption under different scenarios.

2. Circuit Design and Transistor Sizing

The 1-bit full adder features three 1-bit inputs (A, B, and Ci) and two 1-bit outputs (S and Co), and to achieve the desired output, the CMOS structure employs NMOS pull-down networks (PDN) and PMOS pull-up networks (PUN). The transistor-level design of the 1-bit CMOS full adder circuit, which comprises a total of 28 transistors, is illustrated in Figure 1 [1].

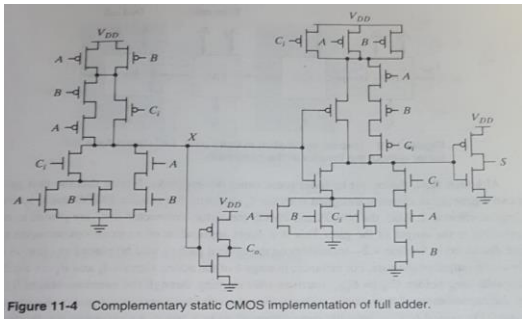

Figure 1 1-bit full adder

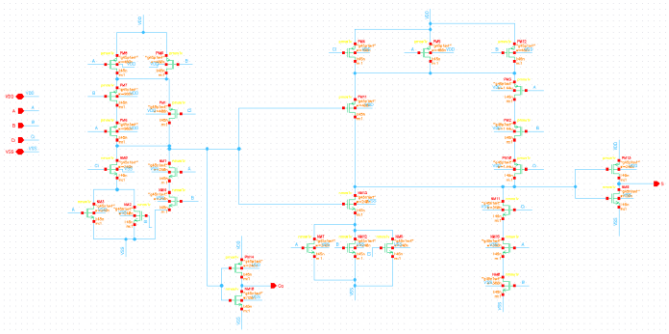

Figure 2 1-bit full adder schematic

Moreover, to ensure equal propagation delays (TpHL= TpLH), it is necessary to size the individual transistors in the Pull-Up Network (PUN) and Pull-Down Network (PDN) to match the sizing ratio of an inverter. Based on the inverter analysis conducted in Project-1, we have $(W/L)p$: $(W/L)n$ =2:1. Figure 3 provides details of the transistor sizing.

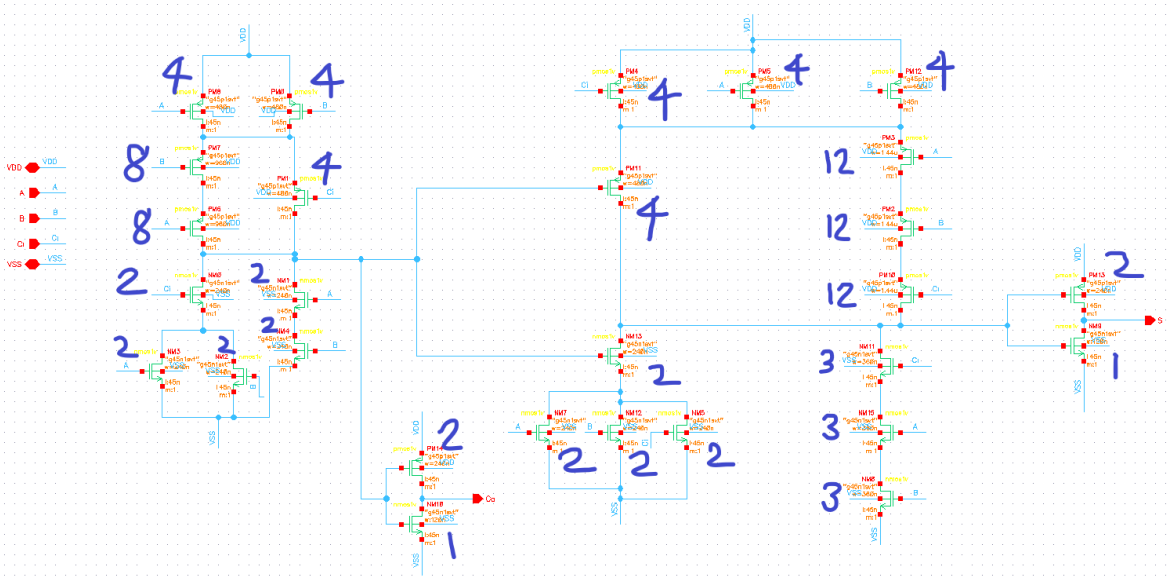

Figure 3 Transistor sizing

3. Simulation Results and analysis

a. Functional waveforms

The image provided below depicts the test bench and the corresponding waveform for the 1-bit full adder. It is evident that the waveform aligns with the truth table of a 1-bit full adder, affirming the correct operation of the testbench.

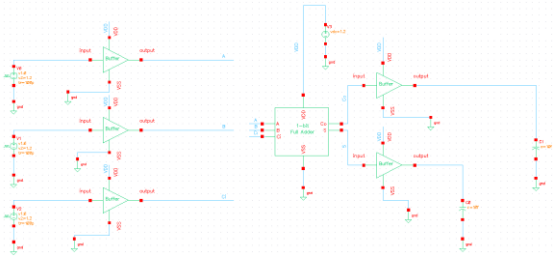

Figure 4 1-bit Full adder Testbench

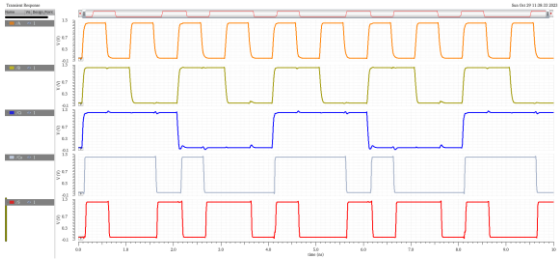

Figure 5 1-bit adder Waveform

Additionally, presented below is a table detailing the delay values for all eight possible input combinations, considering the three inputs (A, B, Ci) while operating under the TT corner and at a temperature of 27°C.

Table 1 Delay values for all possible input combinations under tt corner and at T=27°C

ABCi	DELAY		Comparison (in %)
	Pre-layout (in ps)	Post-layout (in ps)	
000	50.484	85.38205	69.127%
001	76.12	121.845	60.0696%
010	47.30	112.60575	138.067%
011	55.415	83.98	51.5474%
100	47.54	87.7249	84.5286%
101	47.67	92.7357	94.5368%

110	88.525	141.0215	59.3013%
111	50.375	88.3801	75.4444%

The input configuration 110 has been identified as the condition leading to the most significant delay in the circuit's operation, with a recorded delay of 88.525 ps in the pre-layout simulation which further extends to 141.0215 ps in the post-layout simulation.

b. Global mismatch

Table 4 displays the schematic simulation results for delay (Tp), average power (Pavg), and power delay product (PDP) across different process corners (TT, SS, FF, SF, FS) and temperatures (-25°C and 27°C). These simulations were conducted using the input signal combination that exhibits the slowest performance.

Table 2 Corner Simulation Results for Delay, Average Power and PDP (T=27°C)

	TT	SS	FF	SF	FS
TpLH (in ps)	58.6868	70.7312	49.4695	62.4722	55.5002
TpHL (in ps)	97.5927	117.652	82.9632	106.246	91.1108
Tp (in ps)	78.13975	94.1916	66.21635	84.3591	73.3055
Pavg (in uW)	38.1195	37.4615	38.96	38.163	38.1095
PDP (in fWs)	2.978648	3.528559	2.579789	3.219396	2.793636

Table 3 Corner Simulation Results for Delay, Average Power and PDP (T= -25°C)

	TT	SS	FF	SF	FS
TpLH (in ps)	46.184	56.4895	38.2783	49.3397	43.3997
TpHL (in ps)	80.0085	97.4938	67.2408	88.3484	73.6337
Tp (in ps)	63.09625	76.99165	52.75955	68.84405	58.5167
Pavg (in uW)	37.6015	36.9672	38.4287	37.705	37.551
PDP (in fWs)	2.3725	2.8462	2.0275	2.5958	2.1974

c. Local mismatch

A Monte Carlo simulation is conducted under the conditions of 1.2V supply voltage and 27°C temperature on a testbench for 100 distinct samples. The results of these 100 samples are shown in figure 6 and figure 7 and the results are summarized in table 4.

Table 4 Monte Carlo simulation result

	Minimum	Maximum (worst case delay)	Mean
Tp (in ps)	71.4	86.9	78.3678
Avg_power (in uW)	37.9	38.4	38.1236

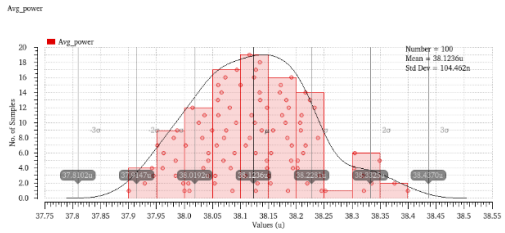

Figure 6 Avg_power Monte carlo waveform

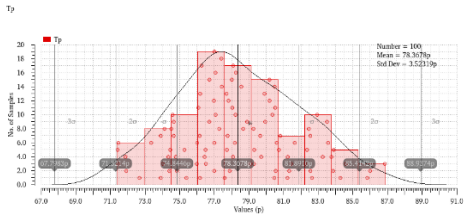

Figure 7 Delay Monte carlo waveform

4. Layouts & Post-layout Simulation

The figure given below represents the Design Rule Checks (DRC) and Layout versus Schematic (LVS) error free layout of a 1-bit full adder.

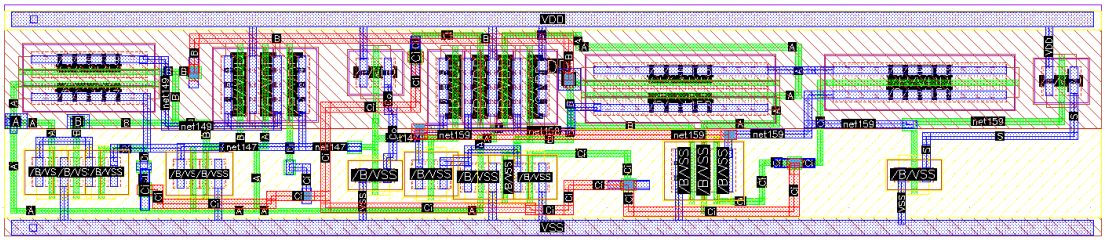

Figure 8 DRC and LVS error free 1-bit adder layout

Post-layout simulation was performed under TT and 27ºC.

Table 5 Post-layout result

Tp (in ps)	121.845
Avg_power (in uW)	45.88
PDP (in fWs)	5.5902

Table 6 Pre-Layout V/S Post layout

Tp	60.0696%
Avg_power	20.35%
PDP	87.679%

5. Conclusion

A 1-bit full adder circuit based on static CMOS technology was implemented using Cadence Virtuoso. Initial simulations were carried out in the pre-layout stage under the TT (Typical Typical) corner conditions to identify the worst-case delay, which occurred when inputs ABC were set to 110.

After this, corner simulations were performed to assess both global mismatch (FF, FS, SF, SS) and local mismatch (Local Simulations). The design was further transformed into a layout, and rigorous checks for Design Rule Checks (DRC) and Layout versus Schematic (LVS) errors were conducted. Post-layout simulations were executed under TT conditions at a temperature of 27°C.Notably, a substantial increase in the post-layout values was observed compared to the pre-layout values. This disparity highlights the impact of physical layout and parasitic elements on the circuit's performance, emphasizing the importance of post-layout simulations in the design process.

6. Reference

[1] J. Rabaey, "Chapter-11", in Digital Integrated Circuits, p. 565.