Project 3: 16-Bit Adder

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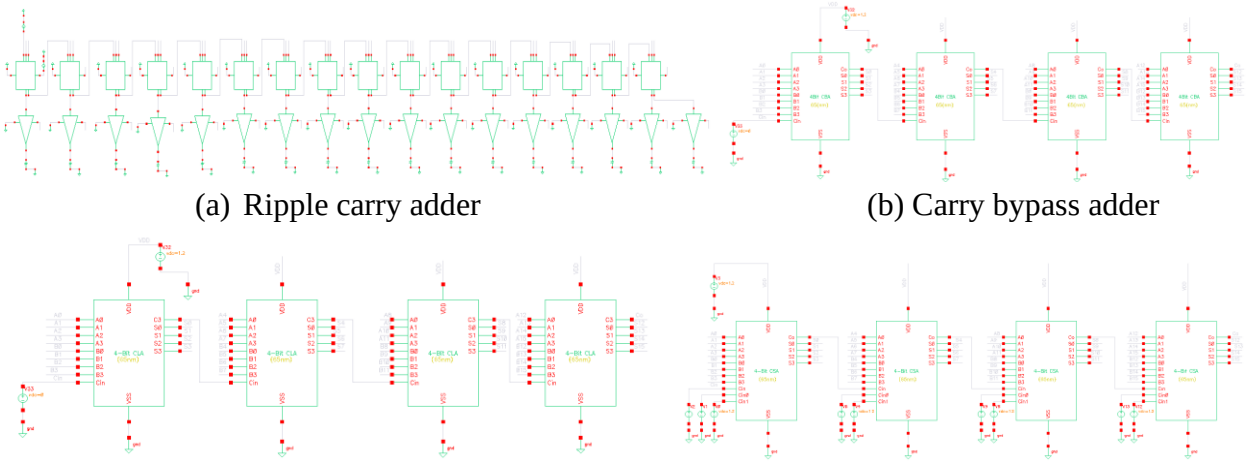
1. Introduction, review and simulation results of 4 different adder architectures

In this project, four different adders were compared based on delay as shown in the Figure 1:
1) Ripple carry adder: A ripple carry adder is built by cascading 1-bit full adders, where the carry output of each full adder is connected to the carry input of the next full adder in the sequence.
2) Carry Bypass adder (CBA): The carry bypass adder operates by bypassing carry propagation when all propagate bits are 1, effectively minimizing delay.
3) Carry Lookahead adder (CLA): The carry lookahead adder involves precomputing carry signals independently of the data inputs, enhancing addition speed by reducing carry propagation delays.
4) Carry select adder (CSA). The carry-select adder concurrently generates sum outputs with both possible carry inputs and selects the sum and cout using the 2x1 mux based on the carry-in signal.



(a) Ripple carry adder (b) Carry bypass adder

(c) Carry look-ahead adder (d) Carry select adder

Figure 1 Four Different adder architectures

The delay is minimal for the addition of A=0000 0000 0000 000 and B=1111 1111 1111 1111 (where Cin=0) in the 16-bit carry bypass adder compared to the other three adders. Simulations were conducted under TT and 27 ◦C conditions, with results summarized in Table 1a. Given the lower delay for the **CBA adder**, it has been selected for further analysis.
Propagation delay (tp) = average (tpHL, tpLH)
Power delay Product (PDP) = Avg_Power × tp

Table 1 Delay, Power & PDP for four different adders

	Tp (ps)	Power (uW)	PDP (fWs)
Ripple Carry	656.3	402.4	264.0951
CBA	354.4	485	171.884
CLA	380.4	471.1	179.2064
CSA	373.2	607.9	226.8683

2. Architecture and transistor-level circuit design of Carry bypass adder

In a 4-bit carry bypass adder (CBA), the generation (Gi) and propagation (Pi) bits are employed to determine the carry bit, akin to a Carry Look-Ahead (CLA) adder. However, in the CBA, if the logical AND operation (P0, P1, P2, P3) equals 1, then Cin (input carry) equals Cout (output carry). The bypassing of carry propagation under specific conditions, enhancing its speed for certain input combinations. The equations governing this adder are as follows:

$Gi=Ai \ \& \ Bi$

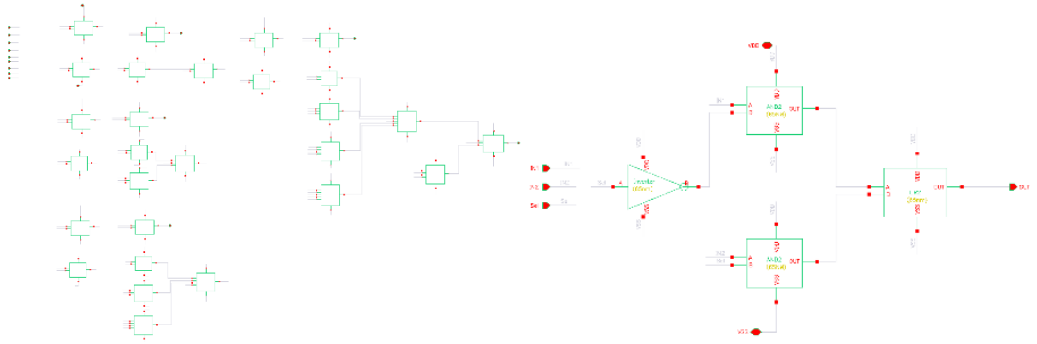
$Pi=Ai \ XOR \ Bi$

$Ci+1=Gi+(Pi \times Ci)$

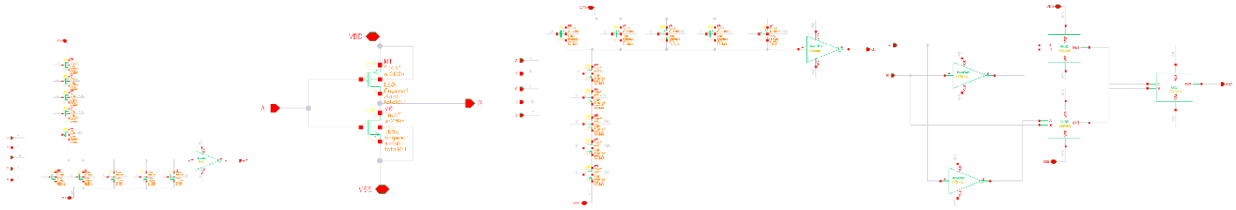
$Si=Pi+ \ Ci$

If AND (P0, P1, P2, P3) =1 then Cin=Cout.

where Ai and Bi are the inputs and Ci and Si are carry and sum respectively.



(a) 4-bit adder architecture (b) 2x1 Mux



(c) OR5 (d) Inverter (e) AND5 (f) XOR2

Figure 2 Architecture and transistor-level circuit design of Carry bypass adder

3. Simulation results and analysis (Carry bypass adder)

3.1 Functional waveforms

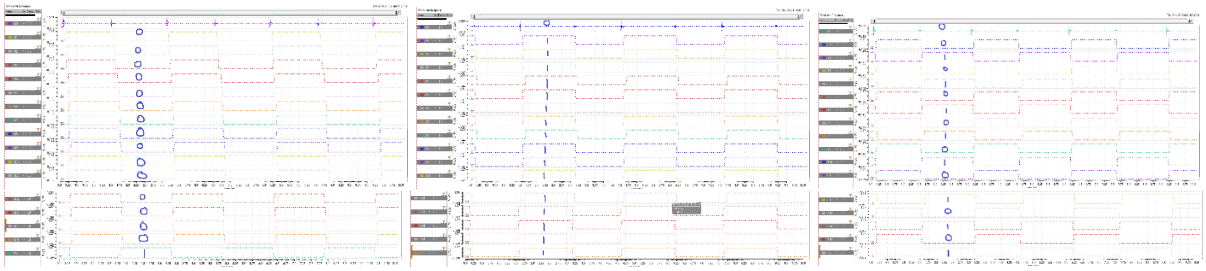
For the 16-bit Carry Bypass Adder, vector additions were executed under TT, 27°C as follows:

Vector A: 0000 0000 0000 0001 + 1111 1111 1111 1111 = 1 0000 0000 0000 0000 (Cout=1)

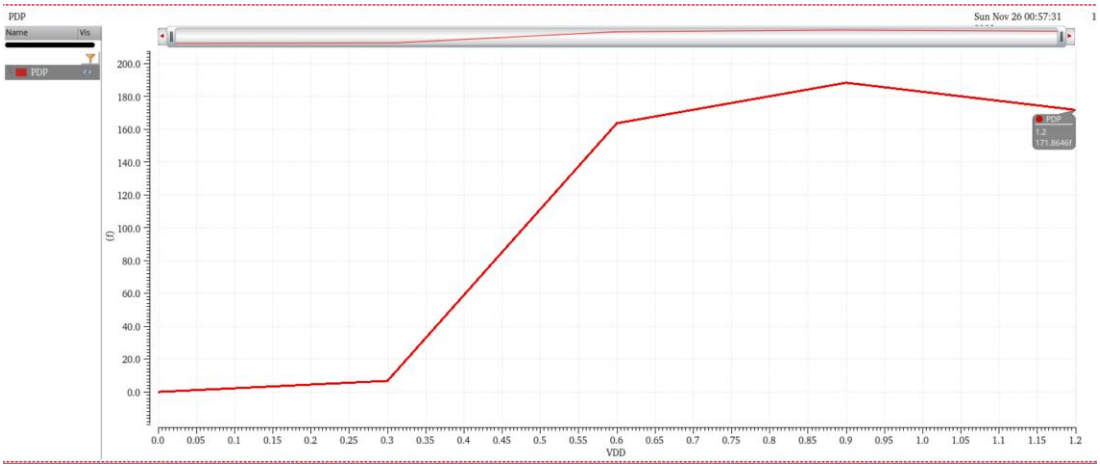
Vector B: 1111 1111 1111 1111 + 1111 1111 1111 1111 = 1 1111 1111 1111 1111 (Cout=1)

Vector C: 1010 1010 1010 1010 + 1010 1010 1010 1010 = 1 0101 0101 0101 0100 (Cout=1)

The functional waveforms for these three vectors are represented in Figure 3.



(a) Vector A (b) Vector B (c) Vector C



(d) PDP vs. Power supply voltage

Figure 3 Functional waveforms of vector additions and PDP vs VDD

3.2 Global mismatch: corner/temperature

A global mismatch simulation was executed for a 16-bit carry bypass adder under three different conditions: 1) FF (-25°C), 2) TT (27°C), and 3) SS (85°C). The simulation results, detailing parameters such as Delay, power, and power delay product, are shown in Table 2.

Table 2 Corner Simulations results for Carry bypass adder

	Delay (ps)			Power (uW)			PDP (fWs)		
	FF (-25°C)	TT (27°C)	SS (85°C)	FF (-25°C)	TT (27°C)	SS (85°C)	FF (-25°C)	TT (27°C)	SS (85°C)
Vector A	280.8	354.4	465.4	569.4	485	454.6	159.8875	171.884	211.5708
Vector B	56.14	71.32	93.97	378.1	344	327.2	21.22653	24.5341	30.74698
Vector C	56.26	71.52	94.28	389.8	355.4	338.6	21.93015	25.4183	31.92321

3.3 PDP vs. power-supply voltage

A parametric analysis was conducted by varying the design variable, VDD, across the range of 0 to 1.2 V with vector A under TT, 27°C conditions for 16 but carry bypass adder. The corresponding graphical representation of this parametric study is illustrated in Figure 3(d) where it was observed that with increase in VDD PDP increased too.

4. Conclusion

In conclusion, this laboratory study involved the selection and comparison of four different adders for vector A under TT (27°C) conditions. The analysis revealed that the carry bypass adder exhibited the smallest delay, measuring at 354.4ps. Successful execution of three vector additions further validated the functionality of the Carry Bypass Adder (CBA). Additionally, the carry bypass adder demonstrated total adding times of less than 400ps for nearly all corner and temperature combinations, except for the SS (85°C) condition. Furthermore, during power supply variation, it was noted that an increase in VDD corresponded to an increase in the power delay product.