Project-1: Designing Basic Logical Gates (Inverter, NAND, NOR)

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PART 1 (Inverter Design):

1.1 Inverter Design

The inverter is designed by using PMOS as pull-up network and NMOS as pull-down network. The PMOS and NMOS are connected in series as shown in Fig 1.1.

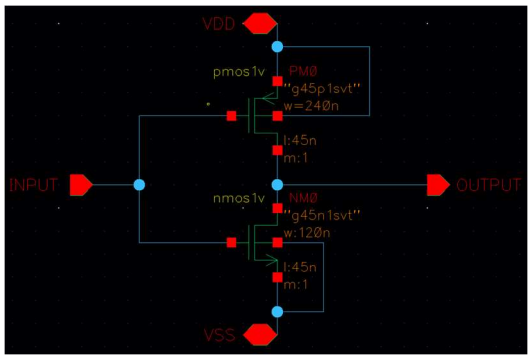

Fig 1.1 Inverter Schematic

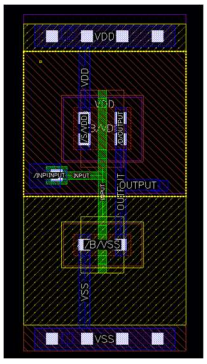

Fig 1.2 Inverter Layout

1.2 DC and Transient Simulations

The DC simulations covered a range of input voltages from 0V to VDD (1.2V). Transient simulations were conducted, and multiple parameters were computed.

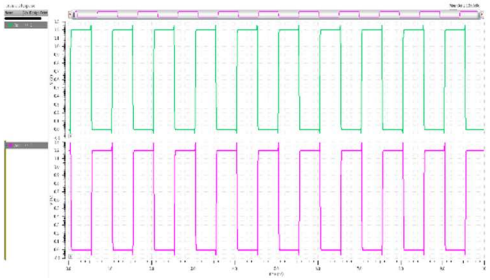

Fig 1.3 Transient Simulation

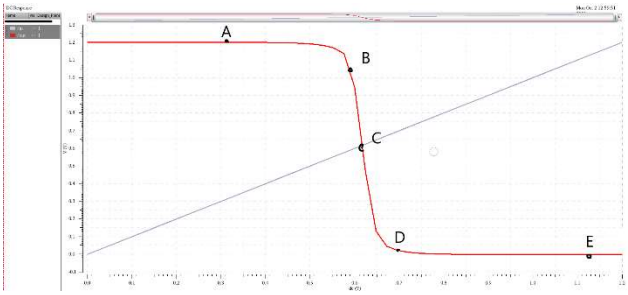

Fig 1.4 DC Simulation

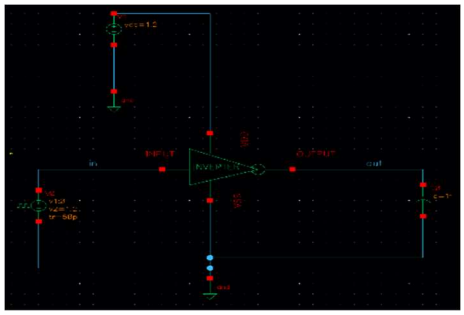

Fig 1.5 Inverter Testbench (without buffer)

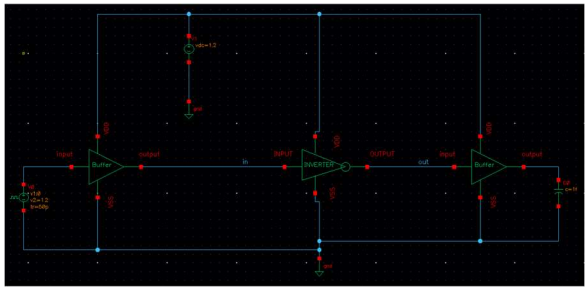

Fig 1.6 Inverter Testbench (with buffer)

Propagation delay (tp) = max (tpHL, tpLH)

Power delay Product (PDP) = Avg_Power × tp

Table 1.1 Pre-layout

tpHL	7.637p
tpLH	7.005p
tp	7.637p
Avg_power	5.283u
PDP	40.346a

Table 1.2 Post Layout

tpHL	9.745p
tpLH	8.926p
tp	9.745p
Avg_power	5.715u
PDP	55.692a

Table 1.3 Pre vs Post Layout

tpHL	27.6%
tpLH	27.4%
tp	27.6%
Avg_power	8.177%
PDP	38.036%

Table 1.4 Region of Operation of CMOS Inverter

Region of operation	Vin	Vout	PMOS	NMOS
A	<VTO,n	VOH	Linear	Cut-off
B	VIL	VOH	Linear	Saturation
C	VTH	VTH	Saturation	Saturation
D	VIH	VOL	Saturation	Linear
E	>(VDD+VTO,P)	VOL	Cut-off	Linear

PART 2 (NAND gate design)

2.1 NAND design

In the NAND gate design, the PUN employs 2 PMOS in parallel, and the PDN uses 2 NMOS in series as depicted in Figure 2.1.

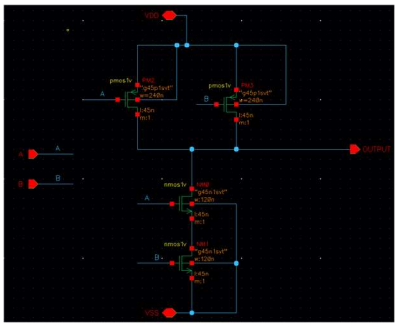

Fig 2.1 NAND gate schematic

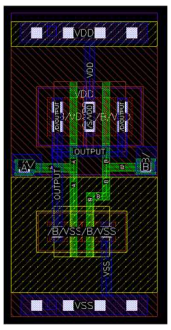

Fig 2.2 NAND gate layout

2.2 Transient Simulations

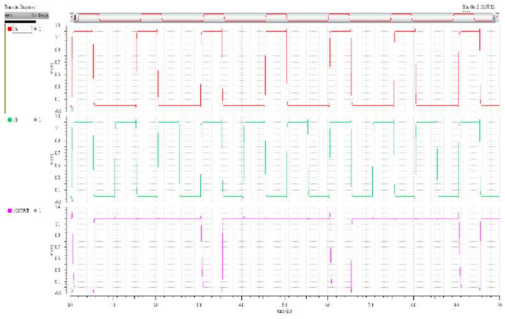

Fig 2.3 Transient Simulations

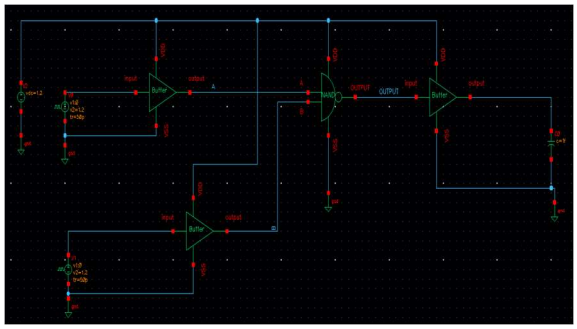

Fig 2.4 NAND Testbench

Table 2.1 Pre-layout

tpHL	16.01p
tpLH	5.693p
tp	16.01p
Avg_power	4.342u
PDP	69.515a

Table 2.2 Post-layout

tpHL	21.39p
tpLH	8.138p
tp	21.39p
Avg_power	5.089u
PDP	108.85a

Table 2.3 Pre vs Post layout

tpHL	33.6%
tpLH	42.95%
Tp	33.6%
Avg_power	17.2%
PDP	56.58%

PART 3 (NOR gate design):

3.1 NOR design

The NOR gate is designed by using 2 PMOS transistors in series, acting as PUN, and 2 NMOS transistors in parallel, acting as PDN.

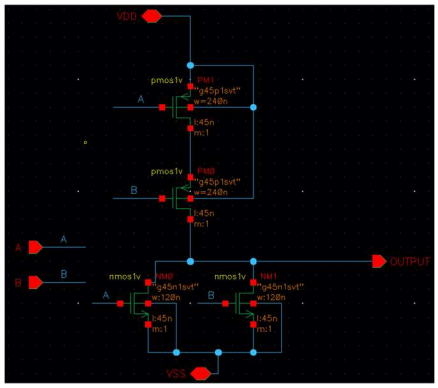

Fig 3.1 NOR schematic

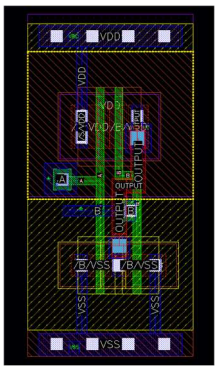

Fig 3.2 NOR layout

3.2 Transient Simulations

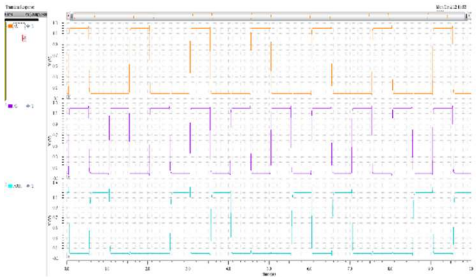

Fig 3.3 Transient Simulations

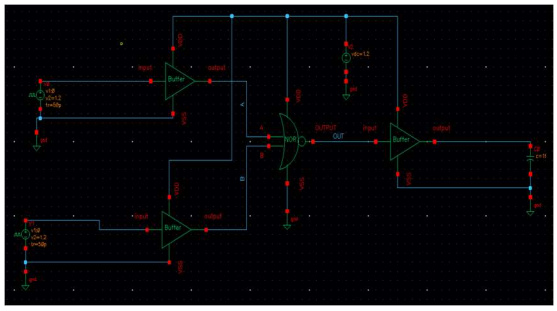

Fig 3.4 NOR Testbench

Table 3.1 Pre-layout

tpHL	8.538p
tpLH	12p
tp	12p
Avg_power	5.459u
PDP	65.508a

Table 3.2 Post Layout

tpHL	11.44p
tpLH	17.07p
tp	17.07p
Avg_power	6.321u
PDP	107.899a

Table 3.3 Pre vs Post Layout

tpHL	33.99%
tpLH	42.25%
Tp	42.25%
Avg_Power	15.79%
PDP	64.711%