Tirth Halvadia

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Education

University of Waterloo **September 2023 – September 2024**

Master of Electrical and Computer Engineering

Relevant Coursework: RTL Digital Systems, Digital Integrated Circuits, Microelectronic Processing Technology, Methods and Principles of Safety-Critical Embedded Software

Technical Skills

- **Languages**: Verilog, SystemVerilog, Python
- **Simulation and EDA Tools**: Cadence Virtuoso, Intel Quartus Prime, Xilinx Vivado, ModelSim, LTspice, Proteus Design Suite, NI LabVIEW, NI Multisim
- **Hardware Description and Design Concepts**: RTL Design, Integrated Circuits, CMOS Transistors, Digital Signal Processing, Digital Systems
- **Operating System**: Linux, Windows
- **Version Control** : Git

Experience

Institute for Plasma Research **December 2022 – March 2023**

Intern

- Developed and implemented clock synchronization solutions for data acquisition applications using NI LabVIEW, PXIe cards, a GPS receiver module, a function generator, and a CRO, optimizing the system for precise DAQ functionality.
- Achieved a precise ±15ms timestamp accuracy when synchronizing with the engineering station's internal clock.
- Significantly improved timing accuracy to 0.9µs by integrating GPS timestamps with precise 1Hz external triggers from a function generator
- Reached an impressive 10ns timing accuracy by fully synchronizing the clock with GPS-based timestamps.

Projects

Matrix Multiplication Using Systolic Array Architecture - Hardware Design/FPGA Project **(Github)**

- Designed and implemented a systolic array-based matrix multiplication core using Verilog and SystemVerilog, adding cascaded counters and control modules to automate data flow, thereby enhancing computation efficiency.
- Simulated, synthesized, and deployed the design on the Xilinx PYNQ FPGA+ARM SoC, successfully tested with an input array size of 16 (M=16) and a processing matrix size of 4 (N=4), while leveraging AXI protocol for efficient memory interfacing and batch folding to enhance data reuse.

UART Communication System - Digital Design/FPGA Project **(Github)**

- Designed a UART communication system in Verilog with configurable baud rates and data widths, with verified testbenches for transmitter (PISO) and receiver (SIPO) modules in Xilinx Vivado, including parity bit error handling for reliability.
- Achieved timing closure at 250 MHz with positive timing margins and generated bitstreams for deployment on the ZedBoard Zynq FPGA

Hexadecimal to Seven Segment Display - Digital Design/FPGA Project **(Github)**

- Engineered a Verilog model to process hexadecimal inputs with 3-bit encoding, facilitating representation across the hexadecimal spectrum.
- Utilized Verilog for both the design and test-bench creation, along with Xilinx Vivado for simulation, synthesis, and implementation on the ZedBoard Zynq Evaluation and Development Kit, culminating in the generation of bitstreams.

Designing Basic Logical Gates - VLSI/IC Design Project **(Github)**

- Designed schematic, layout, and test-bench for Inverter, NAND, and NOR gates using Cadence Virtuoso, ensuring error-free layout by resolving DRC and LVS issues to meet design standards.
- Performed parasitic capacitance extraction and post-layout transient simulations to analyze circuit performance, ensuring design integrity and functionality.

16-Bit Adder - VLSI/Digital Circuit Design Project **(Github)**

- Designed and evaluated four types of 16-bit adders using Cadence Virtuoso, with the Carry Bypass Adder (CBA) achieving the lowest propagation delay of 354.4ps.
- Conducted comprehensive corner and temperature simulations (-25°C to 85°C) for the CBA, demonstrating robust performance with delays ranging from 280.8ps to 465.4ps across various conditions.