Tirth Halvadia

548-577-2539 tirthhalvadia@gmail.com linkedin.com/in/tirth-halvadia/ github.com/Tirthhalvadia

Education

University of Waterloo **2023 – 2024**
Master of Electrical and Computer Engineering *Waterloo, Canada*
Relevant Courses: ECE627 RTL Digital Systems, ECE637 Digital Integrated Circuits, ECE 631 Microelectronic Processing Technology, ECE652 Methods and Principles of Safety-critical Embedded Software

Dharmsinh Desai University **2019 – 2023**
Bachelor of Electronics and Communication Engineering *Gujarat, India*

Experience

Institute for Plasma Research **Dec 2022 – Mar 2023**
Intern *Gujarat, India*
- Collaborated effectively with a dedicated team to conceive, develop, and implement clock synchronization solutions for data acquisition applications using NI LabVIEW and PXIe cards for DAQ purposes.
- Successfully attained a remarkable ±15ms timestamp accuracy when utilizing the engineering station's time.
- Significantly enhanced time accuracy to 0.9us by integrating GPS timestamps with precise 1Hz external triggers.
- Accomplished an impressive 10ns time accuracy after synchronizing the clock using GPS timestamps.

Projects

Matrix Multiplication with FPGA-based Systolic Array Architecture **Github**
- Developed hardware modules enabling matrix multiplication utilizing a systolic array architecture.
- Engineered two memory interface modules to support storage for input and output matrices.
- Produced bit streams for configuration of the Xilinx PYNQ FPGA+ARM SoC.

UART Communication System **Github**
- Developed and implemented testbenches using Xilinx Vivado, ensuring reliable transmission with parity error detection.
- Designed and implemented a complete UART communication system in Verilog, supporting configurable baud rates and data widths, deployed on ZedBoard Zynq FPGA.
- Achieved 250 MHz clock frequency with positive timing margins.

Synthesis and Implementation of Hexadecimal to 7 segment Display **Github**
- Engineered a Verilog model to process hexadecimal inputs with 3-bit encoding, facilitating representation across the hexadecimal spectrum.
- Utilized Verilog for both the design and test-bench creation, along with Xilinx Vivado for simulation, synthesis, and implementation on the ZedBoard Zynq Evaluation and Development Kit, culminating in the generation of bitstreams.

Designing Basic Logical Gates **Github**
- Proficiently designed schematic, layout, and test-bench for Inverter, NAND, and NOR gates using Cadence Virtuoso software.
- Ensured error-free layout by resolving DRC and LVS issues.
- Performed parasitic capacitance extraction and post-layout transient simulations to analyze circuit performance, ensuring design integrity and functionality.

16-Bit Adder **Github**
- Designed and evaluated four types of 16-bit adders with the help of Cadence Virtuoso.
- Generated comprehensive functional, corner, and temperature simulations to assess performance.
- Demonstrated the Carry Bypass Adder's (CBA) efficiency with total adding times of less than 400ps for most conditions, highlighting the importance of power-supply voltage optimization for enhanced performance.

Technical Skills

Languages: Verilog, SystemVerilog, Python
Simulation and EDA Tools: Cadence Virtuoso, Intel Quartus Prime, Xilinx Vivado, ModelSim, LTspice, Proteus Design Suite, NI LabVIEW, NI Multisim
Hardware Description and Design Concepts: RTL Design, Integrated Circuits, CMOS Transistors, Digital Signal Processing, Digital Systems
Operating System: Linux, Windows
Version Control : Git

Volunteer Work

Shrimad Rajchandra Love and Care **2017 – Present**
Volunteer
- Managed events occasionally, coordinating logistics and ensuring smooth operations alongside regular departmental responsibilities.