

# TIRTH HALVADIA

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## Education

### University of Waterloo

2023 – 2024

*Master of Electrical and Computer Engineering*

*Waterloo, Canada*

Relevant Courses: ECE627 RTL Digital Systems, ECE637 Digital Integrated Circuits, ECE 631 Microelectronic Processing Technology, ECE652 Methods and Principles of Safety-critical Embedded Software

### Dharmsinh Desai University

2019 – 2023

*Bachelor of Electronics and Communication Engineering*

*Gujarat, India*

## Experience

### Institute for Plasma Research

Dec 2022 – Mar 2023

*Intern*

*Gujarat, India*

- Collaborated effectively with a dedicated team to conceive, develop, and implement clock synchronization solutions for data acquisition applications using NI LabVIEW and utilizing PXIe cards for DAQ purposes.
- Successfully attained a remarkable  $\pm 15\text{ms}$  timestamp accuracy when utilizing the engineering station's time.
- Significantly enhanced time accuracy to  $0.9\mu\text{s}$  by integrating GPS timestamps with precise 1Hz external triggers.
- Accomplished an impressive  $10\text{ns}$  time accuracy after synchronizing the clock using GPS timestamps.

## Projects

### Matrix Multiplication with FPGA-based Systolic Array Architecture

[Github](#)

- Developed hardware modules enabling matrix multiplication utilizing a systolic array architecture.
- Engineered two memory interface modules to support storage for input and output matrices.
- Produced bit streams for configuration of the Xilinx PYNQ FPGA+ARM SoC.

### Synthesis and Implementation of Hexadecimal to 7 segment Display

[Github](#)

- Engineered a Verilog model to process hexadecimal inputs with 3-bit encoding, facilitating representation across the hexadecimal spectrum.
- Utilized Verilog for both the design and testbench creation, along with Xilinx Vivado for simulation, synthesis, and implementation on the ZedBoard Zynq Evaluation and Development Kit, culminating in the generation of bitstreams.

### Designing Basic Logical Gates

[Github](#)

- Proficiently designed schematic, layout, and test-bench for Inverter, NAND, and NOR gates using Cadence Virtuoso software.
- Ensured error-free layout by resolving DRC and LVS issues.
- Performed parasitic capacitance extraction and post-layout transient simulations to analyze circuit performance, ensuring design integrity and functionality.

### 1-Bit Full Adder

[Github](#)

- Utilized Cadence Virtuoso to design and analyze a 1-bit static CMOS full adder circuit to assess variability.
- Conducted comprehensive corner and Monte Carlo simulations to assess variability and random mismatch effects.
- Demonstrated substantial performance improvements compared to pre-layout values through thorough simulation and analysis.

### 16-Bit Adder

[Github](#)

- Designed and evaluated four types of 16-bit adders with the help of Cadence Virtuoso.
- Generated comprehensive functional, corner, and temperature simulations to assess performance.
- Demonstrated the Carry Bypass Adder's (CBA) efficiency with total adding times of less than  $400\text{ps}$  for most conditions, highlighting the importance of power-supply voltage optimization for enhanced performance.

## Technical Skills

**Languages:** Verilog, SystemVerilog, Python, C/C++,

**Simulation and EDA Tools:** Cadence Virtuoso, Intel Quartus Prime, Xilinx Vivado, ModelSim, LTspice, Proteus Design Suite, NI Labview, NI Multisim

**Hardware Description and Design Concepts:** RTL Design, Integrated Circuits, CMOS Transistors, Digital Signal Processing, Digital Systems

**Operating System:** Linux, Windows

## Volunteer Work

### Shrimad Rajchandra Love and Care

2017 – Present

*Volunteer*

- Managed events occasionally, coordinating logistics and ensuring smooth operations alongside regular departmental responsibilities.