Tirth Halvadia

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Education

University of Waterloo **2023 – 2024**

Master of Electrical and Computer Engineering

Relevant Coursework: ECE627 RTL Digital Systems, ECE637 Digital Integrated Circuits, ECE 631 Microelectronic Processing Technology, ECE652 Methods and Principles of Safety-critical Embedded Software

Experience

Institute for Plasma Research **Dec 2022 – Mar 2023**

Intern

- Collaborated effectively with a dedicated team to conceive, develop, and implement clock synchronization solutions for data acquisition applications using NI LabVIEW and PXIe cards for DAQ purposes.
- Successfully attained a remarkable ±15ms timestamp accuracy when utilizing the engineering station's time.
- Significantly enhanced time accuracy to 0.9us by integrating GPS timestamps with precise 1Hz external triggers.
- Accomplished an impressive 10ns time accuracy after synchronizing the clock using GPS timestamps.

Projects

Matrix Multiplication Using Systolic Array Architecture on FPGA **Github**

- Designed and implemented a systolic array-based matrix multiplication core on FPGA, leveraging AXI protocol for efficient memory interfacing.
- Employed batch folding technique to handle larger matrices, enhancing data reuse and reducing memory overhead.
- Integrated cascaded counters and control modules to automate data flow through rows and columns, improving computation efficiency.
- Produced bit streams for configuration of the Xilinx PYNQ FPGA+ARM SoC.

UART Communication System **Github**

- Designed and implemented a complete UART communication system in Verilog, supporting configurable baud rates and data widths.
- Developed and verified testbenches for UART transmitter (PISO) and receiver (SIPO) modules using Xilinx Vivado, incorporating parity bit error handling to ensure reliable data transmission.
- Achieved timing closure at 250 MHz with positive timing margins and generated bitstreams for deployment on the ZedBoard Zynq FPGA

Synthesis and Implementation of Hexadecimal to Seven Segment Display **Github**

- Engineered a Verilog model to process hexadecimal inputs with 3-bit encoding, facilitating representation across the hexadecimal spectrum.
- Utilized Verilog for both the design and test-bench creation, along with Xilinx Vivado for simulation, synthesis, and implementation on the ZedBoard Zynq Evaluation and Development Kit, culminating in the generation of bitstreams.

Designing Basic Logical Gates **Github**

- Proficiently designed schematic, layout, and test-bench for Inverter, NAND, and NOR gates using Cadence Virtuoso software.
- Ensured error-free layout by resolving DRC and LVS issues.
- Performed parasitic capacitance extraction and post-layout transient simulations to analyze circuit performance, ensuring design integrity and functionality.

16-Bit Adder **Github**

- Designed and evaluated four types of 16-bit adders with the help of Cadence Virtuoso.
- Generated comprehensive functional, corner, and temperature simulations to assess performance.
- Demonstrated the Carry Bypass Adder's (CBA) efficiency with total adding times of less than 400ps for most conditions, highlighting the importance of power-supply voltage optimization for enhanced performance.

Technical Skills

Languages: Verilog, SystemVerilog, Python
Simulation and EDA Tools: Cadence Virtuoso, Intel Quartus Prime, Xilinx Vivado, ModelSim, LTspice, Proteus Design Suite, NI LabVIEW, NI Multisim
Hardware Description and Design Concepts: RTL Design, Integrated Circuits, CMOS Transistors, Digital Signal Processing, Digital Systems
Operating System: Linux, Windows
Version Control : Git