American International University-Bangladesh (AIUB)
Faculty of Engineering

DIGITAL LOGIC AND CIRCUITS
OBE Assignment [30 marks]
Summer Semester 2020-21
Submission Deadline: 08.08.2021
Submission Link: https://forms.gle/8H8gDqCtH7YXvX8j7

CO3	Formulate solutions of a complex engineering problem with conflicting requirements by applying information, concepts and procedures in engineering fundamentals of digital logic and circuits at gate and transistor level.	P.a.3.C3

Recently you have been registered for COVID-19 vaccination. In the vaccination center, only 4 people are allowed in a queue with maintaining three feet distance in front of a small room. If more than 2 people enter the room at the same time an alarm goes off. Each awaiting applicant has one digital token with sensor to detect their presence in the room.

Your task is to:

i. Outline the necessary steps in correct sequence of the standard procedure to design a digital system and design the system. Also show the outlined steps, which will trigger the alarm and implement the system with CMOS logic.

ii. The human audible ranges from 20Hz – 20kHz. However, any sound below 250Hz is considered to be disturbingly low pitched and any sound above 4500Hz is considered to be disturbingly high pitched. Design the alarm timer circuit with a frequency of **M5 Hz** and a duty cycle of **N%** [where **M= C+O+V+I+D** and **N = 100 – M]**. However, if M5 Hz is not within soothing hearing limits, take frequency, f =400Hz. Choose the capacitor value from the given list based on the suitability of your requirements. (C = 50uF/250uF/470uF)

Direction: The numbers COVID are the middle five digits of your ID (SS-COVID-S)
(In case the last two letters of your ID is 00, use 36 instead.)

Submission Guidelines:

** The assignment should only be **submitted in the proper link**.
** The assignment will **not be accepted after the submission deadline**.
** You MUST write your **CLASS SERIAL, ID, NAME, PAGE NUMBER** on top of the page.
** The assignment MUST be submitted in **PDF** format.
** Any trace of **copying will result in 0** for that section.

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MARKING RUBRIC:

CP	Assessment Criteria	Evaluation Criteria				Marks
		Poor [1-4]	Average [5-6]	Good [7-8]	Excellent [9-10]	
K3, P1	Outline of the standard procedure of digital system design	More than three steps are incorrect or missing and not in correct sequence	One or Two steps of the standard procedure is missing with a one or two steps not in sequence.	All the steps of the procedure have been identified with one or two steps not in correct sequence	All the steps of the procedure have been identified and in correct sequence	
	Digital Triggering Circuit Design.	Design flow has major errors and transistor level design has major flaws.	Design Flow has major error with error carried forward to transistor level design	Design Flow has minor error with error carried forward to transistor level design	Accurate Design Flow with transistor level design having no or minor errors	
P2, P6	Alarm/ Buzzer Design	Alarm design has major flaws which does not comply with the conflicting requirements with major calculation errors.	Alarm design has major flaws which does not comply with the conflicting requirements but with minor calculation errors.	Alarm design is correct and complies to the conflicting requirements but, with major calculation errors.	The alarm design is correct and comply to the requirements with no or minor calculation errors.	
					Total Marks Obtained	