Integrated Circuit Technologies

Introduction

When working with an IC or Integrated Circuit as an engineer we should be aware of the following factors:

1. The integration level
2. The logic family or technology
3. The logic level parameters
4. The performance parameters

Integration Level

The integration level of an IC or a semiconductor chip gives us an idea about the number of gates that are present in the chip.

Integration Level for Integrated Circuits.

- Small Scale Integration (SSI) (<12 gates/chip).
- Medium Scale Integration (MSI) (<100 gates/chip).
- Large Scale Integration (LSI) (…1K gates/chip).
- Very Large Scale Integration (VLSI) (…10K gates/chip).
- Ultra Large Scale Integration (ULSI) (…100K gates/chip).
- Giga Scale Integration (GSI) (…1M gates/chip).

Examples:

- **Pentium III Coppermine(32-bit, large cache): 21,000,000 gates**
- **Pentium 4 Willamette (32-bit, large cache): 42,000,000 gates**
- **Core 2 Duo Conroe (dual-core 64-bit, large caches): 291,000,000 gates**
- **ARM Cortex-A9 (32-bit, (optional) SIMD, caches):26,000,000 gates**
- **Atom (32-bit, large cache): 47,000,000**

Definition of Logic Level Parameters

Different Logic Families usually operate at different voltage and current levels. Before knowing the particular levels for different families one should first be acquainted with the logic level parameters and their definitions.

Voltage Parameters

High-Level Output Voltage, V_{OH} (MIN): This is the minimum output voltage available at the output under stated loaded condition which corresponds to logic '1'.

Low-Level Output Voltage, V_{OL} (MAX): This is the maximum output voltage available at the output under stated loaded condition which corresponds to logic '0'

High-Level Input Voltage, V_{IH} (MIN): This is the minimum voltage required at an input to be recognized as a logic '1'.

Low-Level Input Voltage, V_{IL} (MAX): This is the maximum voltage at an input which will be recognized as a logic '0'.

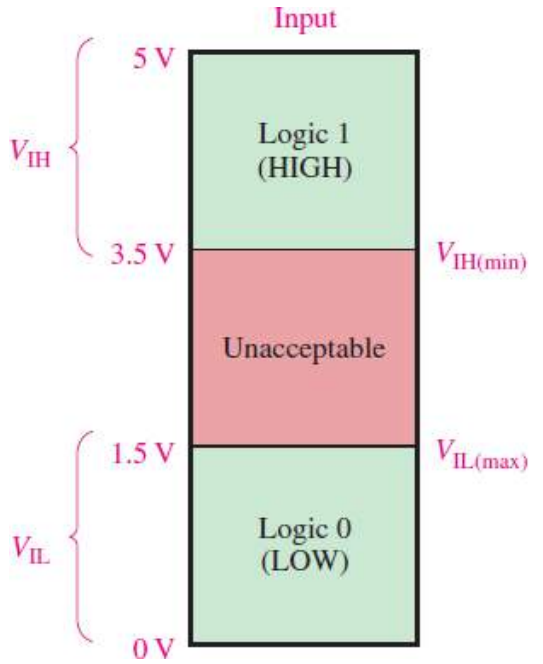
Current Parameters

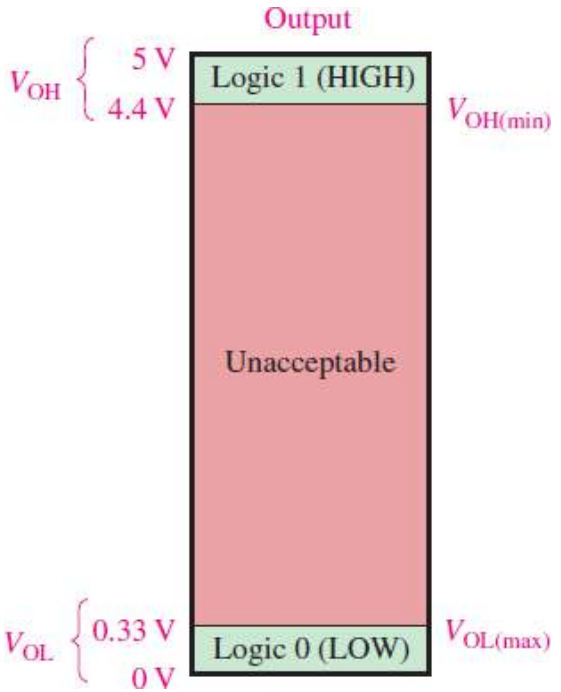
High-Level Output Current, I_{OH} : This is the maximum current at the output under specified loaded condition that a gate can sink at logic level '1'.

Low-Level Output Current, I_{OL}: This is the maximum current a gate can sink at specified load at logic '0',

High-Level Input Current, I_{IH}: This is the minimum current a supply must provide in order to maintain the logic '1'.

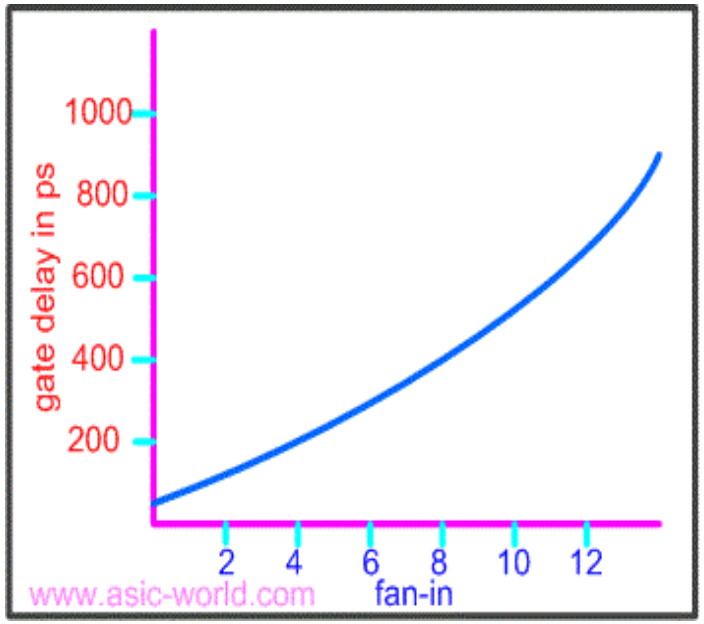
Low-Level Input Current, I_{IL}: This is the minimum current that must be provided in order maintain a logic '0'.





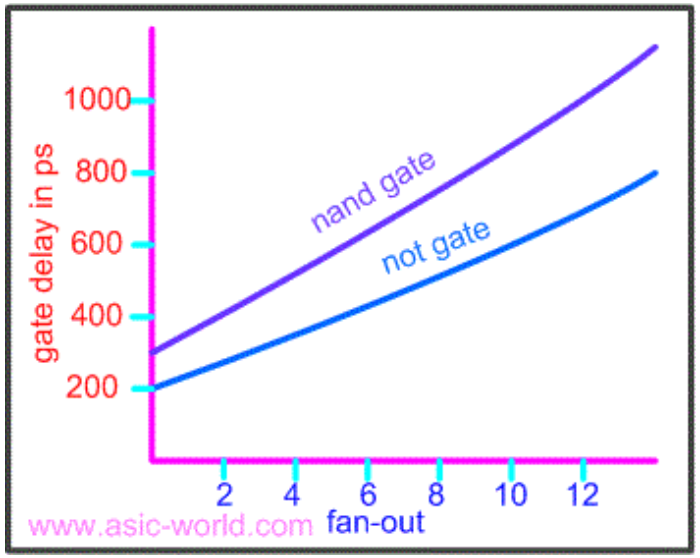
Performance Parameters of Logic Families

Fan-In: It is the number of input that can be connected to a particular gate. As more inputs are connected the delay in the input side increases. Delay approximately has a quadratic relationship with Fan-in.



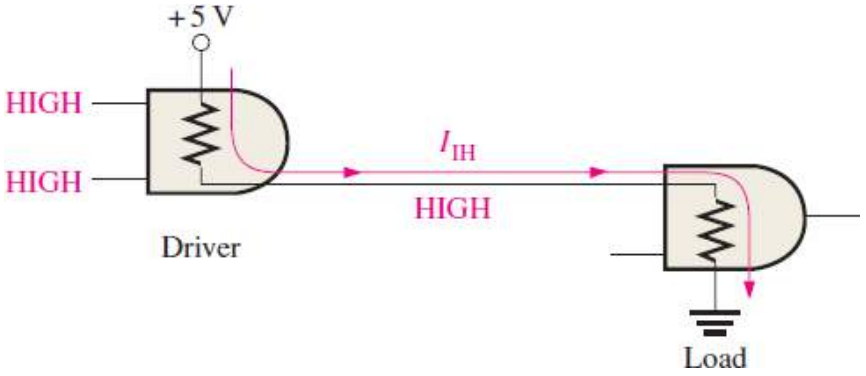
Fan-Out: The maximum number of logic input that the output of a gate can drive reliably without any unacceptable voltage degradation is called Fan-out. As in the case of Fan-in, delay increases with Fan-out as well.

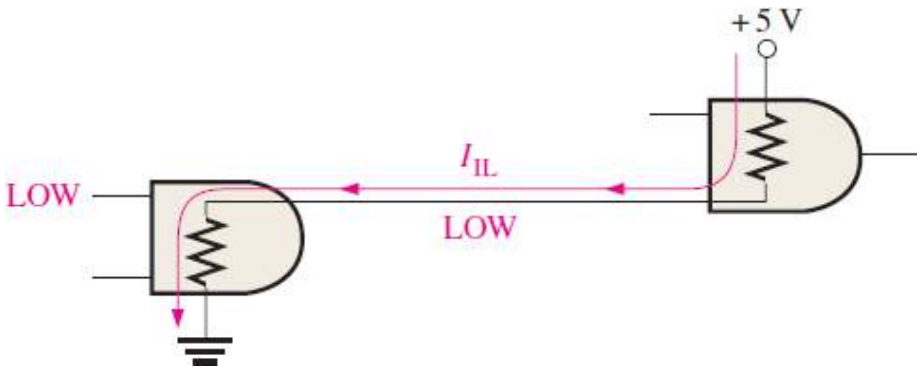
$$\mathbf{DC\ Fanout} = \mathbf{min}\left(\frac{\mathbf{I_{OH}}}{\mathbf{I_{IH}}}, \frac{\mathbf{I_{OL}}}{\mathbf{I_{IL}}}\right)$$



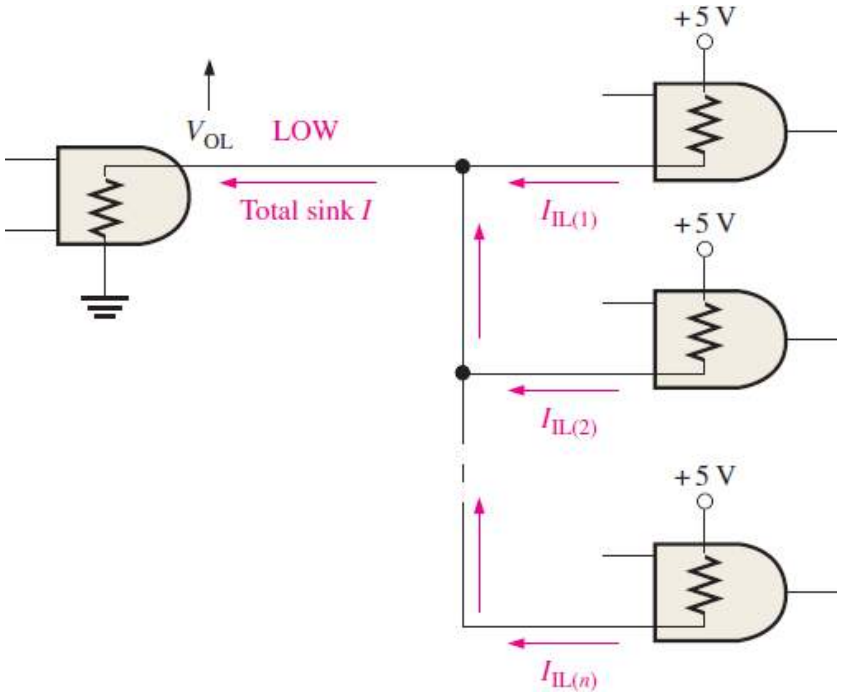
Performance Parameters of Logic Families

Loading and Fan Out: When the output of a gate is connected to the input of one or more gates, a load is created on the driver gate. There is a limit to the number of input that the output a gate can drive. This is determined by the fan-out.

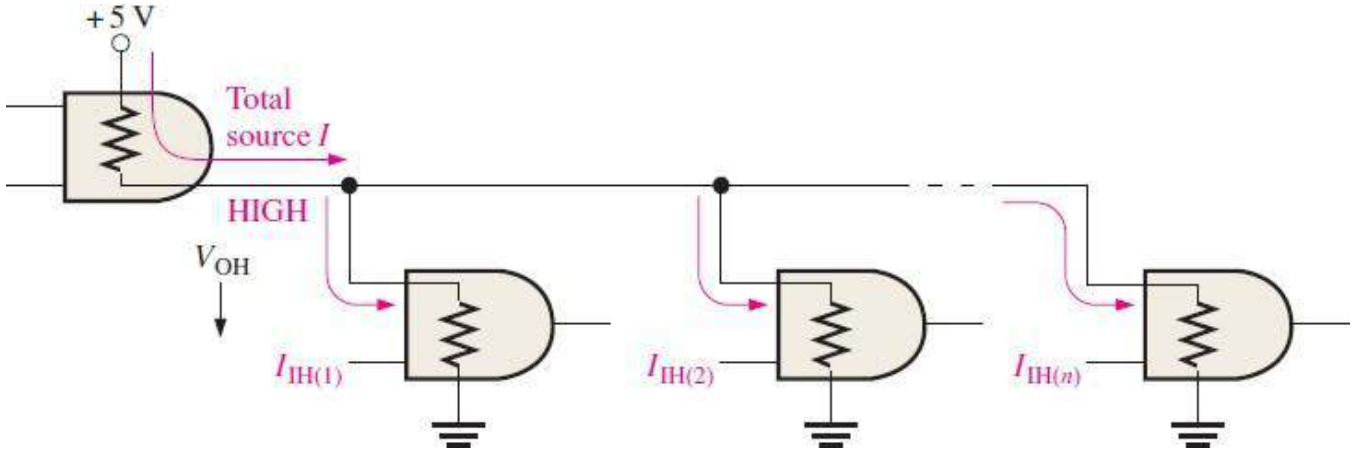




TTL loading in HIGH and LOW state



TTL loading in LOW state



TTL loading in HIGH state

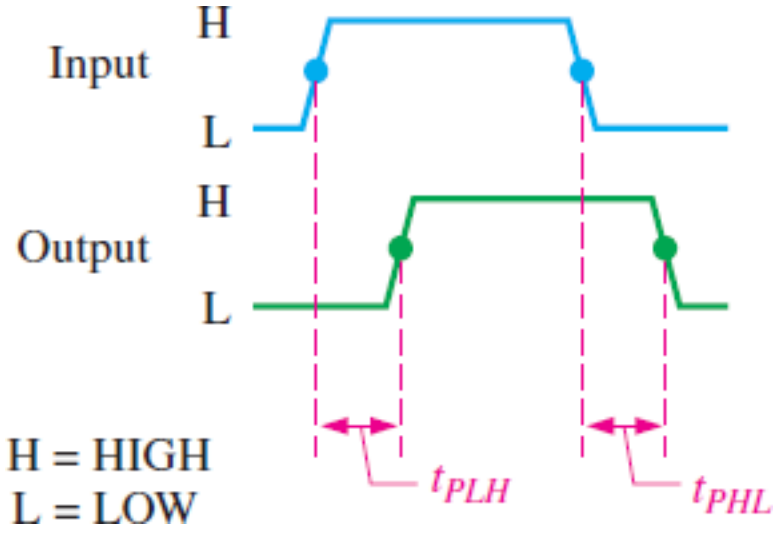
Performance Parameters of Logic Families

Propagation Delay: The time elapsed between 50% change in input wave-form to the 50% change in output wave-form.

T_{pHL}: Propagation delay for High to Low.

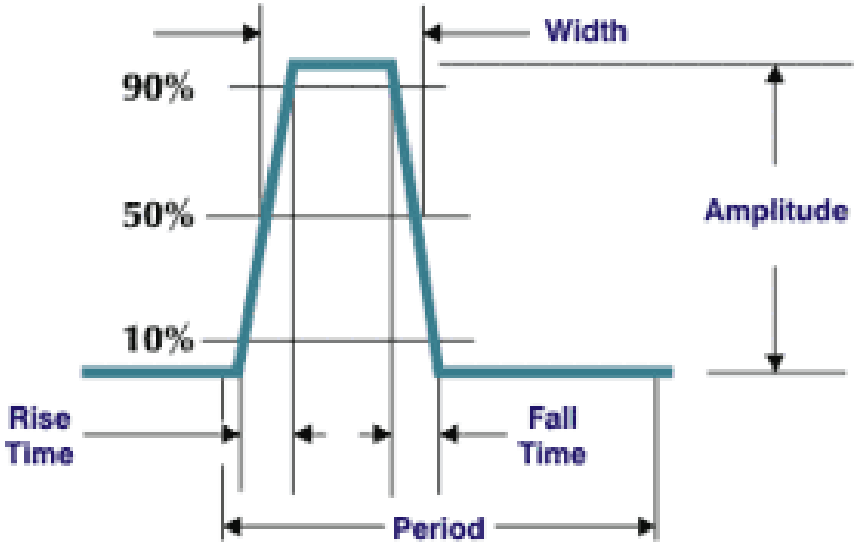
T_{pLH}: Propagation delay for Low to High.

$$t_{PD} = \frac{1}{2}(t_{PHL} + t_{PLH})$$



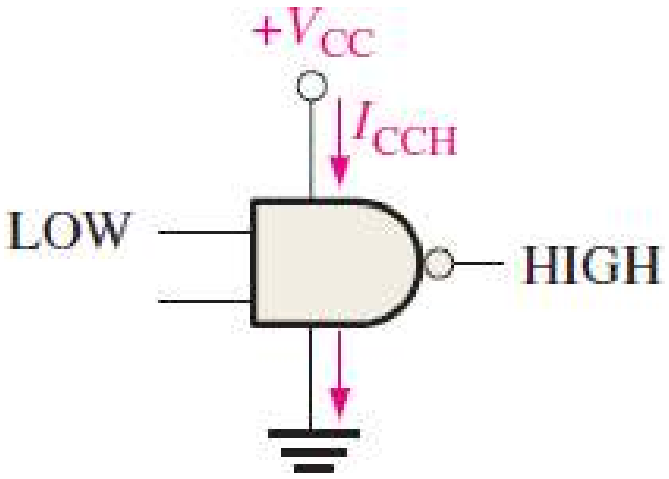
Time Rise, t_r: The time required for a logic to rise from 10% of its value to 90% of the value.

Time Fall, t_f: The time required for the logic to fall from 90% of its value to 10% of its value.



Performance Parameters of Logic Families

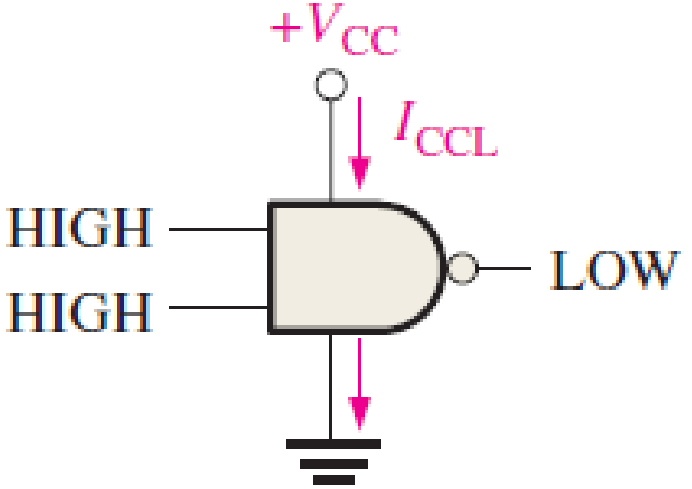
Power Dissipation: A gate draws in current both in HIGH and LOW states. Therefore, in both states a gate dissipates power. The current associated with HIGH state is named I_{CCH} and the current associated with LOW state is named I_{CCL}. Therefore,



Power Dissipation in HIGH state, $P_{DH} = V_{CC}I_{CCH}$
Power Dissipation in LOW state, $P_{DL} = V_{CC}I_{CCL}$

So the average power dissipated in a cycle with duty cycle of X%is,

$$\mathbf{PD} = \frac{(\mathbf{X} \times \mathbf{P_{DH}}) + \left((\mathbf{100} - \mathbf{X})\mathbf{P_{DL}}\right)}{\mathbf{100}}$$



- Find the average power dissipated for a NAND gate with $V_{CC} = 5V$, $I_{CCH} = 4mA$ and $I_{CCL} = 2mA$ when the duty cycle is:
  a) 40%
  b) 75%
  c) 100%
  d) 0%
  e) 25%

Performance Parameters of Logic Families

Speed Power Product: It is a very important parameter of comparison for logic circuit where both power dissipation and propagation delay are together needed to be considered. The speed power product and its significance can be understood from the following equation:

$$\mathbf{P_D = \frac{CV_{CC}V_L}{T_D}}$$

where C is the capacitance, V_{CC} is the common collector voltage, V_L is the logic swing of voltage and T_D is the propagation delay. We can rewrite this equation as,

$$\mathbf{P_D T_D = CV_{CC}V_L}$$

For a logic family, V_{CC}, C and V_L are all constant. Therefore, if we decrease power dissipation then propagation delay will increase and if we decrease propagation delay power dissipation will increase. Therefore, there will always be a trade-off between the two parameters. However, to decrease both we will need to change construction parameter.

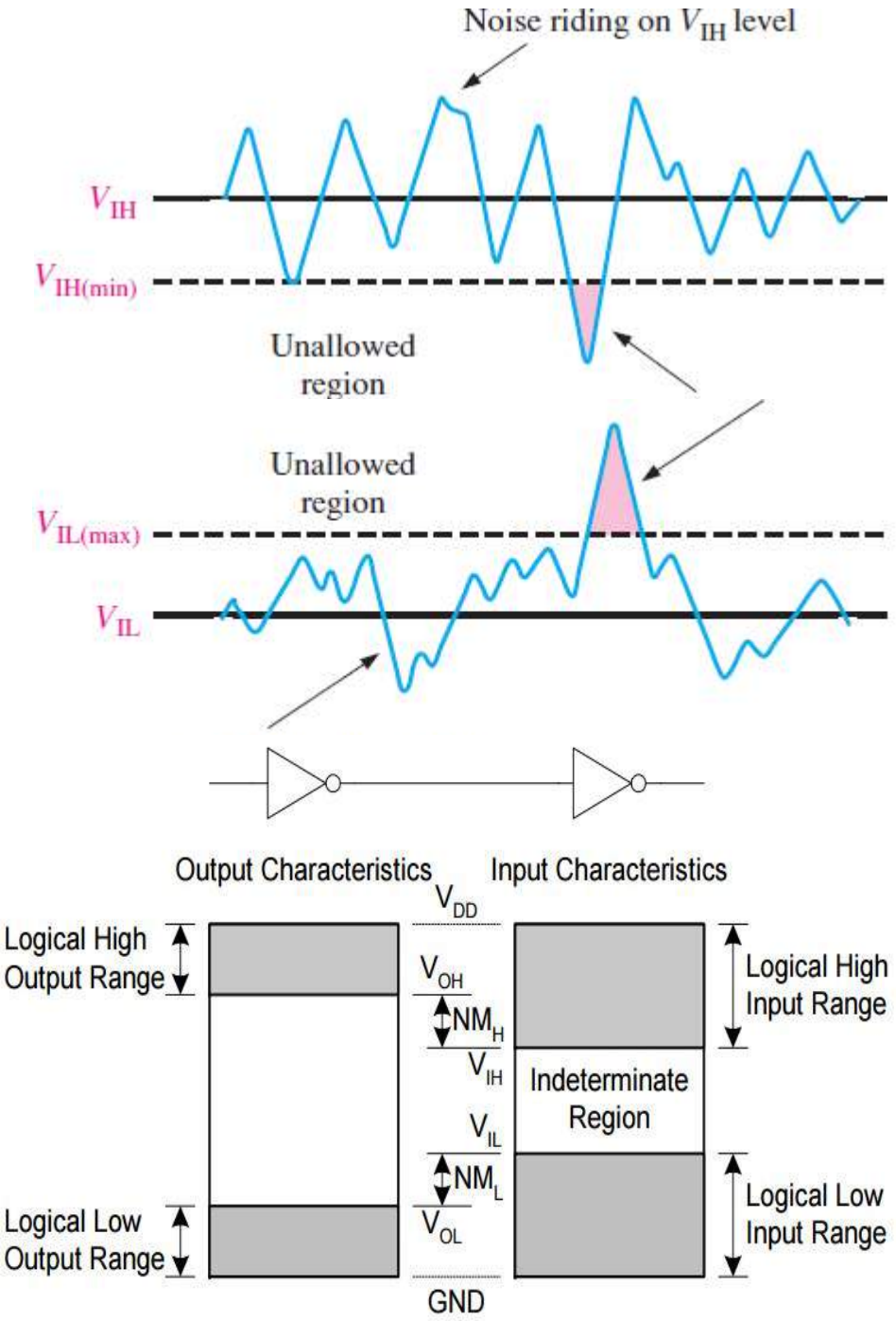
Performance Parameters of Logic Families

Noise Immunity: All electrical circuits are susceptible to noise. Noise is the presence of unwanted induced voltage in the electrical circuit. This unwanted induced voltage can disrupt the operation of a digital circuit. In order to not get adversely affected by noise the circuit should have some amount of noise immunity. Noise Immunity is the ability to tolerate unwanted voltage fluctuation.

Noise Margin: The amount of unwanted voltage a circuit can tolerate is measured by the noise margin. There are two noise margins: High Level Noise Margin and Low Level Noise Margin.

$$\mathbf{NM_L = V_{IL} - V_{OL}}$$

$$\mathbf{NM_H = V_{OH} - V_{IH}}$$



Digital Logic Families

Digital integrated circuits are classified not only by their complexity or logical operation, but also by the specific circuit technology to which they belong. The circuit technology is referred to as a digital logic family.

The basic circuit in each technology is a NAND, NOR, or an inverter gate.

The Logic Families are :

- RTL → Resistor-Transistor Logic
- DTL → Diode Transistor Logic
- I^2L → Integrated Injection Logic
- ECL → Emitter Collector Logic
- TTL → Transistor Transistor Logic
- MOS→ Metal Oxide Semiconductor
- CMOS → Complementary MOS

Special Characteristics

The characteristics of IC digital logic families are usually compared by analyzing the circuit of the basic gate in each family.
The most important parameters that are evaluated and compared are

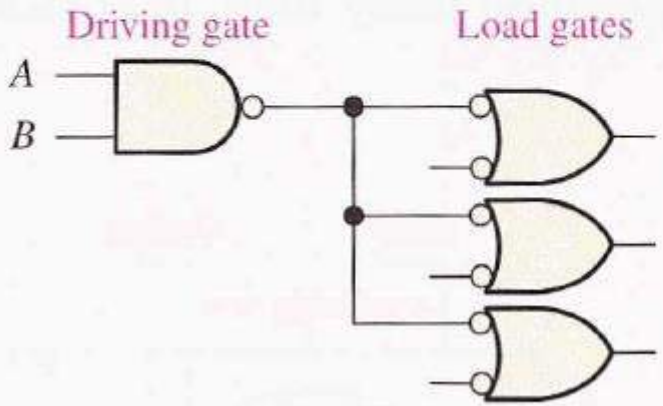
- Fan-Out
- Fan-In
- Power Dissipation
- Propagation Delay
- Speed-Power Product
- Noise Margin

Fan-Out

When the output of a logic gate is connected to one or more inputs of other gates, a load on the driving gate is created, as shown in Figure 1 . There is a limit to the number of load gate inputs that a given gate can drive. This limit is called the **fan-out** of the gate.

FIGURE 1

Loading a gate output with gate inputs.



Fan-Out

The fan-out of a gate specifies the number of standard loads that can be connected to the output of the gate without degrading its normal operation.
A standard load is usually defined as the amount of current needed by an input of another gate in the same logic family. Sometimes the term *loading* is used instead of fan-out.
This term is derived because the output of a gate can supply a limited amount of current, above which it ceases to operate properly and is said to be overloaded.
Each input consumes a certain amount of current from the gate output, so that each additional connection adds to the load of the gate.
Exceeding the specified maximum load may cause a malfunction because the circuit cannot supply the power demanded from it.
The fan-out is the maximum number of inputs that can be connected to the output of a gate, and is expressed by a number.

Fan-Out

- The fan-out of the gate is calculated from the ratio I_{OH}/I_{IH} or I_{OL} / I_{IL}
- For example, the standard TTL gates have the following values for the currents:

$$I_{OH} = 400\ \mu A$$

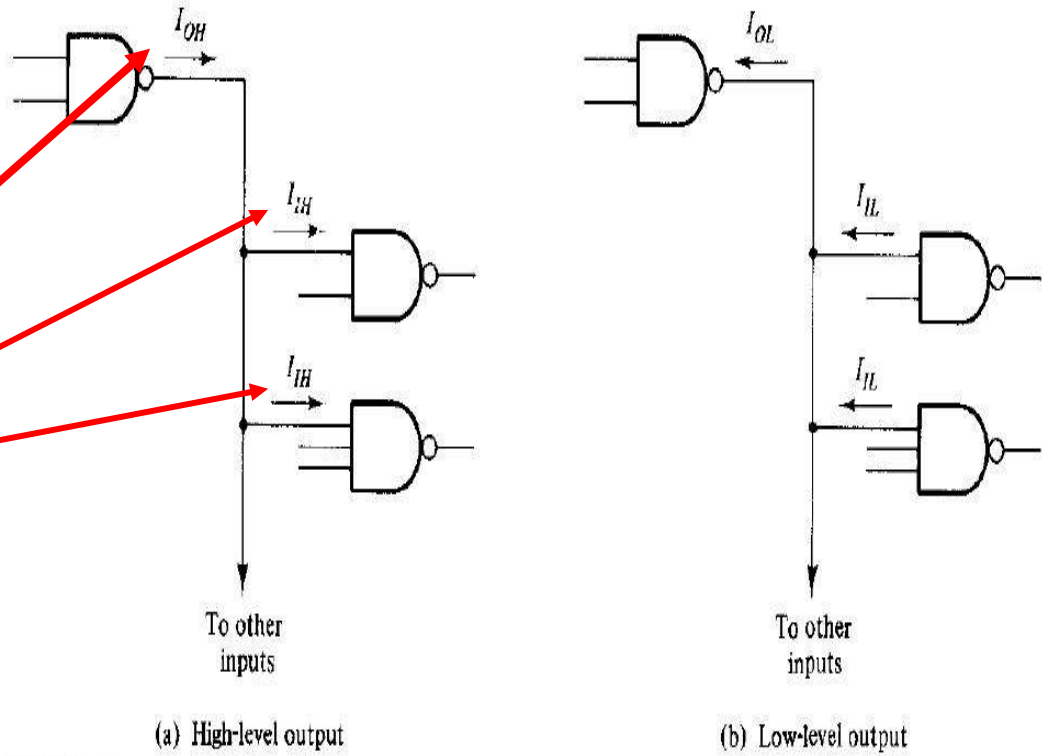
$$I_{IH} = 40\ \mu A$$

$$I_{OL} = 16\ mA$$

$$I_{IL} = 1.6\ mA$$

The two ratios give the same number in this case:

$$\frac{400\ \mu A}{40\ \mu A} = \frac{16\ mA}{1.6\ mA} = 10$$



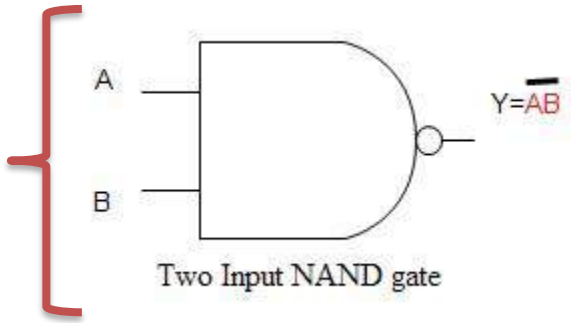
(a) High-level output (b) Low-level output

FIGURE 2
Fan-out computation

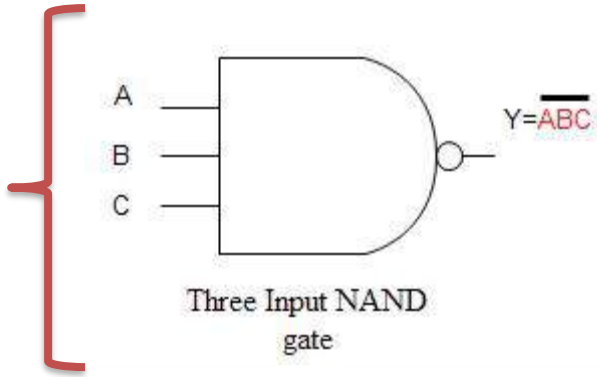
Fan-In

The fan in defined as the maximum number of inputs that a logic gate can accept.
If number of input exceeds, the output will be undefined or incorrect.
It is specified by manufacturer and is provided in the data sheet.

Fan In = 2



Fan In = 3



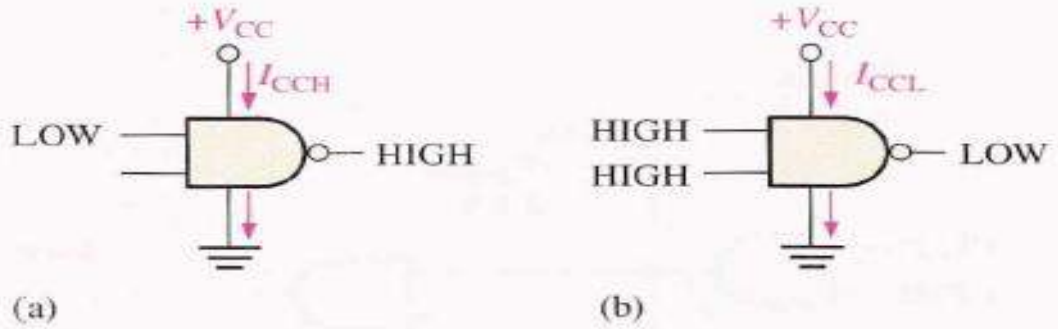
Power Dissipation

Power Dissipation

A logic gate draws current from the dc supply voltage source, as indicated in Figure 3. When the gate is in the HIGH output state, an amount of current designated by I_{CCH} is drawn; and in the LOW output state, a different amount of current, I_{CCL}, is drawn.

FIGURE 3

Currents from the dc supply. Conventional current direction is shown. Electron flow notation is opposite.



As an example, if I_{CCH} is specified as 1.5 mA when V_{CC} is 5 V and if the gate is in a static (nonchanging) HIGH output state, the **power dissipation** (P_D) of the gate is

$$P_D = V_{CC}I_{CCH} = (5\text{ V})(1.5\text{ mA}) = 7.5\text{ mW}$$

Power Dissipation

The power dissipation is a parameter expressed in milliwatts (mW) and represents the amount of power needed by the gate.
The number that represents this parameter does not include the power delivered from another gate; rather, it represents the power delivered to the gate from the power supply.
An IC with four gates will require, from its power supply, four times the power dissipated in each gate.
When gate is pulsed, its output switches back and forth between HIGH and Low, and the amount of supply current varies between I_{CCH} and $I_{CCL.}$ The average power dissipation depends on the duty cycle is 50%, the output is HIGH half the time and LOW the other half. The average Supply Current is Therefore:

$$I_{CC} = \frac{I_{CCH} + I_{CCL}}{2}$$

The average power dissipation is

$$P_D = V_{CC} I_{CC}$$

Power Dissipation

A certain gate draws 2 μA when its output is HIGH and 3.6 μA when its output is LOW. What is its average power dissipation if V_{CC} is 5 V and the gate is operated on a 50% duty cycle?

Solution The average I_{CC} is

$$I_{CC} = \frac{I_{CCH} + I_{CCL}}{2} = \frac{2.0\,\mu\text{A} + 3.6\,\mu\text{A}}{2} = 2.8\,\mu\text{A}$$

The average power dissipation is

$$P_D = V_{CC}I_{CC} = (5\text{ V})(2.8\,\mu\text{A}) = \mathbf{14\,\mu W}$$

Related Problem A certain IC gate has an $I_{CCH} = 1.5\,\mu$A and $I_{CCL} = 2.8\,\mu$A. Determine the average power dissipation for 70% duty cycle operation if V_{CC} is 5 V.

Propagation Delay

When a signal passes (propagates) through a logic circuit, it always experiences a time delay, as illustrated in Figure 4 . A change in the output level always occurs a short time, called the **propagation delay time,** later than the change in the input level that caused it.

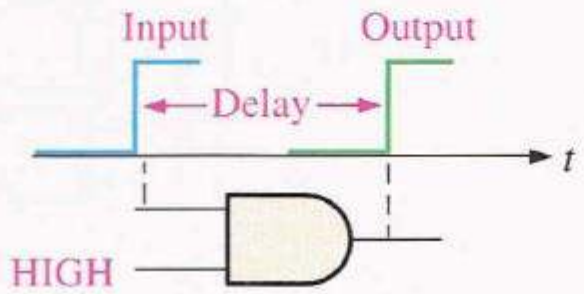


FIGURE 4

A basic illustration of propagation delay time.

Propagation Delay

- t_{PHL}: The time between a designated point on the input pulse and the corresponding point on the output pulse when the output is changing from HIGH to LOW.
- t_{PLH}: The time between a designated point on the input pulse and the corresponding point on the output pulse when the output is changing from LOW to HIGH.

These propagation delay times are illustrated in Figure **5** , with the 50% points on the pulse edges used as references.

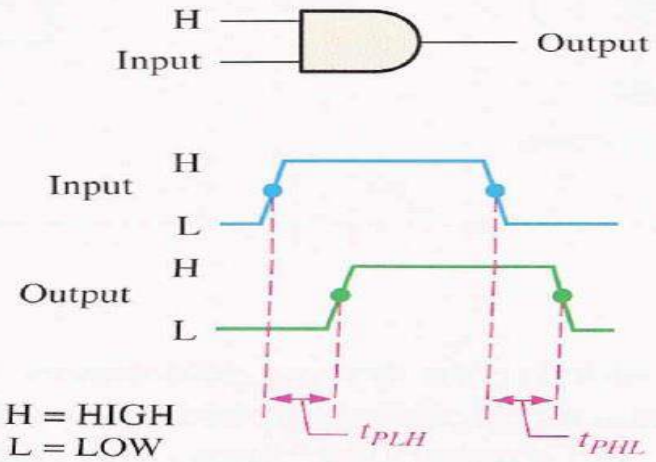


FIGURE 5
Propagation delay times.

Speed Power Product

The speed power product provides the basis for the comparison of logic circuits when both propagation delay time and power dissipation are important considerations in the selection of the type of logic to be used in a certain application.
The lower the speed-power the better.
The unit of speed-power product is Pico joule(pJ).

Speed-Power Product = Propagation Delay × Power Dissipation

Table lists parameters for three types of gates. Basing your decision on the speed-power product, which one would you select for best performance?

TABLE

	t_{PLH}	t_{PHL}	P_D
Gate *A*	1 ns	1.2 ns	15 mW
Gate *B*	5 ns	4 ns	8 mW
Gate *C*	10 ns	10 ns	0.5 mW

Noise Margin

Unwanted signals are referred to as *noise.*
There are two types of noise to be considered :

- **DC noise is** caused by a drift in the voltage levels of a signal.
- AC noise is a random pulse that may be created by other switching signals.

Noise margin is the maximum noise voltage added to an input signal of a digital circuit that does not cause an undesirable change in the circuit output.
Noise margin is expressed in volts and represents the maximum noise signal that can be tolerated by the gate.

Noise Margin

5. Voltage specifications for three types of logic gates are given in Table . Select the gate that you would use in a high-noise industrial environment.

	$V_{OH(MIN)}$	$V_{OL(MAX)}$	$V_{IH(MIN)}$	$V_{IL(MAX)}$
Gate *A*	2.4 V	0.4 V	2 V	0.8 V
Gate *B*	3.5 V	0.2 V	2.5 V	0.6 V
Gate *C*	4.2 V	0.2 V	3.2 V	0.8 V

Bipolar-transistor Characteristics

TABLE 10-1
Typical *npn* Silicon Transistor Parameters

Region	V_{BE} (V)*	V_{CE} (V)	Current Relationship
Cutoff	< 0.6	Open circuit	$I_B = I_C = 0$
Active	0.6–0.7	> 0.8	$I_C = h_{FE} I_B$
Saturation	0.7–0.8	0.2	$I_B \geq I_{CS}/h_{FE}$

*V_{BE} will be assumed to be 0.7 V if the transistor is conducting, whether in the active or saturation region.

References

1. Thomas L. Floyd, “Digital Fundamentals” 8th edition, Prentice Hall – Pearson Education.
2. M. Morris Mano, “Digital Logic & Computer Design” Prentice Hall