Lecture -8
Integrated Circuit Technology-2

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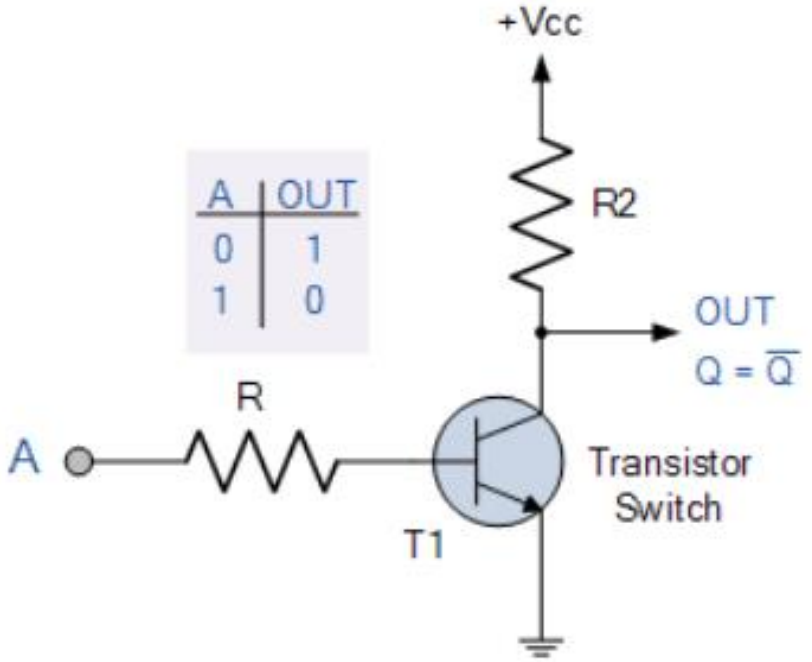
Resistor-Transistor Logic (RTL)

- It is the first the first logic family to have been commercially used but now it is obsolete.
- The basic circuit of the RTL digital logic family is the NOR gate.
- The voltage levels for the circuit are 0.2 V for the low level and from 1 to 3.6 V for the high level.
- The fan-out of the RTL gate is limited by the value of the output voltage when high.
- As the output is loaded with inputs of other gates, more current is consumed by the load.
- Any voltage below 1 V in the output may not drive the next transistor into saturation as required.
- The power dissipation of the RTL gate is about 12 mW.
- The propagation delay averages 25 ns.
- **Disadvantages of RTL Logic are as follows:**
  - It's relatively slow.
  - Low noise immunity and noise margin.
  - Low Fan-out (Approx. 3~5)
  - Expensive due to fabrication of resistor.
  - It can not operate above 4MHz.

NOT Gate Using RTL

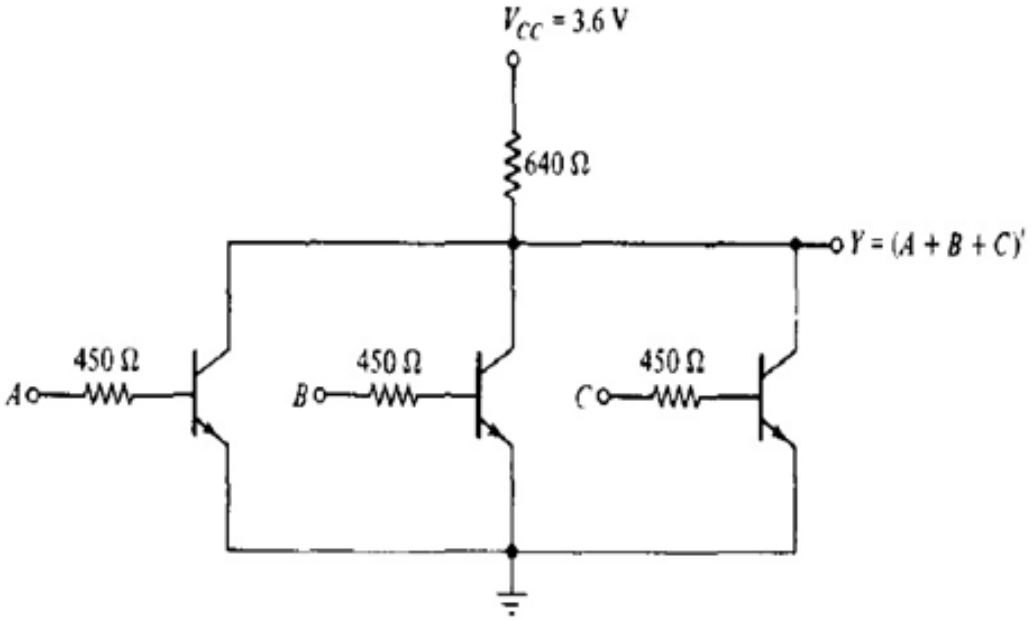
- The figure in the left shows an RTL NOT gate.
- The operation of the RTL gate is as follows:
  - When the input is LOW, the transistor T1 is at cutoff region. The output is $+V_{CC}$.
  - When the input is HIGH, the transistor T1 is ON and in saturation region. The output is LOW. The voltage across the output terminal is the saturation voltage 0.2V
  - The table below summarizes the operation.



Input	Transistor Status	Output
A=Low	T1=OFF, Cut-off Region	$Q=+V_{CC}$, High
A=High	T1=ON, Saturation Region	$Q=V_{CE(SAT)}=0.2V$, Low

NOR Gate Using RTL

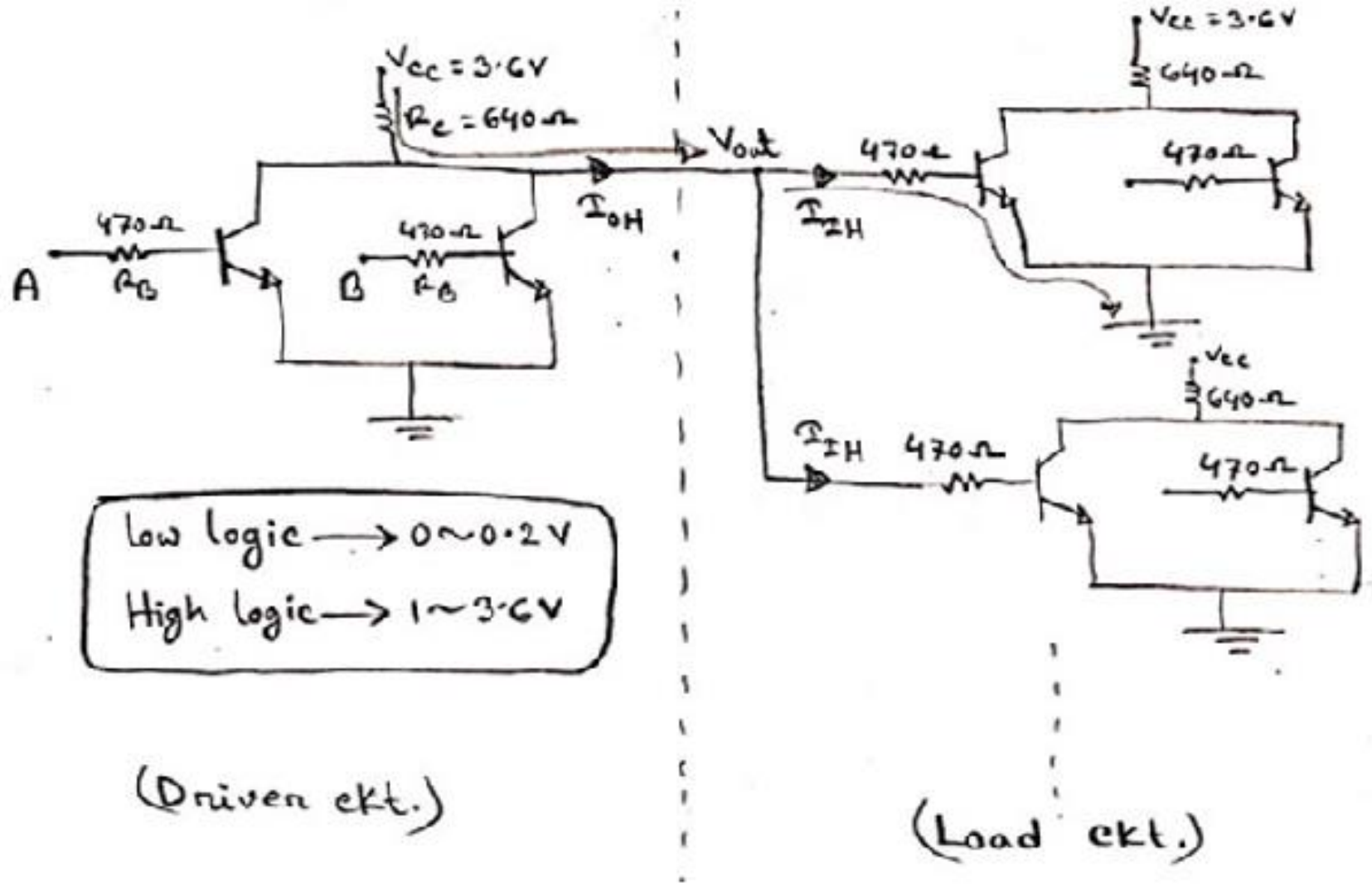
- If any input of the RTL gate is high, the corresponding transistor is driven into saturation. This causes the output to be low, regardless of the states of the other transistors.
- If all inputs are low at 0.2 V, all transistors are cut off because VBE < 0.6 V. This causes the output of the circuit to be high, approaching the value of supply voltage VCC.
- The table below summarizes the operation.



Input	Transistor Status	Output
All inputs are LOW	All transistors are OFF and in cutoff region	$Q = +V_{CC}$, High
Any one input/ Two input/ all inputs is HIGH	Corresponding transistor turns ON and is in saturated region	$Q = V_{CE(SAT)} = 0.2V$, Low

Fanout Calculation for RTL NOR

- For the given circuit calculate the Fan-out of RTL NOR ?



Fanout Calculation for RTL NOR

$$\text{Fan-out, } N = \frac{I_{OH}}{I_{IH}}$$

A	B	Y_{NOR}
0	0	1
0	1	0
1	0	0
1	1	0

KVL in driven ckt,

$$3.6 - 640 \times I_{OH} - 1 = 0$$

$$\Rightarrow I_{OH} = \frac{3.6-1}{640} = 0.00406\ A$$

KVL in load ckt,

$$1 - 470 \times I_{IH} - 0.7 = 0$$

$$\Rightarrow I_{IH} = \frac{1-0.7}{470} = 0.000638\ A$$

$$\therefore N = \frac{I_{OH}}{I_{IH}} = \frac{0.00406}{0.000638} = 6.36 \approx 6$$

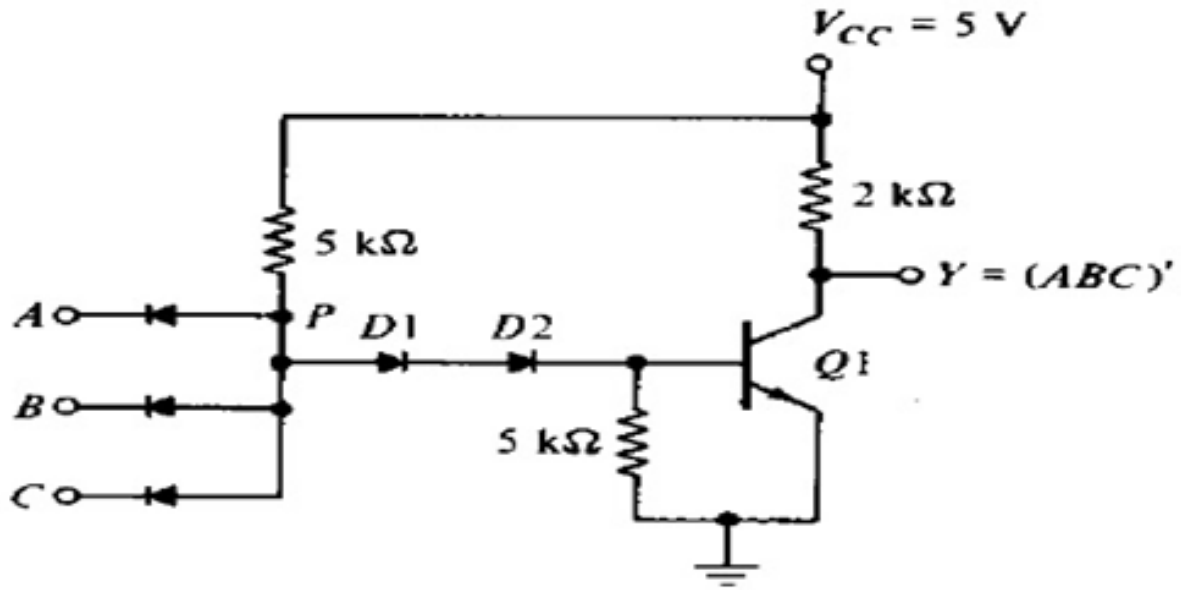
∴ Fan-out is 6.

Diode-Transistor Logic (DTL)

- It is currently an obsolete technology.
- The basic circuit in the DTL digital logic family is the NAND gate.
- Each input is associated with one diode.
- The diodes and the 5-kΩ resistor form an AND gate.
- The transistor serves as a current amplifier while inverting the digital signal.
- The two voltage levels are 0.2 V for the low level and between 4 and 5 V for the high level.
- The power dissipation of a DTL gate is about 12 mW.
- The propagation delay averages 30 ns.
- The noise margin is about I V and a fan-out as high as 8 is possible.
- **Disadvantages of DTL logic family are as follows:**
  - Relatively lower speed.
  - Propagation delay is higher than RTL.

NAND Gate Using DTL

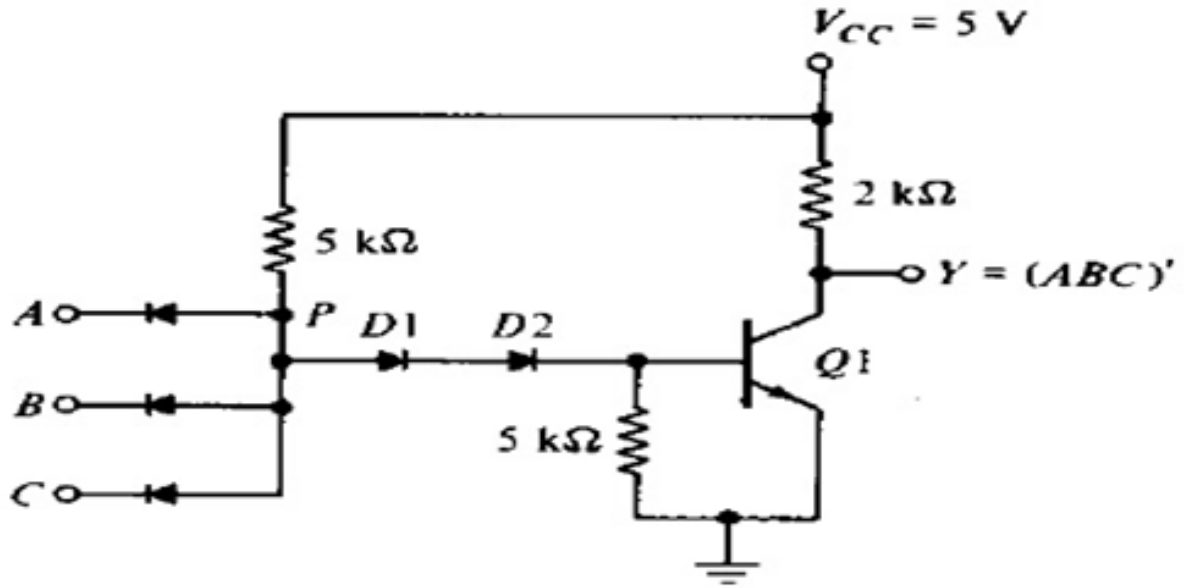
- If any input of the gate is low at 0.2 V, the corresponding input diode conducts current through Vcc and the 5-kΩ resistor into the input node.
- The voltage at point P is equal to the input voltage of 0.2 V plus a diode drop of 0.7 V, for a total of 0.9 V.
- For the transistor to start conducting, the voltage at point P must overcome a potential of one VBE drop in Q 1 plus two diode drops across D 1 and D 2, or 3 X 0.6 = 1.8 V.
- Since the voltage at P is maintained at 0.9 V by the input conducting diode, the transistor is cut off and the output voltage is high at 5 V.



NAND Gate Using DTL

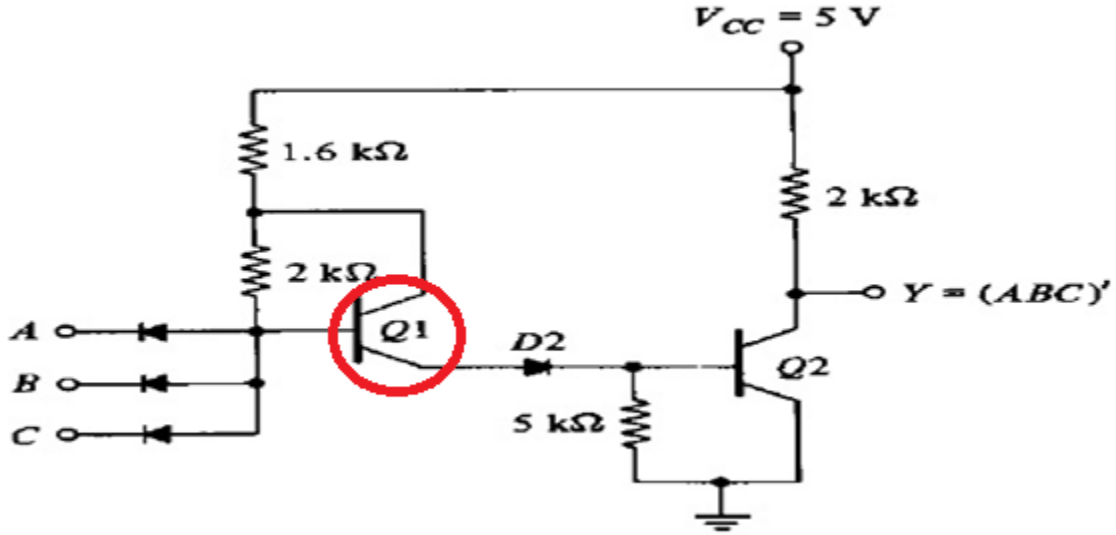
- If all inputs of the gate are high, the transistor is driven into the saturation region.
- The voltage at P now is equal to V_{BE} plus the two diode drops across D I and D 2, or 0.7 x 3 = 2.1 V.
- Since all inputs are high at 5 V and $V_P = 2.1$ V, the input diodes are reverse biased and off.
- The base current is equal to the difference of currents flowing in the two 5-kΩ resistors and is sufficient to drive the transistor into saturation.
- With the transistor saturated, the output drops to VCE of 0.2 V, which is the low level for the gate.

Input	Transistor and Diode Status	Output
Any input is Low (0.2 V)	Corresponding input diode is forward biased. Q1 is off and in cutoff region. $V_P = (0.2 + 0.7)V$	Y=+V_{CC}, High
All inputs are High (5V)	All input diode is reverse biased. D1 & D2 is forward biased. Q1 is ON and in saturation region.	Y=$V_{CE(SAT)}$=0.2V, Low



NAND Gate Using Modified DTL

- The fan-out of the DTL gate is limited by the maximum current that can flow in the collector of the saturated transistor.
- The fan-out of a DTL gate may be increased by replacing one of the diodes in the base circuit with a transistor.



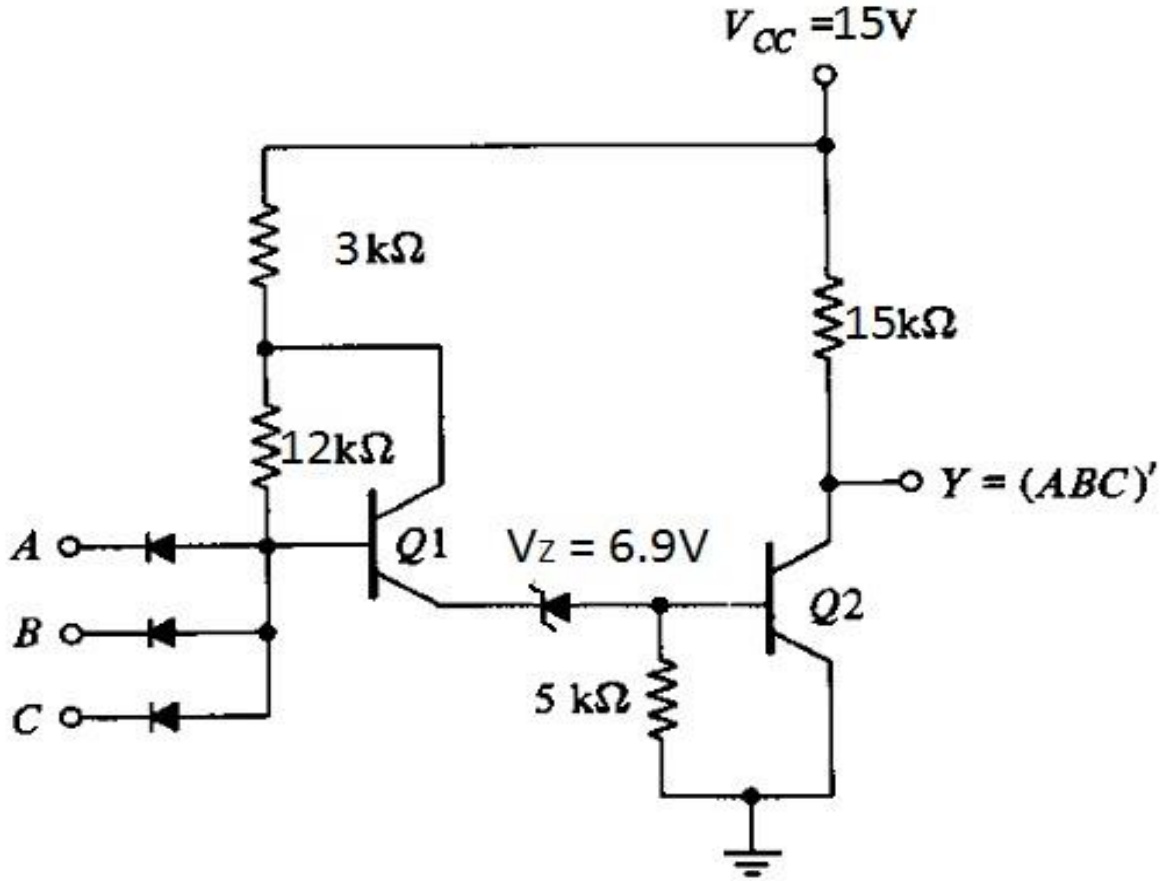
- Transistor Q1 is maintained in the **active region** when output transistor Q2 is **saturated**.
- Therefore, the modified circuit can supply a larger amount of base current to the output transistor.
- The output transistor can now draw a larger amount of collector current before it goes out of saturation.
- Part of the collector current comes from the conducting diodes in the loading gates when Q 2 is saturated.
- Thus, an increase in allowable collector saturated current allows more loads to be connected to the output, which increases the fan-out capability of the gate.

NAND Gate Using HTL

- Due to presence of electrical motor's on-off control circuits, High voltage switches etc. are used in industrial environment, Thereby noise level is very high.
- So DTL redesigned with a power supply of 15V and the D2 is replaced by a Zener diode with a breakdown voltage of 6.9 V.
- So HTL posses a high threshold of noise immunity.
- To conduct Q2, the emitter of Q1 must rise to a potential,

$$V_{BE}\,(Q2) + V_Z = 0.7 + 6.9 = 7.6\,V$$

- So, Only if the noise signal is greater than 7.6 V , then it will be able to change the state. Higher noise immunity.



Transistor-Transistor Logic

- The original basic TTL gate was a slight improvement over the DTL gate.
- As the TTL technology progressed, additional improvements were added to the point where this logic family became the most widely used family in the design of digital systems.
- The propagation delay of a transistor circuit that goes into saturation depends mostly on two factors: storage time and *RC* time constants.
- Reducing the storage time decreases the propagation delay. [RC T_P]
- Reducing resistor values in the circuit reduces the *RC* time constants and decreases the propagation delay.
- Of course, the trade-off is higher power dissipation because lower resistances draw more current from the power supply. The speed of the gate is inversely proportional to the propagation delay.
- In the low-power TTL gate, the resistor values are higher than in the standard gate to reduce the power dissipation, but the propagation delay is increased. [R↑ so P_D↓ but T_P↑]
- In the high-speed TTL gate, resistor values are lowered to reduce the propagation delay, but the power dissipation is increased. . [R↓ so T_P↓ but P_D↑]

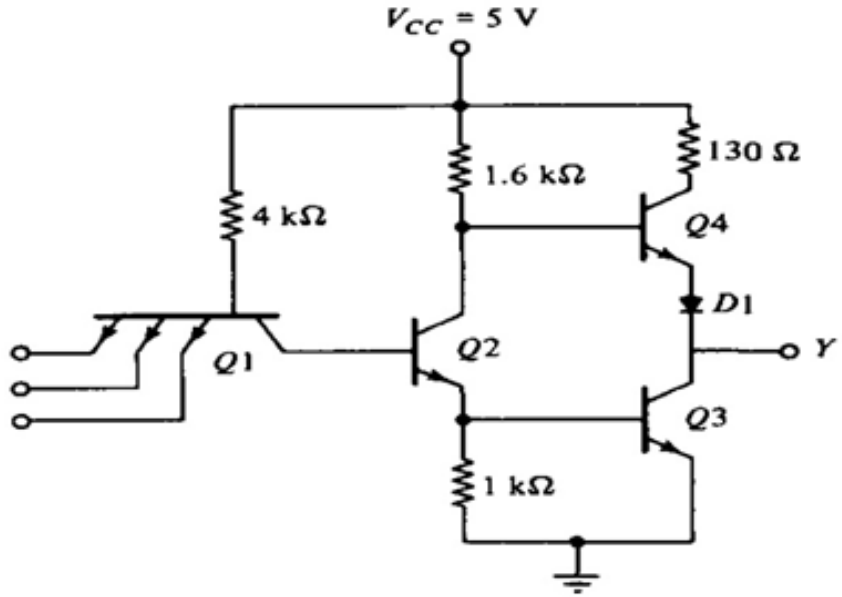
Transistor-Transistor Logic

- The Schottky TTL gate was the next improvement in the technology.
- The effect of the Schottky transistor is to remove the storage time delay by preventing the transistor from going into saturation.
- The low-power Schottky TTL sacrifices some speed for reduced power dissipation.
- It is equal to the standard TTL in propagation delay, but has only one fifth the power dissipation
- Recent innovations have led to the development of the advanced Schottky series.
- The advanced low-power Schottky has the lowest speed-power product and is the most efficient series. It is replacing all other low· power versions in new designs.
- TTL gates in all the available series come in three different types of output configuration:

1. **Open -collector output**
2. **Totem-pole output**
3. **Three-state (or tristate) output**

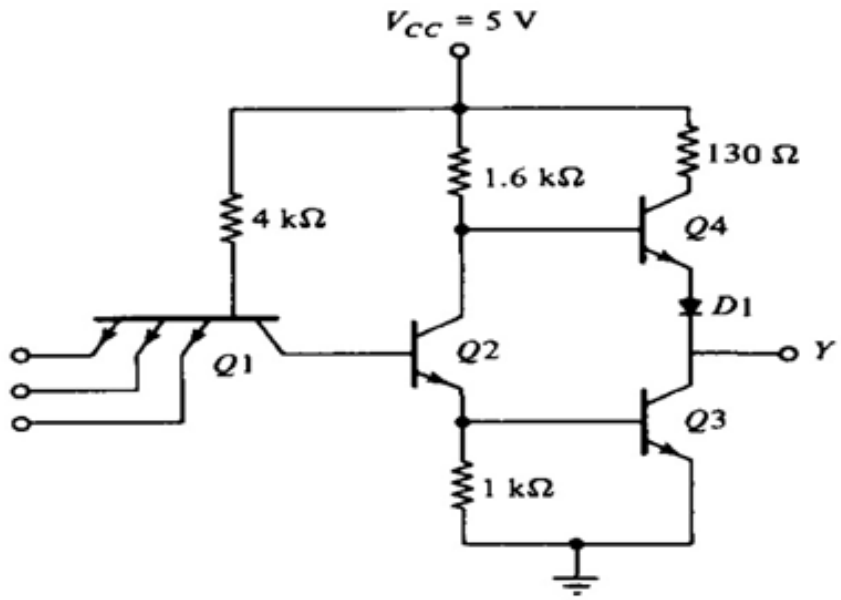
TTL with Totem Pole

- The output impedance of a gate is normally a resistive plus a capacitive load.
- The capacitive load consists of the capacitance of the output transistor, the capacitance of the fan-out gates, and any stray wiring capacitance.
- When the output changes from the low to the high state, the output transistor of the gate goes from saturation to cutoff and the total load capacitance, C, charges exponentially from the low to the high voltage level with a time constant equal to RC.
- For the open-collector gate, R is the external resistor marked RL.
- Typical operating value C = 15 pF and RL = 4 kΩ. Propagation delay, tP = 35ns.
- With an active pull-up circuit replacing the passive pull-up resistor RL , the propagation delay is reduced to 10 ns.



NAND using TTL with Totem Pole

Input	Transistor and Diode Status	Output
Any input is Low (0.2 V)	• Corresponding BE junction of Q1 is forward biased. • Voltage at the base of Q1 is: $0.2V + 0.7V = 0.9V$ • Q2 and Q3 is in cutoff region. • Q4 is ON and in D1 is in forward bias.	Y= High
All inputs are High (5V)	• All BE junctions of Q1 is revered biased. • Potential at base of Q1 is 2.1V. • Q2 and Q3 are in saturation region. • Q4 is in cutoff region.	$Y=V_{CE(SAT)}=0.2V$, Low



- The reason for placing the diode in the circuit is to provide a diode drop in the output path and thus ensure that Q4 is cut off when Q3 is saturated.
- For Q3 to start conducting, the path from Q1 to Q3 must be overcame.
- One diode drop in B-C junction of Q1 + two VBE drop in Q2 & Q3 = 3 × 0.7 = 2.1 V
- To conduct Q4, base voltage must have = 0.7 (VBE of Q4)+ 0.7 (D1) = 1.4 V.

NAND using TTL with Totem Pole

Advantage of totem pole output:

- When the output changes to the high state because one of the inputs drops to the low state, transistors Q2 and Q3 go into cutoff. However, the output remains momentarily low because the voltages across the load capacitance cannot change instantaneously.
- The current needed to charge the load capacitance causes Q4 to momentarily saturate, and the output voltage rises with a time constant RC.
- But R in this case is equal to 130Ω, plus the saturation resistance of Q4, plus the resistance of the diode, for a total of approximately 150Ω.
- This value of R is much smaller than the passive pull-up resistance used in the open-collector circuit.
- Therefore, the transition from the low to high level is much faster.

References

1. Thomas L. Floyd, “Digital Fundamentals” 11th edition, Prentice Hall – Pearson Education.

Thank You