**Title**: Design of a Digital to Analog and Analog to Digital Converters.

**Part I: Design of a Digital to Analog Converter**

# Introduction:

This lab describes the design of a Digital to Analog Converter (DAC). Two types of design are shown in this lab, binary weighted DAC and R/2R ladder DAC design. Finally student will compare both the design to conclude which design is efficient and why.

# Theory and Methodology:

One common requirement in electronics is to convert signals back and forth between analog and digital forms. Most such conversions are ultimately based on a *digital-to- analog converter* circuit. Therefore, it is worth exploring just how we can convert a digital number that represents a voltage value into an actual analog voltage.

# Digital-to-Analog Converters

In [electronics,](http://en.wikipedia.org/wiki/Electronics) a digital-to-analog converter (DAC, D/A, D2A or D-to-A) is a function that converts digital data (usually binary) into an [analog signal](http://en.wikipedia.org/wiki/Analog_signal) [(current,](http://en.wikipedia.org/wiki/Analog_signal) [voltage,](http://en.wikipedia.org/wiki/Voltage) or [electric](http://en.wikipedia.org/wiki/Electric_charge) [charge).](http://en.wikipedia.org/wiki/Electric_charge) An [analog-to-digital converter](http://en.wikipedia.org/wiki/Analog-to-digital_converter) (ADC) performs the reverse function. Unlike analog signals, [Digital data](http://en.wikipedia.org/wiki/Digital_data) can be transmitted, manipulated, and stored without degradation, albeit with more complex equipment. But a DAC is needed to convert the digital signal to analog, for example to drive an earphone or loudspeaker amplifier and produce sound (analog air pressure waves).

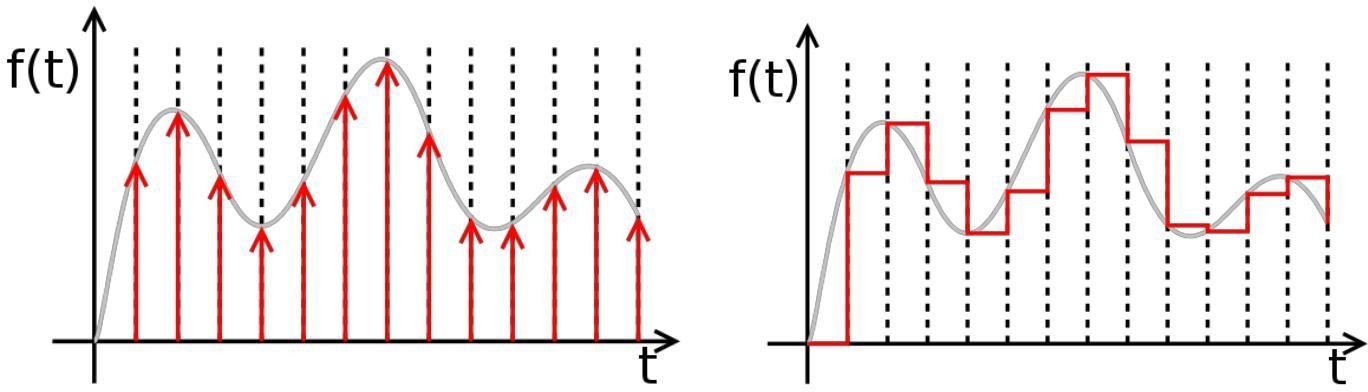
DACs and their inverse, ADCs, are part of an enabling technology that has contributed greatly to the 'digital revolution'. To illustrate this, consider a typical long-distance telephone call. The callers voice is converted into an analog electrical signal by a microphone. The analog signal

is then converted to a digital stream by an ADC. That digital stream is then divided into packets where it will be mixed with other digital data, not necessarily audio. The digital packets are then sent to the destination, but each packet may take a completely different route and may not even arrive at the destination in the correct time order. The digital voice data is then extracted from the packets and assembled into a digital data stream. A DAC converts it into an analog

electrical signal which drives an audio amplifier which in turn drives a loudspeaker which finally produces sound. Of course, this is a simplified and stylized description, but it does illustrate one vital role of ADCs and DACs.

There are several DAC [architectures;](http://en.wikipedia.org/wiki/Hardware_architecture) the suitability of a DAC for a particular application is determined by six main parameters: physical size, power consumption, [resolution,](http://en.wikipedia.org/wiki/Resolution_%28audio%29) speed, accuracy, cost. Due to the complexity and the need for precisely matched [components,](http://en.wikipedia.org/wiki/Electronic_components) all but the most specialist DACs are implemented as [integrated circuits](http://en.wikipedia.org/wiki/Integrated_circuits) (ICs). Digital-to-analog conversion can degrade a signal, so a DAC should be specified that that has insignificant errors in terms of the application.

DACs are commonly used in [music players](http://en.wikipedia.org/wiki/Digital_audio_player) to convert digital data streams into analogue audio signals. They are also used in [televisions](http://en.wikipedia.org/wiki/Television) and [mobile phones](http://en.wikipedia.org/wiki/Mobile_phone) to convert digital video data into analog video signals which connect to the screen drivers to display monochrome or color images. These two applications use DACs at opposite ends of the speed/resolution trade-off. The audio DAC is a low speed high resolution type while the video DAC is a high speed low to medium resolution type. Discrete DACs would typically be extremely high speed low resolution power hungry types, as used in military radar systems. Very high speed test equipment, especially sampling oscilloscopes, may also use discrete DACS.



|  |  |  |
| --- | --- | --- |
| Ideally sampled signal |  | Piecewise constant output of an |
|  |  | idealized DAC lacking a |
|  |  | [reconstruction filter.](http://en.wikipedia.org/wiki/Reconstruction_filter) In a practical |
|  |  | DAC, a filter or the finite |
|  |  | bandwidth of the device smoothes |
|  |  | out the step response into a |
|  |  | continuous curve. |

A digital-to-analog converter, or DAC for short, converts a digitally coded number to a voltage proportional to the number. For example, if a number N is supplied to a DAC, the output voltage will be proportional to N: Vout = N × B The constant of proportionality, B, is normally determined from the ratio of the reference voltage, Vref, and the maximum value that N can have, Nmax, B = Vref / Nmax so that Vout = Vref N / Nmax A common way to make a DAC is with an OpAmp circuit. Recall the circuit for the summing amplifier.

# Binary Weighted Digital-to-Analog Converter:

A diagram of a circuit

Description automatically generatedThe following circuit is a basic digital-to-analog (D to A) converter. It assumes a 4-bit binary number in Binary-Coded Decimal (BCD) format, using +5 volts as a logic 1 and 0 volts as a logic 0. It will convert the applied BCD number to a matching (inverted) output voltage. The digits 1, 2, 4, and 8 refer to the relative weights assigned to each input. Thus, 1 is the Least Significant Bit (LSB) of the input binary number, and 8 is the Most Significant Bit (MSB).

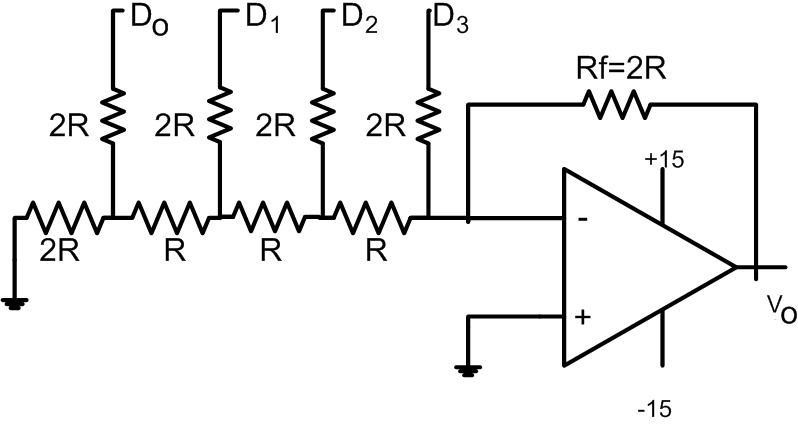
**Fig1:** Binary Weighted Digital to Analog converter.

If the input voltages are accurately 0 and +5 volts, then the "1" input will cause an output voltage of -5 × (4k/20k) = -5 × (1/5) = -1 volt whenever it is a logic 1. Similarly, the "2," "4," and "8" inputs will control output voltages of -2, -4, and -8 volts, respectively. As a result, the output voltage will take on one of 10 specific voltages, in accordance with the input BCD code.

Unfortunately, there are several practical problems with this circuit. First, most digital logic gates do not accurately produce 0 and +5 volts at their outputs. Therefore, the resulting analog voltages will be close, but not really accurate. In addition, the different input resistors will load the digital circuit outputs differently, which will almost certainly result in different voltages being applied to the summer inputs.

# R/2R Ladder Digital-to-Analog Converter:

This improved circuit overcomes the problem of using many resistors. Instead it uses only two valued resistor.



**Fig 2:** R/2R Ladder DAC

The circuit above performs D to A conversion a little differently. Typically the inputs are driven by CMOS gates, which have low but equal resistance for both logic 0 and logic 1. Also, if we use the same logic levels, CMOS gates really do provide +5 and 0 volts for their logic levels.

The input circuit is a remarkable design, known as an R-2R ladder network. It has several advantages over the basic summer circuit we saw first:

1. Only two resistance values are used anywhere in the entire circuit. This means that only two values of precision resistance are needed, in a resistance ratio of 2:1. This requirement is easy to meet, and not especially expensive.
2. The input resistance seen by each digital input is the same as for every other input. The actual impedance seen by each digital source gate is 3R. With a CMOS gate resistance of 200 ohms, we can use the very standard values of 10k and 20k for our resistors.
3. The circuit is indefinitely extensible for binary numbers. Thus, if we use binary inputs instead of BCD, we can simply double the length of the ladder network for an 8-bit number (0 to 255) or double it again for a 16-bit number (0 to 65535). We only need to add two resistors for each additional binary input.
4. The circuit lends itself to a non-inverting circuit configuration. Therefore we need not be concerned about intermediate inverters along the way. However, an inverting version can easily be configured if that is appropriate.

# Apparatus:

|  |  |  |
| --- | --- | --- |
| 1) | IC741 OPAMP | 1[pcs] |
| 2) | Resistors as required. | 14[pcs] |
| 3) | Oscilloscope. |  |

Simulation and Results:

Binary Weighted Digital to Analog converter

A diagram of a circuit

Description automatically generated

|  |  |
| --- | --- |
| SIMULATION | |
| A computer screen shot of a diagram  Description automatically generated  D3 = 0, D2 = 0, D1 = 0, D0 = 0, Vout = 3.05 mv | A computer screen shot of a diagram  Description automatically generated  D3 = 0, D2 = 0, D1 = 0, D0 = 1, Vout = -621.94 mv |
| A computer screen shot of a diagram  Description automatically generated    D3 = 0, D2 = 0, D1 = 1, D0 = 0, Vout = -1.247 v | A computer screen shot of a diagram  Description automatically generated  D3 = 0, D2 = 0, D1 = 1, D0 = 1, Vout = -1.872 v |

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| --- | --- |
| SIMULATION | |
| A computer screen shot of a diagram  Description automatically generated  D3 = 0, D2 = 1, D1 = 0, D0 = 0, Vout = -2.497 V | A computer screen shot of a diagram  Description automatically generated  D3 = 0, D2 = 1, D1 = 0, D0 = 1, Vout = -3.122 V |
| A computer screen shot of a diagram  Description automatically generated  D3 = 0, D2 = 1, D1 = 1, D0 = 0, Vout = - 3.747 V | A computer screen shot of a diagram  Description automatically generated  D3 = 0, D2 = 1, D1 = 1, D0 = 1, Vout = - 4.37 V |
| A computer screen shot of a diagram  Description automatically generated  D3 = 1, D2 = 0, D1 = 0, D0 = 0, Vout = - 4.987 V  A computer screen shot of a diagram  Description automatically generated  D3 = 1, D2 = 0, D1 = 1, D0 = 0, Vout = - 6.027 V | A computer screen shot of a diagram  Description automatically generated  D3 = 1, D2 = 0, D1 = 0, D0 = 1, Vout = -5.568 V  A computer screen shot of a diagram  Description automatically generated  D3 = 1, D2 = 0, D1 = 1, D0 = 1, Vout = - 6.032 V |
| A computer screen shot of a diagram  Description automatically generated  D3 = 1, D2 = 1, D1 = 0, D0 = 0, Vout = -5.902 V | A computer screen shot of a diagram  Description automatically generated  D3 = 1, D2 = 1, D1 = 0, D0 = 1, Vout = - 5.771 V |
| A computer screen shot of a diagram  Description automatically generated  D3 = 1, D2 = 1, D1 = 1, D0 = 0, Vout = - 5.64 V | A computer screen shot of a diagram  Description automatically generated  D3 = 1, D2 = 1, D1 = 1, D0 = 1, Vout = - 5.509 V |

A circuit board with wires and switches

Description automatically generated HARDWARE PICTURE

D3 = 1, D2 = 0, D1 = 0, D0 = 1, Vout = - 5.64 V (from the table below)

A sheet of paper with numbers and a number

Description automatically generated

Table – 1 : Values obtained from Hardware Measurement

Graphs(Simulation vs Hardware)

A graph with numbers and steps

Description automatically generated

R/2R Ladder DAC

A diagram of a ladder dac

Description automatically generated

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| --- | --- |
| SIMULATION | |
| A computer screen shot of a diagram  Description automatically generated  D3 = 0, D2 = 0, D1 = 0, D0 = 0, Vout = 2.14 mv | A computer screen shot of a computer program  Description automatically generated    D3 = 0, D2 = 0, D1 = 0, D0 = 1, Vout = - 310.356 mV |
| A computer screen shot of a computer program  Description automatically generated    D3 = 0, D2 = 0, D1 = 1, D0 = 0, Vout = - 622.851 mV | A computer screen shot of a computer  Description automatically generated  D3 = 0, D2 = 0, D1 = 1, D0 = 1, Vout = - 935.345 mV |

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| --- | --- |
| SIMULATION | |
| A computer screen shot of a computer  Description automatically generated  D3 = 0, D2 = 1, D1 = 0, D0 = 0, Vout = - 1.248 V | A computer screen shot of a computer  Description automatically generated  D3 = 0, D2 = 1, D1 = 0, D0 = 1, Vout = - 1.56 V |
| A computer screen shot of a diagram  Description automatically generated  D3 = 0, D2 = 1, D1 = 1, D0 = 0, Vout = - 1.873 V | A computer screen shot of a computer program  Description automatically generated  D3 = 0, D2 = 1, D1 = 1, D0 = 1, Vout = - 2.185 V |
| A computer screen shot of a computer  Description automatically generated    D3 = 1, D2 = 0, D1 = 0, D0 = 0, Vout = - 2.497 V | A computer screen shot of a computer  Description automatically generated  D3 = 1, D2 = 0, D1 = 0, D0 = 1, Vout = - 2.809 V |
| A computer screen shot of a computer  Description automatically generated  D3 = 1, D2 = 0, D1 = 1, D0 = 0, Vout = - 3.12 V | A computer screen shot of a computer  Description automatically generated  D3 = 1, D2 = 0, D1 = 1, D0 = 1, Vout = - 3.429 V |
| A computer screen shot of a computer  Description automatically generated  D3 = 1, D2 = 1, D1 = 0, D0 = 0, Vout = - 3.733 V | A computer screen shot of a computer  Description automatically generated  D3 = 1, D2 = 1, D1 = 0, D0 = 1, Vout = - 4.027 V |
| A computer screen shot of a computer  Description automatically generated    D3 = 1, D2 = 1, D1 = 1, D0 = 0, Vout = - 4.301 V | A computer screen shot of a computer  Description automatically generated  D3 = 1, D2 = 1, D1 = 1, D0 = 1, Vout = - 4.532 V |

HARDWARE PICTURE

A electronic device with wires and wires

Description automatically generated

D3 = 0, D2 = 1, D1 = 0, D0 = 0, Vout = - 5.64 V (from the table below)

A diagram of a circuit

Description automatically generated

Table – 2 : Values obtained from Hardware Measurement

Graphs(Simulation vs Hardware)

A graph with numbers and lines

Description automatically generated

**Questions for report writing:**

1. Why R/2R Ladder Digital-to-Analog Converter is preferable than Binary weighted Digital-to-Analog Converter.

Answer:

The R/2R ladder digital-to-analog converter (DAC) is often preferable to the binary weighted DAC due to its inherent simplicity and better manufacturing tolerances. In the R/2R ladder DAC, only two resistor values, R and 2R, are used, simplifying the design and minimizing the need for precise resistor matching. This simplicity results in improved tolerance to manufacturing variations, making R/2R ladder DACs more cost-effective and easier to produce with consistent performance. On the other hand, binary weighted DACs require a set of resistors with precisely defined binary-weighted values, leading to increased complexity and potential challenges in maintaining accurate resistor ratios during manufacturing. Therefore, the R/2R ladder architecture is often favored for its practical advantages in terms of simplicity and manufacturability. Additionally, R/2R ladder DACs tend to exhibit better performance in terms of speed and power consumption compared to binary weighted DACs. The ladder structure minimizes the number of resistor values needed, reducing the overall complexity of the circuit and allowing for faster signal conversion. This simplicity also translates into lower power requirements, making R/2R ladder DACs more energy-efficient. Furthermore, R/2R ladder DACs are inherently more forgiving in terms of resistor mismatches, which can be crucial in real-world manufacturing scenarios where achieving perfect component matching may be challenging. In summary, the R/2R ladder DAC stands out as a practical choice, offering a balance between performance, simplicity, and manufacturability in various digital-to-analog conversion applications.

# Discussion and Conclusion:

In the Binary Weighted DAC and R/2R DAC experiment, we delve into the principles and practical aspects of digital-to-analog conversion, gaining a comprehensive understanding of two distinct DAC architectures. The Binary Weighted DAC involves varying the weights of binary inputs, emphasizing the significance of bit-wise contributions to the output voltage. This experiment allows us to explore the concept of weighted resistor networks and their impact on accuracy and linearity. Meanwhile, the R/2R DAC introduces the utilization of resistor ladder networks, offering insights into a widely used and efficient digital-to-analog conversion technique. We learn the crucial role of resistor ratios in achieving precise voltage outputs and the implications of resistor mismatches on overall performance.In our implementation of the Binary Weighted DAC, we utilized a 1k-ohm resistor as the Most Significant Bit (MSB) and an 8k-ohm resistor as the Least Significant Bit (LSB). This resistor configuration played a crucial role in defining the weights of the individual bits in the binary input, directly influencing the output voltage levels. The choice of a 1k-ohm resistor for the MSB, being the highest weight bit, highlights the emphasis on precision and control at the higher-order bits. On the other hand, the use of an 8k-ohm resistor for the LSB emphasizes the diminishing significance of lower-order bits in determining the overall output voltage.

The resistor values contribute to the linearity and accuracy of the DAC, as the voltage contribution from each bit is directly proportional to the weight assigned by the corresponding resistor. Careful consideration of resistor values is essential in achieving the desired resolution and dynamic range in the digital-to-analog conversion process. This aspect of the experiment allows us to witness the practical implications of resistor selection on the performance of the Binary Weighted DAC and emphasizes the importance of maintaining precision in resistor values to minimize errors and enhance the overall accuracy of the DAC output.

The experiment provides hands-on experience in constructing and analyzing these DAC circuits, enabling us to witness firsthand the translation of digital information into continuous analog signals. By comparing and contrasting the two DAC architectures, we deepen our understanding of the trade-offs involved in choosing a particular design for a given application. Additionally, the experiment underscores the importance of resistor precision, matching, and network configuration in minimizing errors and achieving high-fidelity analog outputs. Overall, we emerge from the Binary Weighted DAC and R/2R DAC experiment with a nuanced understanding of DAC principles, practical design considerations, and the ability to optimize these circuits for diverse applications in electronic systems and communication technologies.

# Part II: Design of a flash Analog to Digital Converter Introduction:

Flash analog-to-digital converters, also known as parallel ADCs, are the fastest way to convert an analog signal to a digital signal. Flash ADCs are ideal for applications requiring very large bandwidth, but they consume more power than other ADC architectures and are generally limited to 8-bit resolution. This tutorial will discuss flash converters and compare them with other converter types.

In this experiment, students will learn how flash ADC works by implementing a 2 bit flash ADC.

# Theory and Methodology:

Flash converters are extremely fast compared to many other types of ADCs which usually narrow in on the "correct" answer over a series of stages. Compared to these, a Flash converter is also quite simple and, apart from the analog comparators, only requires logic for the final conversion to binary.

For best accuracy often a sample-and-hold circuit is inserted in front of the ADC input. This is needed for many ADC types (like successive approximation ADC), but for Flash ADCs there is no real need for this, because the comparators are the sampling devices.

A Flash converter requires a huge number of comparators compared to other ADCs, especially as the precision increases. A Flash converter requires comparators for an *n*-bit conversion. The size, power consumption and cost of all those comparators make Flash converters generally impractical for precisions much greater than 8 bits (255 comparators). In place of these comparators, most other ADCs substitute more complex logic and/or analog circuitry which can be scaled more easily for increased precision.

# Implementation:



Fig1: A 2-bit Flash ADC Example Implementation with Bubble Error Correction and Digital Encoding

Flash ADCs have been implemented in many technologies, varying from silicon based bipolar (BJT) and complementary metal oxide FETs (CMOS) technologies to rarely used III- V technologies. Often this type of ADC is used as a first medium sized analog circuit verification.

The earliest implementations consisted of a reference ladder of well matched resistors connected to a reference voltage. Each tap at the resistor ladder is used for one comparator, possibly preceded by an amplification stage, and thus generates a logical '0' or '1' depending if the measured voltage is above or below the reference voltage of the resistor tap. The reason to add an amplifier is twofold: it amplifies the voltage difference and therefore suppresses the comparator offset, and the kick-back noise of the comparator towards the reference ladder is also strongly suppressed. Typically designs from 4-bit up to 6-bit, and sometimes 7-bit are produced.

Designs with power-saving capacitive reference ladders have been demonstrated. In addition to clocking the comparator(s), these systems also sample the reference value on the input stage. As the sampling is done at a very high rate, the leakage of the capacitors is negligible.

Recently, offset calibration has been introduced into flash ADC designs. Instead of high precision analog circuits (which increase component size to suppress variation) comparators with relatively large offset errors are measured and adjusted. A test signal is applied and the offset of each comparator is calibrated to below the LSB size of the ADC.

Another improvement to many flash ADCs is the inclusion of digital error correction. When the ADC is used in harsh environments or constructed from very small integrated circuit processes, there is a heightened risk a single comparator will randomly change state resulting in a wrong code. Bubble error correction is a digital correction mechanism that will prevent a comparator that has, for example, tripped high from reporting logic high if it is surrounded by comparators that are reporting logic low.

This circuit is the simplest to understand. It is constructed from a series of comparators, each one comparing the input signal to a unique reference voltage. The comparator outputs connect to the inputs of a priority encoder circuit, which then produces a binary output. The following illustration shows a Flash ADC 2-bit circuit:

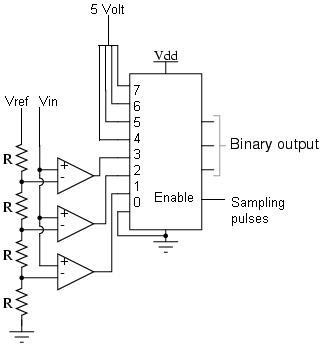


Fig 2: A 2 bit flash ADC.

An N bit flash ADC requires 2N – 1 number of comparators.

Vref is a stable reference voltage provided by a precision voltage regulator as part of the converter circuit, not shown in the schematic. As the analog input voltage exceeds the reference voltage at each comparator, the comparator outputs will sequentially saturate to a high state. The priority encoder generates a binary number based on the highest-order active input, ignoring all other active inputs.

# IC Pin Configurations:

# Apparatus:

|  |  |  |  |
| --- | --- | --- | --- |
| 1) | Trainer Board | : |  |
| 2) | Op-Amp | : | IC741 |
| 3) | Resistors | : | 1KΩ |
| 4) | 8 to 3 bit priority encoder | : | IC74148 |

# Experimental Procedure:

Construct a 2 bit flash ADC. Document the output values for different input values. Draw the output wave shapes for different inputs.

# Simulation and Measurement:



Fig 2: A 2 bit flash ADC.

Simulation Outputs

A computer screen shot of a computer screen

Description automatically generated

Vref = 4 V, Vin = 3.25 V, Output = A2 = 0, A1 = 1, A0 = 1 (Decimal 3)

Vref = 4 V, Vin = 2.25 V, Output = A2 = 0, A1 = 1, A0 = 0 (Decimal 2)A computer screen shot of a computer screen

Description automatically generated

A computer screen shot of a computer screen

Description automatically generated

Vref = 4 V, Vin = 1.25 V, Output = A2 = 0, A1 = 0, A0 = 1 (Decimal 1)

A computer screen shot of a computer screen

Description automatically generated

Vref = 4 V, Vin = 0.25 V, Output = A2 = 0, A1 = 0, A0 = 0 (Decimal 0)

# Discussion:

The Simulated experimental setup involved the utilization of three operational amplifiers (op-amps) to construct a 2-bit flash analog-to-digital converter. Four input voltages were applied to the system, representing digital states: 3.25 V, 2.25 V, 1.25 V, and 0.25 V. The significance of this experiment lies in the fundamental understanding and implementation of flash ADCs, which are known for their high-speed conversion capabilities. The flash ADC architecture is particularly valuable in applications where rapid analog-to-digital conversion is crucial, such as in communication systems and signal processing.

The choice of four discrete voltage levels enables a 2-bit resolution, dividing the input range into four distinct bins. The op-amps function as comparators, comparing each input voltage to a set reference voltage and generating corresponding binary outputs. Despite the theoretical simplicity of flash ADCs, real-world implementations may exhibit errors in their output. This discrepancy can arise from various sources, including op-amp non-idealities, parasitic elements in the circuit, and imperfect matching of components. The presence of errors in the output is a common challenge in ADC design and can impact the overall accuracy of the conversion process. Analyzing these errors is essential for improving the performance of the ADC and gaining insights into the practical limitations of the implemented circuit. Overall, this experiment provides valuable hands-on experience in the design and analysis of flash ADCs, contributing to the development of skills essential for electronic circuit design and signal processing applications. Upon completion of the 2-bit Flash ADC experiment, we gained valuable insights into the practical implementation of analog-to-digital converters

(ADCs) and their application in signal processing. The experiment provides a hands-on opportunity to understand the intricacies of flash ADC architecture, the role of operational amplifiers in comparator circuits, and the impact of discrete voltage levels on digital conversion. Moreover, the experiment fosters a deeper comprehension of the challenges associated with real-world ADC implementations, such as minimizing errors arising from component non-idealities and parasitic elements..

# Reference:

Thomas L. Floyd, *Digital Fundamentals*, 9 Edition, 2006, Prentice Hall.