Digital Logic and Circuits

Mid-term Assignment (Summer 20-21)

Submission Link: https://forms.gle/R72GBQwyXsHCbGFZ6

Submission Deadline: 30.06.2021 (11:59:59 pm)

Instructions:

I. **Complete the assignment in a fresh piece of paper.**
II. **Write your ID on top of each page you use for writing.**
III. **After completion, take picture of all the pages and make a pdf out of it.**
IV. **Rename the file with your ID only as XXXXX (ID: AB-XXXXX-C).**
V. **Please make sure that the file size does not exceed 10MB.**
VI. **Once you have pdf, upload your pdf in the link above.**

Questions:

1. For the function $F(A, B, C, D) = \sum(1,2,4,7,9)$ and $d(A, B, C, D) = (10,11,12,13,14,15)$, where d(A,B,C,D) represents don't care condition. **10 Marks**

a) Construct the truth-table.
b) Find the minimal SOP using K-Map.
c) Draw the logic circuit of the minimal SOP using Basic gates.
d) Draw the logic circuit using only NAND gates.

2. For the function $F(A, B, C, D) = \sum(0,1,6,7,8,9,12,13)$ and $d(A, B, C, D) = (4,5,14,15)$, where d(A,B,C,D) represents don't care condition. **10 Marks**

a) Construct the truth-table.
b) Find the minimal SOP using K-Map.
c) Draw the logic circuit using only NOR gates.
d) Draw the logic circuit using CMOS.

3. Design a Full-Subtractor using two 4-to-1 MUXs. Take inputs A and C_{IN} as your selector inputs. You should clearly show all the procedure and draw the logic circuit of your implementation. (** You are not required to show the internal logic circuit of a MUX**) **10 Marks**