

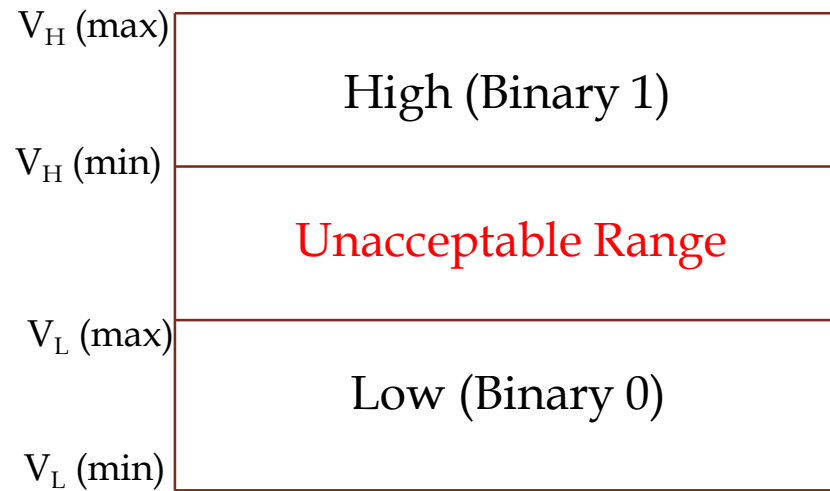
Introduction to Logic, Logic Gates and Boolean Algebra

Topics to be covered

Logic Gates

- Logic Gates are the basic building blocks of any digital system. A logic gate can have one or more than one input but only one output. The relationship between the input/s and the output is based on a **certain logic**. The gates are named based on the logic.
- The names of the logic gates are:
 - Basic Gates:
 - NOT Gate or Inverter
 - AND Gate
 - OR Gate
 - Universal Gates:
 - NAND Gate
 - NOR Gate
 - Exclusive Gates:
 - Exclusive-OR Gate
 - Exclusive-NOR

❧ **Bit:** in binary system we know that there are two digits 0 (low voltage) and 1 (high voltage). The voltages used to represent a '1' or '0' are called logic levels

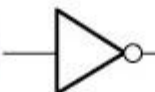


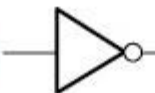
- ❧ Pulse is when clock frequency is applied to a circuit.
- ❧ Rising edge and falling edge.
- ❧ Periodic and non-periodic waveforms.
- ❧ Timing diagram

Inverter(NOT gate)



Output of an inverter is opposite/complement of its input.

LOW (0) —  — HIGH (1)

HIGH (1) —  — LOW (0)

| A | X |
|---|---|
| 0 | 1 |
| 1 | 0 |

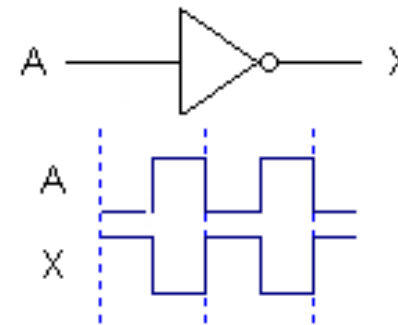
Truth table

0 = LOW

1 = HIGH

$$X = \overline{A}$$

Boolean expression

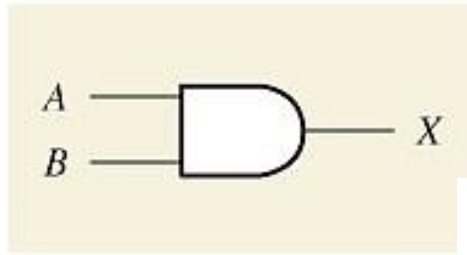


Pulsed waveforms

When the input is LOW, the output
is HIGH

When the input is HIGH, the
output is LOW

AND Gate



Distinctive shape symbol

The output of an AND gate is **HIGH** only when all inputs are **HIGH** and **LOW** when any input is **LOW**.

| A | B | X |
|---|---|---|
| 0 | 0 | 0 |
| 0 | 1 | 0 |
| 1 | 0 | 0 |
| 1 | 1 | 1 |

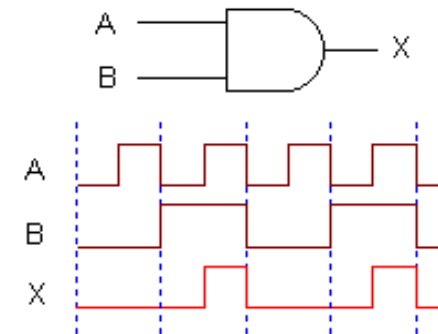
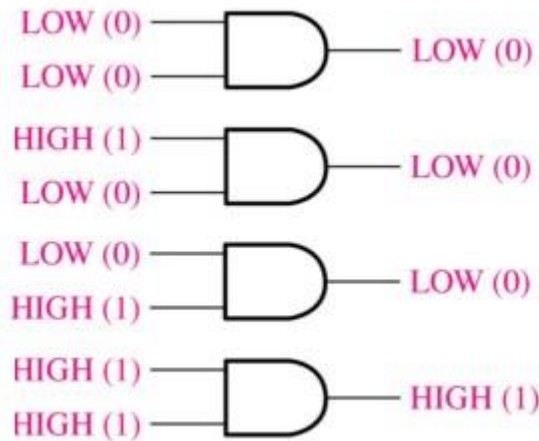
$$X = AB$$

Boolean
expression

Truth
table

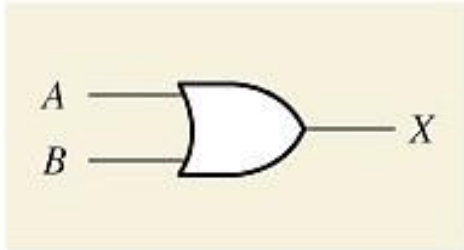
0 = LOW
1 = HIGH

$$N = 2^n$$



Pulsed
waveforms

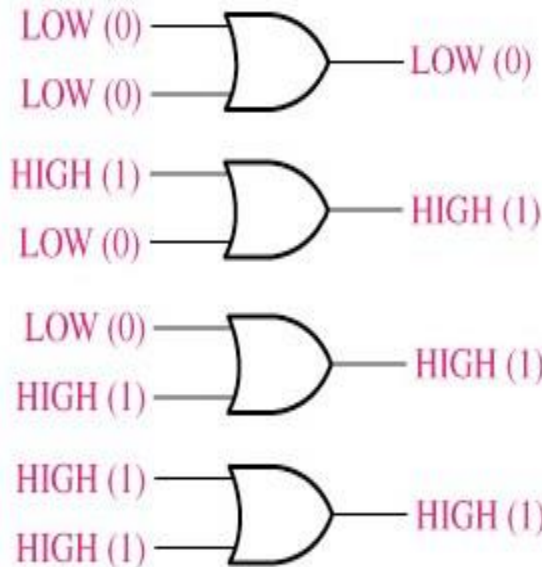
The OR Gate



Distinctive shape symbol

The output of an OR gate is **HIGH** whenever one or more inputs are **HIGH** and **Low** when all inputs are **LOW**

$$N = 2^n$$



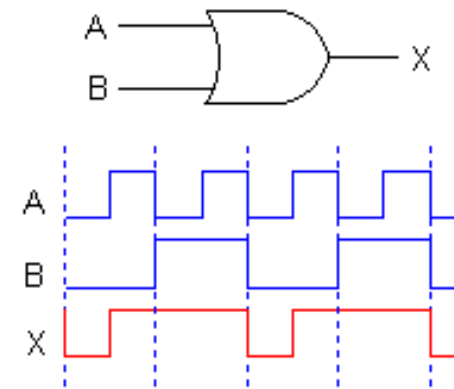
| A | B | X |
|---|---|---|
| 0 | 0 | 0 |
| 0 | 1 | 1 |
| 1 | 0 | 1 |
| 1 | 1 | 1 |

$$X = A + B$$

Boolean expression

Truth table

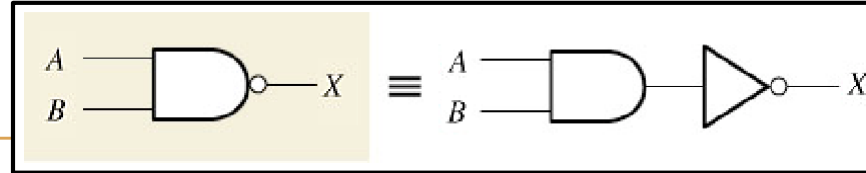
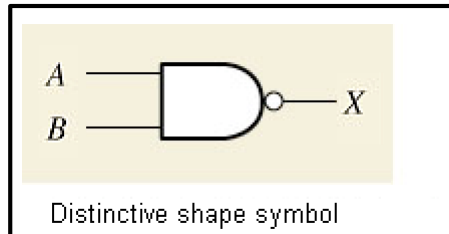
0 = LOW
1 = HIGH



Pulsed waveforms

The NAND Gate

AND



The output of a NAND gate is HIGH whenever one or more inputs are LOW.

| A | B | X |
|---|---|---|
| 0 | 0 | 1 |
| 0 | 1 | 1 |
| 1 | 0 | 1 |
| 1 | 1 | 0 |

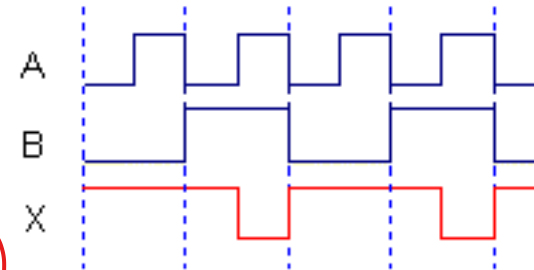
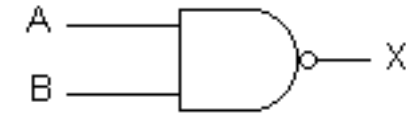
Truth
table

0 = LOW
1 = HIGH

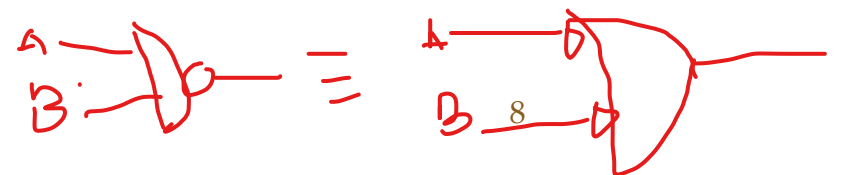
$$X = \overline{AB}$$

Boolean expression

NAND = Negative-OR

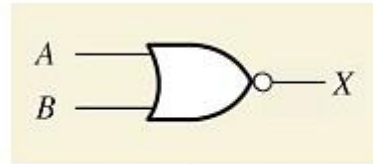


Pulsed waveforms

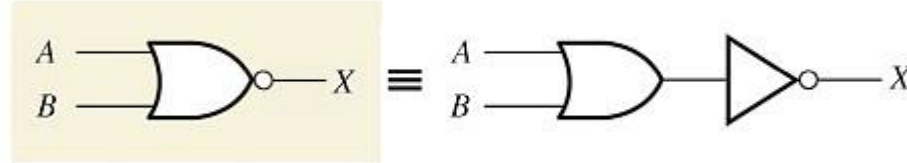


The NOR Gate

\overline{OR}



Distinctive shape symbol



The output of a NOR gate is **LOW** whenever one or more inputs are **HIGH**.

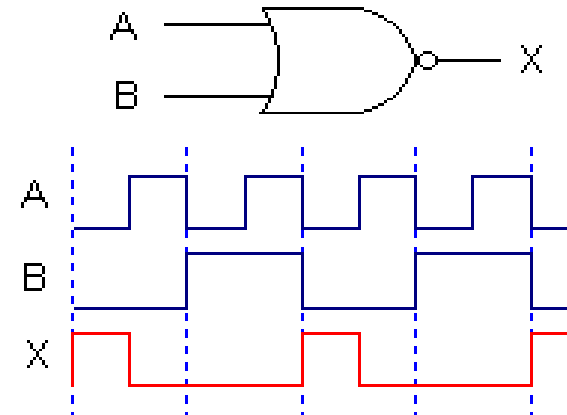
| A | B | X |
|---|---|---|
| 0 | 0 | 1 |
| 0 | 1 | 0 |
| 1 | 0 | 0 |
| 1 | 1 | 0 |

Truth
table

0 = LOW
1 = HIGH

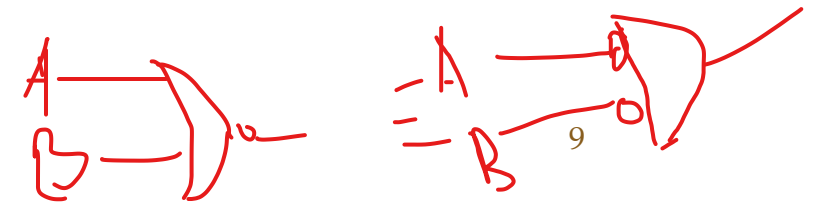
$$X = \overline{A + B}$$

Boolean
expression

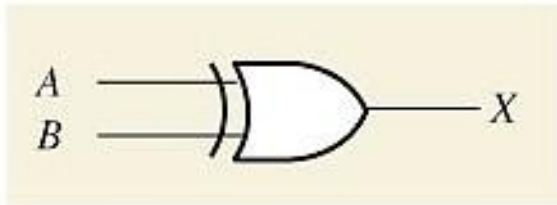


Pulsed waveforms

NOR = Negative = AND



Exclusive-OR



Distinctive shape symbol

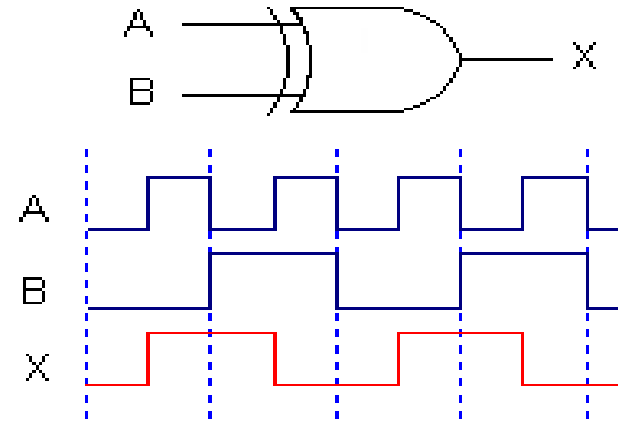
The output of an XOR gate is **HIGH** whenever the **two inputs are different**.

| A | B | X |
|---|---|---|
| 0 | 0 | 0 |
| 0 | 1 | 1 |
| 1 | 0 | 1 |
| 1 | 1 | 0 |

Truth
table

0 = LOW
1 = HIGH

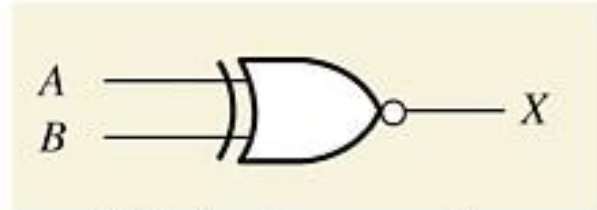
$X = A \oplus B$
Boolean
expression



Pulsed waveforms

The output of an XOR gate is **HIGH** when there are **ODD** number of 1's on the inputs to the gate

Exclusive-NOR Gate



Distinctive shape symbol

The output of an EX-NOR gate is **HIGH** whenever the two inputs are identical.

same

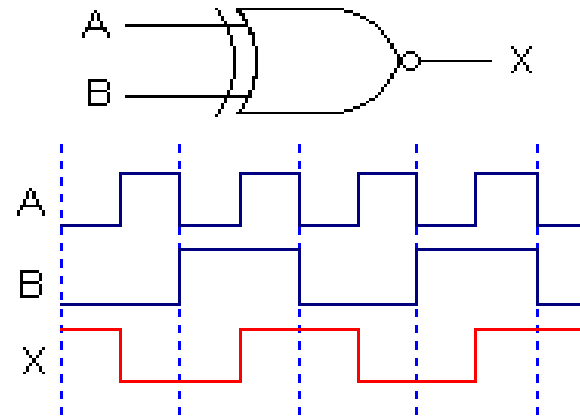
| A | B | X |
|---|---|---|
| 0 | 0 | 1 |
| 0 | 1 | 0 |
| 1 | 0 | 0 |
| 1 | 1 | 1 |

Truth table

0 = LOW
1 = HIGH

$$X = \overline{A \oplus B}$$

Boolean expression



Pulsed waveforms

The output of an EX-NOR gate is **HIGH** when there are **EVEN** number of 1's on the inputs to the gate except when all its inputs are "LOW".



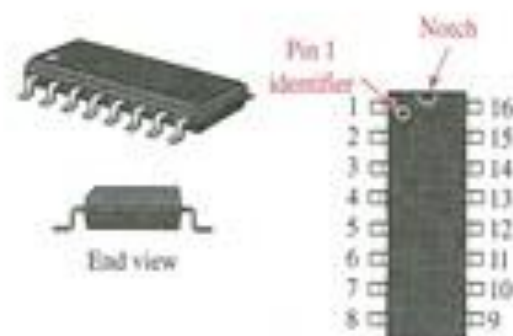
Fixed-Function Integrated Circuits

IC package styles

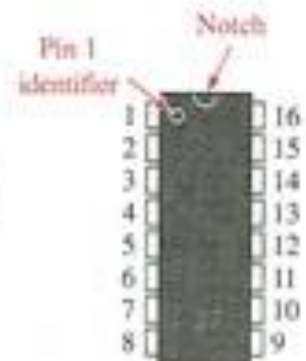
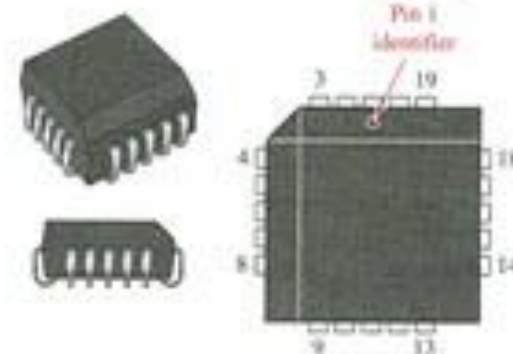
- Dual in-line package (DIP)
- Small-outline IC (SOIC)
- Flat pack (FP)
- Plastic-leaded chip carrier (PLCC)
- Leadless-ceramic chip carrier (LCCC)



End view



End view



IC configurations:

| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|--|-----|-----|-----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|-----|----|----|--|----|----|-----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|-----|----|----|--|----|----|-----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|-----|----|----|
| <table><tr><td>01</td><td>1A</td><td>Vcc</td><td>14</td></tr><tr><td>02</td><td>1B</td><td>4B</td><td>13</td></tr><tr><td>03</td><td>1Y</td><td>4A</td><td>12</td></tr><tr><td>04</td><td>2A</td><td>4Y</td><td>11</td></tr><tr><td>05</td><td>2B</td><td>3B</td><td>10</td></tr><tr><td>06</td><td>2Y</td><td>3A</td><td>09</td></tr><tr><td>07</td><td>GND</td><td>3Y</td><td>08</td></tr></table> <p>7400</p> | 01 | 1A | Vcc | 14 | 02 | 1B | 4B | 13 | 03 | 1Y | 4A | 12 | 04 | 2A | 4Y | 11 | 05 | 2B | 3B | 10 | 06 | 2Y | 3A | 09 | 07 | GND | 3Y | 08 | <table><tr><td>01</td><td>1Y</td><td>Vcc</td><td>14</td></tr><tr><td>02</td><td>1A</td><td>4Y</td><td>13</td></tr><tr><td>03</td><td>1B</td><td>4B</td><td>12</td></tr><tr><td>04</td><td>2Y</td><td>4A</td><td>11</td></tr><tr><td>05</td><td>2A</td><td>3Y</td><td>10</td></tr><tr><td>06</td><td>2B</td><td>3B</td><td>09</td></tr><tr><td>07</td><td>GND</td><td>3A</td><td>08</td></tr></table> <p>7402</p> | 01 | 1Y | Vcc | 14 | 02 | 1A | 4Y | 13 | 03 | 1B | 4B | 12 | 04 | 2Y | 4A | 11 | 05 | 2A | 3Y | 10 | 06 | 2B | 3B | 09 | 07 | GND | 3A | 08 | <table><tr><td>01</td><td>1A</td><td>Vcc</td><td>14</td></tr><tr><td>02</td><td>1Y</td><td>6A</td><td>13</td></tr><tr><td>03</td><td>2A</td><td>6Y</td><td>12</td></tr><tr><td>04</td><td>2Y</td><td>5A</td><td>11</td></tr><tr><td>05</td><td>3A</td><td>5Y</td><td>10</td></tr><tr><td>06</td><td>3Y</td><td>4A</td><td>09</td></tr><tr><td>07</td><td>GND</td><td>4Y</td><td>08</td></tr></table> <p>7404</p> | 01 | 1A | Vcc | 14 | 02 | 1Y | 6A | 13 | 03 | 2A | 6Y | 12 | 04 | 2Y | 5A | 11 | 05 | 3A | 5Y | 10 | 06 | 3Y | 4A | 09 | 07 | GND | 4Y | 08 |
| 01 | 1A | Vcc | 14 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 02 | 1B | 4B | 13 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 03 | 1Y | 4A | 12 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 04 | 2A | 4Y | 11 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 05 | 2B | 3B | 10 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 06 | 2Y | 3A | 09 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 07 | GND | 3Y | 08 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 01 | 1Y | Vcc | 14 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 02 | 1A | 4Y | 13 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 03 | 1B | 4B | 12 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 04 | 2Y | 4A | 11 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 05 | 2A | 3Y | 10 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 06 | 2B | 3B | 09 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 07 | GND | 3A | 08 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 01 | 1A | Vcc | 14 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 02 | 1Y | 6A | 13 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 03 | 2A | 6Y | 12 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 04 | 2Y | 5A | 11 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 05 | 3A | 5Y | 10 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 06 | 3Y | 4A | 09 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 07 | GND | 4Y | 08 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
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| 01 | 1A | Vcc | 14 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 02 | 1B | 4B | 13 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 03 | 1Y | 4A | 12 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 04 | 2A | 4Y | 11 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 05 | 2B | 3B | 10 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 06 | 2Y | 3A | 09 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 07 | GND | 3Y | 08 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 01 | 1A | Vcc | 14 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 02 | 1B | 4B | 13 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 03 | 1Y | 4A | 12 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 04 | 2A | 4Y | 11 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 05 | 2B | 3B | 10 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 06 | 2Y | 3A | 09 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 07 | GND | 3Y | 08 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 01 | 1A | Vcc | 14 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 02 | 1B | 4B | 13 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 03 | 1Y | 4A | 12 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 04 | 2A | 4Y | 11 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 05 | 2B | 3B | 10 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 06 | 2Y | 3A | 09 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 07 | GND | 3Y | 08 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

Integrated Circuits (ICs):

7400 :- Quad 2 I/p NAND.

7404 :- Hex Inverter.

7432 :- Quad 2 I/p OR.

7402 :- Quad 2 I/p NOR.

7408 :- Quad 2 I/p AND.

7486 :- Quad 2 I/p X-OR.

RULES OF BOOLEAN ALGEBRA

Basic rules of Boolean algebra.

1. $A + 0 = A$

2. $A + 1 = 1$

3. $A \cdot 0 = 0$

4. $A \cdot 1 = A$

5. $A + A = A$

6. $A + \bar{A} = 1$

7. $A \cdot A = A$

8. $A \cdot \bar{A} = 0$

9. $\bar{\bar{A}} = A$

10. $A + AB = A$

11. $A + \bar{A}B = A + B$

12. $(A + B)(A + C) = A + BC$



Rule 1. $A + 0 = A$



| A | B | X |
|---|---|---|
| 0 | 0 | 0 |
| 0 | 1 | 1 |
| 1 | 0 | 1 |
| 1 | 1 | 1 |

OR Truth Table

| A | B | X |
|---|---|---|
| 0 | 0 | 0 |
| 0 | 1 | 0 |
| 1 | 0 | 0 |
| 1 | 1 | 1 |

AND Truth Table

Rule 2. $A + 1 = 1$



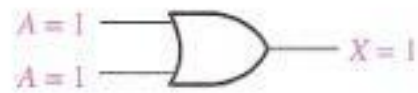
Rule 3. $A \cdot 0 = 0$



Rule 4. $A \cdot 1 = A$



Rule 5. $A + A = A$



1. $A + 0 = A$

2. $A + 1 = 1$

3. $A \cdot 0 = 0$

4. $A \cdot 1 = A$

5. $A + A = A$

6. $A + \bar{A} = 1$

7. $A \cdot A = A$

8. $A \cdot \bar{A} = 0$

9. $\bar{\bar{A}} = A$

10. $A + AB = A$

11. $A + \bar{A}B = A + B$

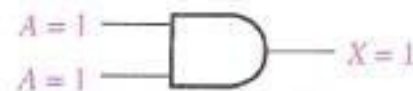
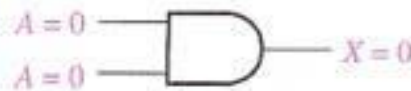
12. $(A + B)(A + C) = A + BC$



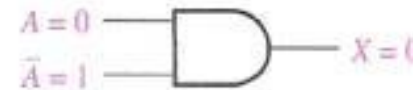
Rule 6. $A + \bar{A} = 1$



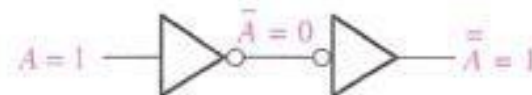
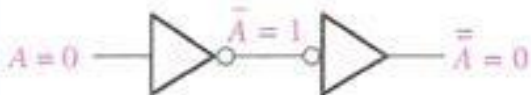
Rule 7. $A \cdot A = A$



Rule 8. $A \cdot \bar{A} = 0$



Rule 9. $\bar{\bar{A}} = A$

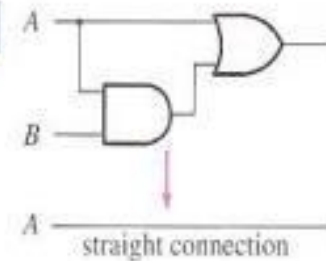


Rule 10. $A + AB = A$

$A + AB = A(1 + B)$ Factoring (distributive law)
 $= A \cdot 1$ Rule 2: $(1 + B) = 1$
 $= A$ Rule 4: $A \cdot 1 = A$

| A | B | AB | A + AB |
|---|---|----|--------|
| 0 | 0 | 0 | 0 |
| 0 | 1 | 0 | 0 |
| 1 | 0 | 0 | 1 |
| 1 | 1 | 1 | 1 |

↑ equal ↑



1. $A + 0 = A$

7. $A \cdot A = A$

2. $A + 1 = 1$

8. $A \cdot \bar{A} = 0$

3. $A \cdot 0 = 0$

9. $\bar{\bar{A}} = A$

4. $A \cdot 1 = A$

10. $A + AB = A$

5. $A + A = A$

11. $A + \bar{A}B = A + B$

6. $A + \bar{A} = 1$

12. $(A + B)(A + C) = A + BC$



Rule 11. $A + \bar{A}B = A + B$

$$\begin{aligned}
 A + \bar{A}B &= (A + AB) + \bar{A}B \\
 &= (AA + AB) + \bar{A}B \\
 &= AA + AB + A\bar{A} + \bar{A}B \\
 &= (A + \bar{A})(A + B) \\
 &= 1 \cdot (A + B) \\
 &= A + B
 \end{aligned}$$

Rule 10: $A = A + AB$

Rule 7: $A = AA$

Rule 8: adding $A\bar{A} = 0$

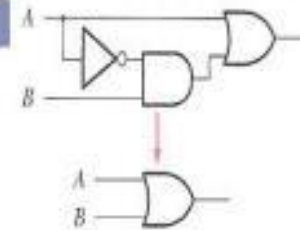
Factoring

Rule 6: $A + \bar{A} = 1$

Rule 4: drop the 1

| A | B | $\bar{A}B$ | $A + \bar{A}B$ | $A + B$ |
|---|---|------------|----------------|---------|
| 0 | 0 | 0 | 0 | 0 |
| 0 | 1 | 1 | 1 | 1 |
| 1 | 0 | 0 | 1 | 1 |
| 1 | 1 | 0 | 1 | 1 |

↑ equal ↑



Rule 12. $(A + B)(A + C) = A + BC$

$$\begin{aligned}
 (A + B)(A + C) &= AA + AC + AB + BC \\
 &= A + AC + AB + BC \\
 &= A(1 + C) + AB + BC \\
 &= A \cdot 1 + AB + BC \\
 &= A(1 + B) + BC \\
 &= A \cdot 1 + BC \\
 &= A + BC
 \end{aligned}$$

Distributive law

Rule 7: $AA = A$

Factoring (distributive law)

Rule 2: $1 + C = 1$

Factoring (distributive law)

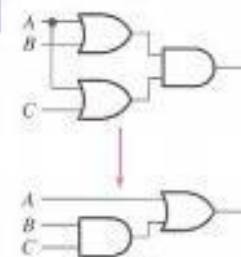
Rule 2: $1 + B = 1$

Rule 4: $A \cdot 1 = A$

- | | |
|----------------------|-------------------------------|
| 1. $A + 0 = A$ | 7. $A \cdot A = A$ |
| 2. $A + 1 = 1$ | 8. $A \cdot \bar{A} = 0$ |
| 3. $A \cdot 0 = 0$ | 9. $\bar{\bar{A}} = A$ |
| 4. $A \cdot 1 = A$ | 10. $A + AB = A$ |
| 5. $A + A = A$ | 11. $A + \bar{A}B = A + B$ |
| 6. $A + \bar{A} = 1$ | 12. $(A + B)(A + C) = A + BC$ |

| A | B | C | $A + B$ | $A + C$ | $(A + B)(A + C)$ | BC | $A + BC$ |
|---|---|---|---------|---------|------------------|------|----------|
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 0 | 0 | 1 | 0 | 1 | 0 | 0 | 0 |
| 0 | 1 | 0 | 1 | 0 | 0 | 0 | 0 |
| 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |
| 1 | 0 | 0 | 1 | 1 | 1 | 0 | 1 |
| 1 | 0 | 1 | 1 | 1 | 1 | 0 | 1 |
| 1 | 1 | 0 | 1 | 1 | 1 | 0 | 1 |
| 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |

↑ equal ↑



Simplification using boolean algebra

Simplification means fewer gates
for the same function

EXAMPLE

$$AB + A(B + C) + B(B + C) \quad \blacksquare \quad B + AC$$

$$AB + A(B + C) + B(B + C)$$

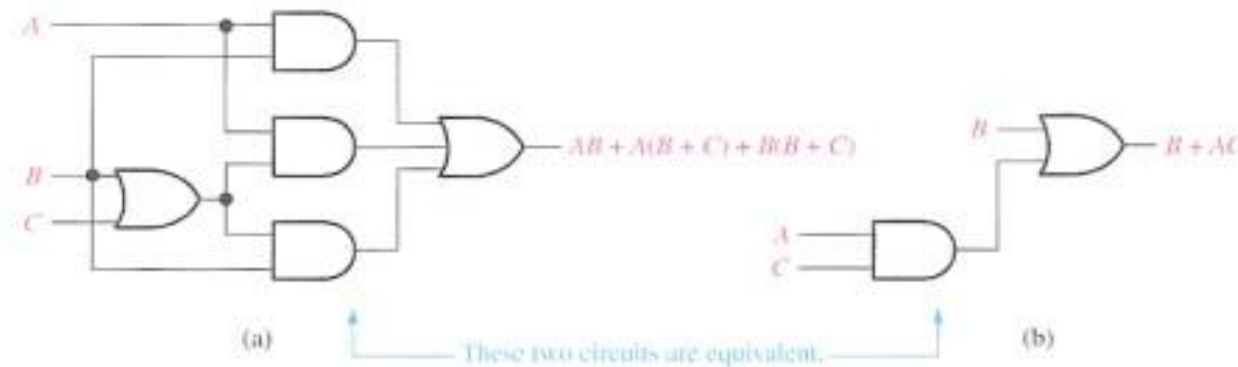
$$AB + AB + AC + BB + BC$$

$$AB + AB + AC + B + BC$$

$$AB + AC + B + BC$$

$$AB + AC + B$$

$$B + AC$$



EXAMPLE

$$[\overline{A}\overline{B}(C + BD) + \overline{A}\overline{B}]C \quad \overline{B}C$$

$$\overline{A}BC + \overline{A}\overline{B}\overline{C} + \overline{A}\overline{B}\overline{C} + \overline{A}\overline{B}\overline{C} + \overline{A}\overline{B}\overline{C} + \overline{A}\overline{B}\overline{C}$$

$$BC + \overline{A}\overline{B} + \overline{B}\overline{C}$$

■

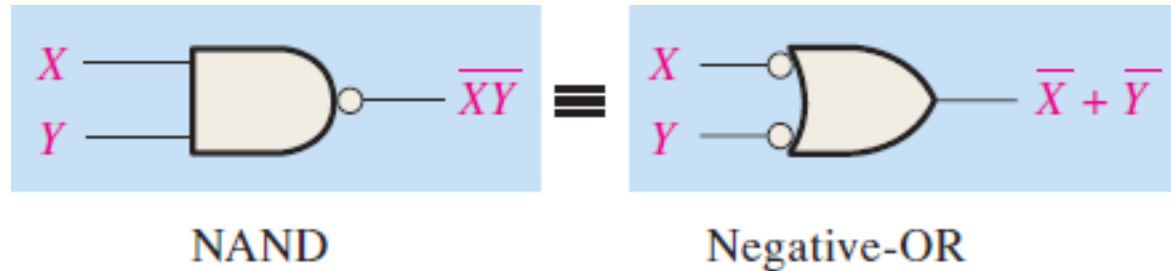
DEMORGAN'S THEOREMS

- The first theorem is stated as follows:

The complement of a product of variables is equal to the sum of the complements of complements of the variable.

The formula of this theorem for two variables is written as

$$\overline{XY} = \overline{X} + \overline{Y}$$



| Inputs | | Output | |
|--------|---|-----------------|-------------------------------|
| X | Y | \overline{XY} | $\overline{X} + \overline{Y}$ |
| 0 | 0 | 1 | 1 |
| 0 | 1 | 1 | 1 |
| 1 | 0 | 1 | 1 |
| 1 | 1 | 0 | 0 |

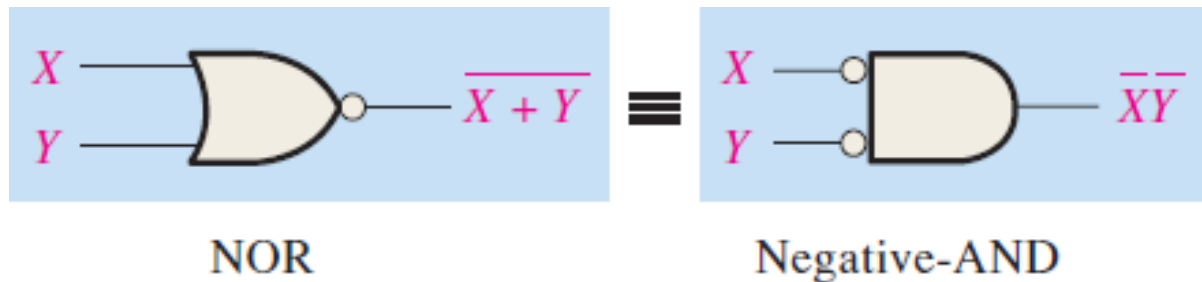
DEMORGAN'S THEOREMS

- The second theorem is stated as follows:

The complement of a sum of variables is equal to the product of the complements of the variables.

The formula of this theorem for two variables is written as

$$\overline{X + Y} = \overline{X} \overline{Y}$$



| Inputs | | Output | |
|--------|-----|--------------------|-----------------------------|
| X | Y | $\overline{X + Y}$ | $\overline{X} \overline{Y}$ |
| 0 | 0 | 1 | 1 |
| 0 | 1 | 0 | 0 |
| 1 | 0 | 0 | 0 |
| 1 | 1 | 0 | 0 |

APPLICATION OF DEMORGAN'S THEOREM

Apply DeMorgan's theorems to the expressions \overline{XYZ} and $\overline{X + Y + Z}$.

Solution

$$\begin{aligned}\overline{XYZ} &= \overline{X} + \overline{Y} + \overline{Z} \\ \overline{X + Y + Z} &= \overline{X} \overline{Y} \overline{Z}\end{aligned}$$

Apply DeMorgan's theorems to the expressions \overline{WXYZ} and $\overline{W + X + Y + Z}$.

Solution

$$\begin{aligned}\overline{WXYZ} &= \overline{W} + \overline{X} + \overline{Y} + \overline{Z} \\ \overline{W + X + Y + Z} &= \overline{W} \overline{X} \overline{Y} \overline{Z}\end{aligned}$$

Apply DeMorgan's theorems to each expression:

(a) $\overline{(\overline{A} + \overline{B}) + \overline{C}}$

(b) $\overline{(\overline{A} + B) + CD}$

(c) $\overline{(A + B)\overline{C}\overline{D} + E + \overline{F}}$

Solution

(a) $\overline{(\overline{A} + \overline{B}) + \overline{C}} = \overline{(\overline{A} + \overline{B})} \overline{\overline{C}} = (A + B)C$

(b) $\overline{(\overline{A} + B) + CD} = \overline{(\overline{A} + B)} \overline{CD} = (\overline{\overline{A}B})(\overline{C} + \overline{D}) = A\overline{B}(\overline{C} + \overline{D})$

(c) $\overline{(A + B)\overline{C}\overline{D} + E + \overline{F}} = \overline{((A + B)\overline{C}\overline{D})} \overline{E + \overline{F}} = (\overline{A} \overline{B} + C + D)\overline{E}F$



APPLICATION OF DEMORGAN'S THEOREM

Apply DeMorgan's theorem to the expression $\overline{\overline{X} + \overline{Y} + \overline{Z}}$.

Apply DeMorgan's theorem to the expression $\overline{\overline{W}\overline{X}\overline{Y}\overline{Z}}$.

Apply DeMorgan's theorems to each of the following expressions:

(a) $\overline{(A + B + C)D}$

(b) $\overline{ABC + DEF}$

(c) $\overline{A\overline{B} + \overline{C}D + EF}$

The Boolean expression for an exclusive-OR gate is $A\overline{B} + \overline{A}B$. With this as a starting point, use DeMorgan's theorems and any other rules or laws that are applicable to develop an expression for the exclusive-NOR gate.

Starting with the expression for a 4-input NAND gate, use DeMorgan's theorems to develop an expression for a 4-input negative-OR gate.

Apply DeMorgan's theorems to the following expressions:

(a) $\overline{ABC} + (\overline{\overline{D} + E})$ (b) $\overline{(A + B)C}$ (c) $\overline{A + B + C} + \overline{\overline{D}E}$



Textbooks:



- ❧ [1] Thomas L. Floyd, “Digital Fundamentals” 11th edition, Prentice Hall.
- ❧ [2] M. Morris Mano, “Digital Logic & Computer Design” Prentice Hall.