



Digital Logic & Circuits

Logic Gates: using RTL

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RTL Logic

- The basic circuit of the RTL digital logic family is the NOR gate.
- The voltage levels for the circuit are 0.2 V for the low level and from 1 to 3.6 V for the high level.
- The fan-out of the RTL gate is limited by the value of the output voltage when high.
- As the output is loaded with inputs of other gates, more current is consumed by the load.
- Any voltage below 1 V in the output may not drive the next transistor into saturation as required.
- The power dissipation of the RTL gate is about 12 mW.
- The propagation delay averages 25 ns.



Disadvantages of RTL Logic

- It's relatively slow.
- Low noise immunity and noise margin.
- Low Fan-out (Approx. 3~5)
- Expensive due to fabricated of resistor.
- It can not operate above 4MHz.

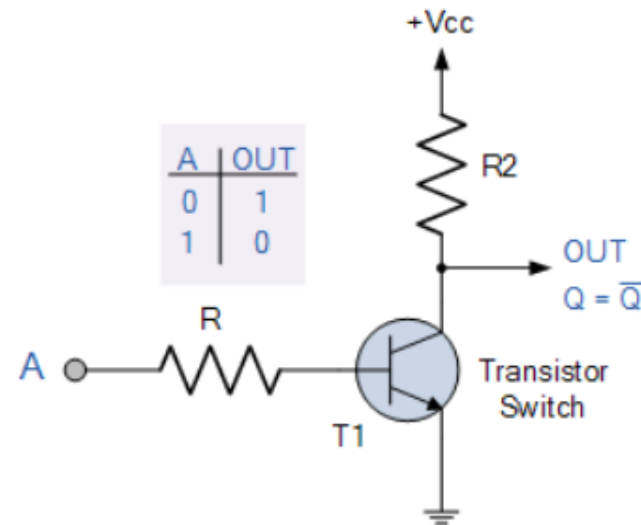




NOT Gate Using RTL Logic

Transistor NOT Gate

A simple 2-input logic NOT gate can be constructed using a RTL Resistor-transistor switches as shown below with the input connected directly to the transistor base. The transistor must be saturated “ON” for an inverted output “OFF” at Q.



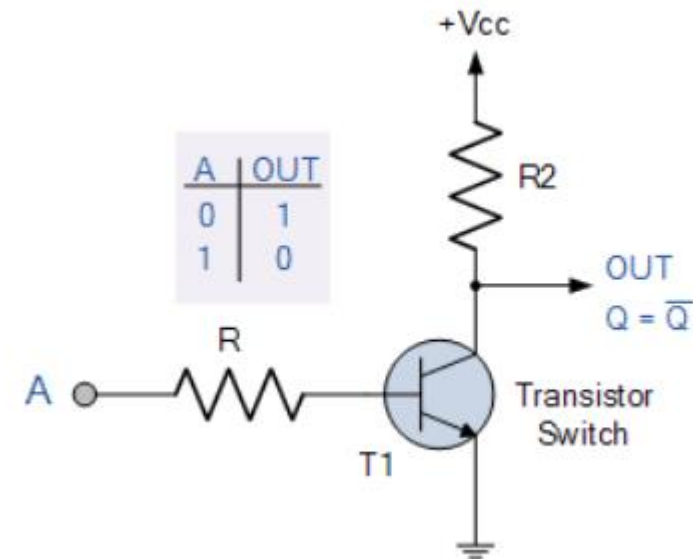


NOT Gate Using RTL Logic

Operation

Input	Transistor Status	Output
A= Low	T1=OFF , Cutoff Region	Q=+Vcc, High
A= High	T1=ON , Saturation Region	Q= $V_{CE(SAT)}=0.2$ V, Low

Circuit

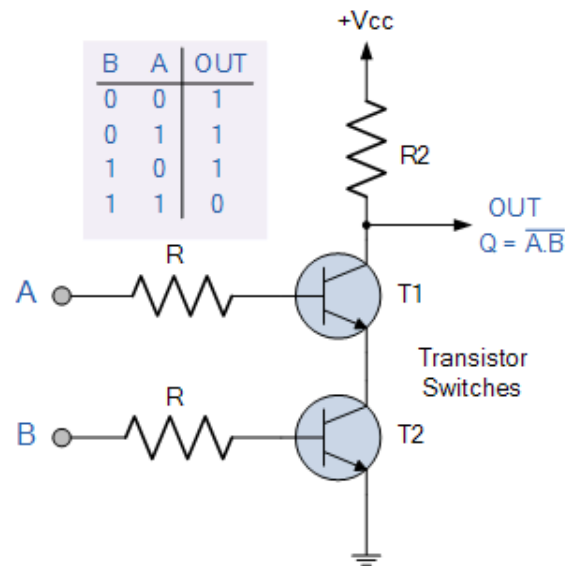




NAND Gate Using RTL Logic

Transistor NAND Gate

A simple 2-input logic NAND gate can be constructed using RTL Resistor-transistor switches connected together as shown below with the inputs connected directly to the transistor bases. Either transistor must be cut-off “OFF” for an output at Q.



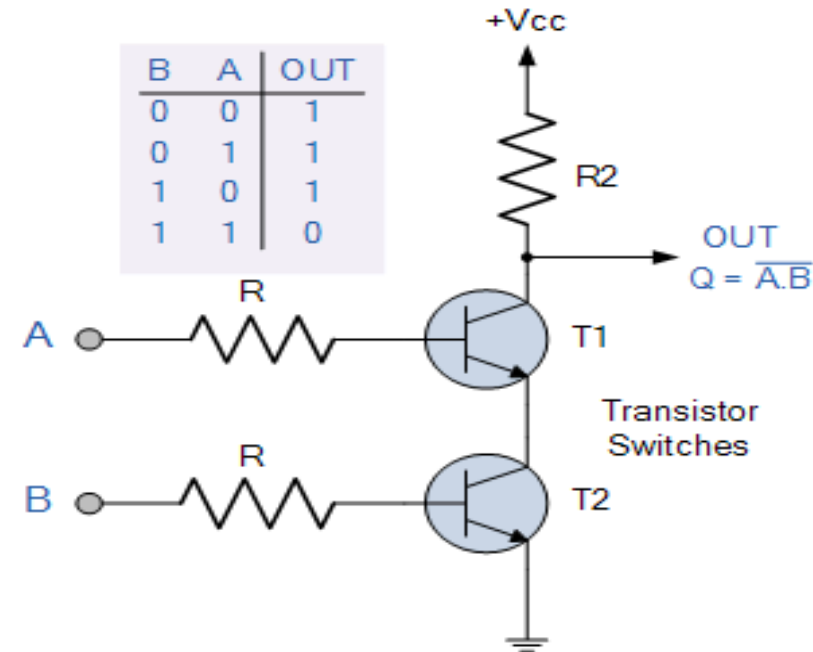


NAND Gate Using RTL Logic

Operation

Input	Transistor Status	Output
A=Low, B=Low	T1= OFF, Cutoff Region T2= OFF, Cutoff Region	Q= Vcc, High
A=Low, B=High	T1= OFF, Cutoff Region T2= ON, Saturation Region	Q= Vcc, High
A=High, B=Low	T1= ON, Saturation Region T2= OFF, Cutoff Region	Q= Vcc, High
A=High, B=High	T1= ON, Saturation Region T2= ON, Saturation Region	Q= Ground, Low

Circuit





NOR Gate Using RTL Logic

- If any input of the RTL gate is high, the corresponding transistor is driven into saturation. This causes the output to be low, regardless of the states of the other transistors.
- If all inputs are low at 0.2 V, all transistors are cut off because $V_{BE} < 0.6$ V. This causes the output of the circuit to be high, approaching the value of supply voltage V_{CC} .

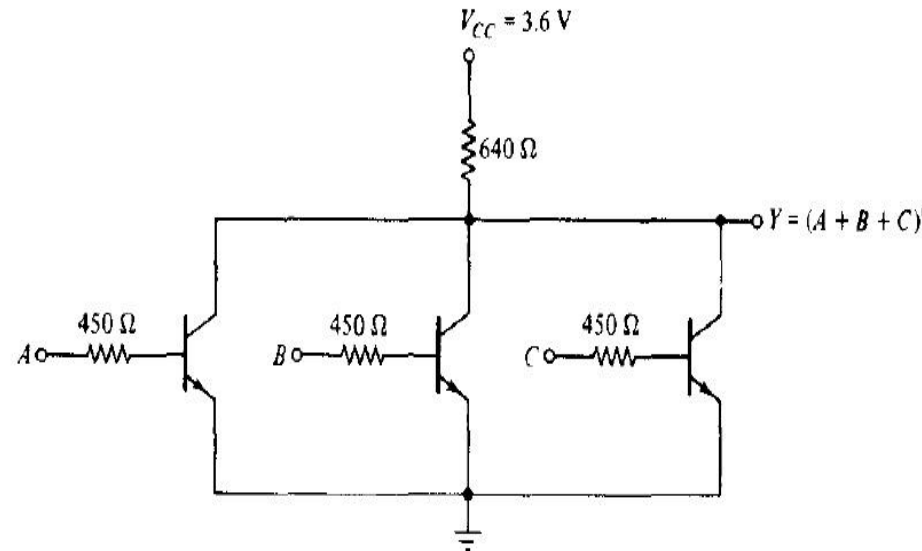


FIGURE
RTL basic NOR gate

****Related Problems will be solved in class.**



NOR Gate Using RTL Logic

Operation

Input	Transistor Status	Output
All input = low	All transistor OFF, Cutoff Region.	Output = V_{CC} , High
Any one input/Two input/all input = High	Corresponding transistor turned ON, Saturation Region	Output = $V_{CE(SAT)} = 0.2$ V. Low

Circuit

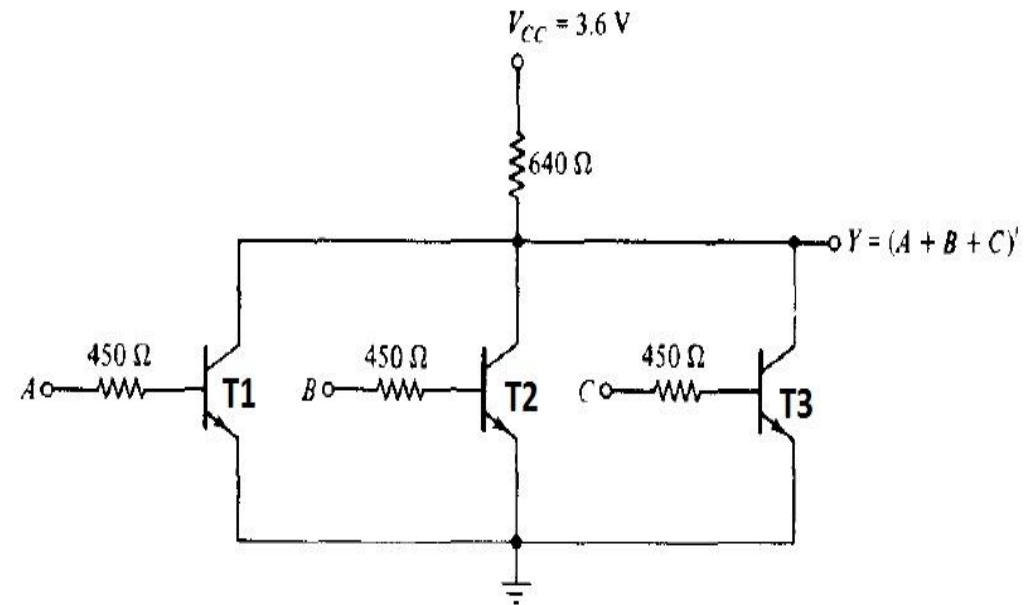
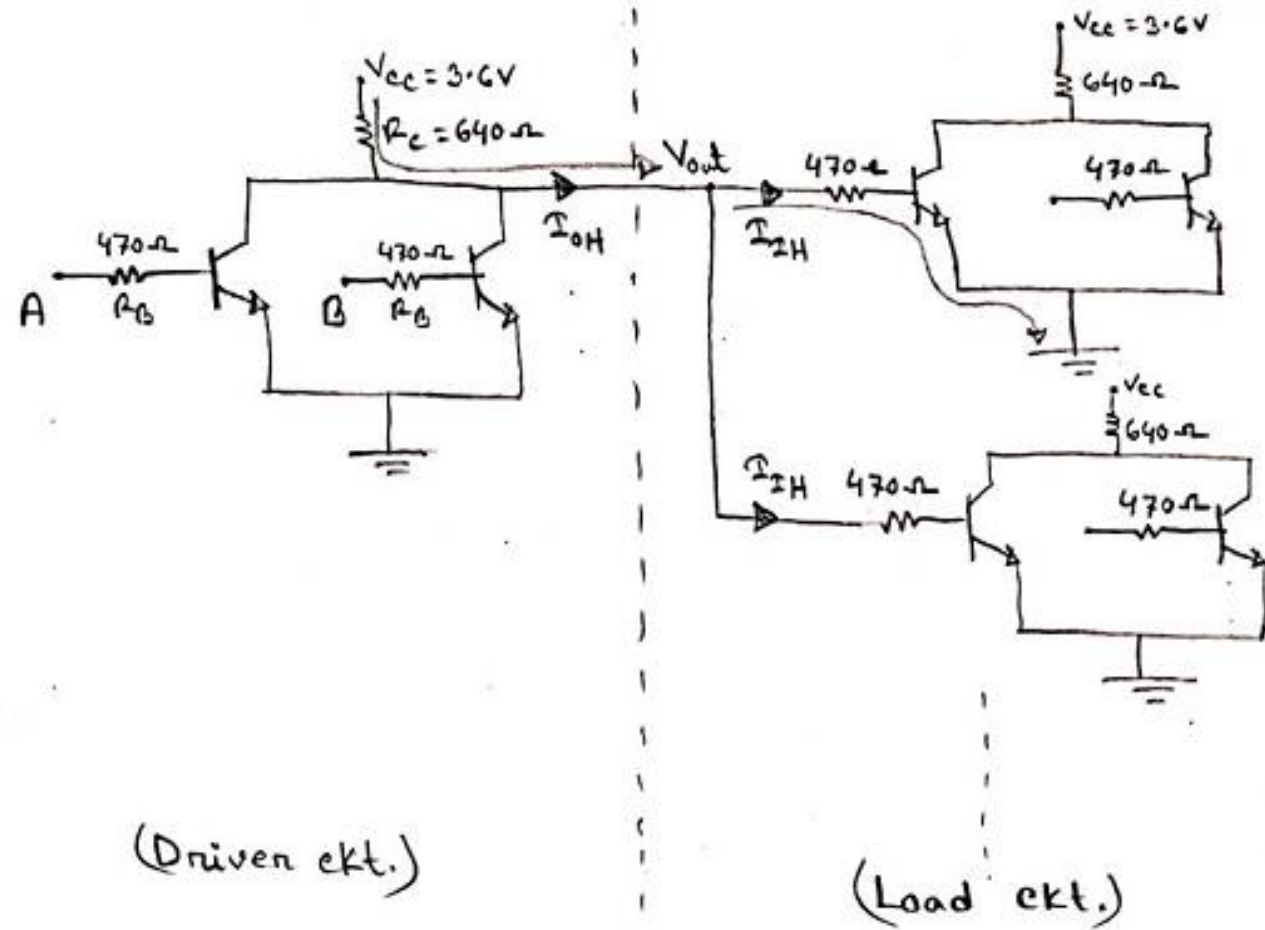


FIGURE
RTL basic NOR gate

Fan-out calculation of RTL NOR:

Low logic $\rightarrow 0 \sim 0.2V$

High logic $\rightarrow 1 \sim 3.6V$



$$\boxed{\text{Fan-out, } N = \frac{I_{OH}}{I_{IH}}}$$

KVL in driven ckt,

$$3.6 - 640 \times I_{OH} - 1 = 0$$

$$\Rightarrow I_{OH} = \frac{3.6 - 1}{640} = 0.00406 \text{ A}$$

KVL in load ckt,

$$1 - 470 \times I_{IH} - 0.7 = 0$$

$$\Rightarrow I_{IH} = \frac{1 - 0.7}{470} = 0.000638 \text{ A}$$

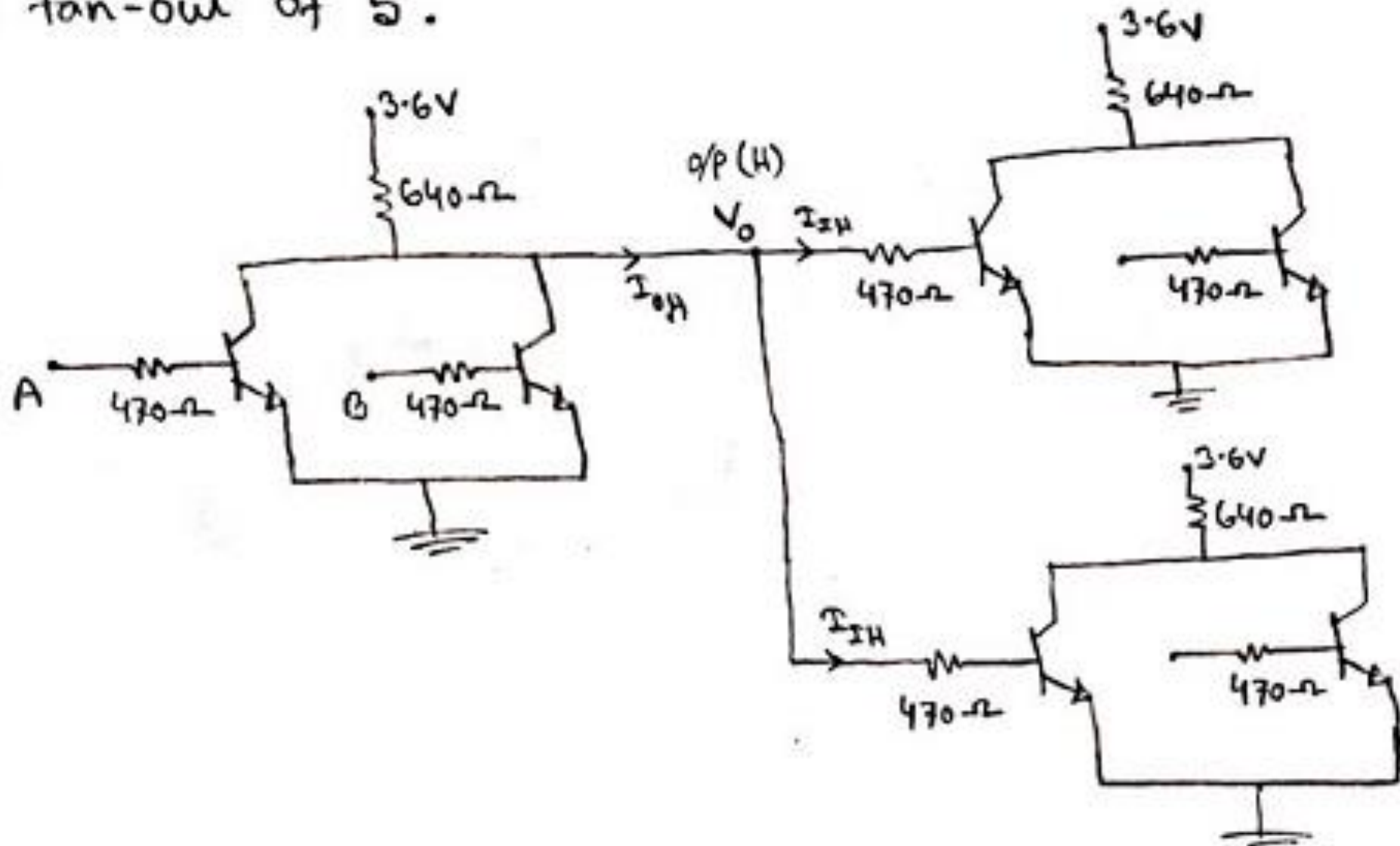
$$\therefore N = \frac{I_{OH}}{I_{IH}} = \frac{0.00406}{0.000638} = 6.36 \approx 6$$

\therefore Fan-out is 6.

A	B	Y_{NOR}
0	0	1
0	1	0
1	0	0
1	1	0

NOR for fan-out of 5.

Soln:



$$N = \frac{I_{OH}}{I_{IH}}$$

$$\Rightarrow 5 = \frac{I_{OH}}{I_{IH}}$$

$$\therefore I_{OH} = 5 I_{IH}$$

Now, KVL in driven ckt: $3.6 - 640 \times I_{OH} - V_{OH} = 0$

$$\Rightarrow -3200 I_{OH} - V_{OH} = -3.6$$

$$\therefore 3200 I_{OH} + V_{OH} = 3.6 \text{ ——— (i)}$$

KVL in load ckt: $V_{OH} - 470 I_{IH} - 0.7 = 0$

$$\therefore -470 I_{IH} + V_{OH} = 0.7 \text{ ——— (ii)}$$

Solving eqn (i) & (ii) [Using calculator],

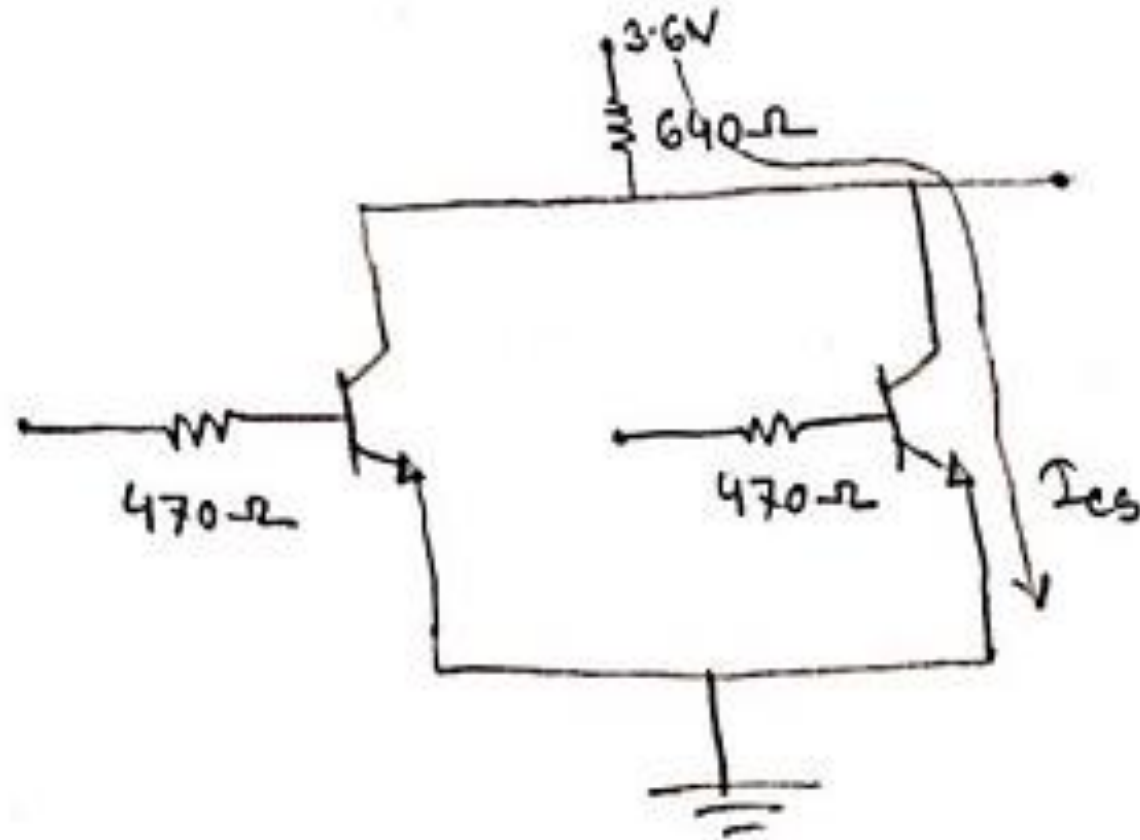
$$I_{IH} = 0.00079 \text{ A}$$

$$V_{OH} = 1.07 \text{ V}$$

$$\underline{\underline{\text{Ans: } 1.07 \text{ V}}}$$

Problem: Find the minimum i/p voltage to drive RTL NOR Transistor in saturation region.

Solⁿ:



$$I_B \geq \frac{I_{cs}}{h_{fe}}$$

$$h_{fe} = 20$$

Applying KVL: $3.6 - 640 I_{cs} - 0.2 = 0$

$$\Rightarrow I_{cs} = \frac{3.6 - 0.2}{640} = 5.31 \text{ mA}$$

$$\therefore I_B \geq \frac{I_{cs}}{h_{fe}}$$

$$\geq \frac{5.31 \text{ mA}}{20}$$

$$\geq 0.265 \text{ mA}$$

Now,

$$V_{in(\min)} - 470 I_B - 0.7 = 0$$

$$\Rightarrow V_{in(\min)} = 470 \times 0.265 \times 10^{-3} + 0.7$$

$$= 0.82 \text{ V}$$

(Ans)

DTL Logic

- The basic circuit in the DTL digital logic family is the NAND gate.
- Each input is associated with one diode.
- The diodes and the 5-k Ω resistor form an AND gate.
- The transistor serves as a current amplifier while inverting the digital signal.
- The two voltage levels are 0.2 V for the low level and between 4 and 5 V for the high level.
- The power dissipation of a DTL gate is about 12 mW.
- The propagation delay averages 30 ns.
- The noise margin is about 1 V and a fan-out as high as 8 is possible.



DTL Logic - Disadvantages

- Relatively lower speed.
- Propagation is higher than RTL.





NAND Gate Using DTL Logic

- If any input of the gate is low at 0.2 V, the corresponding input diode conducts current through V_{CC} and the 5-k Ω resistor into the input node.
- The voltage at point P is equal to the input voltage of 0.2 V plus a diode drop of 0.7 V, for a total of 0.9 V.

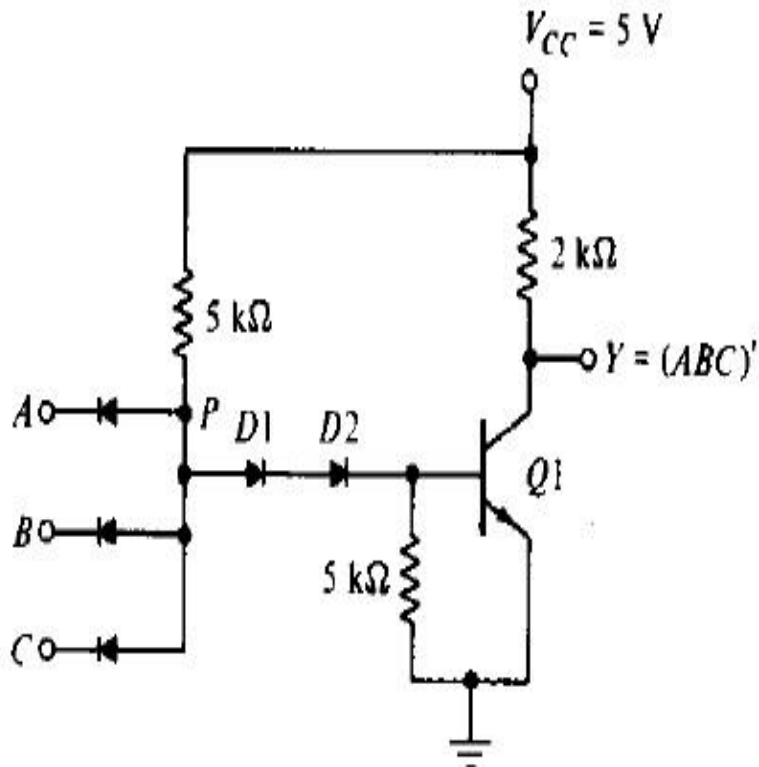
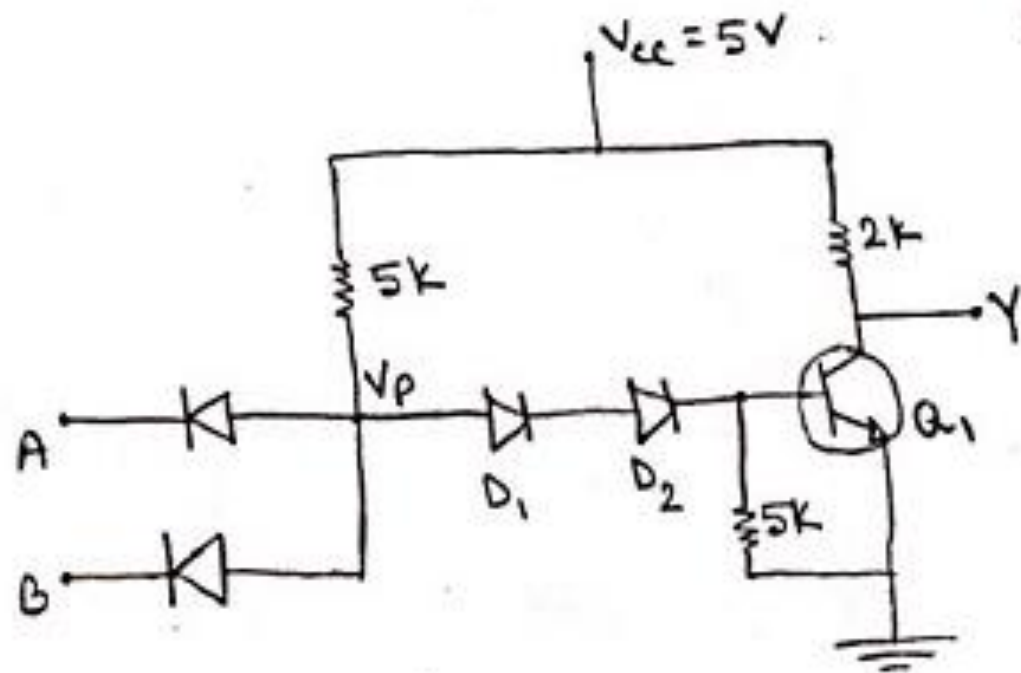


FIGURE
DTL basic NAND gate

DTL NAND:

Low Logic: $0 \sim 0.2 \text{ V}$
High Logic: $4 \sim 5 \text{ V}$



A	B	Y_{NAND}
0	0	1
0	1	1
1	0	1
1	1	0

Fig : 2 i/p DTL NAND ckt.

Operation:

If any of the i/p is low, the corresponding diode is forward biased and conducts current through $5K$ and V_{CC} .

$$\text{So, } V_p = 0.7 + 0.2 = 0.9V$$

For Q_1 to conduct,

$$V_p \geq V_{D_1} + V_{D_2} + V_{BEQ_1}$$

$$\Rightarrow V_p \geq 0.7 + 0.7 + 0.7$$

$$\geq 2.1V$$

But here, V_p is only $0.9V$

So, Q_1 is off

$$\therefore Y = V_{CC} = 5V (\text{high})$$

If all the i/p's are high, corresponding diodes are reversed biased.

$$\text{So, } V_p = V_{D_1} + V_{D_2} + V_{BEQ_1} = (0.7 + 0.7 + 0.7)V = 2.1V$$

Q_1 conducts and saturates

$$\therefore Y = V_{CE} = 0.2V (\text{low})$$

NAND Gate Using DTL Logic

- In order for the transistor to start conducting, the voltage at point P must overcome a potential of one V_{BE} drop in Q_1 plus two diode drops across D_1 and D_2 , or $3 \times 0.6 = 1.8$ V.
- Since the voltage at P is maintained at 0.9 V by the input conducting diode, the transistor is cut off and the output voltage is high at 5 V.
- If all inputs of the gate are high, the transistor is driven into the saturation region.
- The voltage at P now is equal to V_{BE} plus the two diode drops across D_1 and D_2 , or $0.7 \times 3 = 2.1$ V.
- Since all inputs are high at 5 V and $V_P = 2.1$ V, the input diodes are reverse biased and off.
- The base current is equal to the difference of currents flowing in the two 5-k Ω resistors and is sufficient to drive the transistor into saturation.
- With the transistor saturated, the output drops to V_{CE} of 0.2 V, which is the low level for the gate.





NAND Gate Using DTL Logic

Operation

**For Q1 to conduct, $V_p > V_{BE}(Q1) + (2 \times 0.7)$
 $= 0.7 \text{ V} + 1.4 \text{ V} = 2.1 \text{ V}$

Input	Transistor & Diode Status	Output
Any Input = Low (0.2V)	Corresponding input diode forward biased. $V_p = (0.2 + 0.7) \text{ V}$	As $V_p < 2.1 \text{ V}$, Q1 is OFF. Cutoff region. $Y = V_{CC} = 5 \text{ V}$ (High)
All input = High (5 V)	All input diode reverse biased. D1 & D2 forward biased. Q1 ON. Saturation region. $V_p = V_{BE}(Q1) + V_{D1} + V_{D2}$ $= 0.7 + 0.7 + 0.7 = 2.1 \text{ V}$	Q1 is ON. Saturation region. $Y = V_{CE} = 0.2 \text{ V}$ (Low)

Circuit

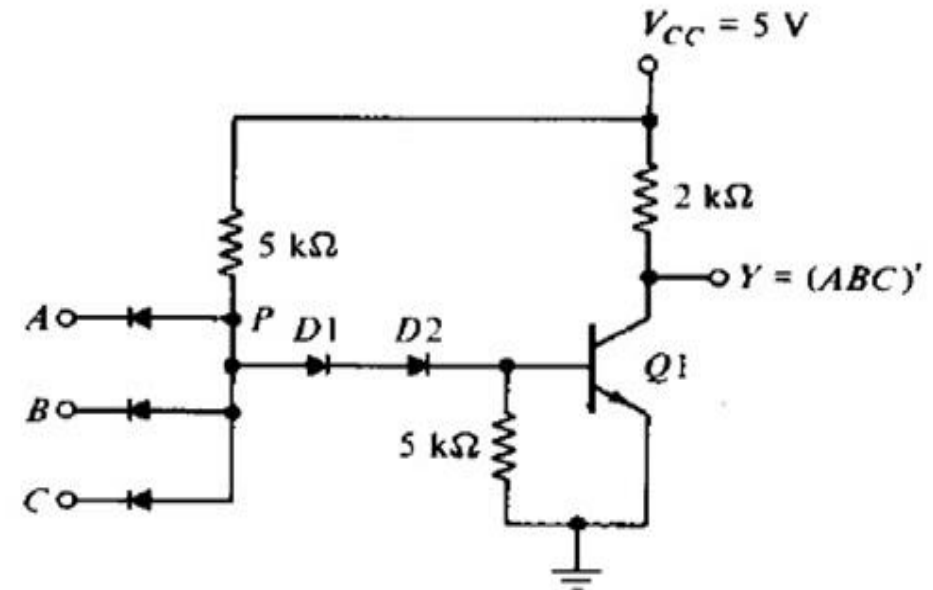
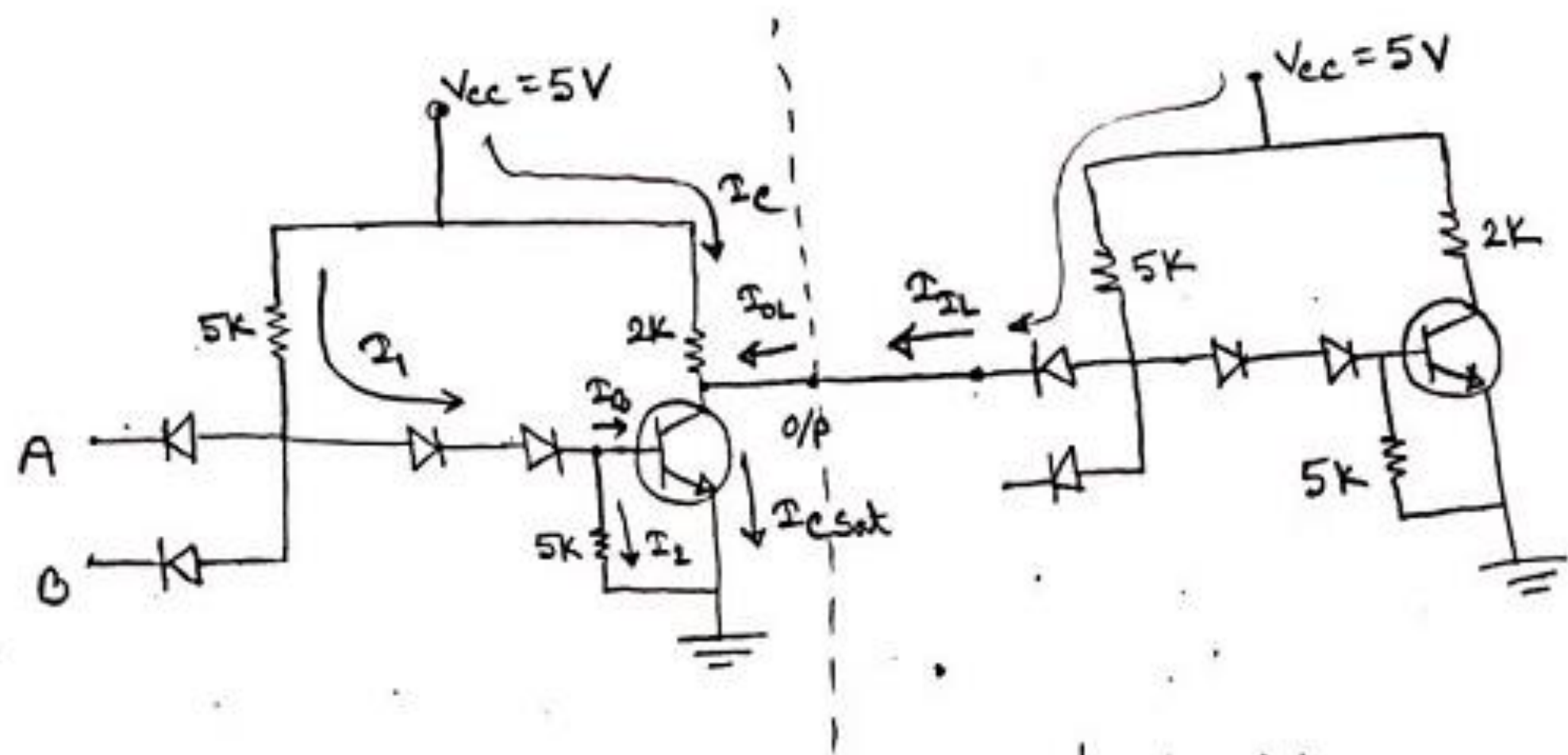


FIGURE
DTL basic NAND gate

Q) Fan-out calculation of DTL NAND :



Fan-out, $N = \frac{I_{OL}}{I_{IL}}$

Applying KVL in load ckt.,

$$5 - I_{IL} \times 5K - 0.7 - 0.2 = 0$$

$$\therefore I_{IL} = 0.82 \text{ mA} \text{ --- (i)}$$

Calculation in driven ckt.,

Applying KCL,

$$I_c + I_{OL} = I_{csat}$$

$$\therefore I_{OL} = I_{csat} - I_c \text{ --- (ii)}$$

Now,

$$I_1 = I_B + I_2$$

$$\Rightarrow I_B = I_1 - I_2$$

$$= \frac{5 - 2.1}{5K} - \frac{0.7}{5K}$$

$$= 0.58 \text{ mA} - 0.14 \text{ mA}$$

$$= 0.44 \text{ mA}$$

A	B	Y_{WAND}
0	0	1
0	1	1
1	0	1
1	1	0

In saturation,

$$I_B \geq \frac{I_{\text{sat}}}{h_{FE}}$$

$$\begin{aligned}\therefore I_{\text{sat}} &= I_B \times h_{FE} \\ &= 0.44 \text{ mA} \times 20 [\because h_{FE} = 20] \\ &= 8.8 \text{ mA}\end{aligned}$$

Again, Applying KVL for determining I_C ,

$$5 - I_C \times 2K - 0.2 = 0$$

$$\therefore I_C = 2.4 \text{ mA}$$

$$\begin{aligned}\text{Eqn (ii)} \Rightarrow I_{OL} &= I_{\text{sat}} - I_C \\ &= 8.8 \text{ mA} - 2.4 \text{ mA} \\ &= 6.4 \text{ mA} \quad \text{--- (iii)}\end{aligned}$$

$$\begin{aligned}\therefore \text{Fan-out, } N &= \frac{I_{OL}}{I_{IL}} \\ &= \frac{6.4 \text{ mA}}{0.82 \text{ mA}} [\text{eqn (i) \& (iii)}] \\ &= 7.8 \\ &\approx 7\end{aligned}$$

So, Fan-out is 7.



NAND Gate Using modified DTL Logic

- The fan-out of the DTL gate is limited by the maximum current that can flow in the collector of the saturated transistor.
- The fan-out of a DTL gate may be increased by replacing one of the diodes in the base circuit with a transistor.

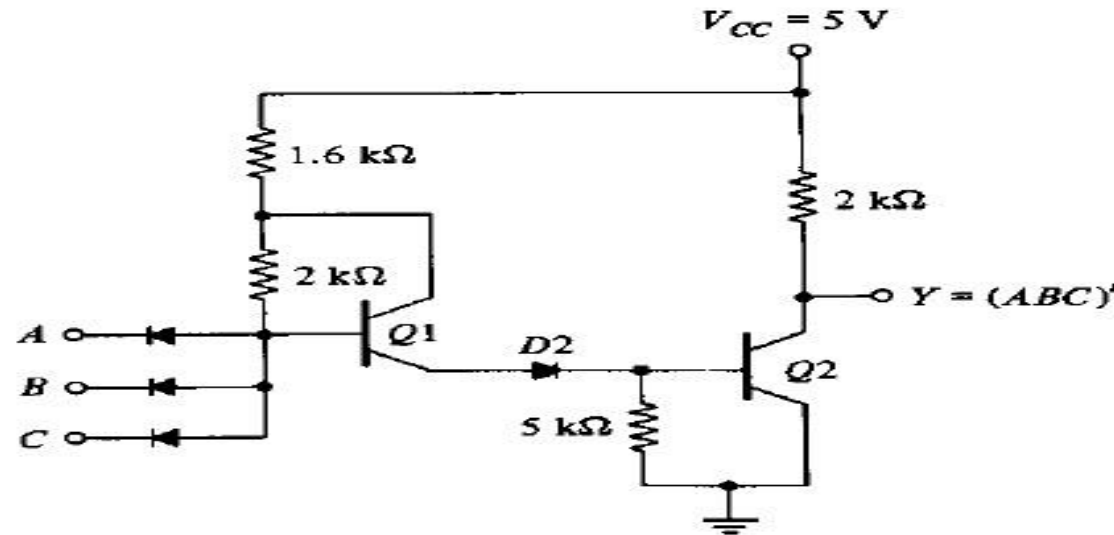


FIGURE
Modified DTL gate



NAND Gate Using modified DTL Logic

- Transistor $Q1$ is maintained in the active region when output transistor $Q2$ is saturated.
- As a consequence, the modified circuit can supply a larger amount of base current to the output transistor.
- The output transistor can now draw a larger amount of collector current before it goes out of saturation.
- Part of the collector current comes from the conducting diodes in the loading gates when $Q2$ is saturated.
- Thus, an increase in allowable collector saturated current allows more loads to be connected to the output, which increases the fan-out capability of the gate.

Modified DTL NAND :

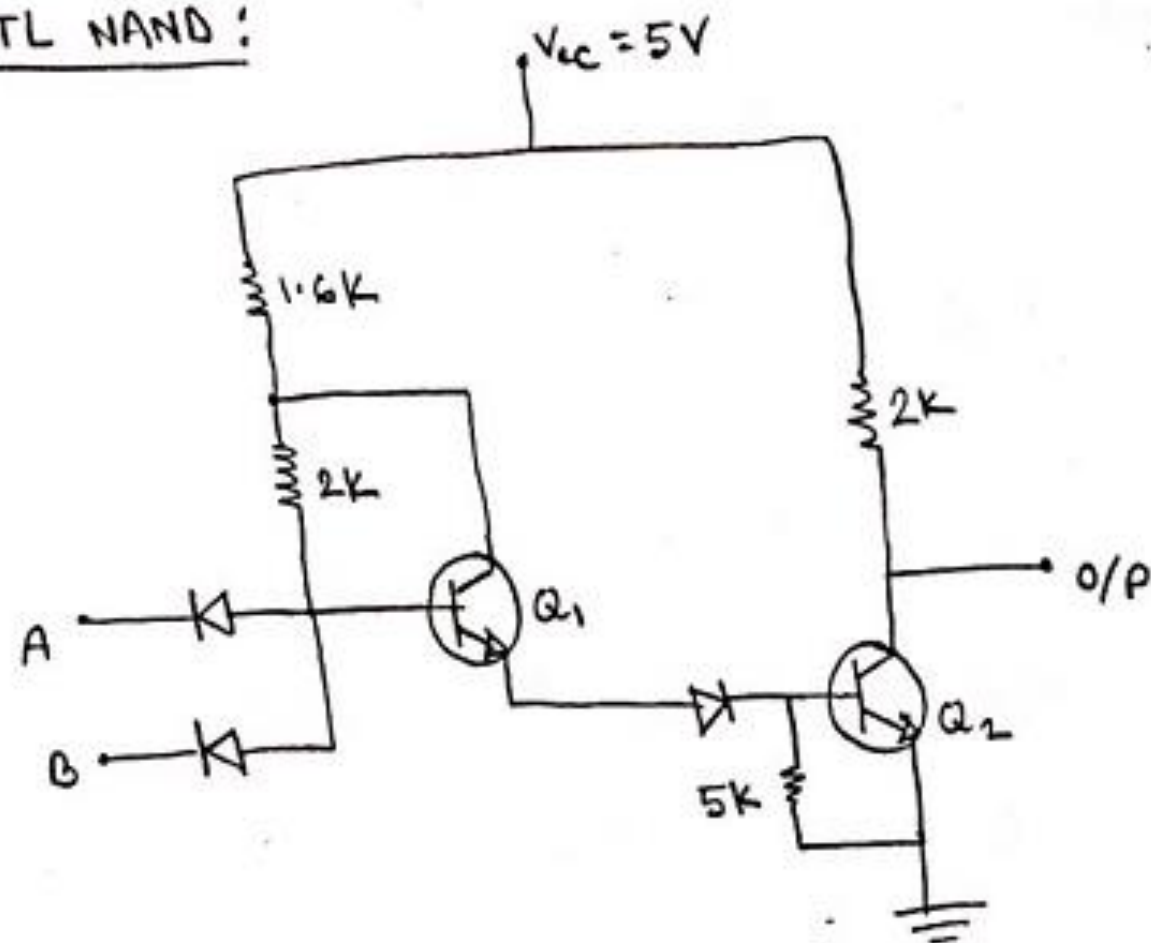
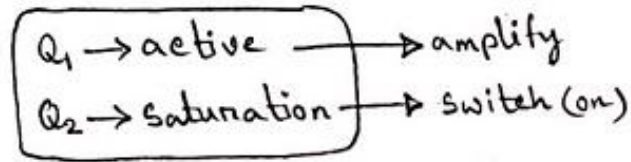


Fig: Modified DTL NAND ckt.

The modified DTL ckt. will be able to provide larger base current to the o/p transistor. The o/p transistor can now draw a larger amount of collector current before it goes into saturation.

Therefore, an increase in allowable collector saturated current allows more loads to be connected to the o/p, which increases the fan-out capability of the gate.



$$\begin{aligned} I_E &= I_C + I_B \\ &= h_{fe} I_B + I_B \\ &= 20 I_B + I_B \\ &= 21 I_B \end{aligned}$$

$$\begin{aligned} I_C &= \beta I_B \\ \therefore I_B &\uparrow \\ \therefore I_C &\uparrow \\ \therefore N &\uparrow \end{aligned}$$

Here, 21 times base current increased. For this reason fanout increases a lot and becomes $N=25$.



NAND Gate Using HTL Logic

- Due to presence of electrical motor's on-off control circuits, High voltage switches etc. are used in industrial environment, Thereby noise level is very high.
- So DTL redesigned with a power supply of 5V and the D2 is replaced by a zener diode with a breakdown voltage of 6.9 V.
- So HTL posses a high threshold of noise immunity.
- To conduct Q2, the emitter of Q1 must rise to a potential,
$$V_{BE}(Q2) + V_Z = 0.7 + 6.9 = 7.6 \text{ V}$$
- So, Only if the noise signal is greater than 7.6 V , then it will be able to change the state. Higher noise immunity.

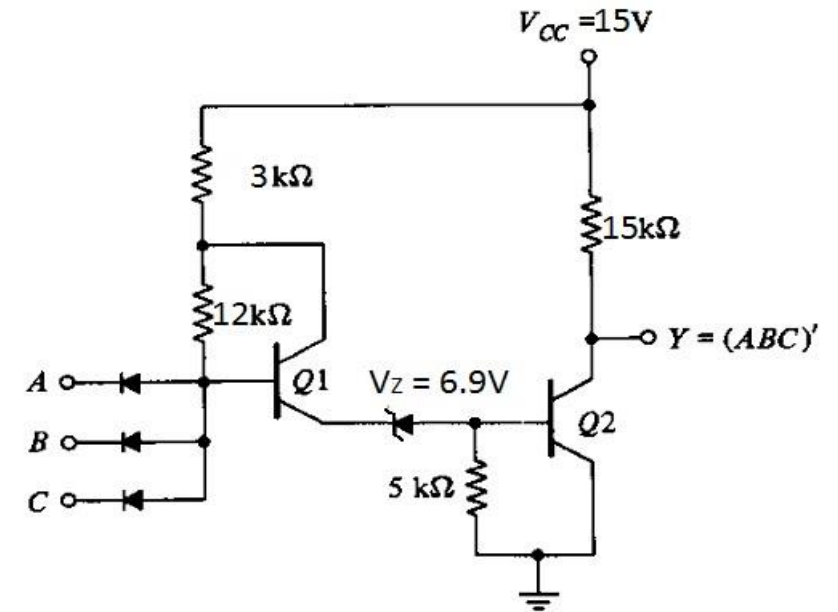
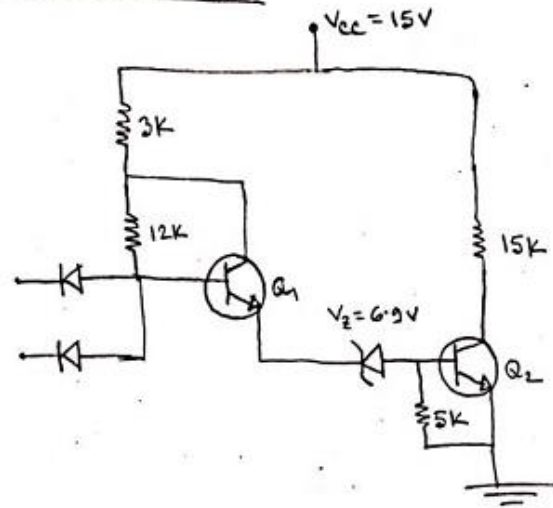


Figure: 3 Input HTL NAND

HTL (High-Threshold Logic)



→ Due to the presence of electric motor's off-on control ckt., high voltage switches are used in an industrial environment, thereby the noise level is quite high.

So, DTL is redesigned by a 15V power supply with a Zener diode of 6.9V.

→ HTL possesses a high threshold to noise immunity
(Noise margin → 7.5V)



TTL Logic

- The original basic TTL gate was a slight improvement over the DTL gate.
- As the TTL technology progressed, additional improvements were added to the point where this logic family became the most widely used family in the design of digital systems.
- The propagation delay of a transistor circuit that goes into saturation depends mostly on two factors: **storage time and RC time constants**.
- Reducing the storage time decreases the propagation delay. [$RC \downarrow T_p \downarrow$]
- Reducing resistor values in the circuit reduces the RC time constants and decreases the propagation delay.
- Of course, the trade-off is higher power dissipation because lower resistances draw more current from the power supply. **The speed of the gate is inversely proportional to the propagation delay.**
- In the **low-power TTL gate**, the resistor values are higher than in the standard gate to reduce the power dissipation, but the propagation delay is increased. [$R \uparrow$ so $P_D \downarrow$ but $T_p \uparrow$]
- In the **high-speed TTL gate**, resistor values are lowered to reduce the propagation delay, but the power dissipation is increased. . [$R \downarrow$ so $T_p \downarrow$ but $P_D \uparrow$]



TTL Logic

- The Schottky TTL gate was the next improvement in the technology.
- The effect of the Schottky transistor is to remove the storage time delay by preventing the transistor from going into saturation.
- The low-power Schottky TTL sacrifices some speed for reduced power dissipation.
- It is equal to the standard TTL in propagation delay, but has only one fifth the power dissipation
- Recent innovations have led to the development of the advanced Schottky series.
- The advanced low-power Schottky has the lowest speed-power product and is the most efficient series. It is replacing all other low-power versions in new designs.
- TTL gates in all the available series come in three different types of output configuration:
 1. Open-collector output
 2. Totem-pole output
 3. Three-state (or tristate) output



Open Collector Output (NAND)

- The multiple emitters in transistor $Q1$ are connected to the inputs. These emitters behave most of the time like the **input diodes** in the DTL gate since they form a pn junction with their common base.
- The base-collector junction of $Q1$ acts as another pn junction diode corresponding to $D1$ in the DTL gate.
- Transistor $Q2$ replaces the second diode, $D2$, in the DTL gate. The output of the TTL gate is taken from the open collector of $Q3$.
- A resistor connected to V_{CC} must be inserted external to the IC package for the output to "pull up" to the high voltage level when $Q3$ is off; otherwise, the output acts as an open circuit.

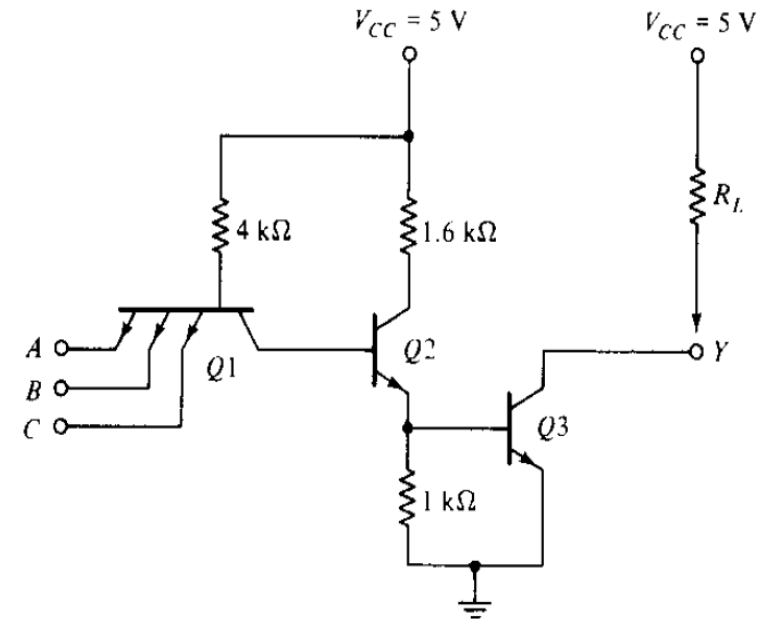


FIGURE
Open-collector TTL gate



Open Collector Output (NAND)

Condition:

❖ For Q3 to start conducting, the path from Q1 to Q3 must overcome.

= One diode drop in B-C junction of Q1 + two V_{BE} drop in Q2 & Q3 = $3 \times 0.7 = 2.1 \text{ V}$

Operation:

Input	Transistor & Diode Status	Output
Any Input = Low(0.2V)	Corresponding BE junction of Q1 is forward biased. Voltage at base of Q1 = $0.2\text{V (I/P)} + 0.7\text{ V (}V_{BE}\text{)} = 0.9\text{V}$	$V_{BE}(\text{Q1}) = 0.9 \text{ V}$. So, Q2 & Q3 Cutoff. $Y = V_{CC} = 5 \text{ V (High)}$
All input = High (5 V)	All BE junction of Q1 is reversed biased. Q2 & Q3 saturation region.	$V_{BE}(\text{Q1}) = 2.1 \text{ V}$. So, Q2 & Q3 Saturates. $Y = V_{CE}(\text{Q3}) = 0.2 \text{ V (Low)}$

Circuit

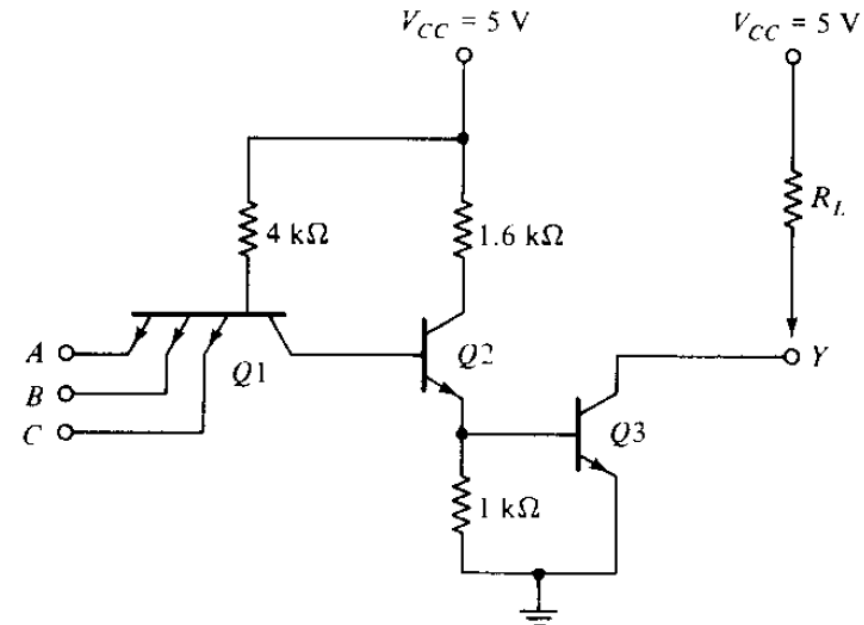


FIGURE
Open-collector TTL gate



Open Collector Output (NAND)

Open-collector gates are used in three major applications:

1. Driving a lamp or relay
2. Performing wired logic
3. Construction of a common-bus system.

External resistor advantage:

- Without an external resistor, the output of the gate will be an open circuit when Q3 is off. An open circuit to an input of a TTL gate behaves as if it has a high-level input (but a small amount of noise can change this to a low level).
- So, External resistor is recommended because of the low noise immunity encountered.



Totem pole Output (NAND)

- The output impedance of a gate is normally a resistive plus a capacitive load.
- The capacitive load consists of the capacitance of the output transistor, the capacitance of the fan-out gates, and any stray wiring capacitance.
- When the output changes from the low to the high state, the output transistor of the gate goes from saturation to cutoff and the total load capacitance, C , charges exponentially from the low to the high voltage level with a time constant equal to RC .
- For the open-collector gate, R is the external resistor marked R_L .
typical operating value $C = 15 \text{ pF}$ and $R_L = 4 \text{ k}\Omega$. Propagation delay, $t_p = 35\text{ns}$.
- With an *active pull-up* circuit replacing the passive pull-up resistor R_L , the propagation delay is reduced to 10 ns .



Totem pole Output (NAND)

Condition

- The reason for placing the diode in the circuit is to provide a diode drop in the output path and thus ensure that Q4 is cut off when Q3 is saturated.
- For Q3 to start conducting, the path from Q1 to Q3 must overcome.
= One diode drop in B-C junction of Q1 + two V_{BE}
drop in Q2 & Q3 = $3 \times 0.7 = 2.1 \text{ V}$
- To conduct Q4, base voltage must have = $0.7 (V_{BE} \text{ of } Q4) + 0.7 (D1) = 1.4 \text{ V}$.

Input	Transistor & Diode Status	Output
Any Input = Low(0.2V)	Corresponding BE junction of Q1 is forward biased. Voltage at base of Q1 = $0.2\text{V (I/P)} + 0.7 \text{ V (} V_{BE} \text{)} = 0.9\text{V}$ Voltage at base of Q2 = 5V	<ul style="list-style-type: none"> Q2 & Q3 Cutoff. Q4 Conducts. D1 Forward biased. Y = (High)
All input = High (5 V)	All BE junction of Q1 is reversed biased. Q2 & Q3 saturation region. Q4 Cutoff region.	$V_{BE} (Q1) = 2.1 \text{ V}$. So, Q2 & Q3 Saturates. $V_B (Q4) = 0.9\text{V}$. So, Q4 cutoff. $Y = V_{CE}(Q3) = 0.2\text{V (Low)}$

Circuit

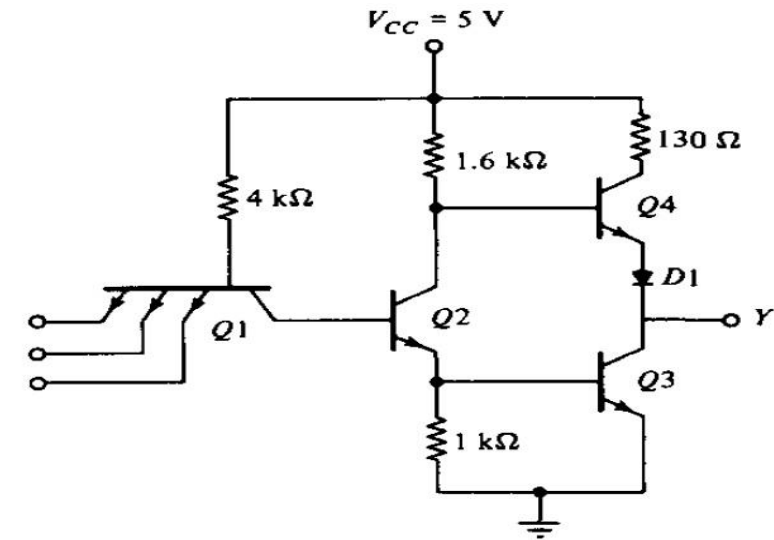


FIGURE
TTL gate with totem-pole output

****This configuration is called a *totem-pole* output because transistor Q4 "sits" upon Q3.**



Totem pole Output (NAND)

Advantage of totem pole output:

- When the output changes to the high state because one of the inputs drops to the low state, transistors $Q2$ and $Q3$ go into cutoff. However, the output remains momentarily low because the voltages across the load capacitance cannot change instantaneously.
- The current needed to charge the load capacitance causes $Q4$ to momentarily saturate, and the output voltage rises with a time constant RC .
- But R in this case is equal to 130Ω , plus the saturation resistance of $Q4$, plus the resistance of the diode, for a total of approximately 150Ω .
- This value of R is much smaller than the passive pull-up resistance used in the open-collector circuit.
- As a consequence, the transition from the low to high level is much faster.



Schottky TTL Gate

- The **Schottky diode** is formed by the junction of a metal and semiconductor, in contrast to a conventional diode, which is formed by the junction of p-type and *n-type* semiconductor material.
- A reduction in storage time results in a reduction of propagation delay. This is because the time needed for a transistor to come out of saturation delays the switching of the transistor from the on condition to the off condition
- Saturation can be eliminated by placing a Schottky diode between the base and collector of each saturated transistor in the circuit.
- The voltage across a conducting Schottky diode is **only 0.4 V**.
- The presence of a Schottky diode between the base and collector prevents the transistor from going into saturation. The resulting transistor is called a **Schottky transistor**.
- The use of Schottky transistors in a TTL decreases the propagation delay without a sacrifice of power dissipation.



Schottky Diode TTL

Description

- The special symbol used for the Schottky transistors and diodes.
- An exception is made of $Q4$ since it does not saturate, but stays in the active region.
- Resistor values have been reduced to further decrease the propagation delay.
- Two new transistors, $Q5$ and $Q6$ have been added, and Schottky diodes are inserted between each input terminal and ground. There is no diode in the totem-pole circuit.
- The new combination of $Q5$ and $Q4$ still gives the two V_{BE} drops necessary to prevent $Q4$ from conducting when the output is low. This combination comprises a double emitter-follower called a **Darlington pair**. The Darlington pair provides a very high current gain and extremely low resistance. This is exactly what is needed during the low-to-high swing of the output, resulting in a decrease of propagation delay.

Circuit

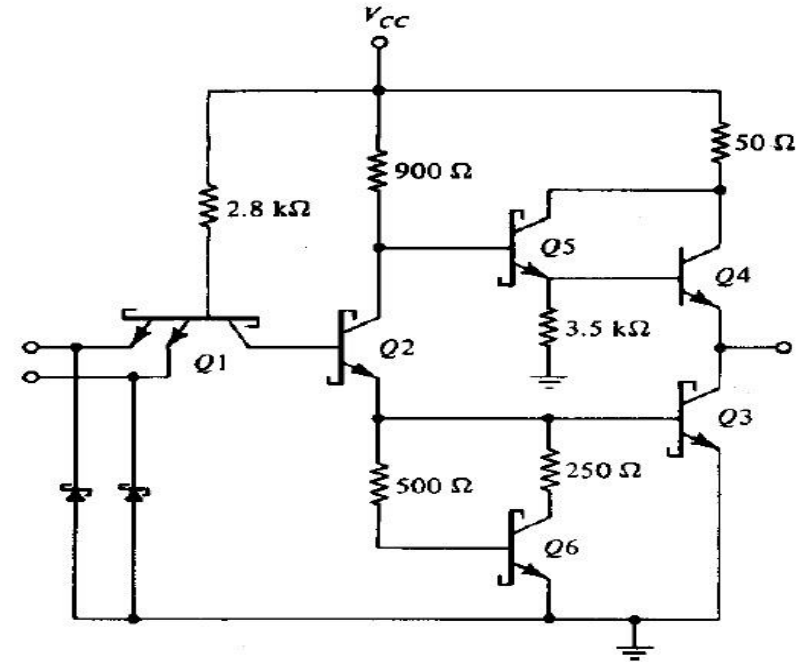
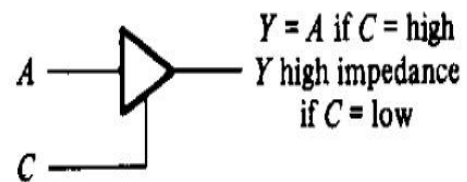


FIGURE
Schottky TTL gate

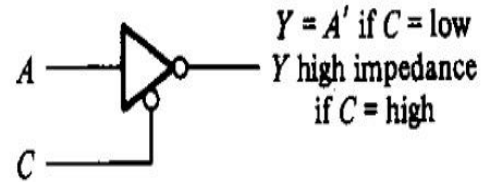


Three-state Gate

- The outputs of two TTL gates with totem-pole structures cannot be connected together as in open-collector outputs.
- However, a special type of totem-pole gate that allows the wired connection of outputs for the purpose of forming a common-bus system. When a totem-pole output TTL gate has this property, it is called *a three-state (or tristate) gate*.



(a) Three-state buffer gate



(b) Three-state inverter gate



Three-state Gate

Description

- A three-state gate exhibits three output states:
 - (1) A low-level state when the lower transistor in the totem-pole is on and the upper transistor is off,
 - (2) A high-level state when the upper transistor in the totem-pole is on and the lower transistor is off, and
 - (3) A third state when both transistors in the totem-pole are off. The third state provides an open circuit or high-impedance state that allows a direct wire connection of many outputs to a common line. Three-state gates eliminate the need for open-collector gates in bus configurations.

Circuit

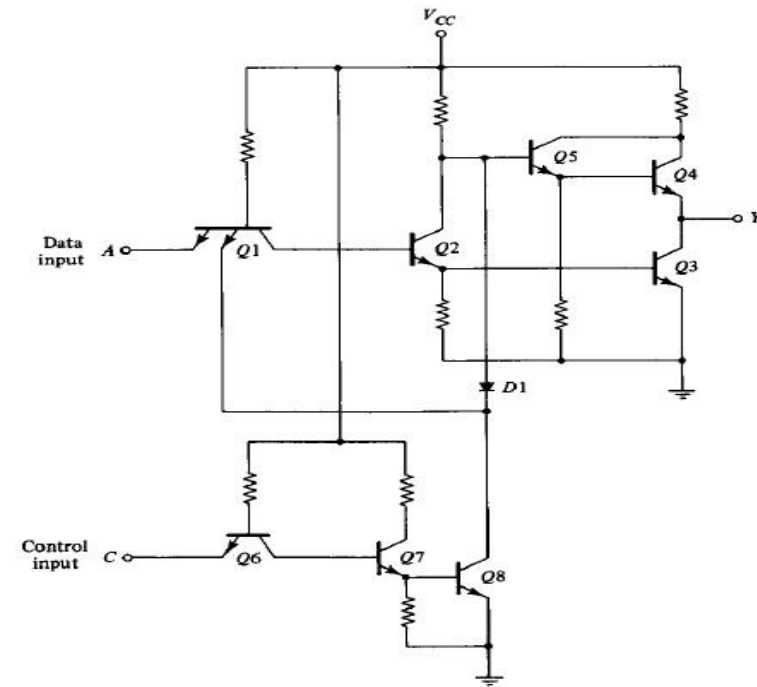
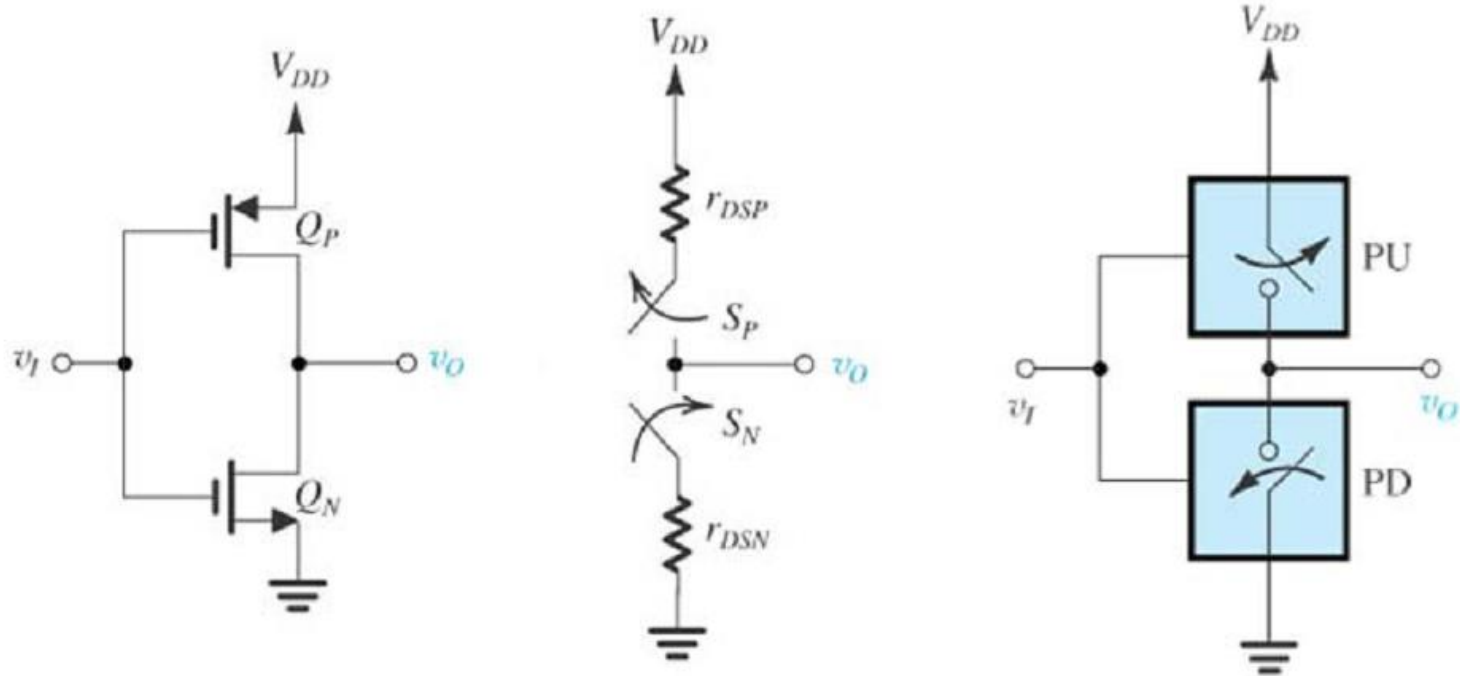


FIGURE
Three-state TTL gate

Circuit diagram for the three-state inverter

CMOS inverter

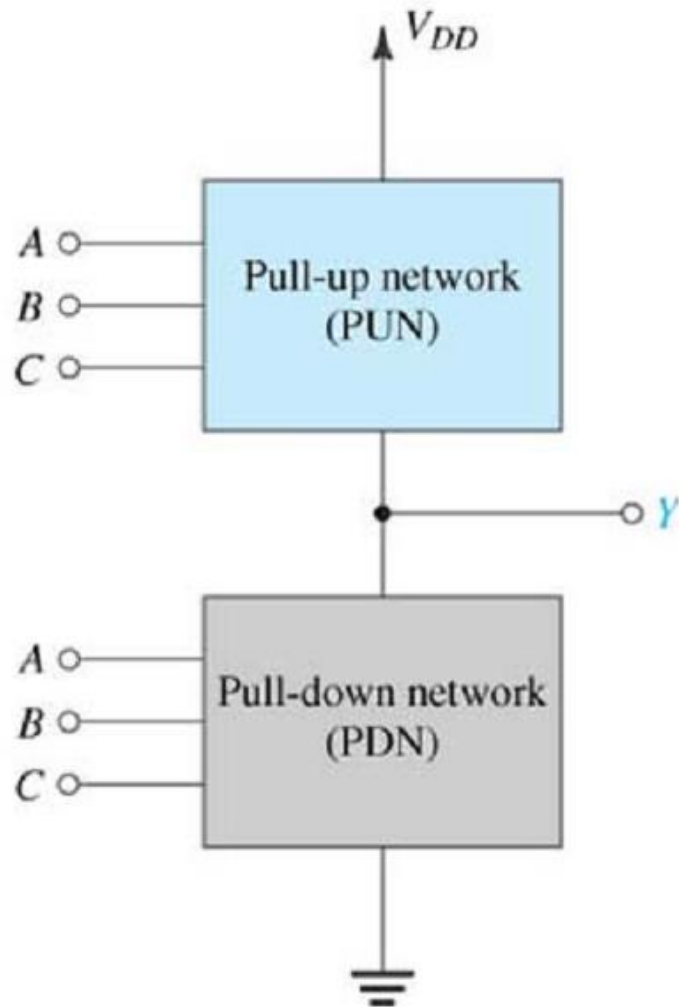


Inverter Circuit

Fig (a) shows a CMOS inverter schematic

Fig (b) shows a CMOS inverter effective resistance model

Fig (c) shows the inverter switch level

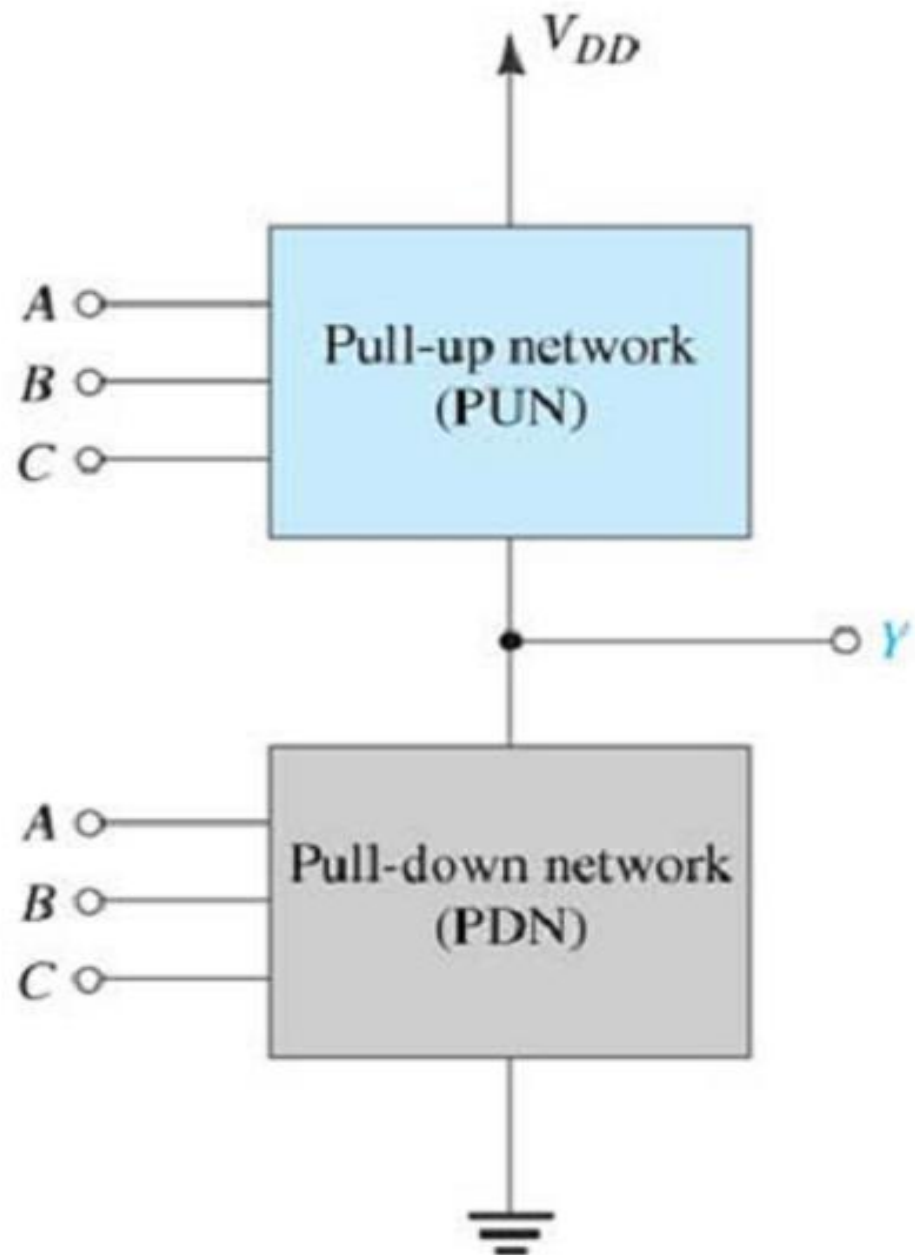


Network of PMOS
transistors

Network of NMOS
transistors

- The pull-up network is made up of only P-MOS
- The pull-down network is made up of only N-MOS

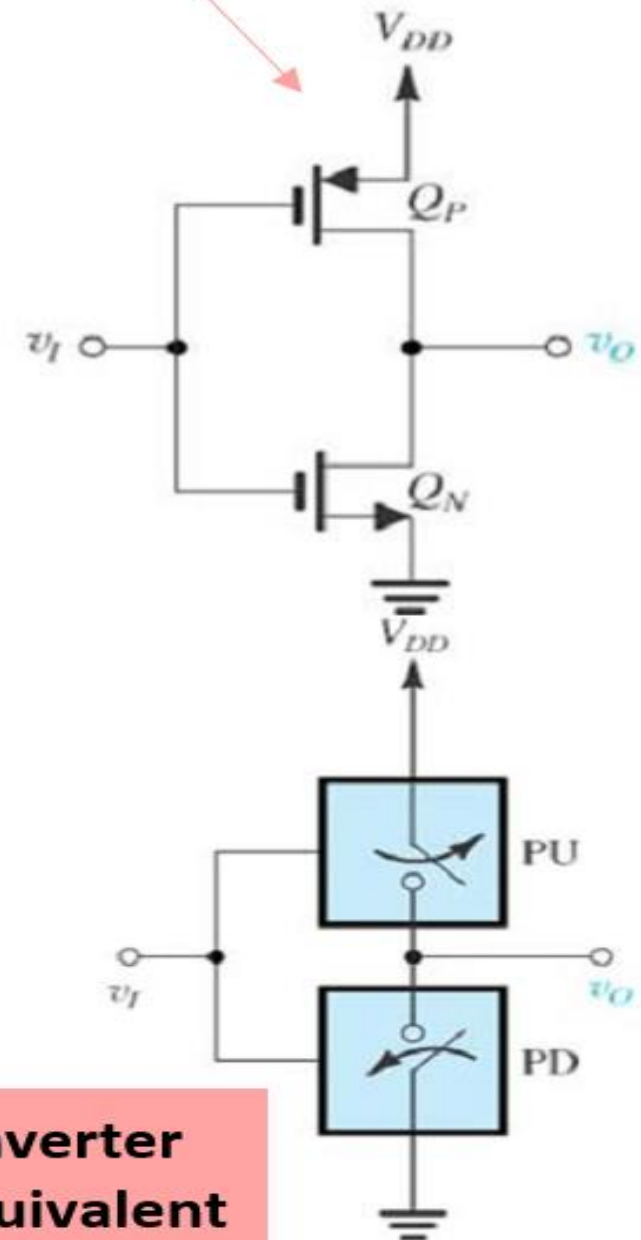
Transistor Configurations:



Network of PMOS transistors

Network of NMOS transistors

CMOS Inverter

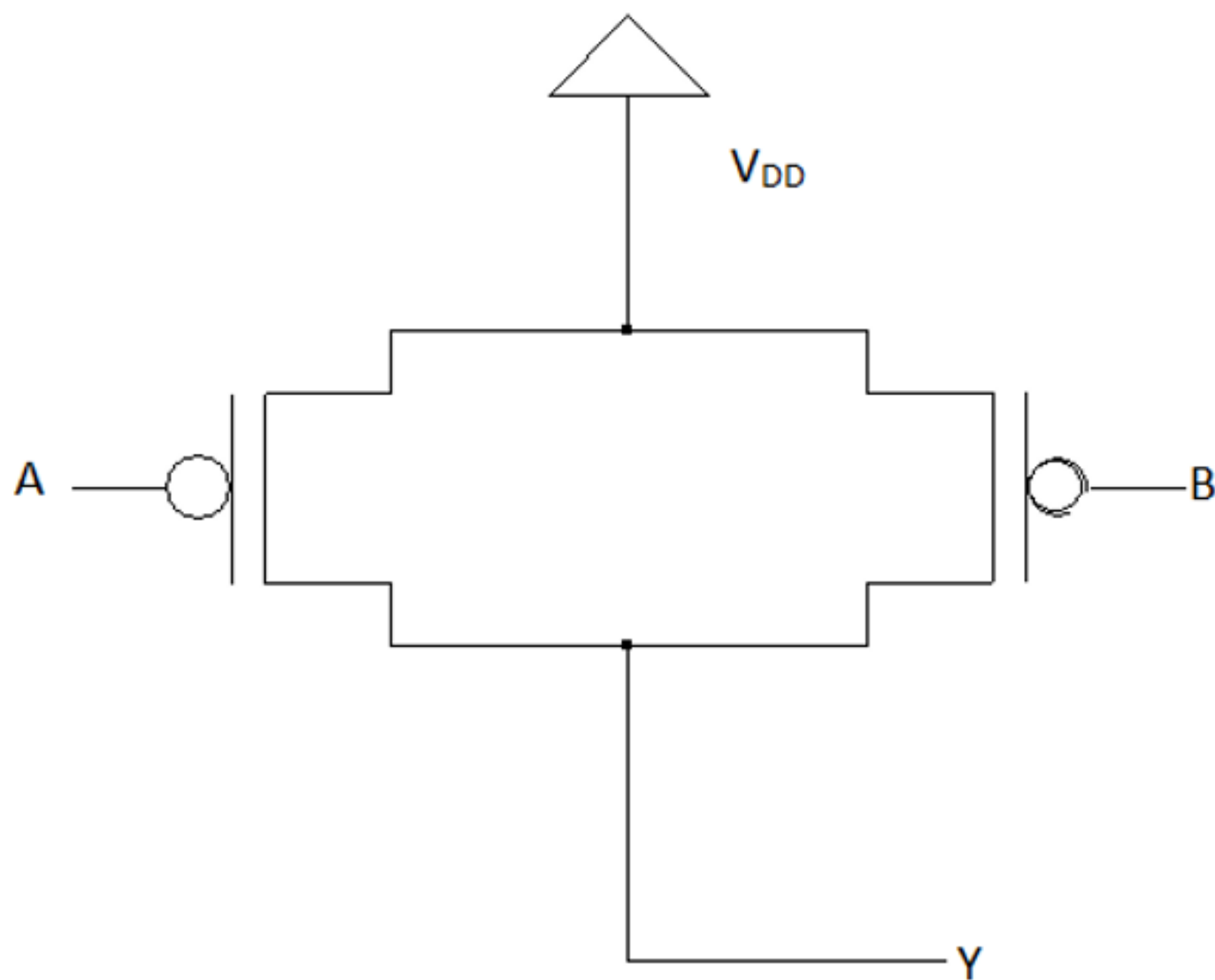


CMOS Inverter
Switch Equivalent

Points to Remember

- P-MOS is used for designing pull-up networks in combinational logic design with CMOS.
- N-MOS is used for designing pull-down networks in combinational logic design with CMOS.
- P-MOS is responsible for driving the output to logic 1/high/ VDD.
- P-MOS is activated using a logic 0/LOW at its gate terminal
- N-MOS is responsible for driving the output to logic 0/LOW/GND
- N-MOS is activated by logic 1/HIGH at its gate terminal.

Parallel Combination of P-MOS:

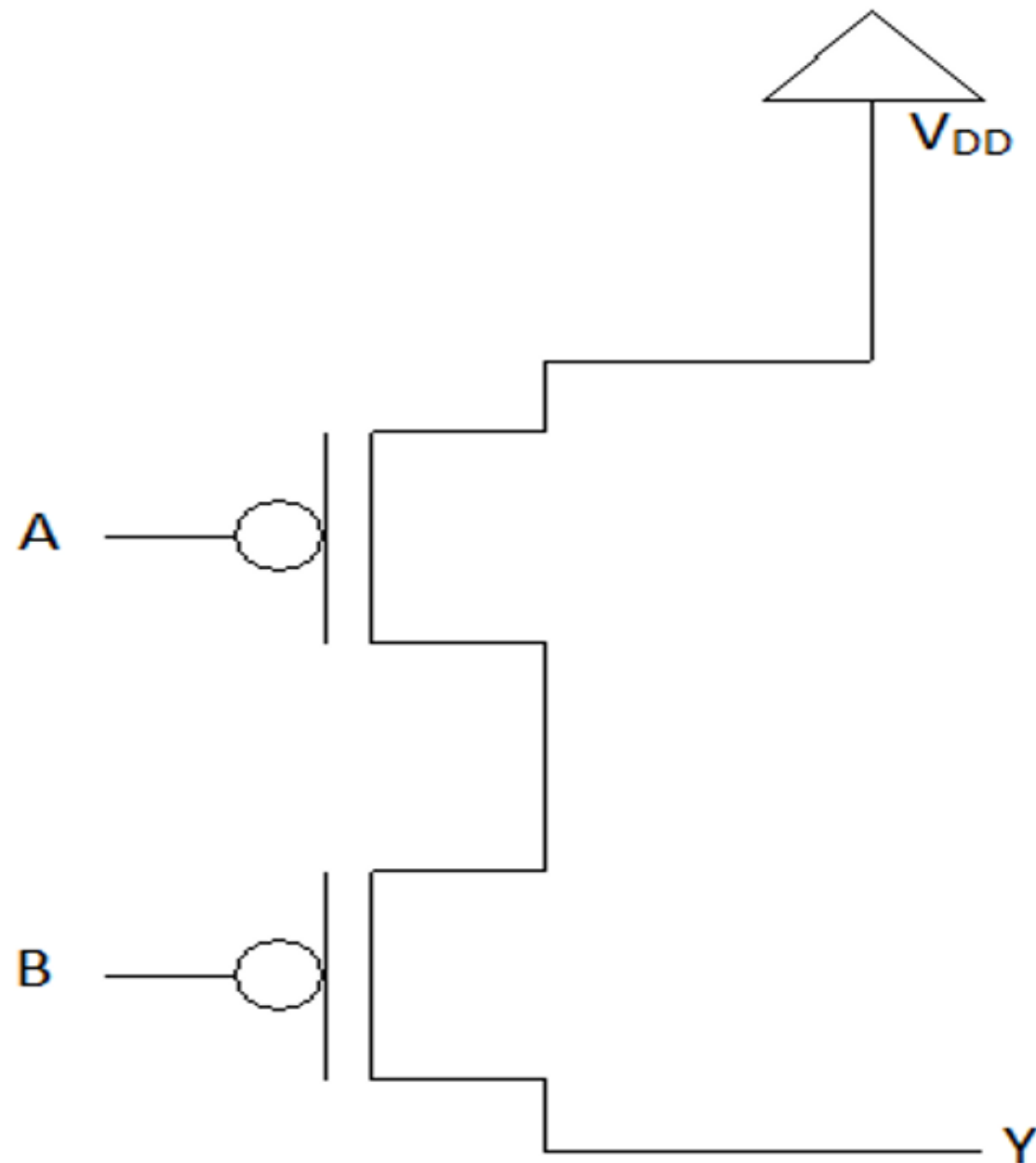


For **Y to be HIGH**, either P-MOS A **OR** P-MOS B has to be active.

For **Y to be HIGH**, either Input A has to be **low/0** **OR** input B has to be **low/0**

$$Y = \bar{A} + \bar{B}$$

Series combination of P-MOS:



☒ For **Y to be HIGH**, both **P-MOS A** **AND** **P-MOS B** has to be active.

☒ For **Y to be HIGH**, both **Input A** **AND** **Input B** has to be **low/0**.

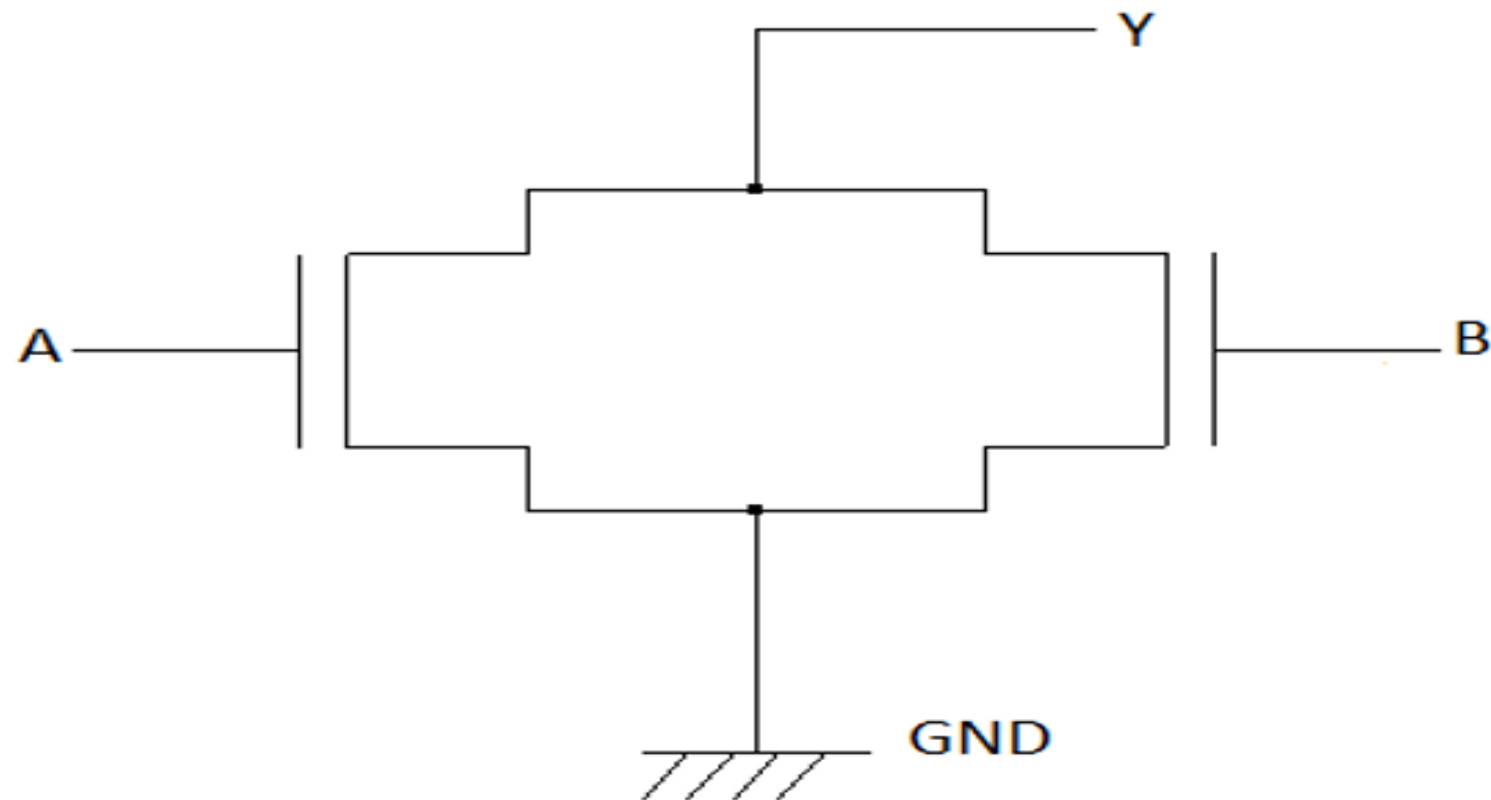
$$Y = \overline{A} . \overline{B}$$

DeMorgan's Laws:

1. $\overline{A + B} = \overline{A} \cdot \overline{B}$

2. $\overline{A \cdot B} = \overline{A} + \overline{B}$

Parallel Combination of N-MOS:

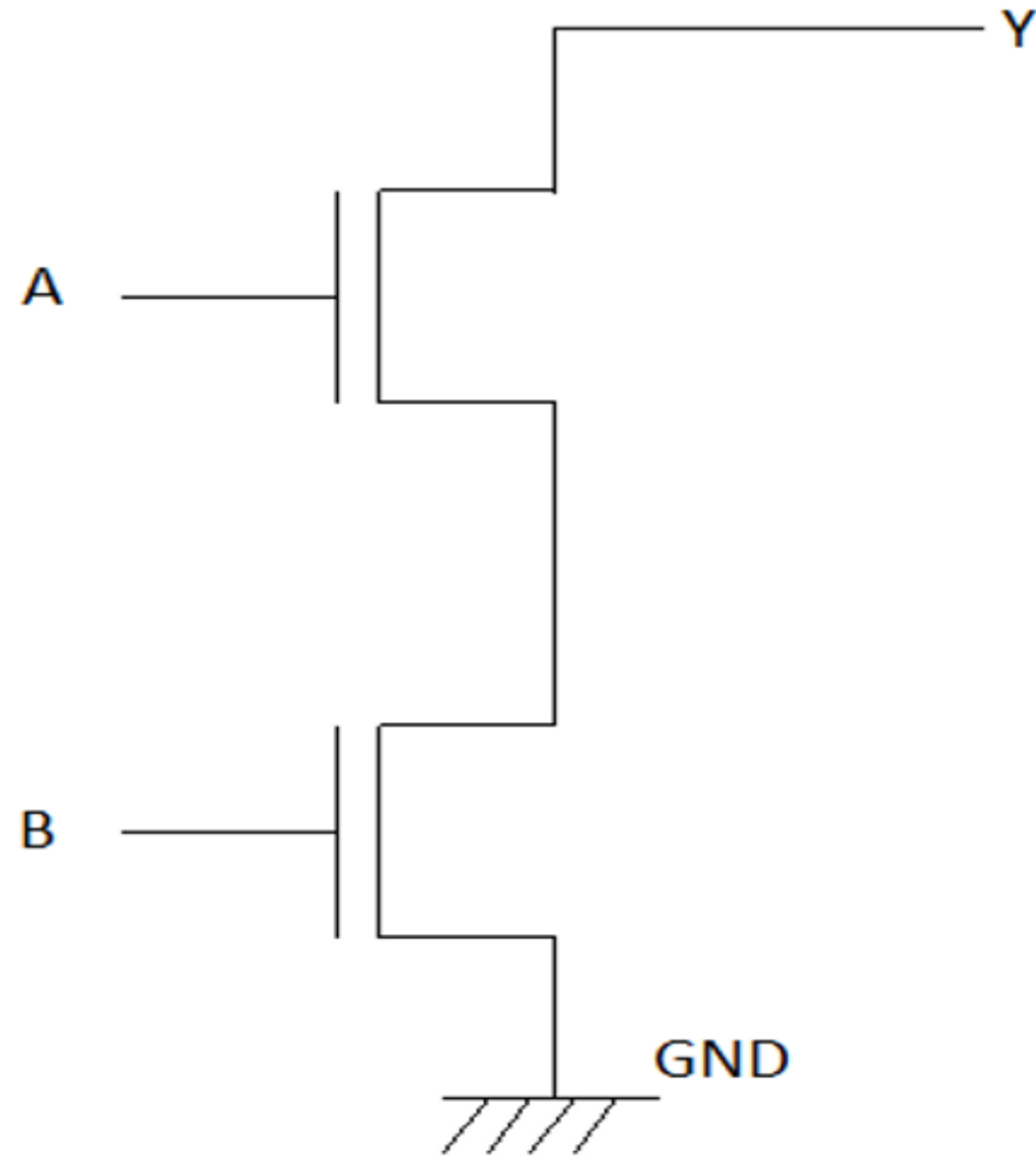


📖 For **Y to be Low**,
either **N-MOS A OR N-MOS B** has to be **active**.

📖 For **Y to be Low**,
either **input A OR input B** has to be **high**.

$$\overline{Y} = A + B$$

Series combination of N-MOS:



☒ For **Y to be Low**, both **N-MOS A** **AND** **N-MOS B** has to be **active**.

☒ For **Y to be Low**, either **input A** **AND** **input B** has to be **high**.

$$\overline{Y} = A.B$$

Designing a Complex/Compound gate:

For Designing complex gates, the following steps have to be followed, in order to come up with a proper design.

1. Both pull-up and pull-down network designs are required.
2. Design requirements are fulfilled using bottom up approach.
3. For complementary MOSFET designs, the pull-down network is designed first.
4. The pull-up network is designed afterwards using De Morgan's Law to break down the equation.

Designing a NAND gate:

SOP Expression:

$$Y = \overline{A \cdot B}$$

Truth Table:

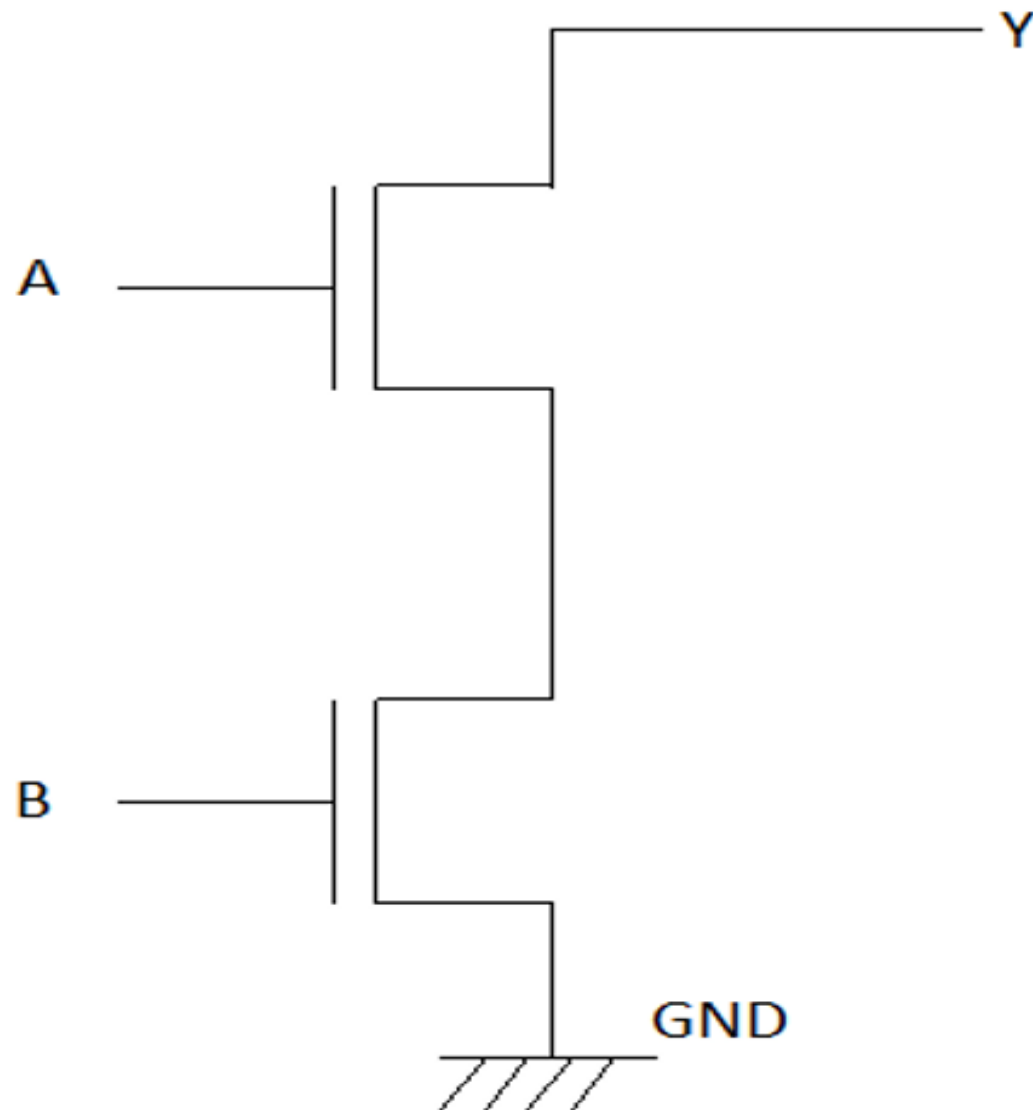
A	B	Y
0	0	1
0	1	1
1	0	1
1	1	0

Pull-down network Design:

For Designing the Pull-down network, the equation has to be modified so that the output becomes low.

$$\rightarrow \overline{Y} = A \cdot B$$

According to the logic available, it matches with the series combination of N-MOS.



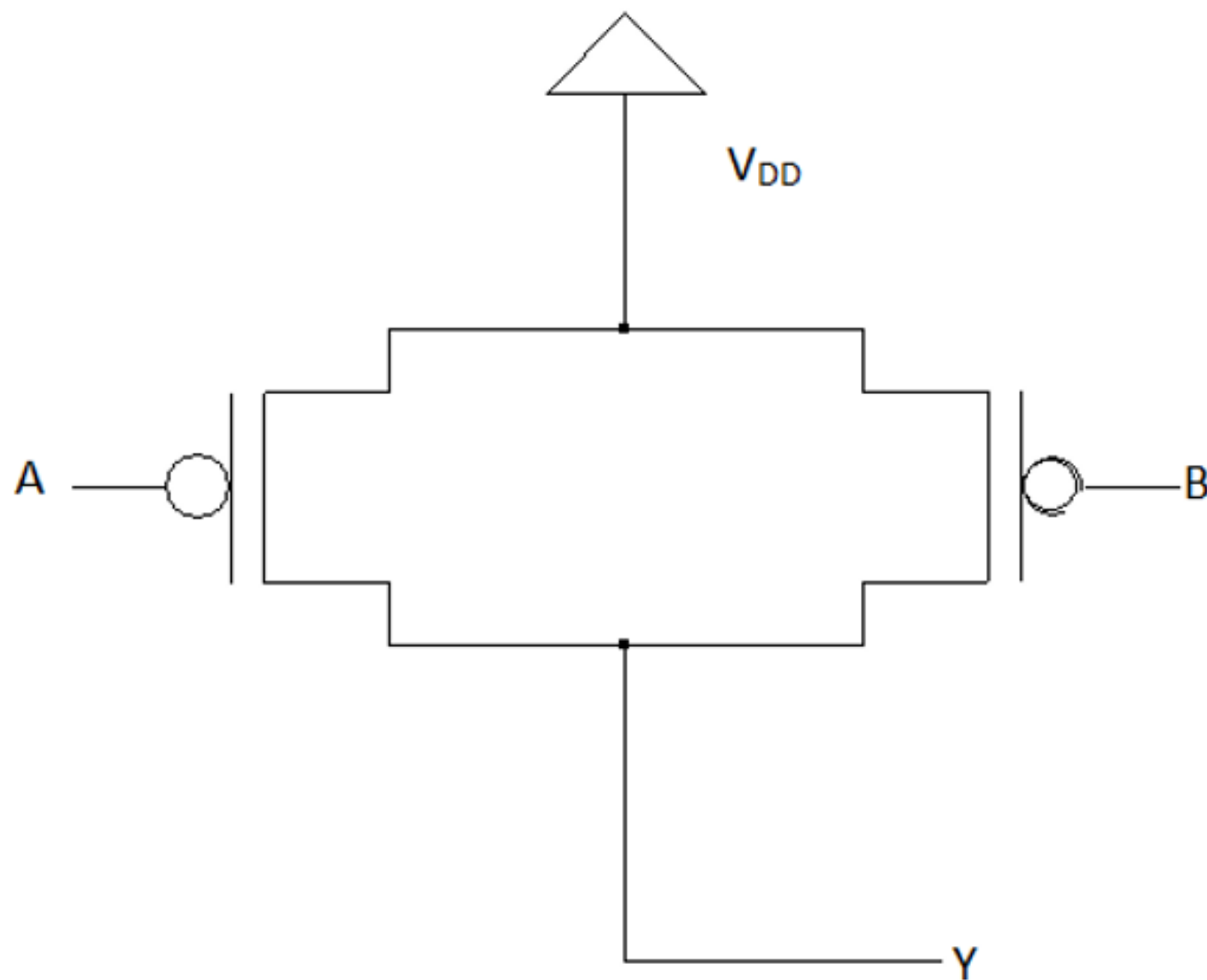
Pull-up network Design:

For designing the Pull-up network, the equation has to be modified so that the output becomes high with individual input combination.

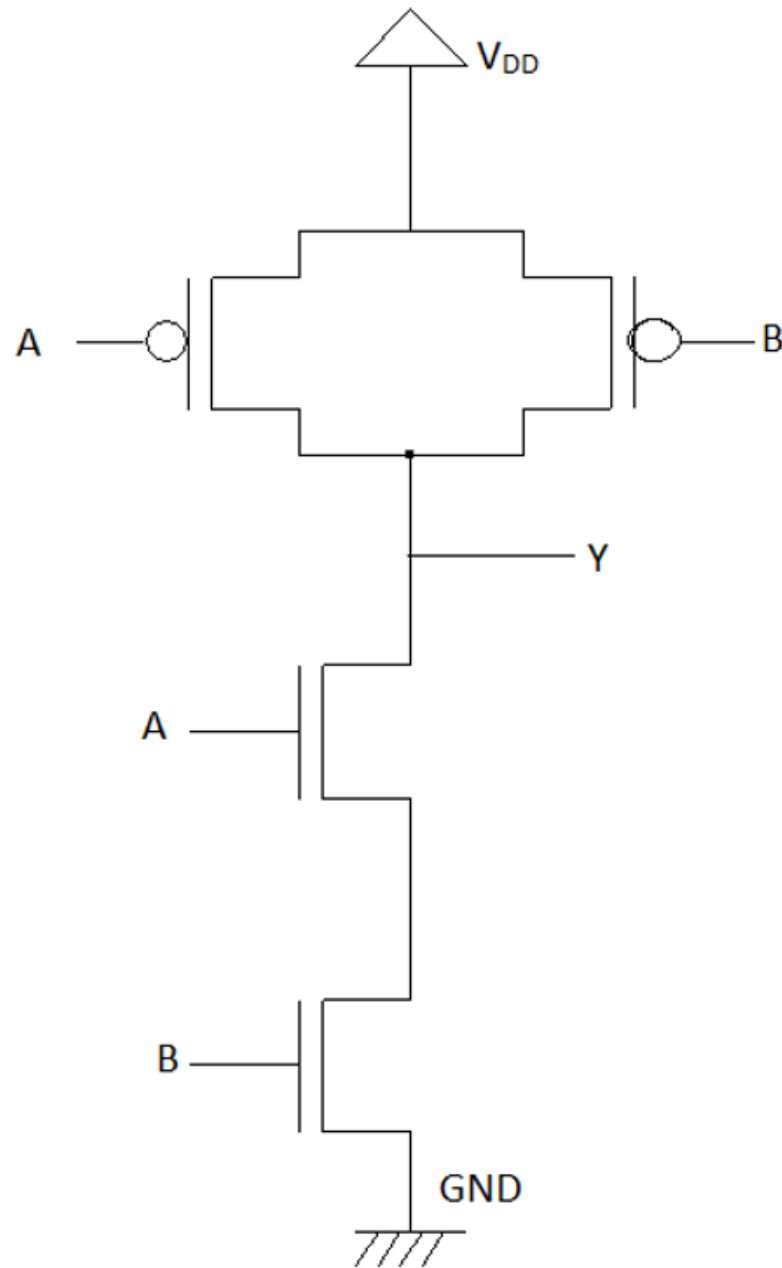
$$\rightarrow Y = \overline{A \cdot B}$$

$$\rightarrow Y = \overline{A} + \overline{B} \text{ (break down using De Morgan's Law)}$$

The available logic matches with the parallel combination of P-MOS



Overall NAND Gate:



Points to Note

- The pull-up inputs do not have any BAR over them.
- The pull-up inputs appear the same way as determined by the pull down network. In this case just A and B. Not \bar{A} and \bar{B} .

Designing a NOR gate:

SOP Expression:

$$Y = \overline{A + B}$$

Truth Table:

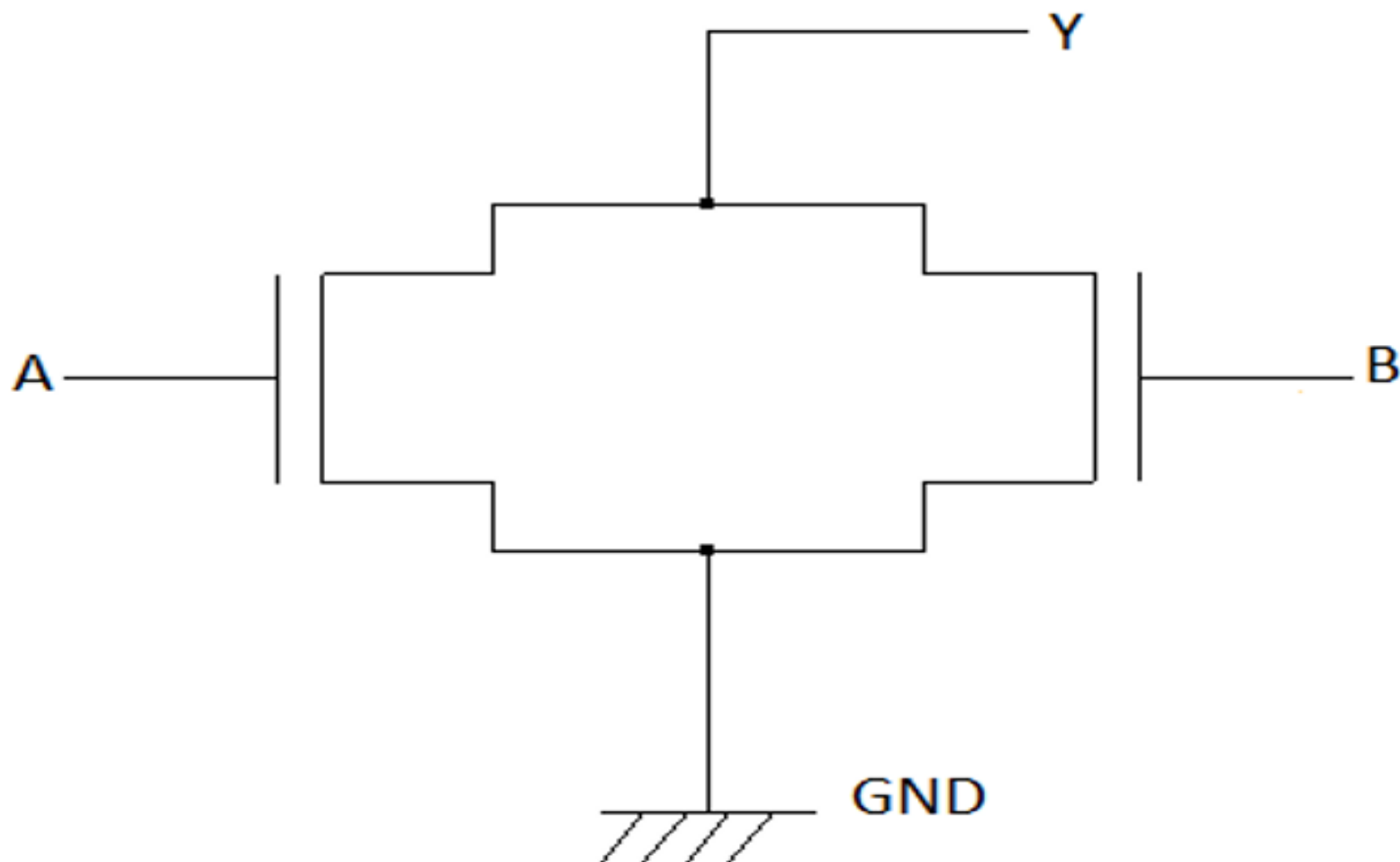
A	B	Y
0	0	1
0	1	0
1	0	0
1	1	0

Pull-down network Design:

For Designing the Pull-down network, the equation has to be modified so that the output becomes low.

$$\overline{Y} = A + B$$

According to the logic available, it matches with the parallel combination of N-MOS.



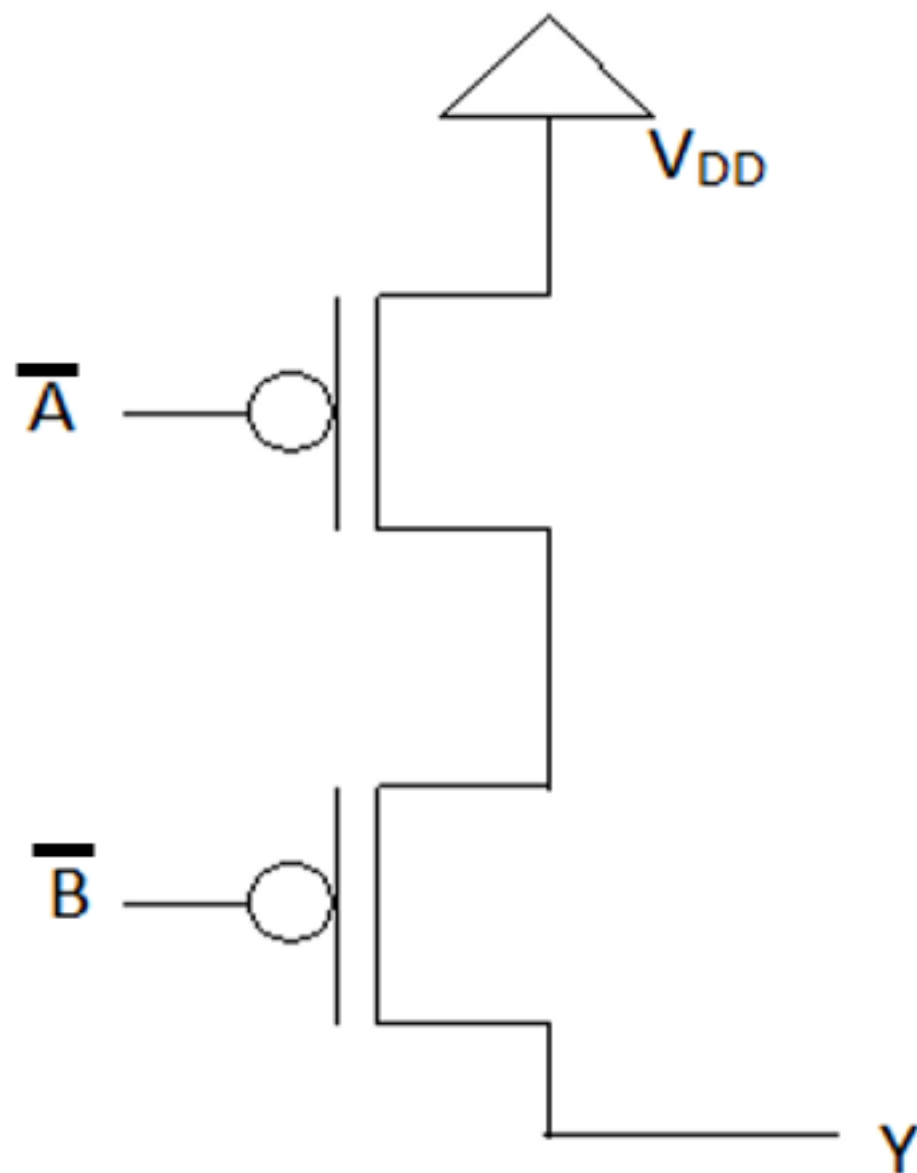
Pull-up network Design:

For designing the Pull-up network, the equation has to be modified so that the output becomes high with individual input combination.

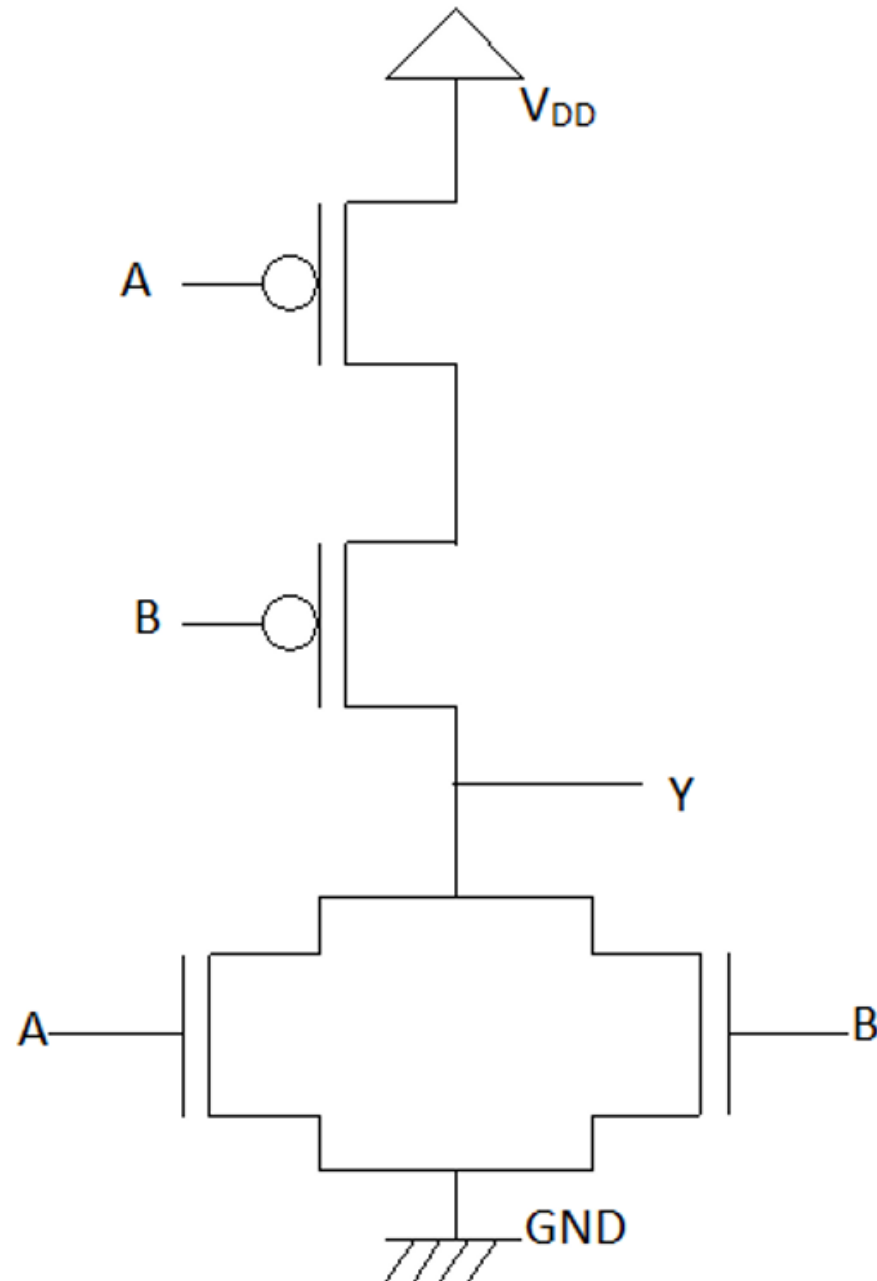
$$\rightarrow Y = \overline{A + B}$$

$$\rightarrow Y = \overline{A} \cdot \overline{B} \text{ (Break down using De Morgan's Law)}$$

The available logic matches with the Series combination of P-MOS



Overall NOR Gate:



Points to Note

- The pull-up inputs do not have any BAR over them.
- The pull-up inputs appear the same way as determined by the pull down network. In this case just A and B. Not \bar{A} and \bar{B} .



References

1. Thomas L. Floyd, “Digital Fundamentals” 8th edition, Prentice Hall – Pearson Education.
2. M. Morris Mano, “Digital Logic & Computer Design” Prentice Hall
3. <https://www.electronics-tutorials.ws>
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