Lecture -7
Integrated Circuit Technology-1

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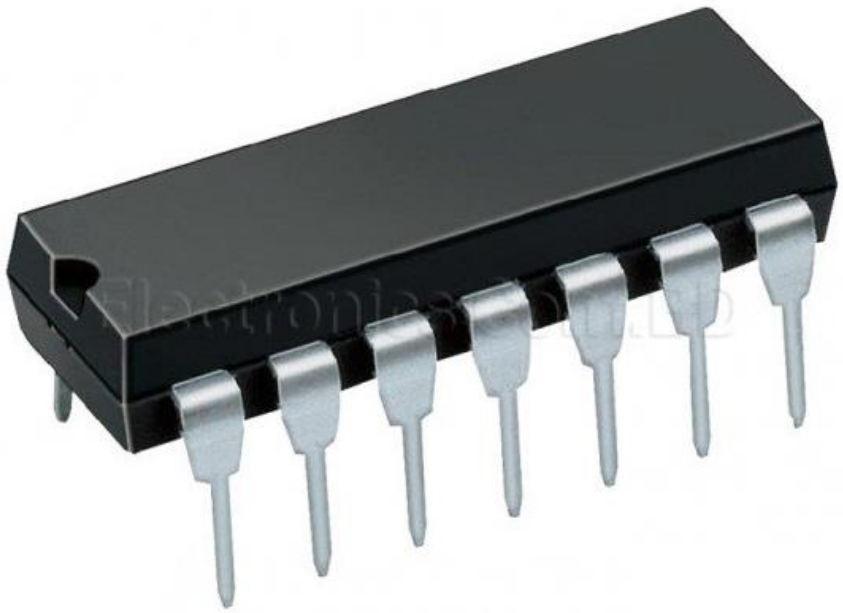
Introduction

- In practice digital circuits are not constructed with individual gates.
- Rather digital circuits are constructed with integrated circuits.
- An integrated circuit (abbreviated as IC) is a small silicon semiconductor, crystal called a chip, containing all the electronic components for the digital gates.
- The various gates are interconnected inside the chip to form the required circuit.
- This cheap is mounted in a ceramic or plastic container, and connections are welded to external pins to form the IC.
- As an engineering when working with an IC we must be aware of the following factors.
  - **The integration level**
  - **The logic family or technology**
  - **The logic level parameters.**
  - **The performance parameters.**



Integration Level

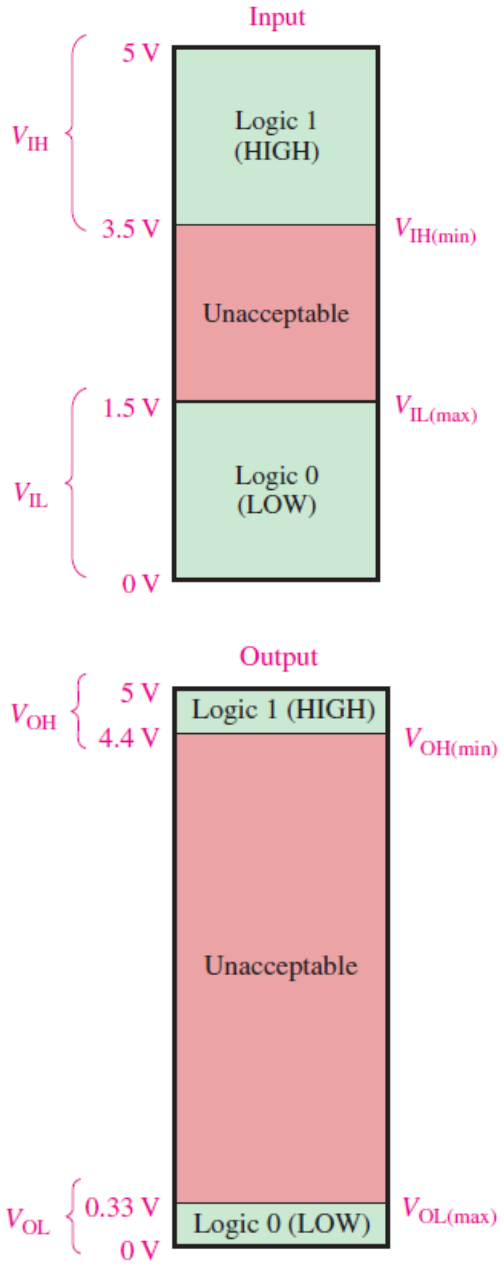
- The integration level of an IC or a semiconductor chip gives us an idea about the number of gates that are present in the chip.
- Integration Level for Integrated Circuits.
  - Small-Scale Integration (SSI) (<12 gates/chip).
  - Medium-Scale Integration (MSI) (<100 gates/chip).
  - Large-Scale Integration (LSI) (…1K gates/chip).
  - Very Large-Scale Integration (VLSI) (…10K gates/chip).
  - Ultra Large-Scale Integration (ULSI) (…100K gates/chip).
  - Giga Scale Integration (GSI) (…1M gates/chip).
- Examples:
  - Pentium III Coppermine(32-bit, large cache): 21,000,000 gates
  - Pentium 4 Willamette (32-bit, large cache): 42,000,000 gates
  - Core 2 Duo Conroe (dual-core 64-bit, large caches): 291,000,000 gates
  - ARM Cortex-A9 (32-bit, (optional) SIMD, caches):26,000,000 gates
  - Atom (32-bit, large cache): 47,000,000

Digital Logic Family

- Digital integrated circuits are classified not only by their complexity or logical operation, but also by the specific circuit technology to which they belong.
- The circuit technology is referred to as a digital logic family.
- The basic circuits in each technology is a NAND, NOR or an inverter gate.
- The logic families are:
  - RTL → Resistor-Transistor Logic
  - DTL → Diode- Transistor Logic
  - I^2L → Integrated injection Logic
  - ECL → Emitter Collector Logic
  - TTL → Transistor-Transistor Logic
  - MOS → Metal Oxide Semiconductor
  - CMOS → Complementary MOS

Logic Level Parameters

- Different Logic Families usually operate at different voltage and current levels.
- **Voltage Parameters**
  - **High-Level Output Voltage, $V_{OH(MIN)}$:** This is the minimum output voltage available at the output under stated loaded condition which corresponds to logic '1'.
  - **Low-Level Output Voltage, $V_{OL(MAX)}$:** This is the maximum output voltage available at the output under stated loaded condition which corresponds to logic '0'
  - **High-Level Input Voltage, $V_{IH(MIN)}$:** This is the minimum voltage required at an input to be recognized as a logic '1'.
  - **Low-Level Input Voltage, $V_{IL(MAX)}$:** This is the maximum voltage at an input which will be recognized as a logic '0'.

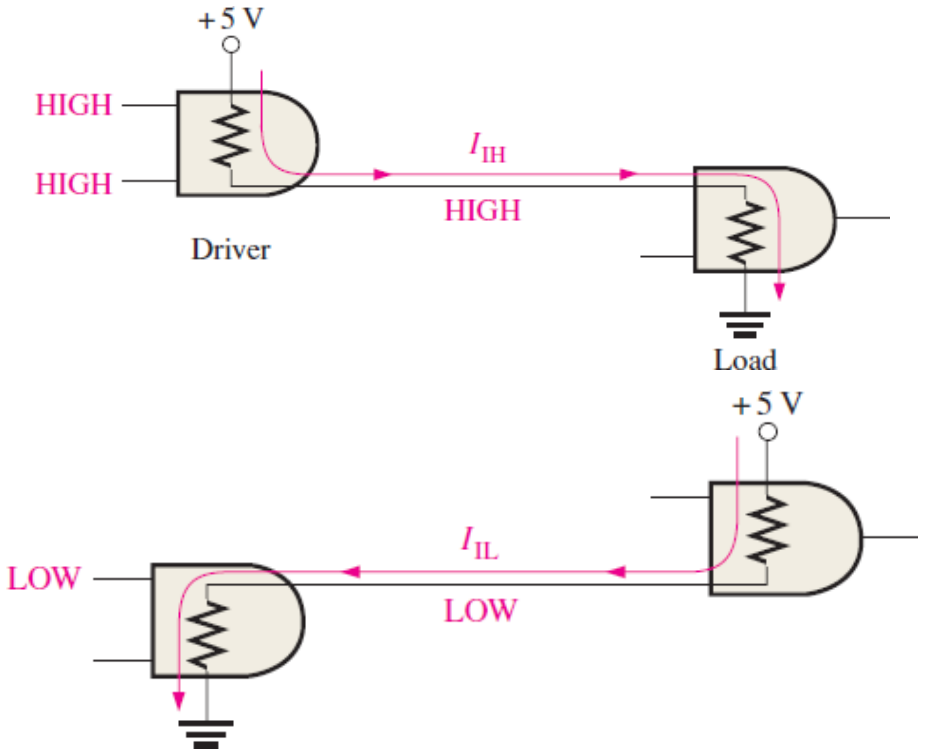


Performance Parameters

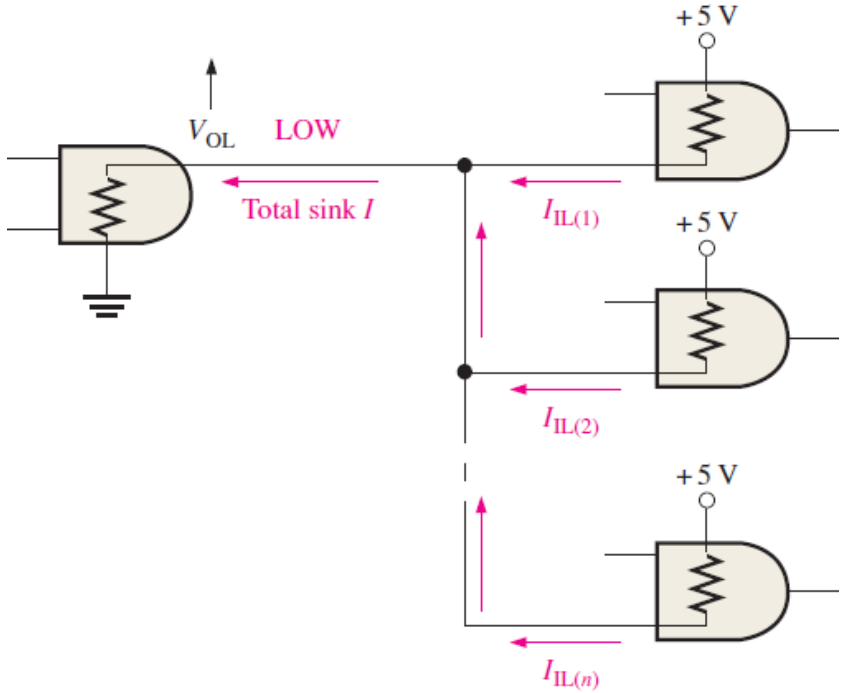
- The performance parameters are also known as the special characteristics of a logic family.
- The characteristics of IC digital logic families are usually compared by analyzing the circuit of the basic gate in each family.
- The most important parameters that are evaluated and compared are
  - Fan-Out
  - Fan-In
  - Power Dissipation
  - Propagation Delay
  - Speed-Power Product
  - Noise Margin

Loading

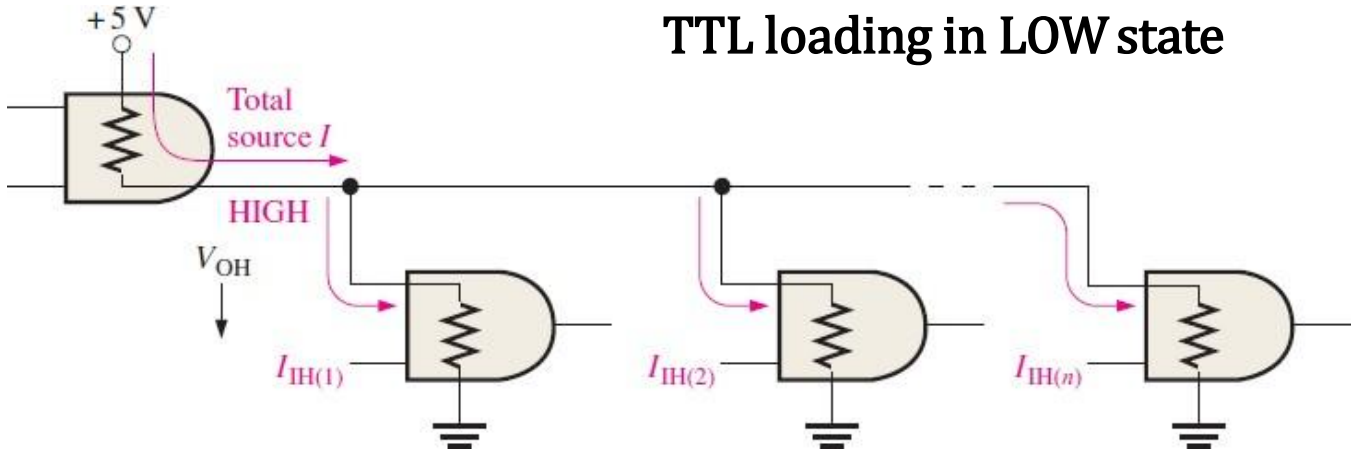
- When the output of a gate is connected to the input of one or more gates, a load is created on the driver gate. There is a limit to the number of input that the output a gate can drive. This is determined by the fan-out.



TTL loading in HIGH and LOW state



TTL loading in LOW state



TTL loading in HIGH state

Performance Parameters: Fan-Out

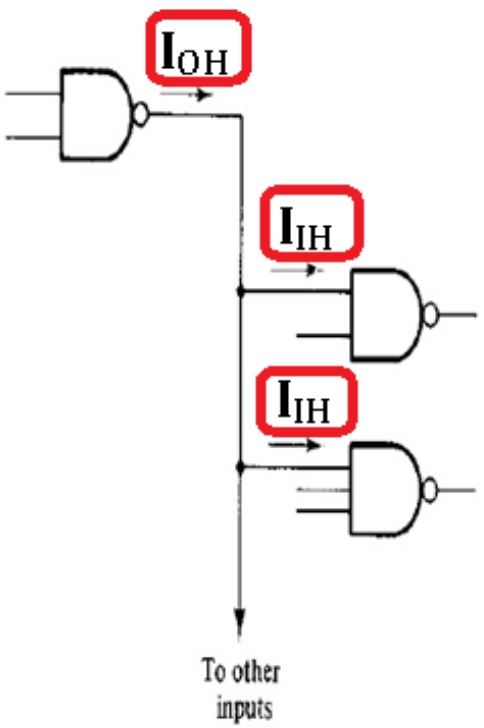
- The **fan-out** of a gate specifies the number of standard loads that can be connected to the output of the gate without degrading its normal operation.
- A **standard load** is usually defined as the amount of current needed by an input of another gate in the same logic family. Sometimes the term loading is used instead of fan-out.
- This term is derived because the output of a gate can supply a limited amount of current, above which it ceases to operate properly and is said to be overloaded.
- Each input consumes a certain amount of current from the gate output, so that each additional connection adds to the load of the gate.
- Exceeding the specified maximum load may cause a malfunction because the circuit cannot supply the power demanded from it.
- Also the propagation delay increases with fan-out.
- The fan-out is the maximum number of inputs that can be connected to the output of a gate and is expressed by a number.

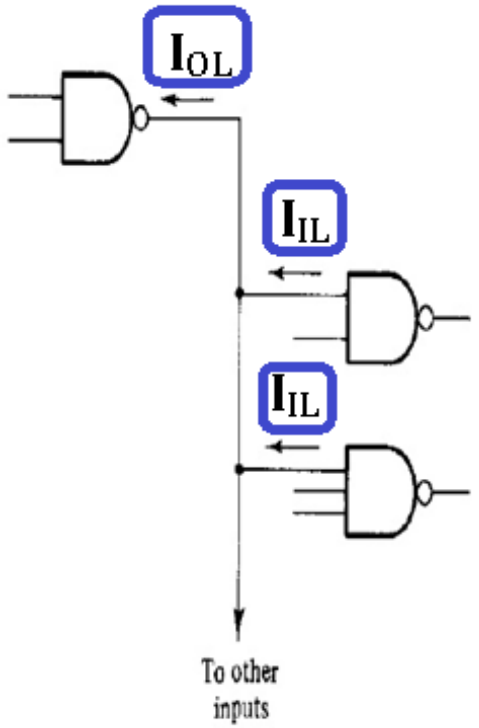
$$\textbf{DC Fanout} = \min\left(\frac{I_{OH}}{I_{IH}}, \frac{I_{OL}}{I_{IL}}\right)$$

Performance Parameters: Fan-Out

- Calculating the Fan-out of a driving gate with the following parameters:
  - $I_{OH} = 400\mu A$ and $I_{IH} = 40\mu A$
  - $I_{IH} = 16mA$ and $I_{IL} = 2mA$
- Solution

$$FO = \min\left(\frac{400\mu A}{40\mu A}, \frac{16mA}{2mA}\right) = 8units$$

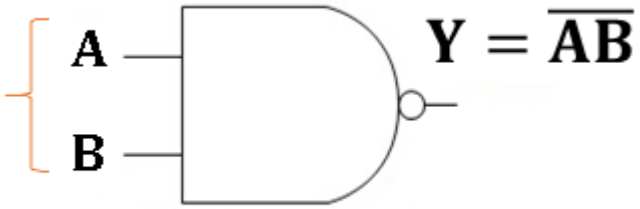




Performance Parameters: Fan-In

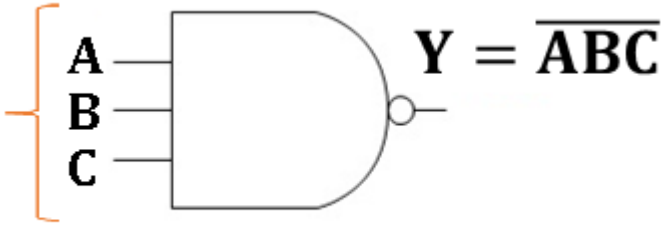
- The fan in defined as the maximum number of inputs that a logic gate can accept.
- If number of input exceeds, the output will be undefined or incorrect.
- It is specified by manufacturer and is provided in the data sheet.
- Delay approximately has a quadratic relation with Fan-In.

Fan In = 2

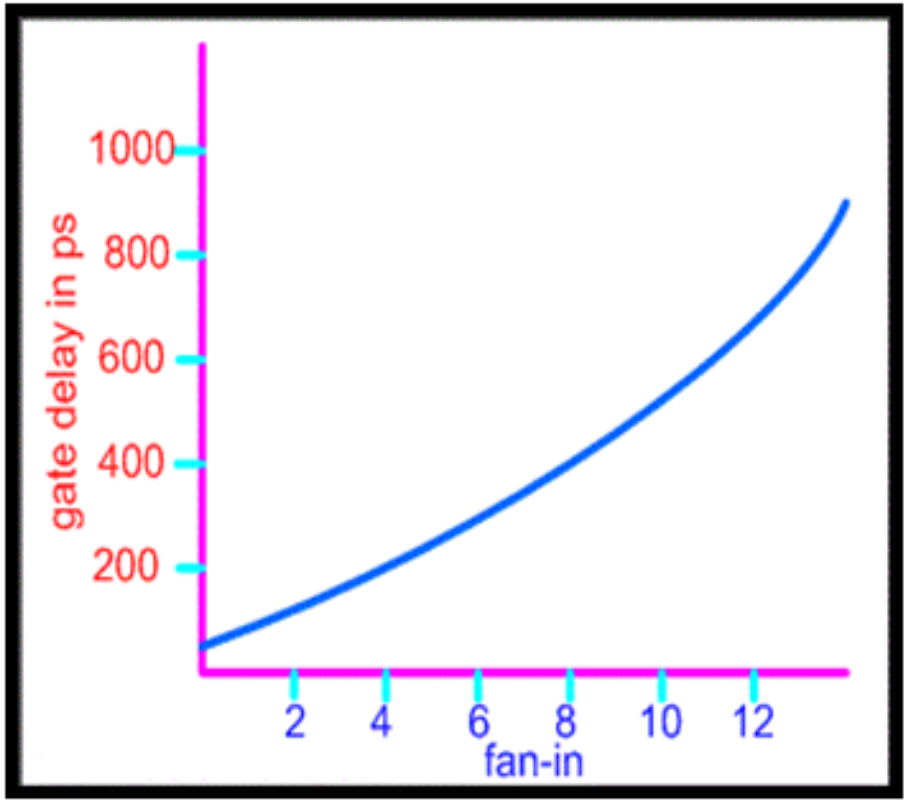


Two Input NAND Gate

Fan In = 3

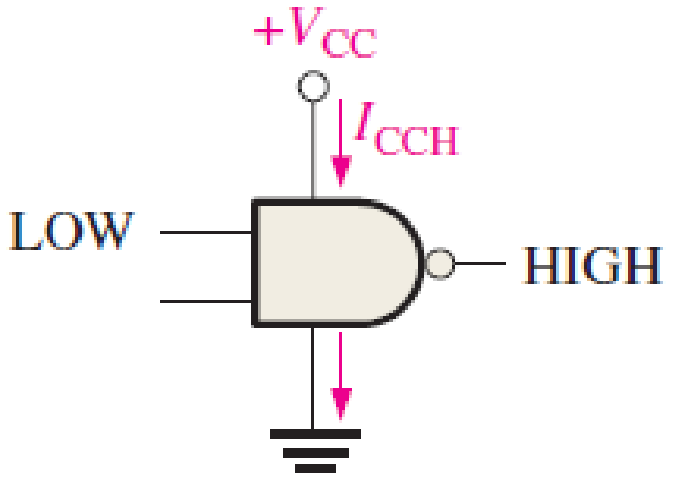


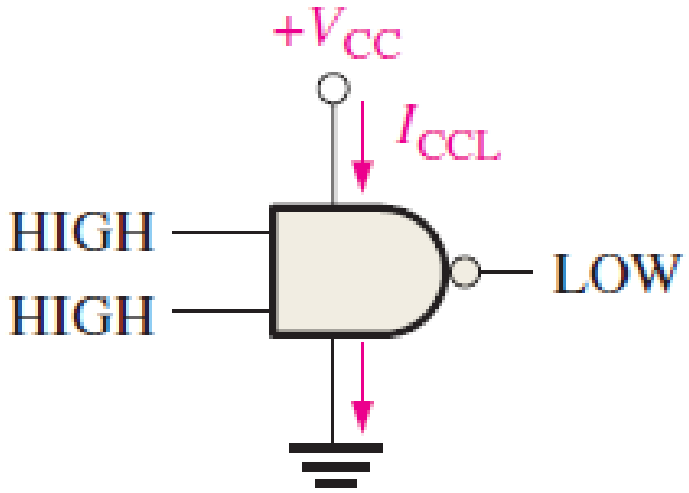
Three Input NAND Gate



Performance Parameters: Power Dissipation

- A gate draws in current both in HIGH and LOW states.
- Therefore, in both states a gate dissipates power.
- The power dissipation is a parameter expressed in milliwatts (mW) and represents the amount of power needed by the gate.
- The number that represents this parameter does not include the power delivered from another gate; rather, it represents the power delivered to the gate from the power supply.
- An IC with four gates will require, from its power supply, four times the power dissipated in each gate.
- The current associated with HIGH state is named I_{CCH}.
- The current associated with LOW state is named I_{CCL}. Therefore,
- Power Dissipation in HIGH state, $P_{DH} = V_{CC}I_{CCH}$
- Power Dissipation in LOW state, $P_{DL} = V_{CC}I_{CCL}$





Performance Parameters: Power Dissipation

- When gate is pulsed, its output switches back and forth between HIGH and Low
- The amount of supply current also varies between ICCH and ICCL.
- The average power is dissipated when the duty cycle is 50%, the output is HIGH half the time and LOW the other half.
- The average power dissipated in a cycle is,

$$\mathbf{PD} = \frac{\mathbf{V_{CC}(I_{CCH} + I_{CCL})}}{\mathbf{2}}$$

- So the power dissipated in a cycle with duty cycle of X%is,

$$\mathbf{PD} = \frac{\mathbf{V_{CC}((X \times I_{CCH}) + ((100 - X)I_{CCL}))}}{\mathbf{100}}$$

- Find the average power dissipated for a NAND gate with $V_{CC} = 5V$, $I_{CCH} = 4mA$ and $I_{CCL} = 2mA$ when the duty cycle is:
  a) 40%
  b) 75%
  c) 20%

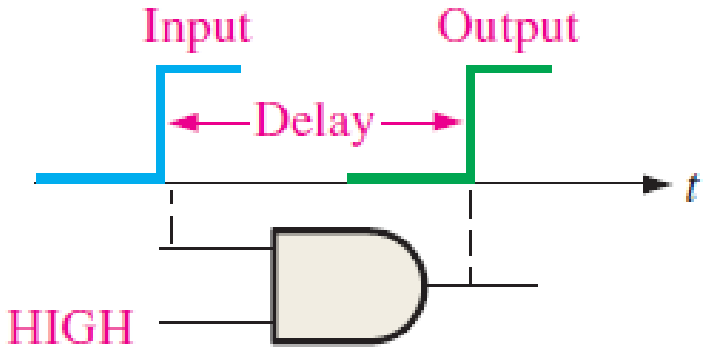
Performance Parameters: Propagation Delay

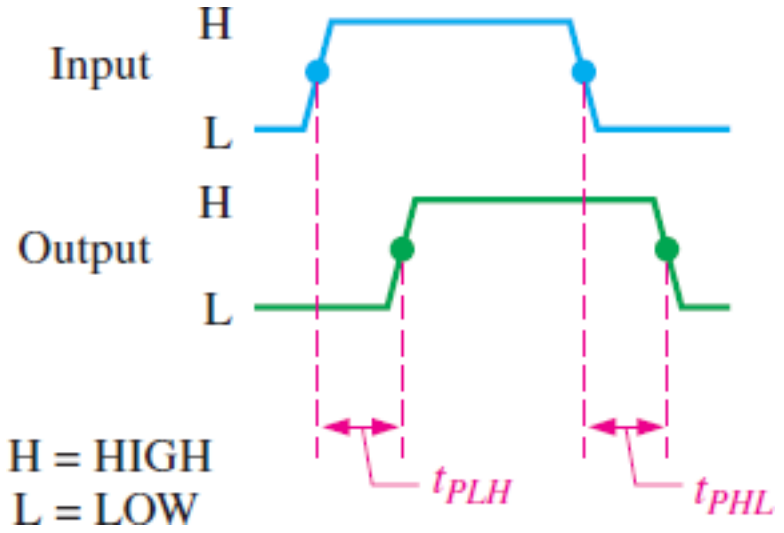
- When a signal passes through a logic circuit, it always experiences a time delay.
- A change in the output level always occurs after a short time, called the propagation delay.
- $\mathbf{T_{PHL}}$: Propagation delay for High to Low.
- $\mathbf{T_{PLH}}$: Propagation delay for Low to High.

$$\mathbf{t_{PD} = \frac{1}{2}(t_{PHL} + t_{PLH})}$$

- As an example, the delays for a standard TTL gate are $t_{PHL} = 7$ ns and $t_{PLH} = 11$ ns. These quantities are given in the TTL data book and are measured with a load resistance of 400 ohms and a load capacitance of 15 pF. The average propagation delay of the TTL gate is:

$$t_{PD} = \frac{11 + 7}{2} = 9 \text{ ns}$$





Performance Parameters: Speed Power Product

- The speed power product provides the basis for the comparison of logic circuits when both propagation delay time and power dissipation are important considerations in the selection of the type of logic to be used in a certain application.
- The lower the speed-power the better.
- The unit of speed-power product is Pico joule(pJ).
- The speed power product can be calculated as:

$$\textbf{SPP} = \textbf{Power Disspation} \times \textbf{Propagation Delay}$$

- The table below lists the parameters for three types of gates. Basing your decision on the speed-power product, which one would you select for best performance?

	t_{PLH}	t_{PHL}	P_D
Gate *A*	1 ns	1.2 ns	15 mW
Gate *B*	5 ns	4 ns	8 mW
Gate *C*	10 ns	10 ns	0.5 mW

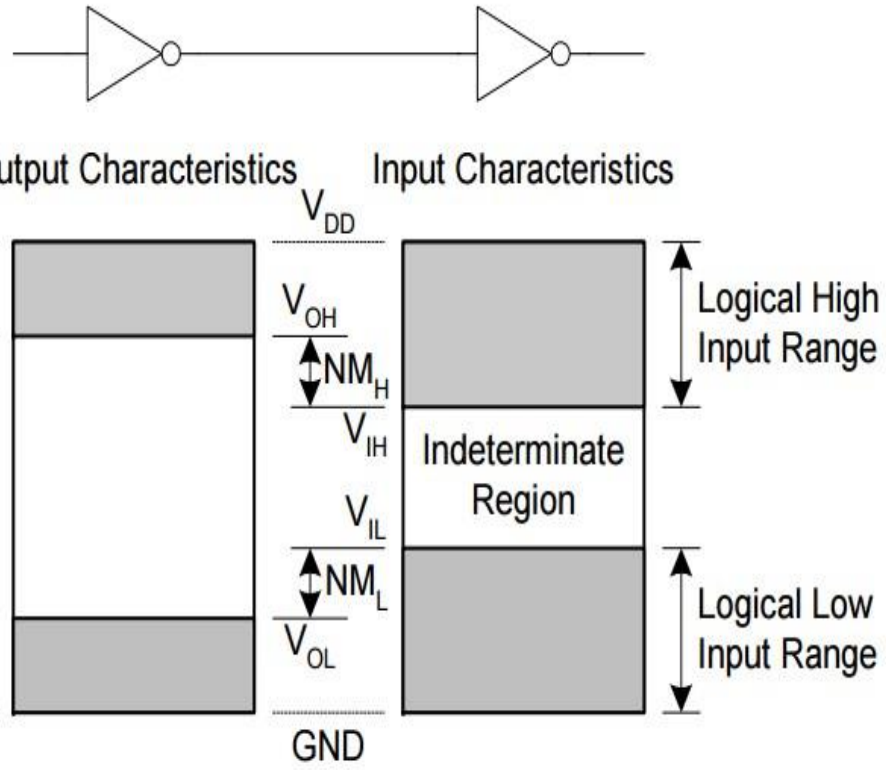
Performance Parameters: Noise Margin

- All electrical circuits are susceptible to noise.
- Unwanted signals are referred to as *noise.*
- This unwanted induced voltage can disrupt the operation of a digital circuit.
- In order to not get adversely affected by noise the circuit should have some amount of noise immunity.
- Noise Immunity is the ability to tolerate unwanted voltage fluctuation.
- There are two types of noise to be considered :
  - **DC noise is** caused by a drift in the voltage levels of a signal.
  - AC noise is a random pulse that may be created by other switching signals.
- Noise margin is the maximum noise voltage added to an input signal of a digital circuit that does not cause an undesirable change in the circuit output.
- Noise margin is expressed in volts and represents the maximum noise signal that can be tolerated by the gate.

Performance Parameters: Noise Margin

- There are two values of noise margin specified for a given logic circuit:
  - the High-level noise margin (V_{NH}) and
  - the Low-level noise margin (V_{NL}).
- There parameters are defined by the following equations:

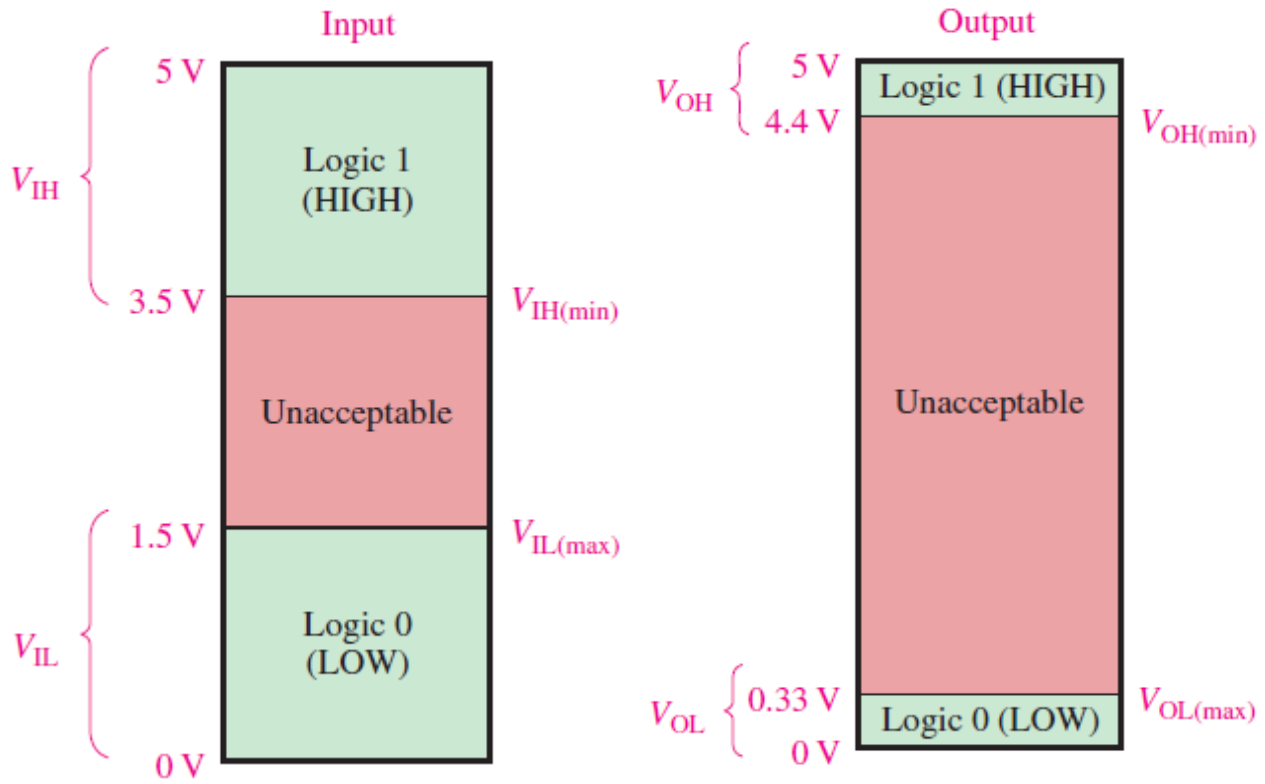
$$V_{NL} = V_{IL} - V_{OL}$$
$$V_{NH} = V_{OH} - V_{IH}$$



Performance Parameters: Noise Margin

- The figure below shows the different voltage level parameters for a +5V CMOS.
- The noise margin for +5V CMOS are:

$$V_{NH} = 4.4V - 3.5V = 0.9V$$
$$V_{NL} = 1.5V - 0.33V = 1.17$$

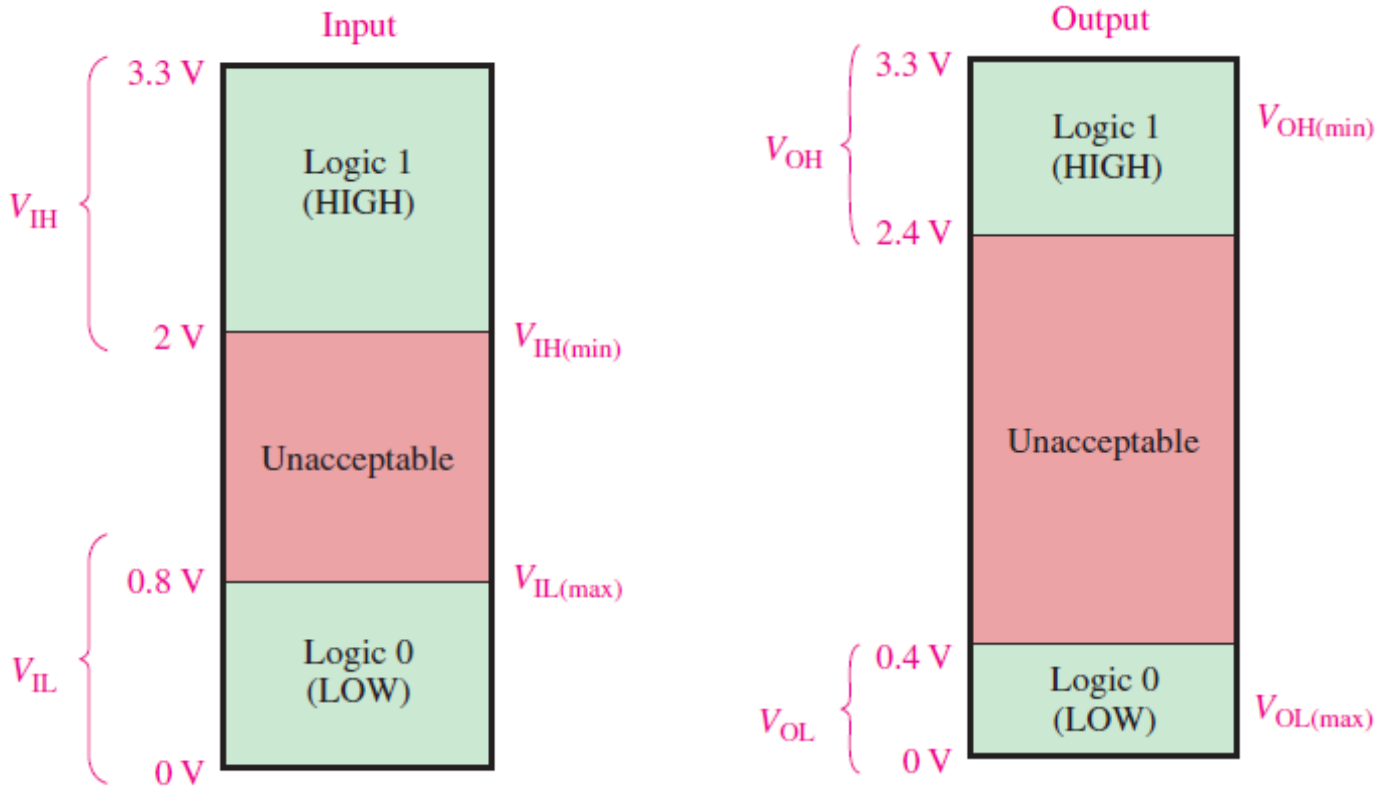


Logic Levels for +5V CMOS

Performance Parameters: Noise Margin

- The figure below shows the different voltage level parameters for a +3.3V CMOS.
- The noise margin for +3.3V CMOS are:

$$V_{NH} = 2.4V - 2V = 0.4V$$
$$V_{NL} = 0.8V - 0.4V = 0.4V$$

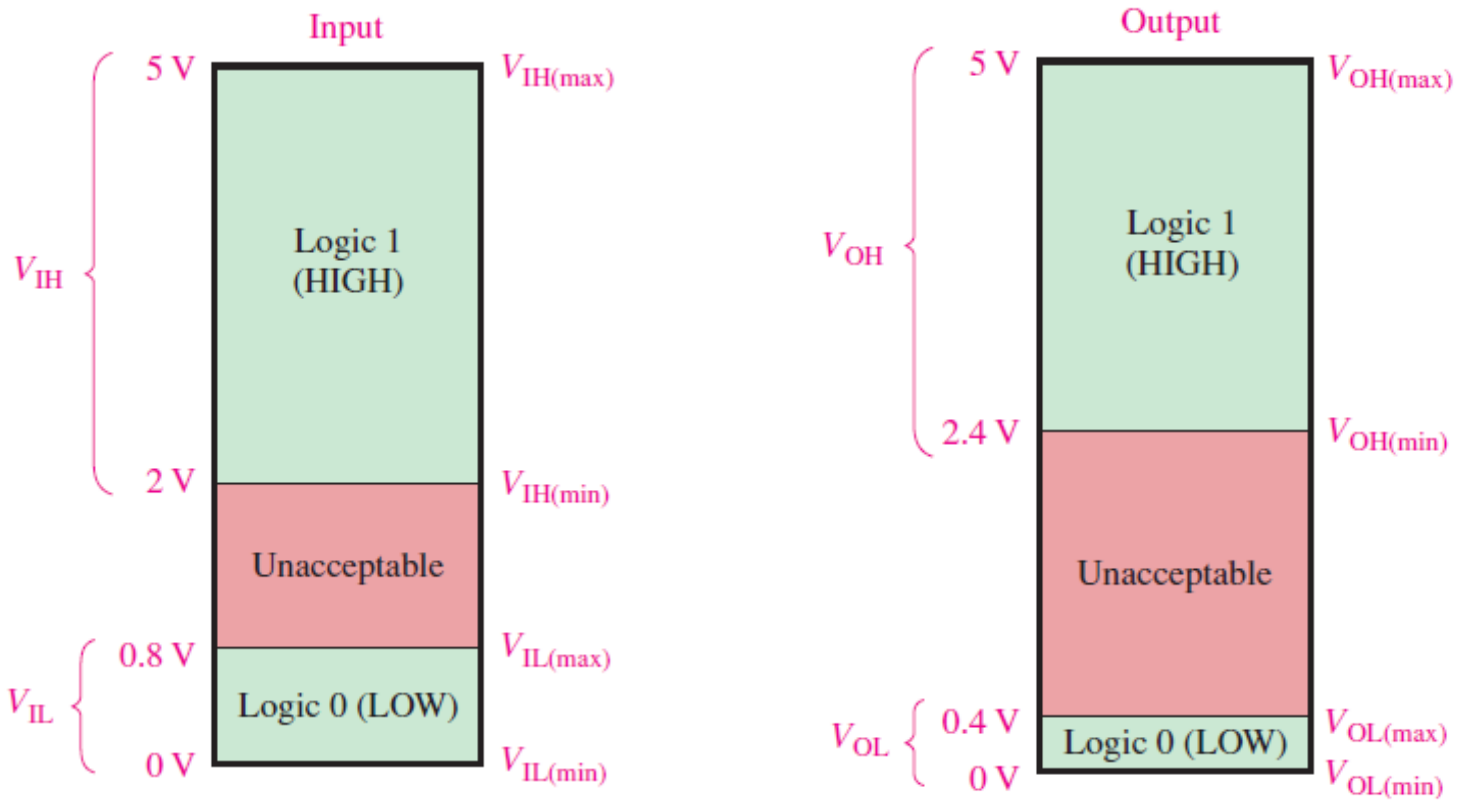


Logic Levels for +3.3 V CMOS

Performance Parameters: Noise Margin

- The figure below shows the different voltage level parameters for TTL.
- The noise margin for TTL are:

$$V_{NH} = 2.4V - 2V = 0.4V$$
$$V_{NL} = 0.8V - 0.4V = 0.4V$$



Logic Levels for TTL

Performance Parameters: Noise Margin

- Voltage specifications for three types of logic gates are given in the Table below. Select the gate that you would use in a high-noise environment.

	$V_{OH(min)}$	$V_{OL(max)}$	$V_{IH(min)}$	$V_{IL(max)}$
Gate *A*	2.4 V	0.4 V	2 V	0.8 V
Gate *B*	3.5 V	0.2 V	2.5 V	0.6 V
Gate *C*	4.2 V	0.2 V	3.2 V	0.8 V

Solution:

- Gate A: $N_{MH} = 2.4V - 2V = 0.4V$; $N_{ML} = 0.8V - 0.4V = 0.4V$
- Gate B: $N_{MH} = 3.5V - 2.5V = 1V$; $N_{ML} = 0.6V - 0.2V = 0.4V$
- Gate C: $N_{MH} = 4.2V - 3.2V = 1V$; $N_{ML} = 0.8V - 0.2V = 0.6V$

References

1. Thomas L. Floyd, “Digital Fundamentals” 11th edition, Prentice Hall – Pearson Education.

Thank You