AMERICAN INTERNATIONAL UNIVERSITY BANGLADESH

Assignment Cover Sheet

Students must complete all details except the faculty use part.

Please submit all assignments to your subject lecturers or the office of the concerne

Assignment Title: OBE assignment Final

Assignment Number: 02 Due Date: 12-12-23 Semester: Fall 23-24

Subject Code:__________ Subject Name: Digital logic circuit Section: K

Course Instructor: Md. Shahariar Parvez Degree Program: BSc CSE

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Total Marks:______ **Marks Obtained:** ______

Faculty comments______________________________

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Solution:

For designing the alarm circuit, the outline will be-

Steps:

① Problem statement analyzing.
② Finding and understanding the input and outputs of the system.
③ Relating the inputs and outputs.
④ Creating the truth table based on condition
⑤ Forming a standard sop equation from the truth table
⑥ Simplifying the sop equation with K-MAP.
⑦ Designing the system circuit by logic gates.
⑧ Implementing the system with CMOS Logic.

Step-1:

From the problem statement, there are four sensor in the car. The ignition activation system of this car is attached to a digital system. If the driver seat is occupied and the driver seatbelt is fastned or the driver seat is occupied and the driver seatbelt is fasten and the passenger seat is occupied and the passenger seatbelt is fastened then the activation system turns on. There are appropiate sensors present for detecting the above.

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Step-2:

There are appropiate sensors present for detecting the alarm activation. which can be regarded as the input of the system.

where,

A = sensor for driver seat
B = sensor for driver seatbelt
C = Sensor. for passenger seat
D = sensor for passenger seatbelt

let's consider the output Y, which will be generated for the above condition.

Step-3:

If we relate between the input and output, it can be said that, when A and B is high or A and B and C and D is high the output will be high, low otherwise.

③

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Step-4:

let's construct the truth table for the system.

A	B	C	D	Y
0	0	0	0	0
0	0	0	1	0
0	0	1	0	0
0	0	1	1	0
0	1	0	0	0
0	1	0	1	0
0	1	1	0	0
0	1	1	1	0
1	0	0	0	0
1	0	0	1	0
1	0	1	0	0
1	0	1	1	0
1	1	0	0	1
1	1	0	1	1
1	1	1	0	1
1	1	1	1	1

Step-5:

$Y = \Sigma(12, 13, 14, 15)$

$= AB\bar{C}\bar{D} + AB\bar{C}D + ABC\bar{D} + ABCD.$

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Step-6:

Simplifying using K-MAP.

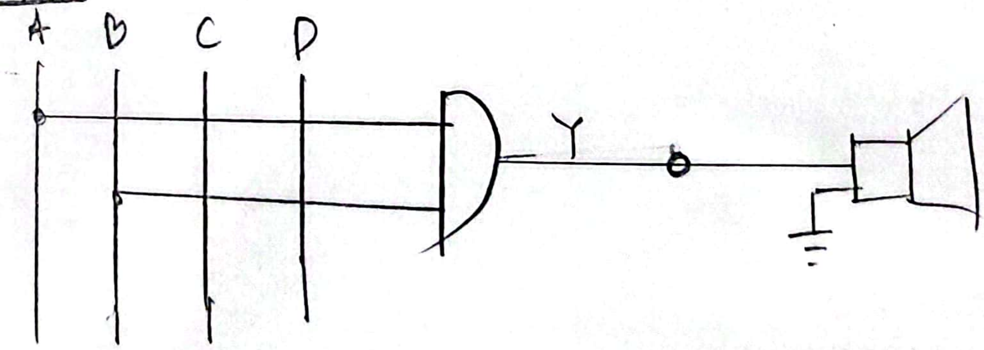
AB \ CD	00	01	11	10
00	0	0	0	0
01	0	0	0	0
11	1	1	1	1
10	0	0	0	0

Gr-1

A	B	C	D	
1	1	0	0	12
1	1	0	1	13
1	1	1	1	
1	1	1	0	
A	B			

$$\boxed{Y = AB}$$

Step-7:



logic circuit diagram using basic logic gates_

Here, when both A and B sensors inputs are high(1), the output of the system will be high and the alarm speaker will get enough voltage to make sound. Hence, the alarm will be triggered.

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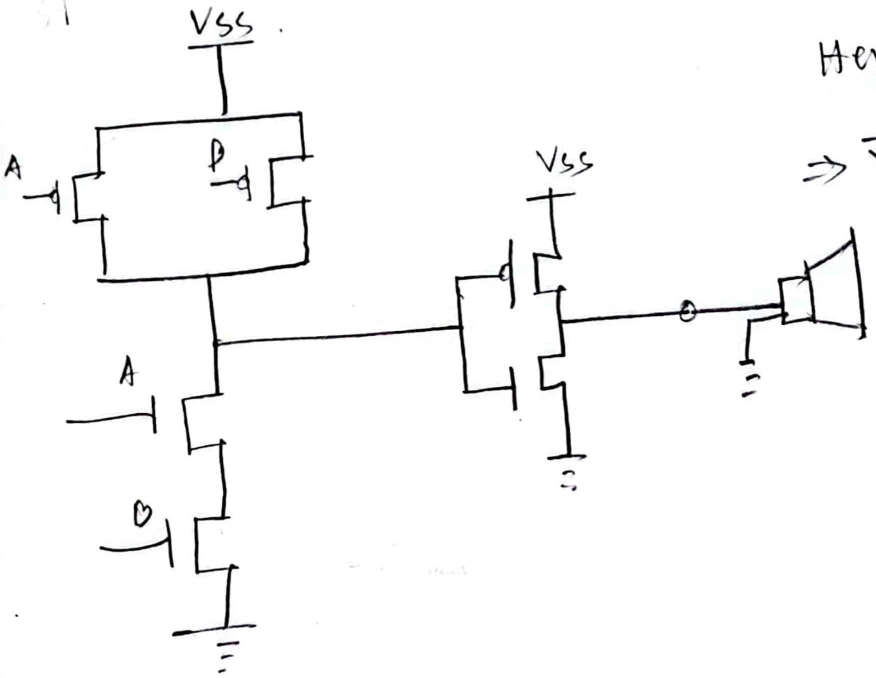
step-8:

Now, implementing the design of the system using CMOS logic.



Here,

$Y = AB$

$\Rightarrow \overline{Y} = \overline{AB} \Rightarrow$ NMOS

$= \overline{A} + \overline{B} \Rightarrow$ PMOS

(ii)

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so,

$P = N + O + I + S + E$

$= 4 + 7 + 0 + 1 + 9$

$= 21$

$\Rightarrow P * 20\ Hz = 21 \times 20\ Hz$

$= 420\ Hz$ [smoothing hearing limits]

$\therefore$ frequency, $f = 420\ Hz$.

$\Rightarrow Q = 100 - P = 100 - 21 = 79$

$\therefore$ Duty cycle $= Q = 79\%$

⑥

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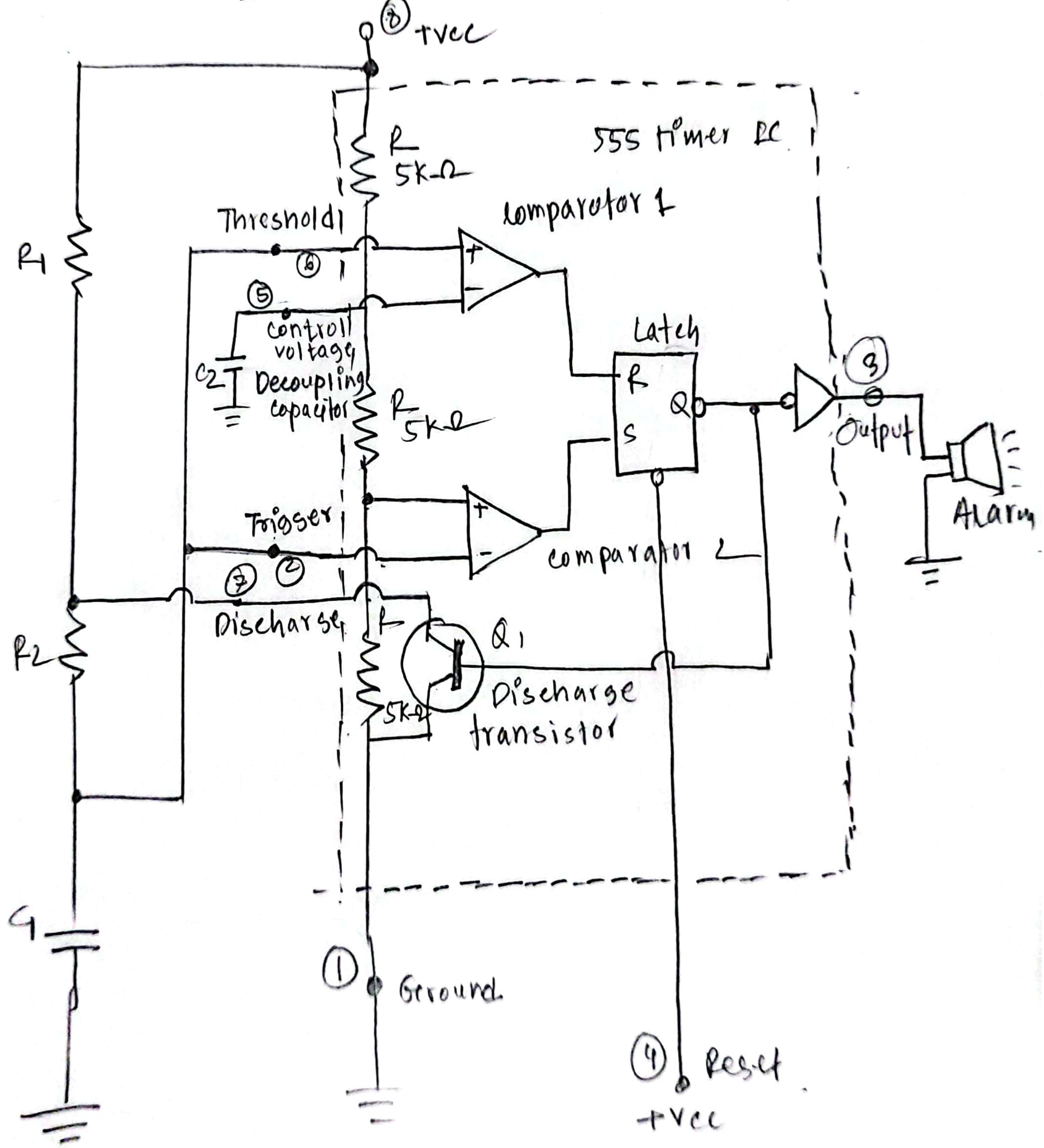
let's design the alarm timer circuit with 555 timer IC and in ASTABLE mode,



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So, 420 Hz is not a very high frequency. so we need a 250 μF (C_1) and a 50(μF) (C_2) as decoopling capacitor.

So, Time period, $T = \frac{1}{f} = \frac{1}{420} = 0.00238$ s.

Now,

Duty cycle, $Q\% = \frac{T_H}{T}$

$\Rightarrow T_H = Q\% \times T$

$= 0.79 \times 0.00238$

$= 0.00188$ s

So, $T_L = T - T_H$

$= 0.00238 - 0.00188$

$= 0.0005$ s

And $T_L = 0.693 R_2 C_1$

$\Rightarrow R_2 = \frac{T_L}{0.693 \times C_1} = \frac{0.0005}{0.693 \times 250 \times 10^{-6}}$

$= 2.886 \Omega$

$\Rightarrow T = 0.693 C_1 (R_1 + 2R_2)$

$\Rightarrow R_1 = \frac{T}{0.693 C_1} - 2R_2$

$= \frac{0.00238}{0.693 \times 250 \times 10^{-6}} - (2 \times 2.886)$

$= 7.965 \Omega$

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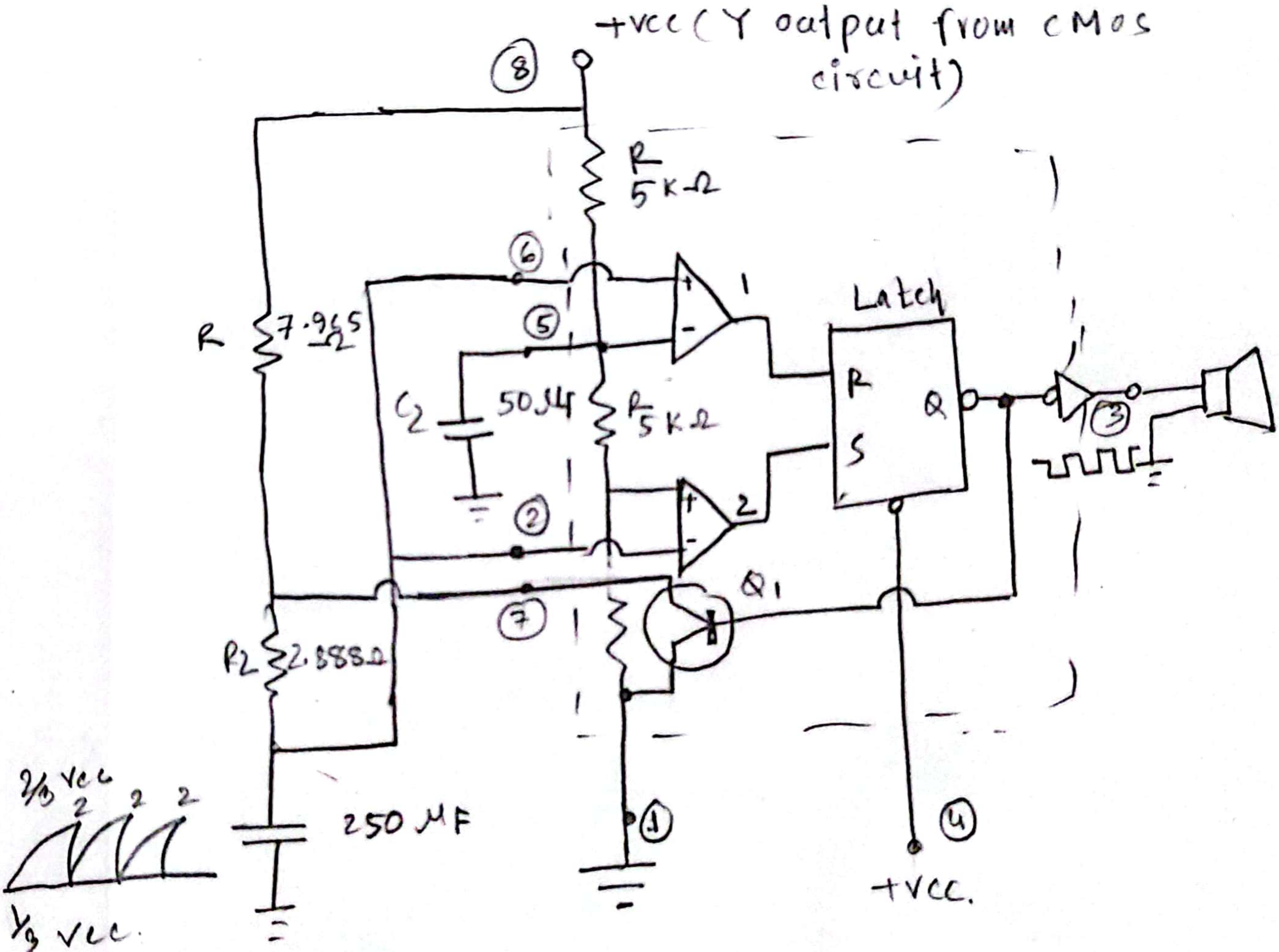
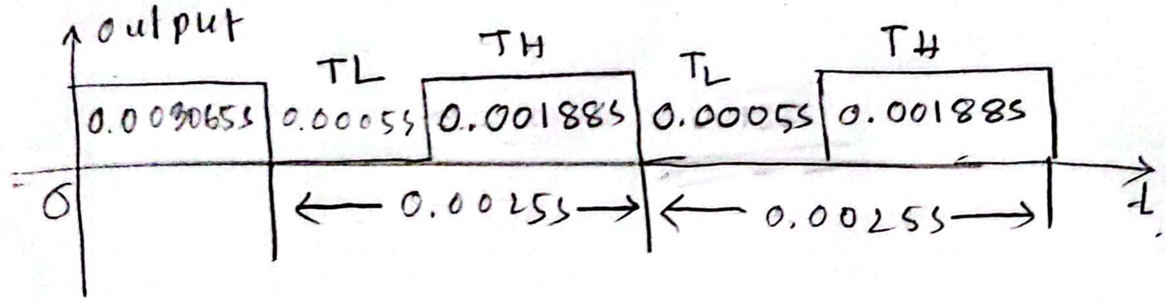
let's draw the final circuit diagram with values:





Initially, the capacitor takes 0.00306 s to charge from 0 to 2/3 Vcc.

So, we get output time period of 0.0025s after the initial 0.00306 s. That's why the alarm will buzz for 0.00188 s and stop for 0.0005 s. It will maintain 420 Hz frequency

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(iii) Limitations :

① The design system heavily relies on accurracy and reliability of sensors. Any inaccuracies in these sensors can lead of false readings and incorrect activation of ignition.

② It may generate false alarms if sensors detect incorrect information.

③ It's functionality is limited to detecting driver and passenger seat occupancy and seat belt status. It does not account for other Factors that could infuence safe driving conditions, such as the condition of the driver, vehicle speed or road conditions.

④ Any failure in the car's electrical system such as a dead battery or othe component failure could affect the function of the system.

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Effect of increasing frequency above 4500 Hz:

① Frequencies above 4500Hz are considered disturbingly high pitched. Increasing the alarm frequency beyond this limit could lead to discomfort, unpleasent or even potential harm to individuals hearing.

② At higher frequency, problem can occur with the 555 timer IC in Astable mode.