Lecture -9
CMOS Logic, Digital System Design

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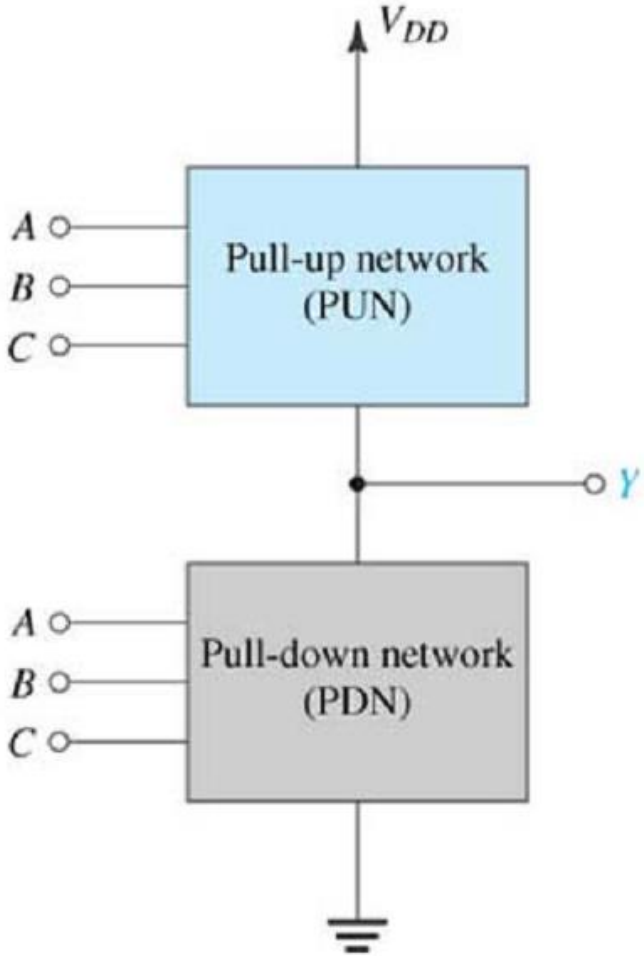
CMOS Logic

- Static CMOS is the most widely used logic family.
- The primary advantage of CMOS structure is robustness, good performance, and low power consumption.
- It falls under the category of static circuit, as at every point of time (except for switching) each gate is connected to either V_{DD} or ground via low resistance path.
- CMOS allows a much higher density of logic functions in a single chip compared to TTL.
- TTL circuits consume more power in comparison to CMOS circuits at rest.
- A CMOS network is a combination of pull-up network (PUN) and pull-down network (PDN).
- The function of the PUN is to provide a connection between V_{DD} and output when the function needs to be 1.
- Similarly the task of the PDN is to provide a connection between output and ground when function needs to be 0.
- The PUN and PDN are constructed in a mutually exclusive fashion such that one and only one of the networks is conducting in any state.

PUN and PDN

- The pull-up network (PUN) provides a connection between V_{DD} and output.
- The PUN network is constructed from PMOS.
- The PUN is constructed from PMOS as they can give strong “ones”.
- On the other hand, the pull-down network provides a connection between output and ground.
- The PDN network is constructed from NMOS.
- The PDN is constructed from NMOS as they can give strong “zeros”.
- At a time, only one of the network is connected to the output.
- The network provides a low resistance path.

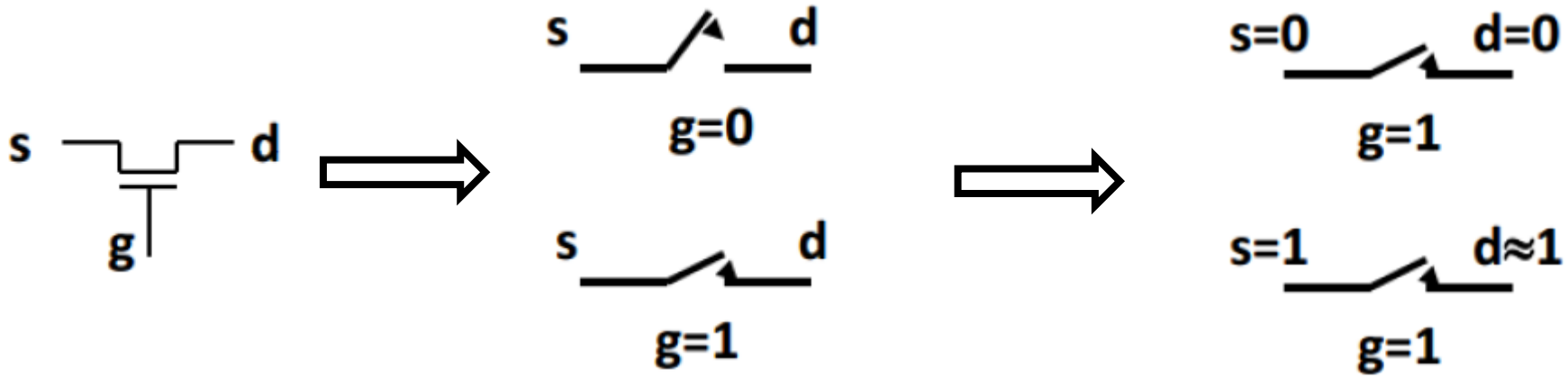


Network of PMOS transistors

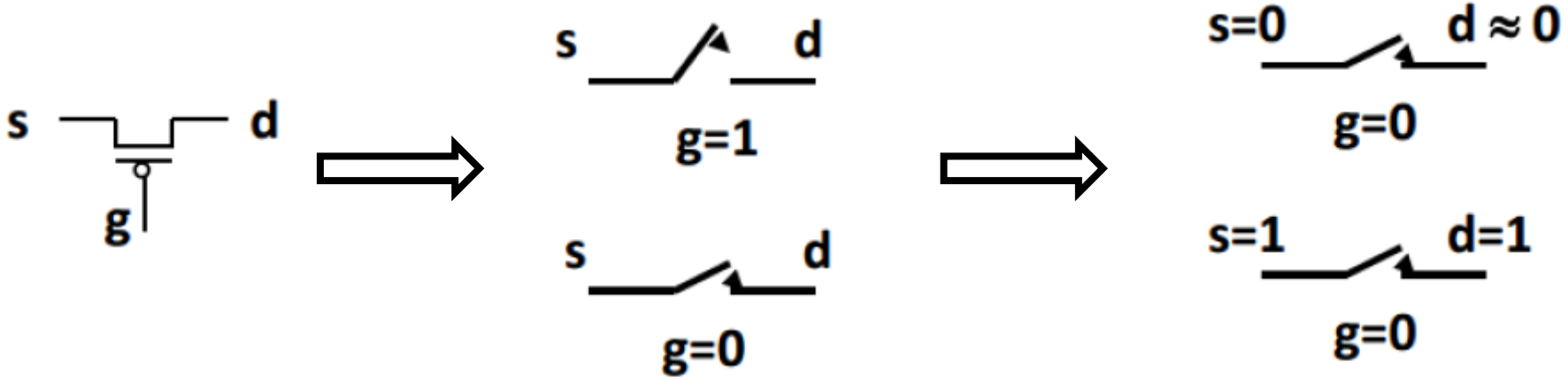
Network of NMOS transistors

PMOS and NMOS as Switches

NMOS



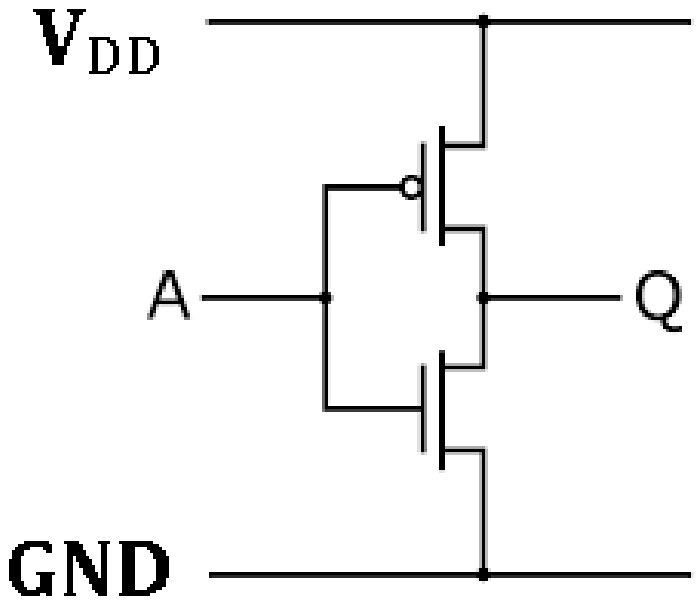
PMOS



NOT Gate using CMOS (CMOS Inverter)

Operation:

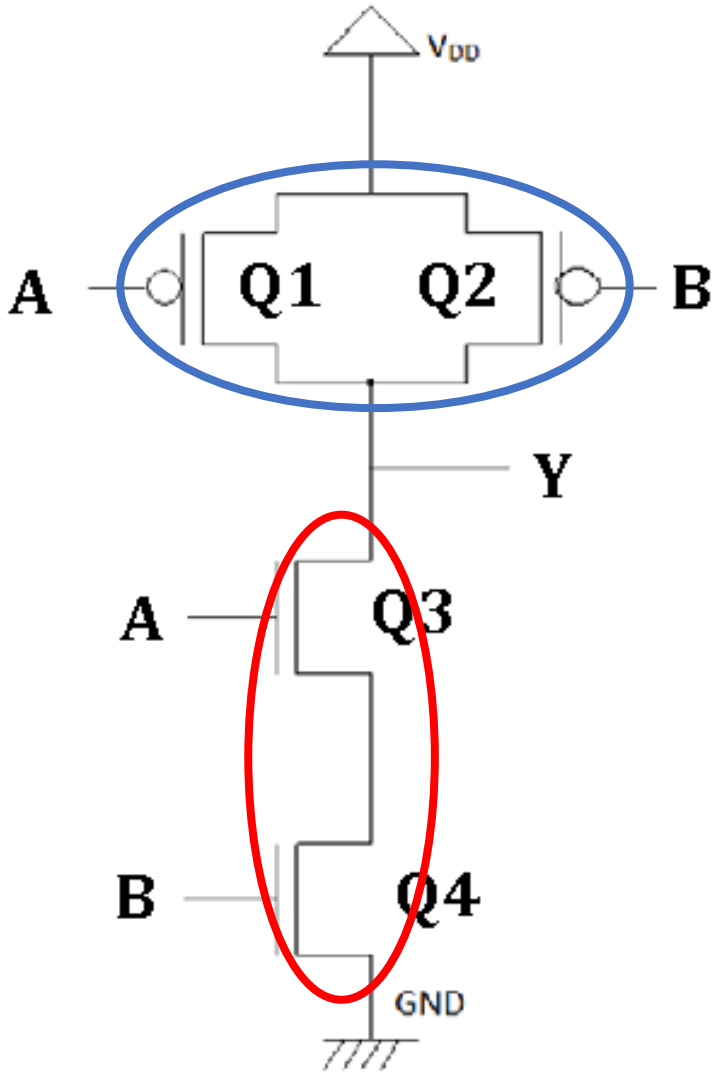
- When A is Low, the PMOS is ON and NMOS is OFF.
- Hence the output is $+V_{DD}$.
- When A is High, the PMOS is OFF an NMOS is ON.
- As a result, the output is Low.
- The table below summarizes the operation.



A	PMOS	NMOS	Q
Low	ON	OFF	$+V_{DD}$
High	OFF	ON	Low

NAND Gate using CMOS (CMOS Inverter)

A	B	Q1 PMOS	Q2 PMOS	Q3 NMOS	Q4 NMOS	Y
0	0	ON	ON	OFF	OFF	$+V_{DD}$
0	1	ON	OFF	OFF	ON	$+V_{DD}$
1	0	OFF	ON	ON	OFF	$+V_{DD}$
1	1	OFF	OFF	ON	ON	Low

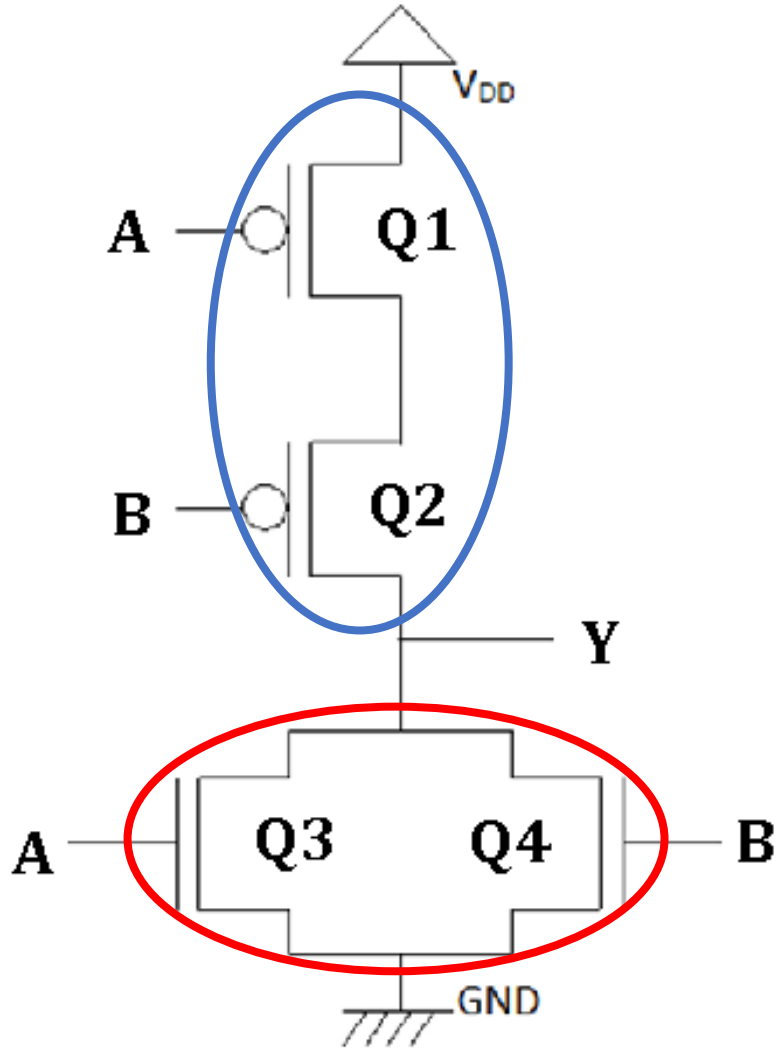


Takeaways:

- When any of the input in **LOW** the output is **HIGH**.
- The Boolean expression for a NAND gate is $\mathbf{Y = \overline{AB}}$.
- The whole circuit can be divided in to two parts, namely PDN and the PUN.
- **PDN/NMOS structure is designed in a series structure.**
- **PUN/PMOS structure is designed in a parallel structure.**

NOR Gate using CMOS (CMOS Inverter)

A	B	Q1 PMOS	Q2 PMOS	Q3 NMOS	Q4 NMOS	Y
0	0	ON	ON	OFF	OFF	$+V_{DD}$
0	1	ON	OFF	OFF	ON	Low
1	0	OFF	ON	ON	OFF	Low
1	1	OFF	OFF	ON	ON	Low



Takeaways:

- When any of the input is HIGH the output is LOW.
- The Boolean expression is $\mathbf{Y = \overline{A + B}}$.
- Similarly, the circuit can be divided in to two parts namely, PDN and PUN.
- **PDN/NMOS structure is designed in parallel structure.**
- **PUN/PMOS structure is designed in series structure.**

Function Implementation with CMOS Logic

- Till now we have seen how to implement two know Boolean expression.
- We have learnt that, for each expression we need to separately have a PUN and a PDN.
- Furthermore, we have seen that, for PUN network a product is implemented using the parallel combination where as, a sum is implemented with a series combination.
- And for the PDN network a product is implemented using series combination and a sum is implemented using parallel combination.
- So can we use these observations to help build some more complex function such as;

$$F = \overline{A + BC}$$

Function design will be shown in class….

Digital System Design

Designing a digital system requires following the steps to be performed:

- Look for the problem statement.
- Find out the inputs and outputs of the system.
- Related the input of your system with the outputs.
- Develop a truth table/ behavior table for your system using input and output relationship that you have established.
- From your truth-table generate a standard output expression, relating the inputs to the outputs.
- Reduce the output expression using either Boolean Algebra or K-MAP.
- Write down your reduced expression (minimized expression)
- Design the system circuit with combinational logic gates.
- Convert the combinational logic gates to transistor level schematic (CMOS schematic)

References

1. Thomas L. Floyd, “Digital Fundamentals” 11th edition, Prentice Hall – Pearson Education.

Thank You