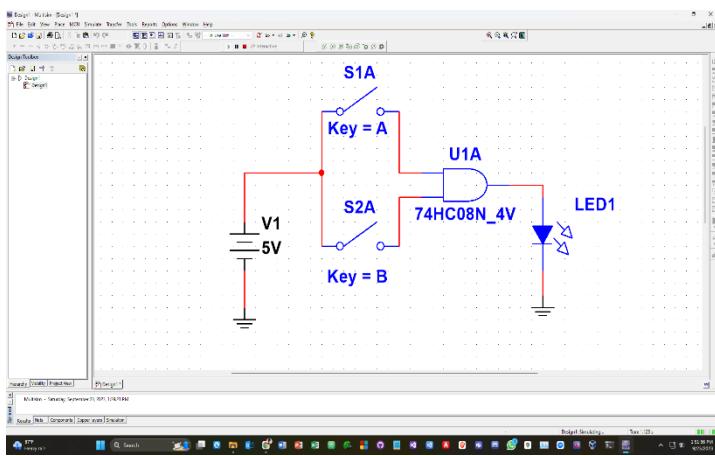
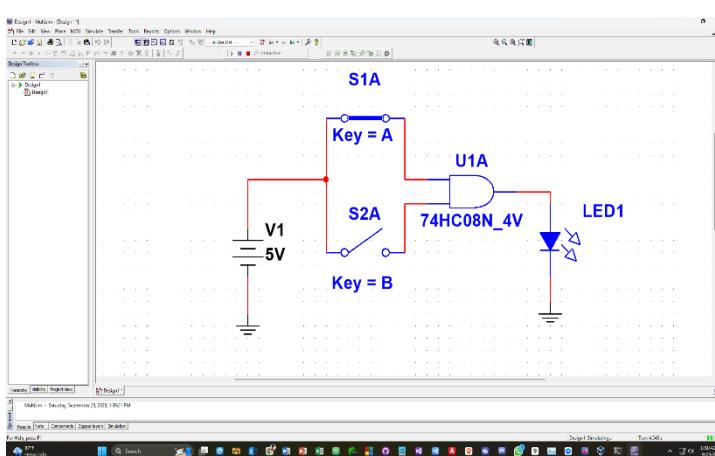
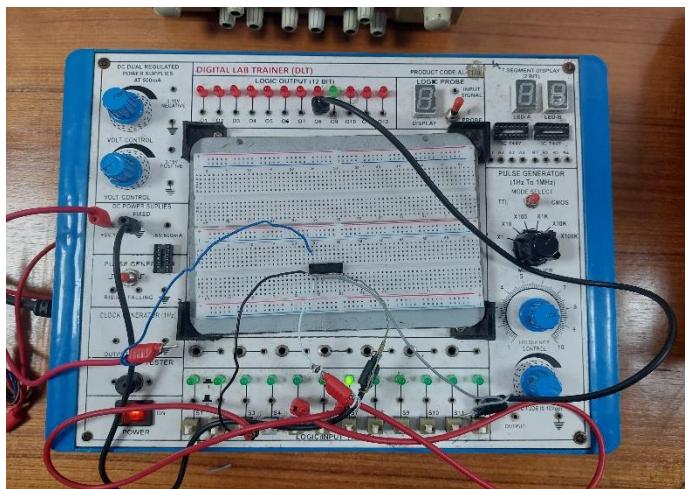
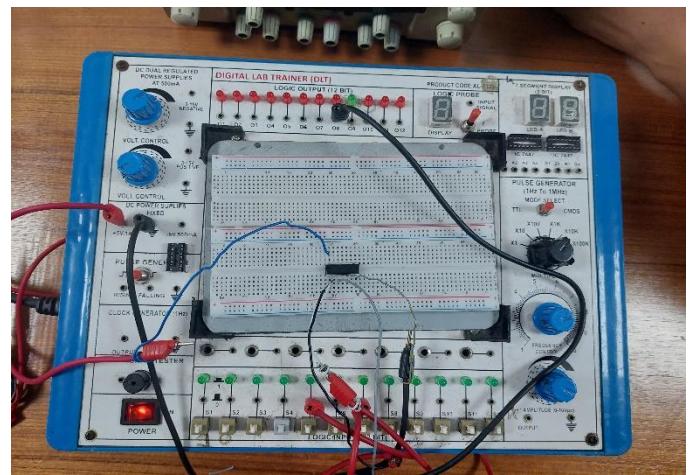


## SIMULATION

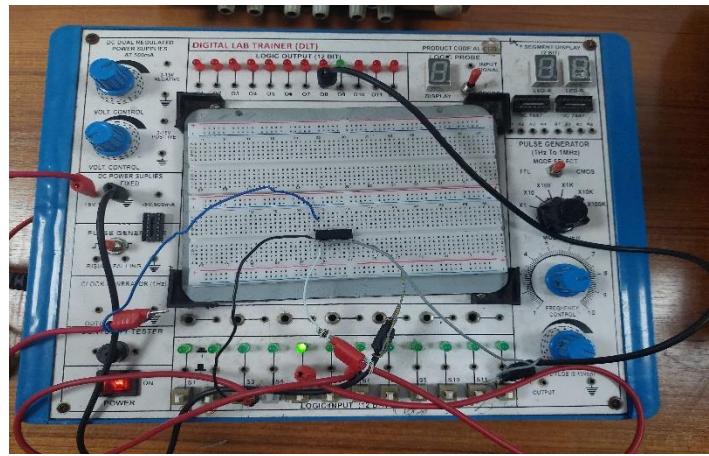


AND Gate  
A = 0, B = 0, Y = 0

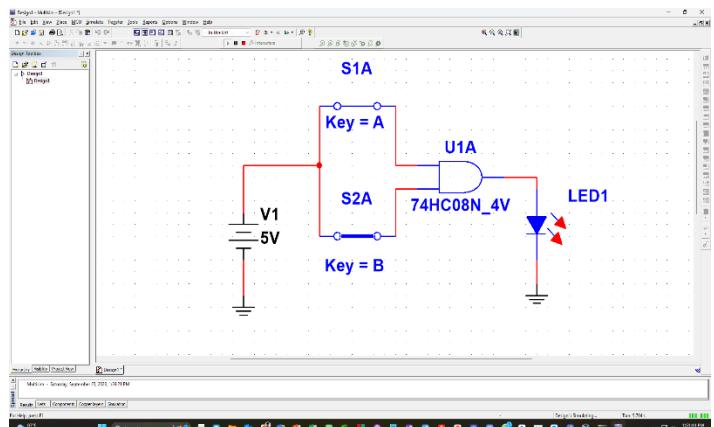
## HARDWARE



AND Gate  
A = 0, B = 1, Y = 0

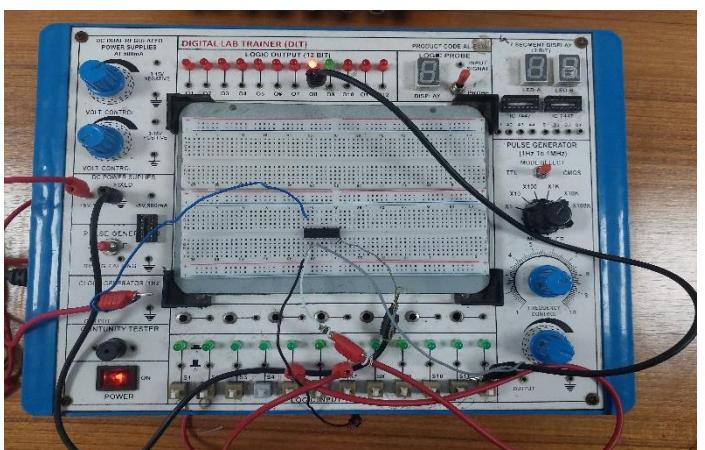
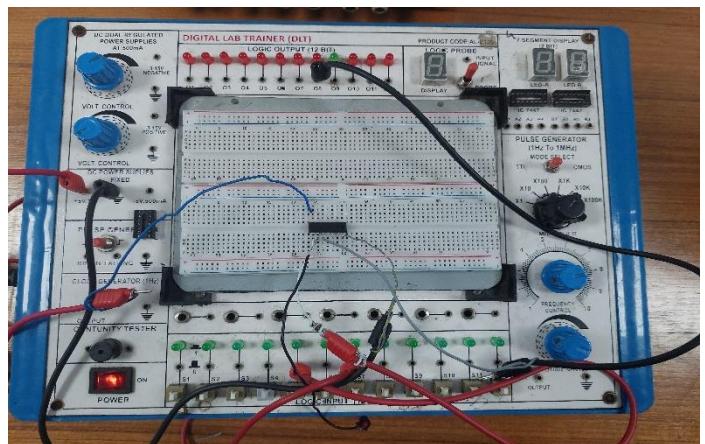
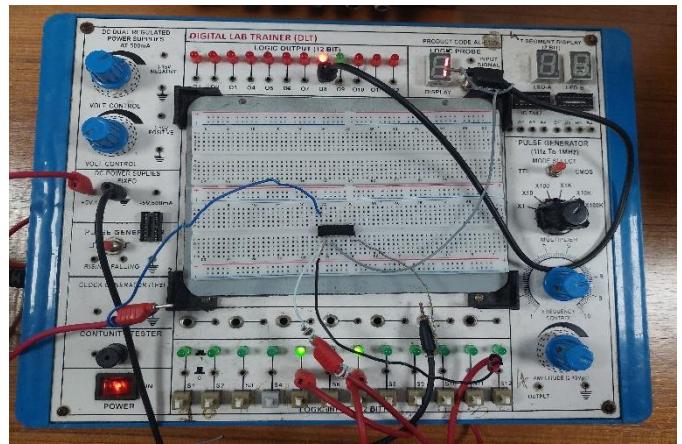


## SIMULATION

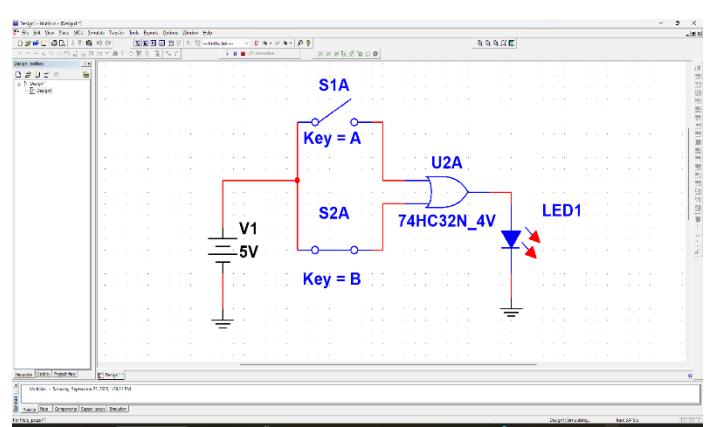


AND Gate  
A = 1, B = 1, Y = 1

## HARDWARE

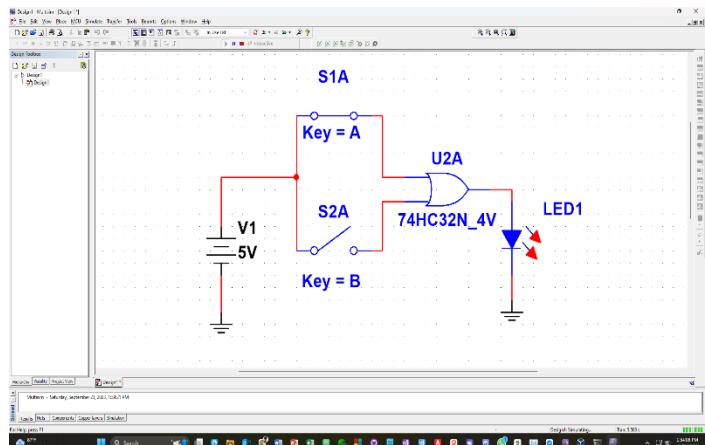


OR Gate  
A = 0, B = 0, Y = 0



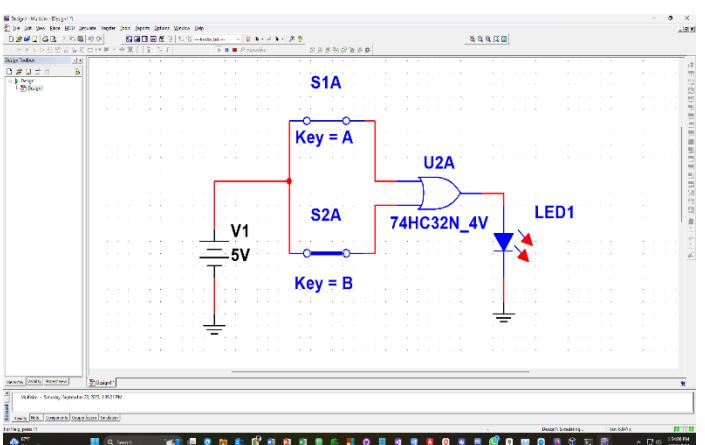
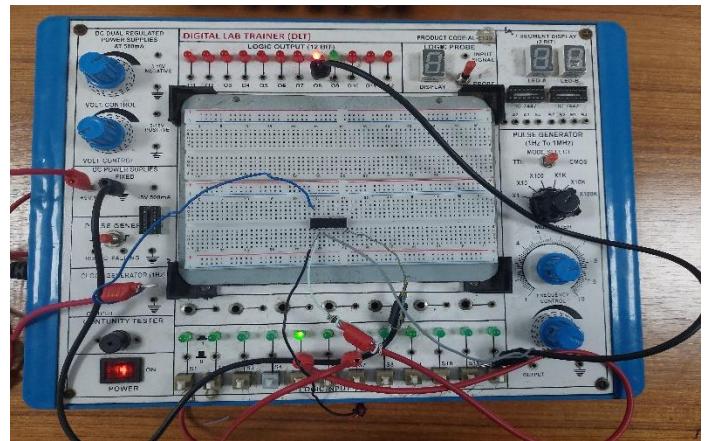
OR Gate  
A = 0, B = 1, Y = 1

## SIMULATION

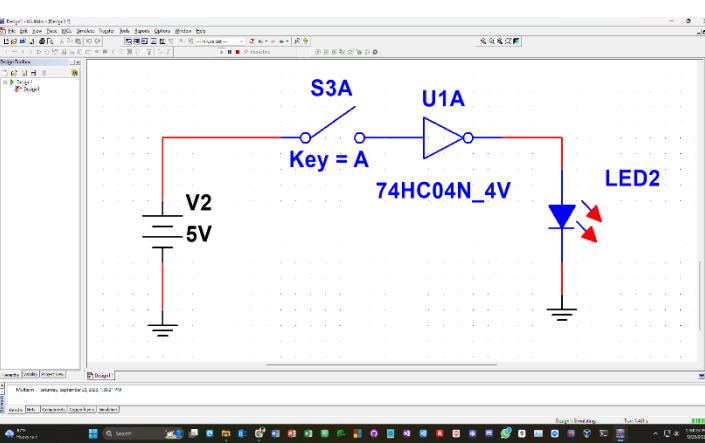
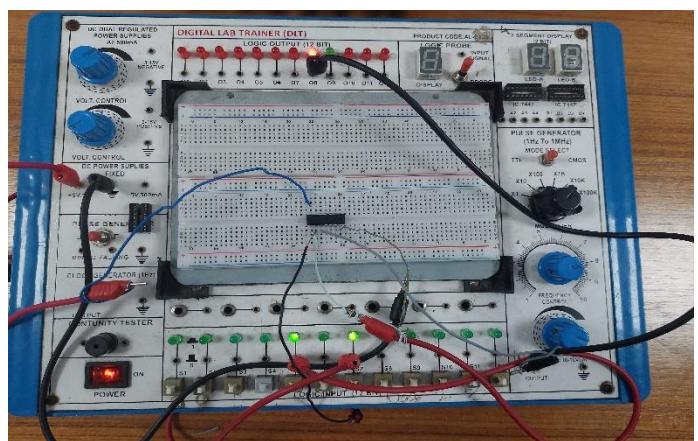


OR Gate  
A = 1, B = 0, Y = 1

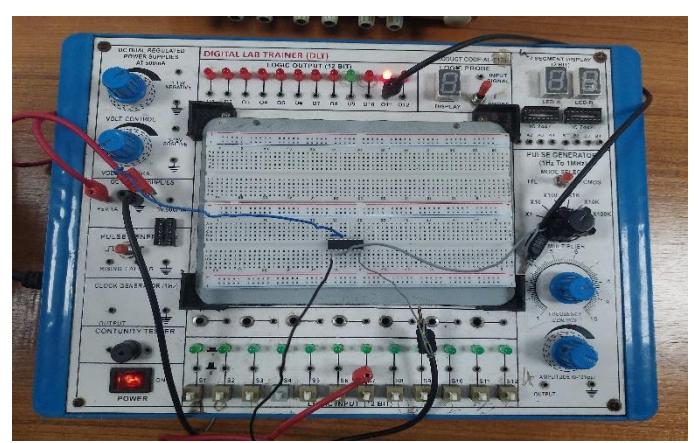
## HARDWARE



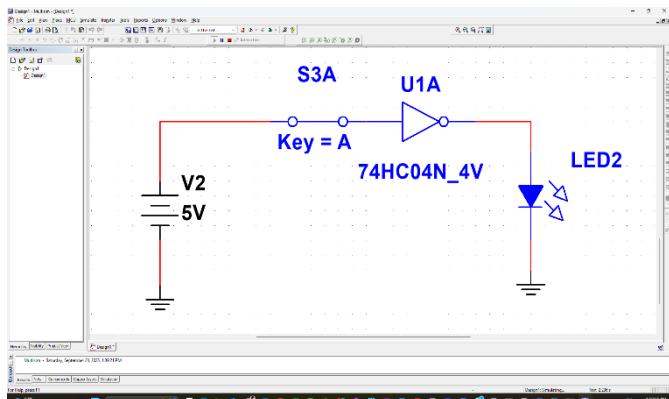
OR Gate  
A = 1, B = 1, Y = 1



NOT Gate  
A = 0, Y = 1



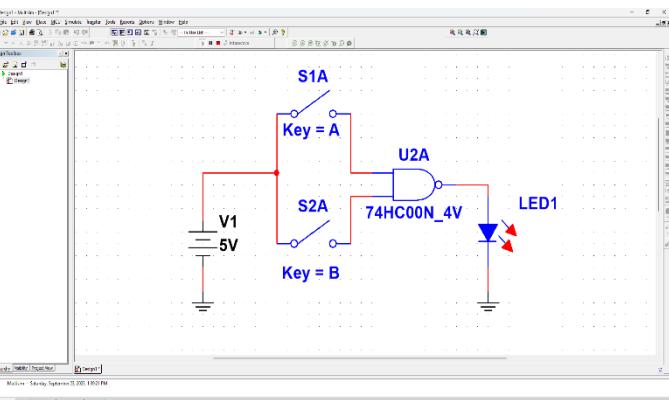
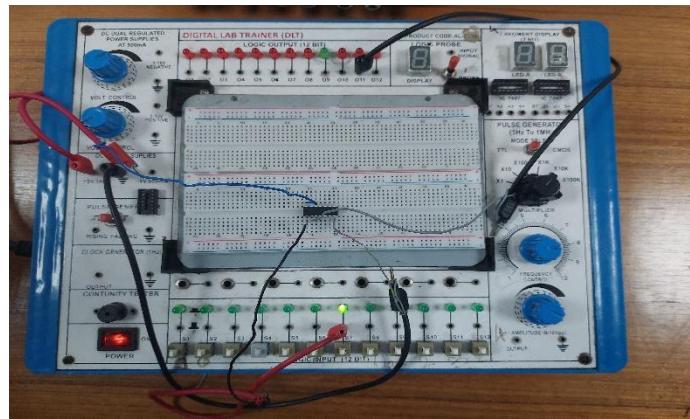
## SIMULATION



NOT Gate

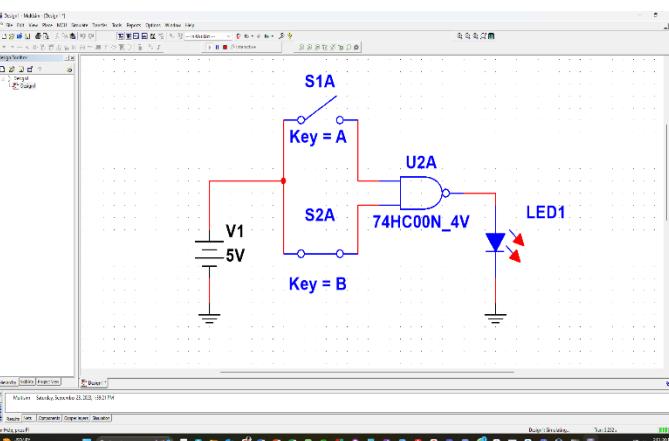
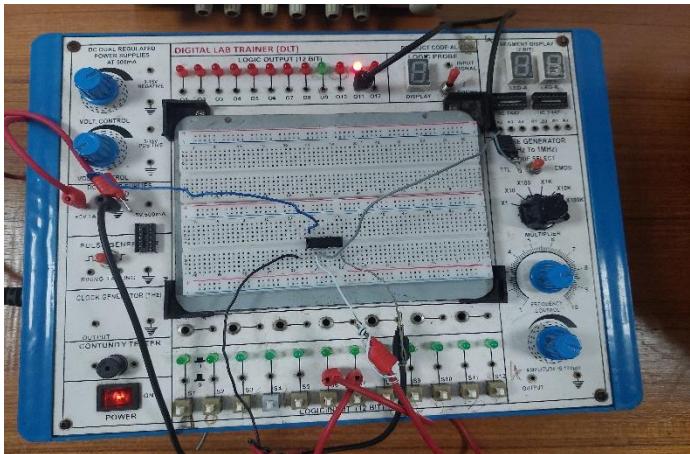
$A = 1, Y = 0$

## HARDWARE



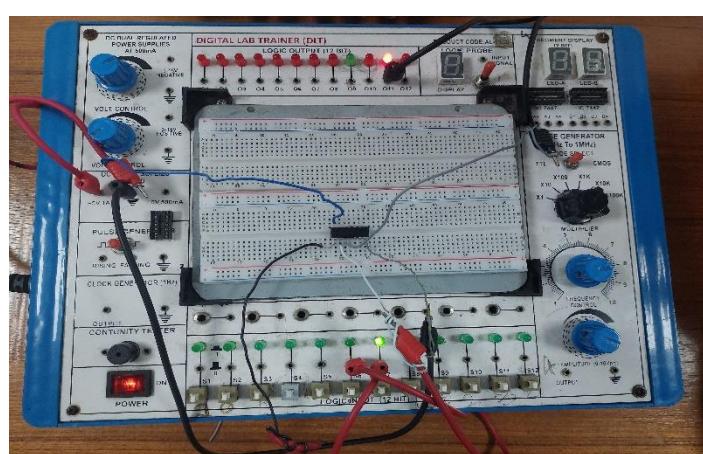
NAND Gate

$A = 0, B = 0, Y = 1$

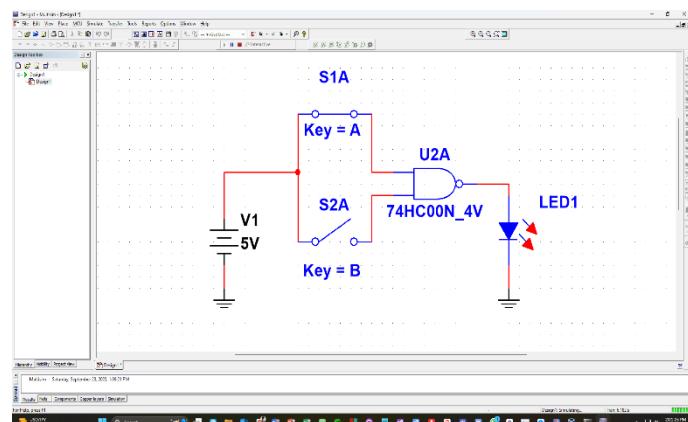


NAND Gate

$A = 0, B = 1, Y = 1$

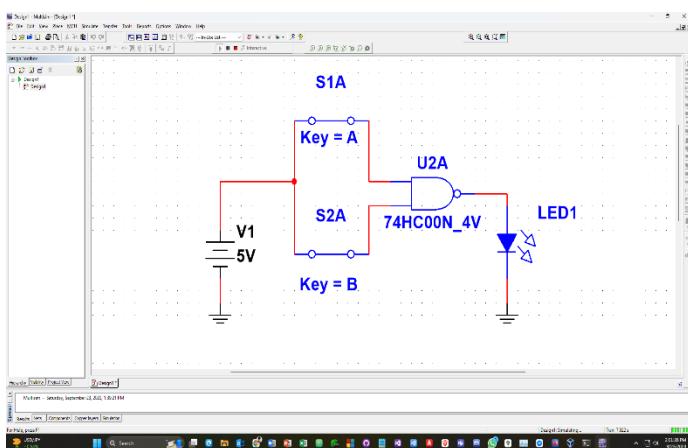
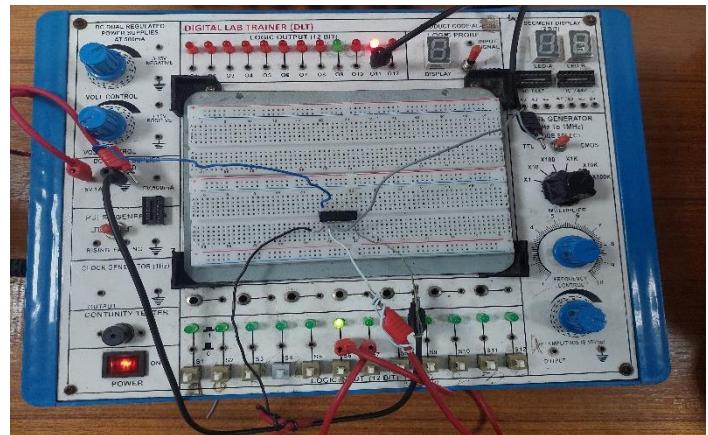


## SIMULATION

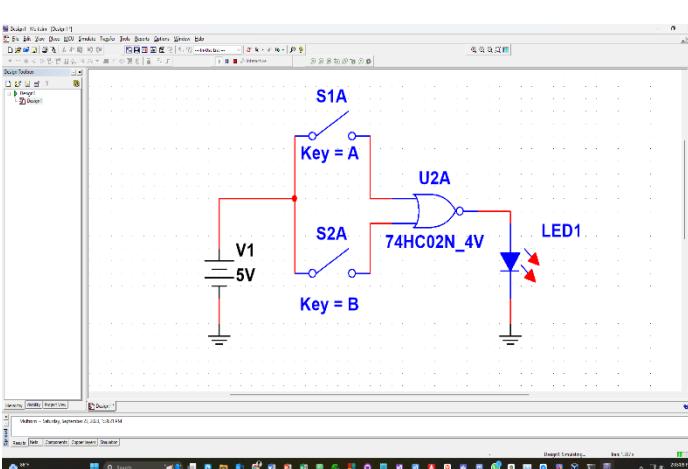
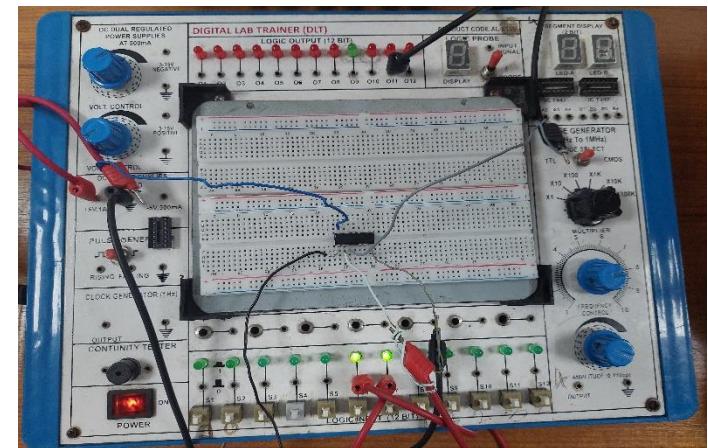


NAND Gate  
A = 1, B = 0, Y = 1

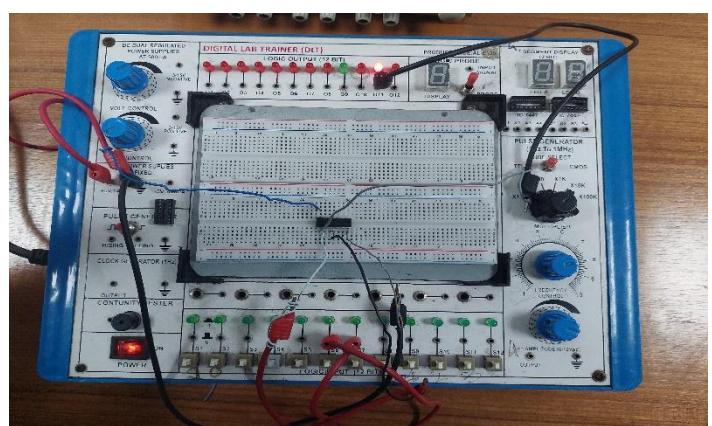
## HARDWARE



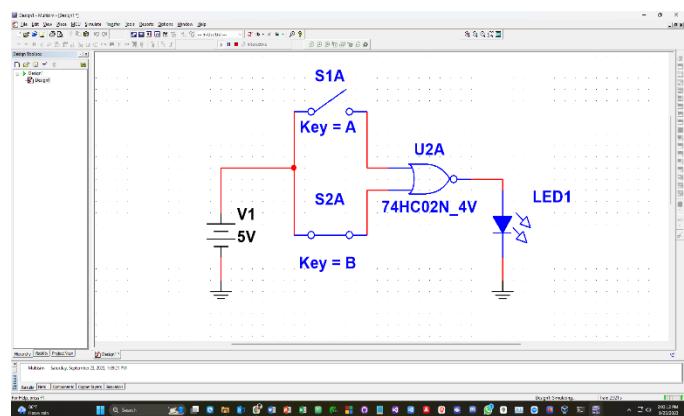
NAND Gate  
A = 1, B = 1, Y = 0



NOR Gate  
A = 0, B = 0, Y = 1

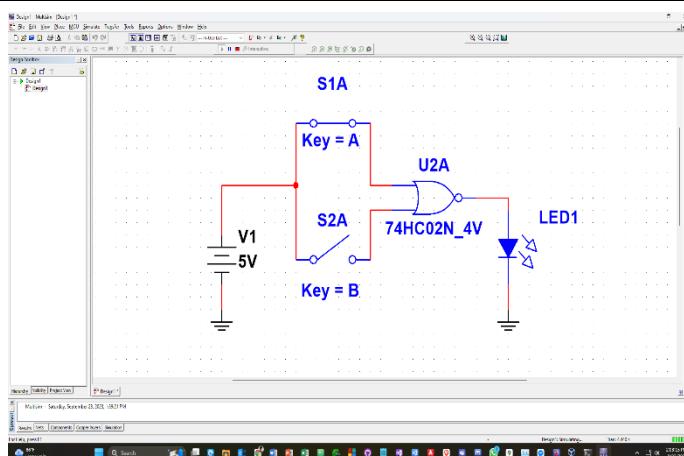
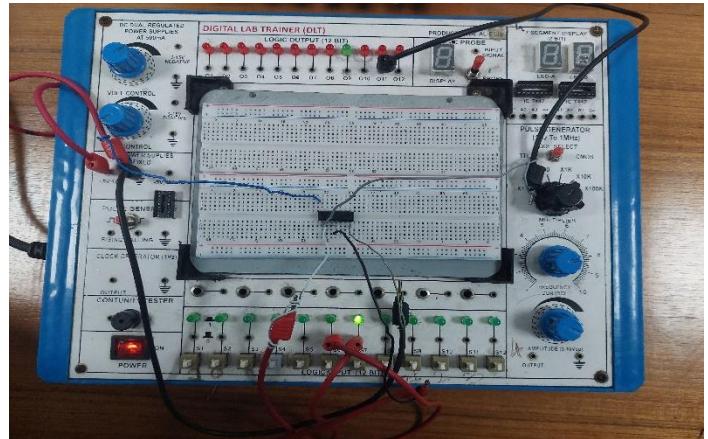


## SIMULATION

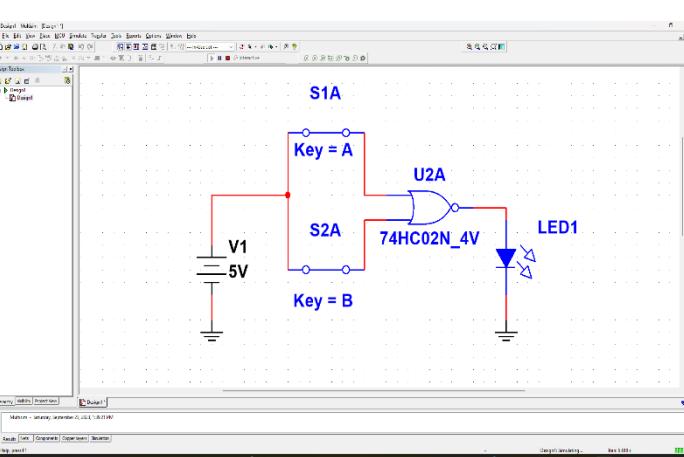
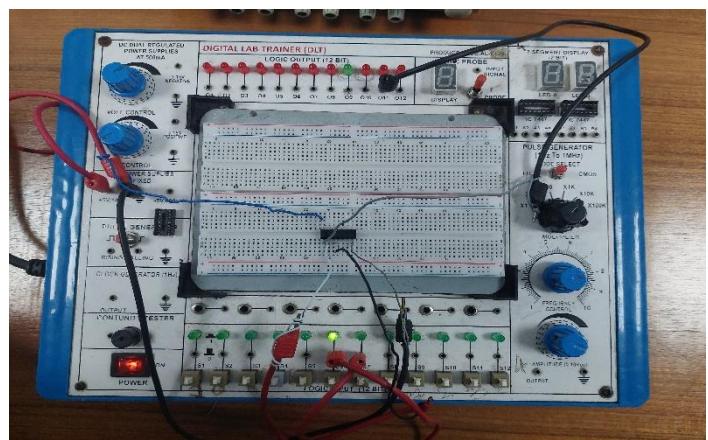


NOR Gate  
A = 0, B = 1, Y = 0

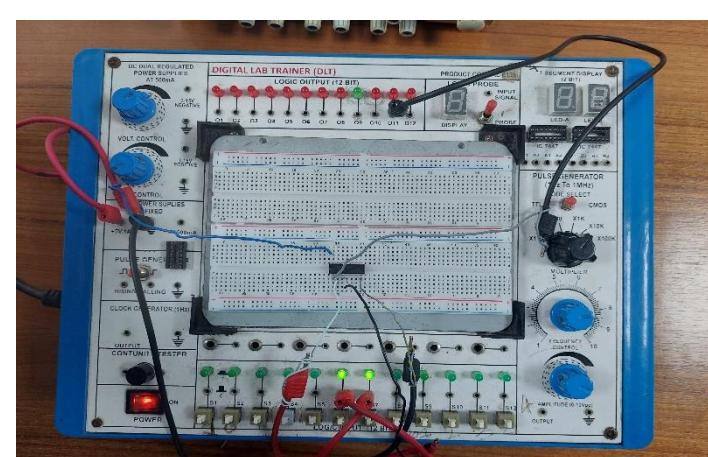
## HARDWARE



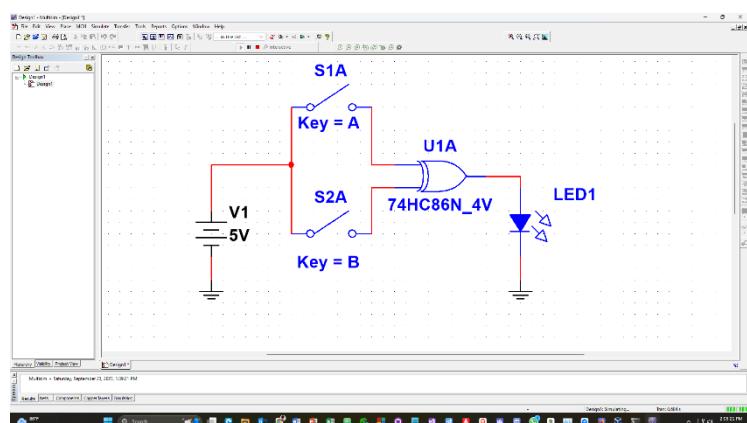
NOR Gate  
A = 1, B = 0, Y = 0



NOR Gate  
A = 1, B = 1, Y = 0



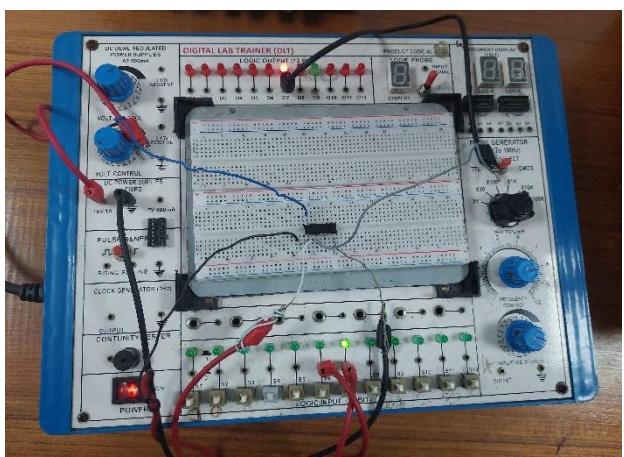
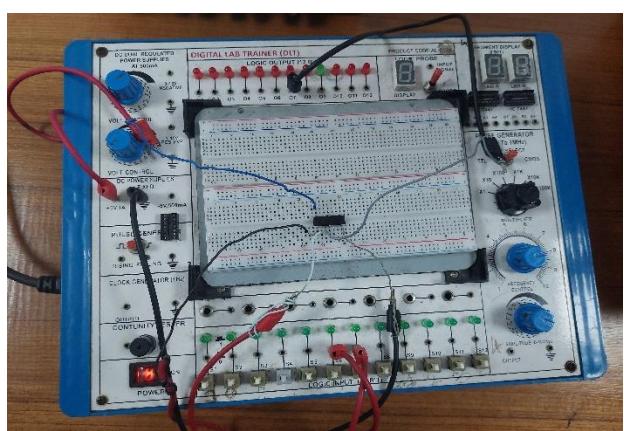
## SIMULATION



XOR Gate

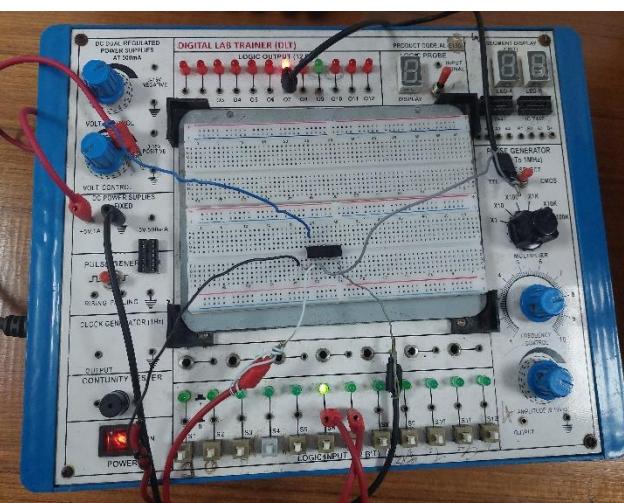
A = 0, B = 0, Y = 0

## HARDWARE



XOR Gate

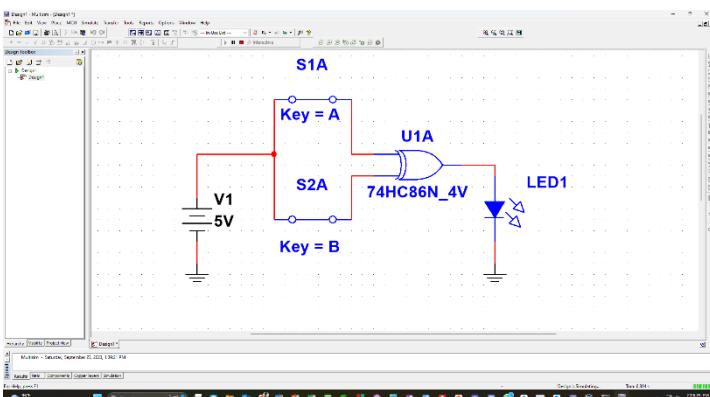
A = 0, B = 1, Y = 1



XOR Gate

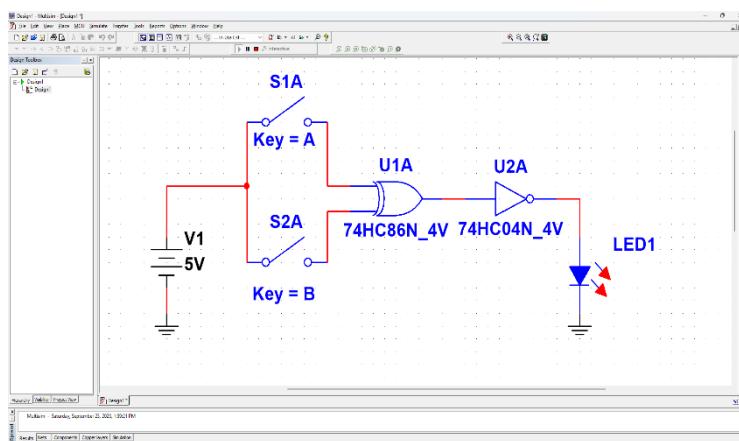
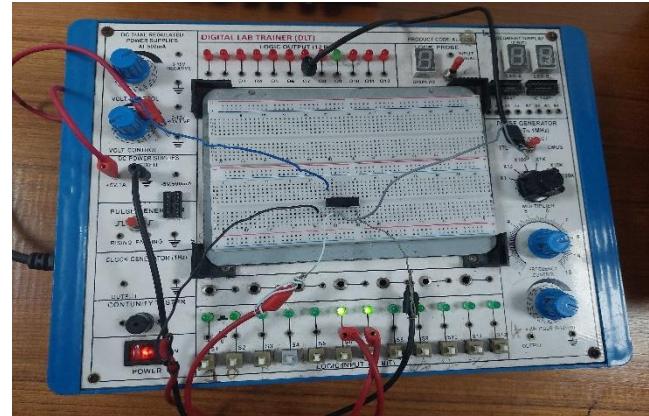
A = 1, B = 0, Y = 1

## SIMULATION

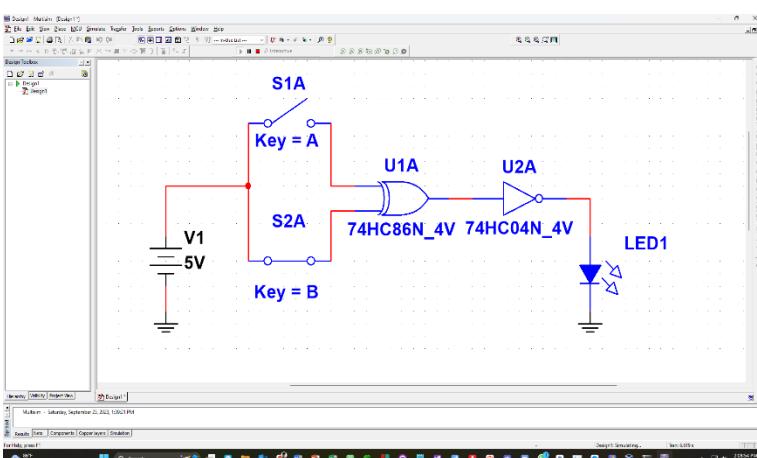
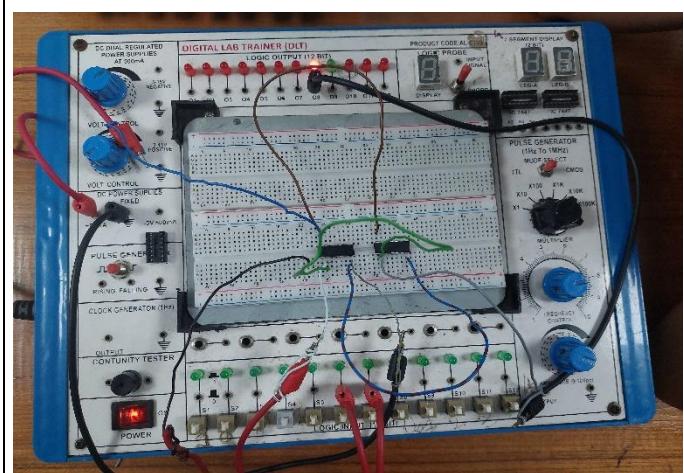


XOR Gate  
A = 1, B = 1, Y = 0

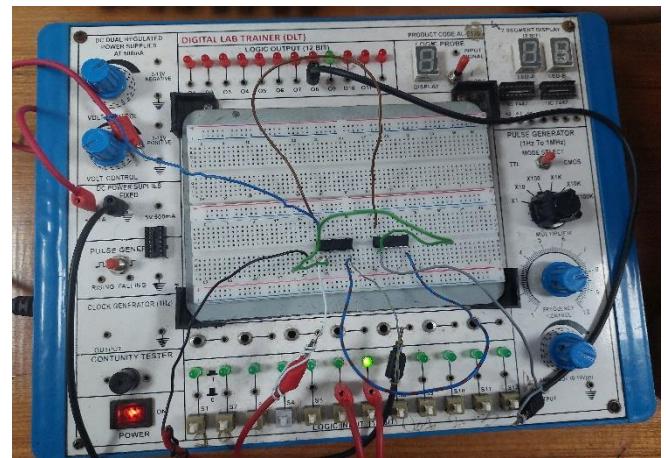
## HARDWARE



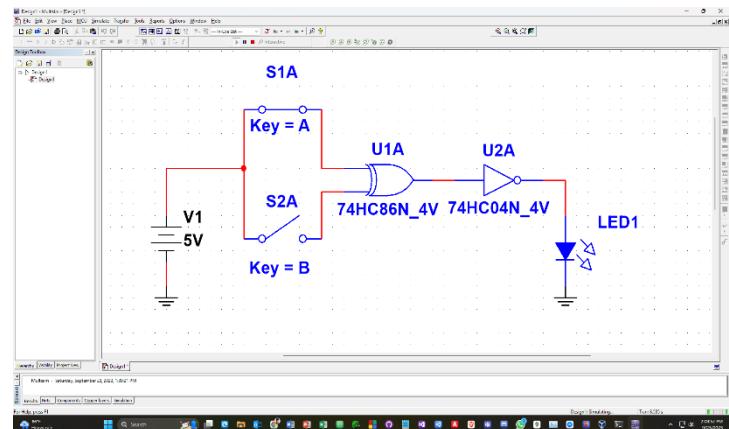
XNOR Gate  
A = 0, B = 0, Y = 1



XNOR Gate  
A = 0, B = 1, Y = 0



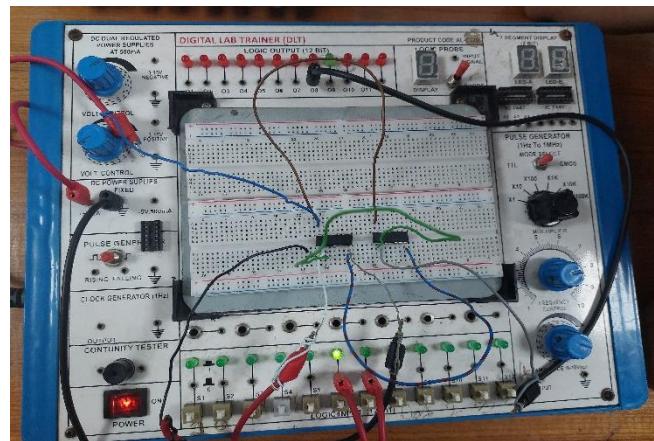
## SIMULATION



XNOR Gate

A = 1, B = 0, Y = 0

## HARDWARE



XNOR Gate

A = 1, B = 1, Y = 1

