

# Electronic Devices

## Final Term Lecture - 07

Reference book:

**Electronic Devices and Circuit Theory (Chapter-7)**

Robert L. Boylestad and L. Nashelsky , (11<sup>th</sup> Edition)



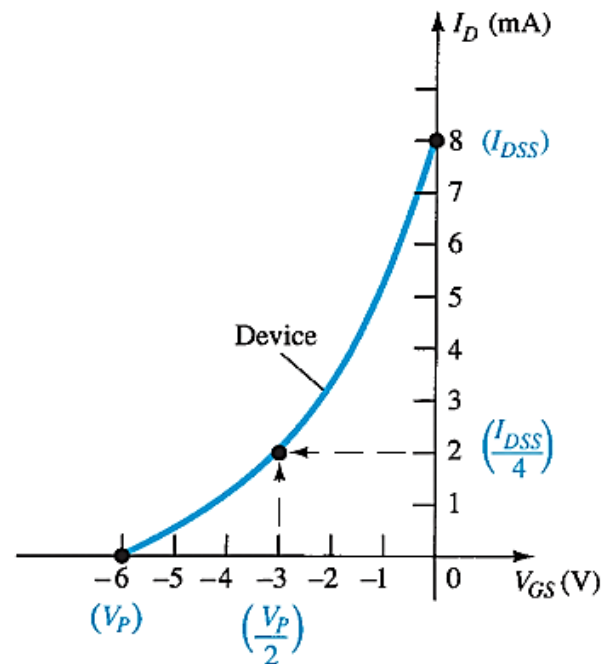
**Faculty of Engineering**

**American International University-Bangladesh**

## SELF-BIAS EXAMPLE Contd.

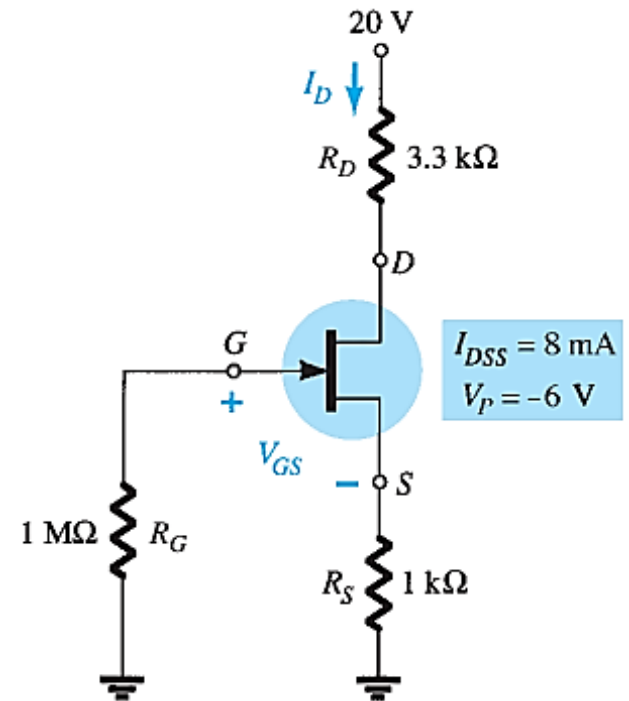
- Plot the **transfer curve** using  $I_{DSS}$  and  $V_P$  using shorthand method:

$V_{GS}$	$I_D$
0	$I_{DSS}$
$0.3V_P$	$I_{DSS}/2$
$0.5V_P$	$I_{DSS}/4$
$V_P$	0mA



**FIG. 7.14**

Sketching the device characteristics for the JFET of Fig. 7.12.



**FIG. 7.12**

Example 7.2.

# SELF-BIAS EXAMPLE Contd.

- Superimpose the **load line** on top of the **transfer curve**:

$$V_{GS_Q} = -2.6 \text{ V}$$

$$I_{D_Q} = 2.6 \text{ mA}$$

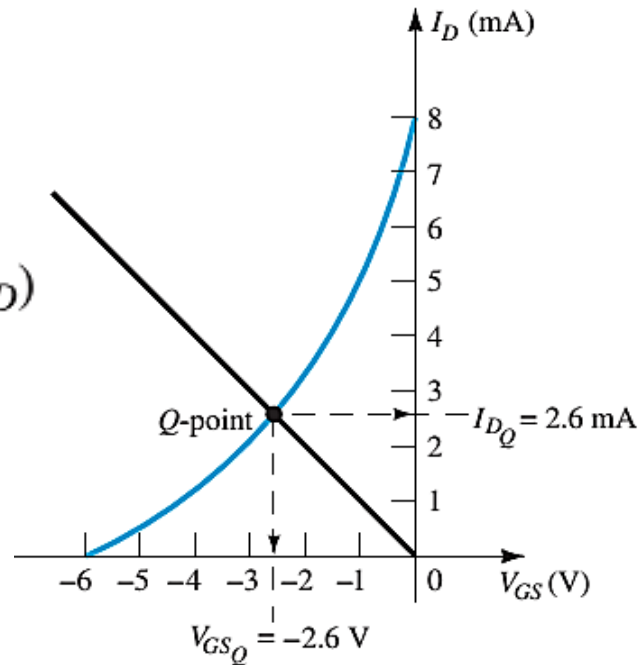
$$V_{DS} = V_{DD} - I_D(R_S + R_D)$$

$$V_S = I_D R_S$$

$$V_G = 0 \text{ V}$$

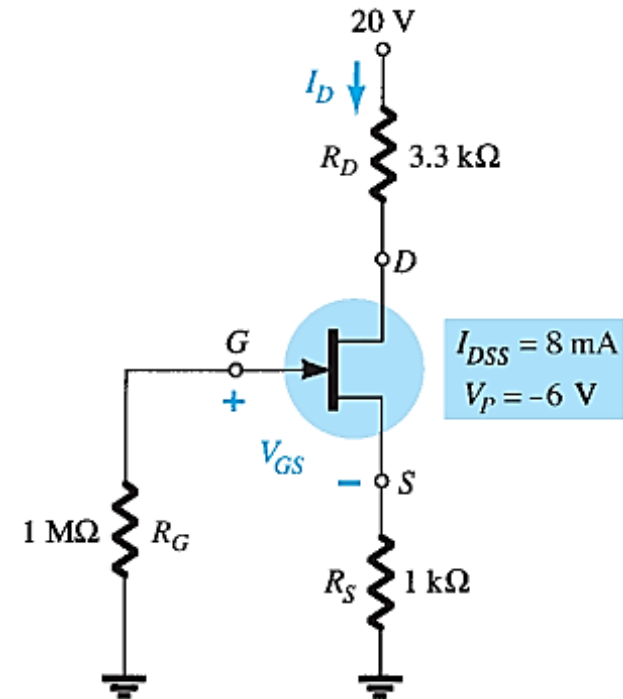
$$V_D = V_{DS} + V_S$$

$$V_D = V_{DD} - I_D R_D$$



**FIG. 7.15**

Determining the  $Q$ -point for the network of Fig. 7.12.

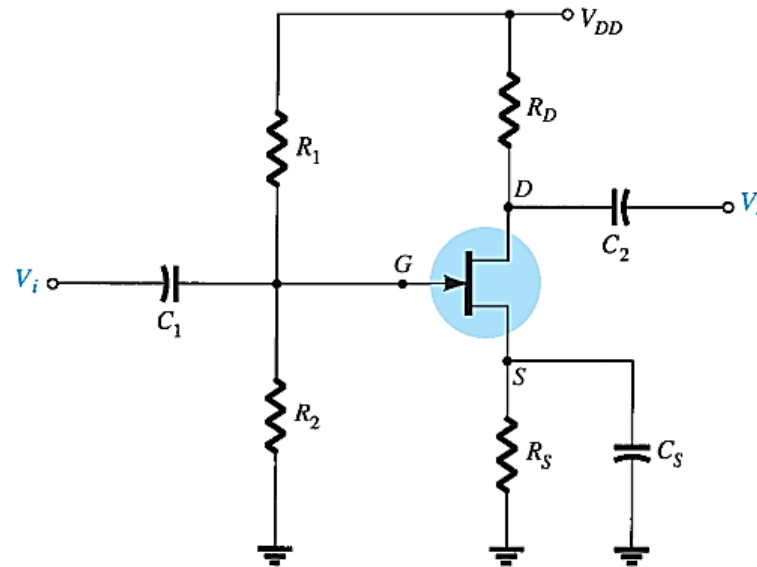


**FIG. 7.12**

Example 7.2.

# JFET: VOLTAGE-DIVIDER BIAS

- The source  $V_{DD}$  **was separated into two equivalent sources** to permit a further separation of the input and output regions of the network.
- Since  $I_G = 0A$ , Kirchoff's current law requires that  $I_{R1} = I_{R2}$  and the series equivalent circuit appearing to the left of the figure can be used to find the level of  $V_G$ .



**FIG. 7.17**

*Voltage-divider bias arrangement.*

# VOLTAGE-DIVIDER BIAS

- $V_G$  can be found using the voltage divider rule:

$$V_G = \frac{R_2 V_{DD}}{R_1 + R_2}$$

- Using Kirchoff's Law on the input loop:

$$V_D = V_{DD} - I_D R_D$$

$$V_{DS} = V_{DD} - I_D (R_D + R_S)$$

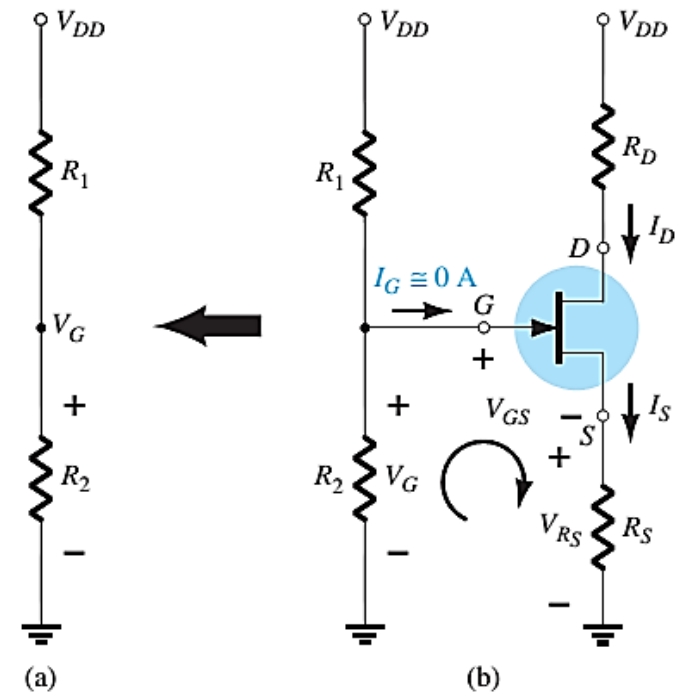
$$V_S = I_D R_S$$

$$V_{GS} = V_G - I_D R_S$$

- Rearranging and using  $I_D = I_S$ :

$$I_{R1} = I_{R2} = \frac{V_{DD}}{R_1 + R_2}$$

- Again the Q point needs to be established by plotting a line that intersects the transfer curve.



**FIG. 7.18**

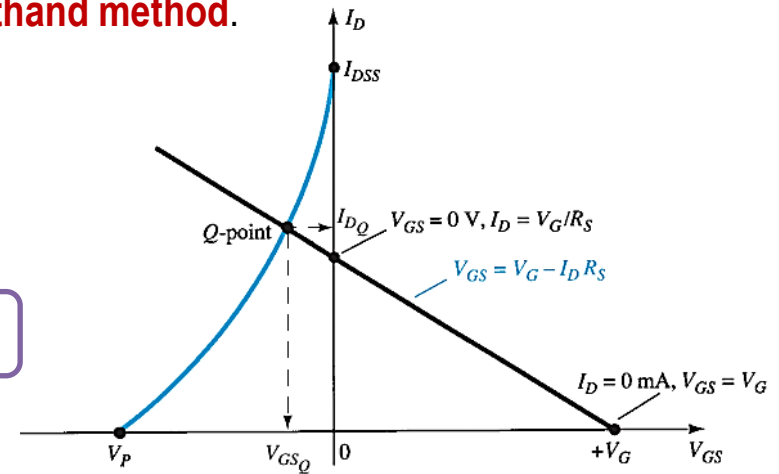
*Redrawn network of Fig. 7.17 for dc analysis.*

# VOLTAGE-DIVIDER BIAS

- **Graphical Approach** ( to find  $V_{GSQ}$  and  $I_{DQ}$ ):
  - Plot a line for:
    - »  $V_{GS} = V_G$  when  $I_D = 0A$
    - »  $V_{GS} = 0V$  when  $I_D = V_G/R_S$ .
  - Plot the **transfer curve** using  $I_{DSS}$  and  $V_P$  using **shorthand method**.
  - The Q-point is located at the intersection.

$V_{GS}$	$I_D$
0	$I_{DSS}$
$0.3V_P$	$I_{DSS}/2$
$0.5V_P$	$I_{DSS}/4$
$V_P$	0mA

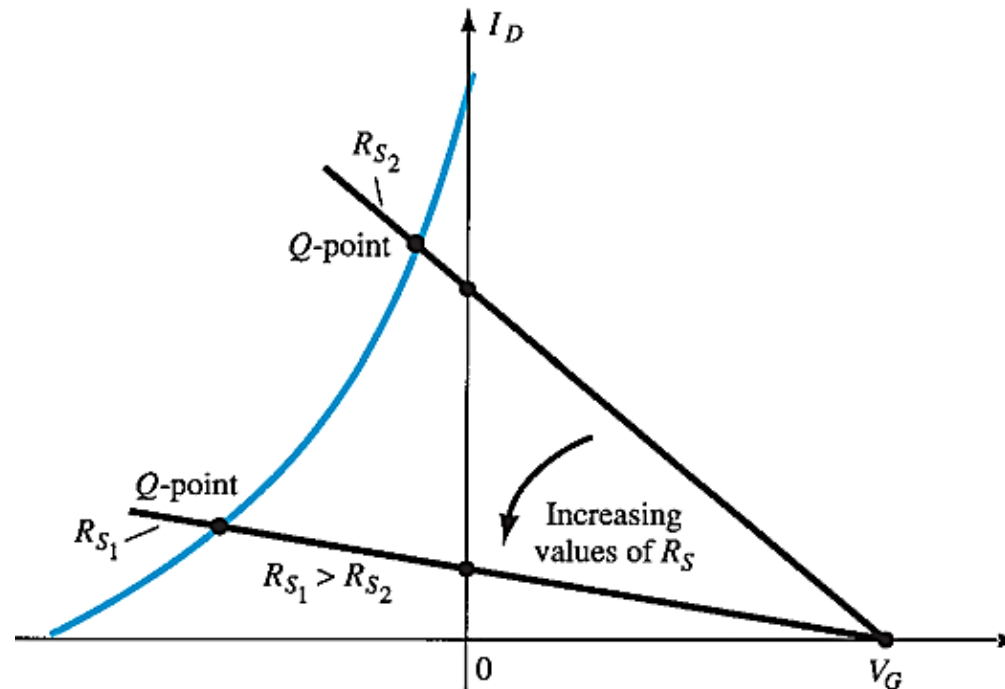
$$V_{GS} = V_G - I_D R_S$$



**FIG. 7.19**

Sketching the network equation for the voltage-divider configuration.

# EFFECT OF INCREASING VALUES OF $R_S$



**FIG. 7.20**

*Effect of  $R_S$  on the resulting Q-point.*

# JFET: VOLTAGE-DIVIDER BIAS EXAMPLE

- Determine  $I_{DQ}$ ,  $V_{GSQ}$ ,  $V_D$ ,  $V_S$ ,  $V_{DS}$  and  $V_{DG}$ .

$$V_G = \frac{R_2 V_{DD}}{R_1 + R_2}$$

$$V_{GS} = V_G - I_D R_S$$

$$V_{DS} = V_{DD} - I_D (R_D + R_S)$$

$$V_{GSQ} = -1.8V$$

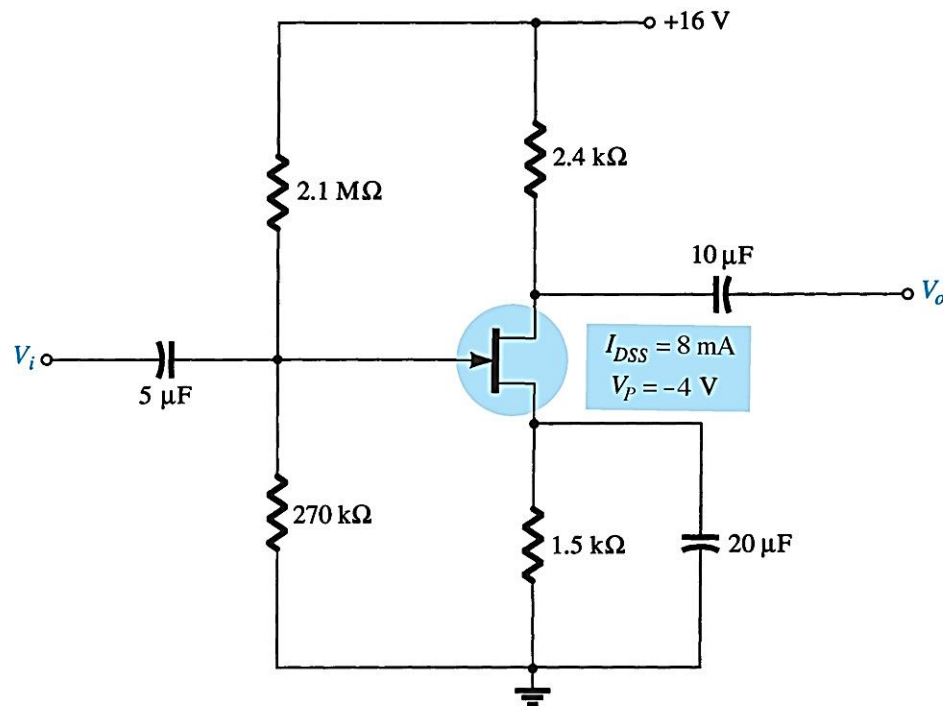
$$I_{DQ} = 2.4mA$$

$$V_D = 10.24V$$

$$V_S = 3.6V$$

$$V_{DS} = 6.64V$$

$$V_{DG} = 8.24V$$





# VOLTAGE-DIVIDER BIAS EXAMPLE Contd.

- **Graphical Approach** ( to find  $V_{GSQ}$  and  $I_{DQ}$ ):
  - Plot a line for:
    - »  $V_{GS} = V_G$  when  $I_D = 0A$
    - »  $V_{GS} = 0V$  when  $I_D = V_G/R_S$ .
  - Plot the **transfer curve** using  $I_{DSS}$  and  $V_P$  using **shorthand method**.
  - Identify the Q-point.

$$V_G = \frac{R_2 V_{DD}}{R_1 + R_2}$$

$$V_S = I_D R_S$$

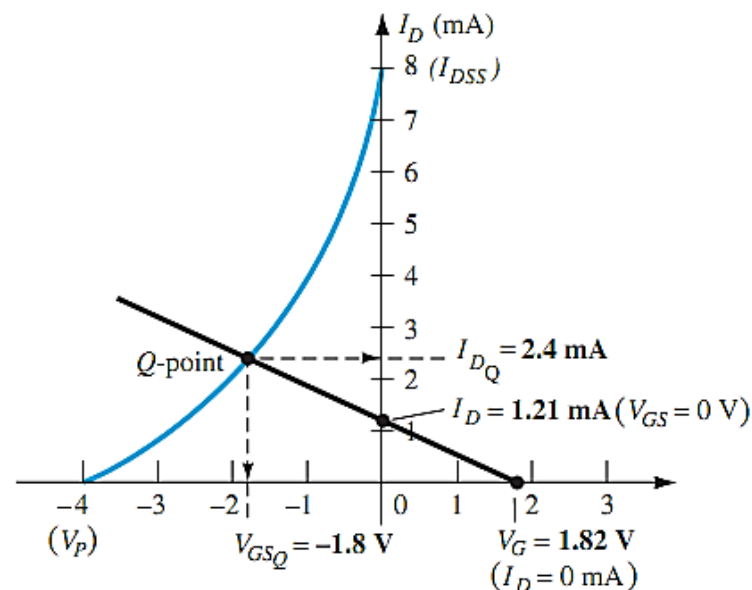
$$V_{DS} = V_{DD} - I_D (R_D + R_S)$$

$$V_{GS} = V_G - I_D R_S$$

$$V_{DS} = V_D - V_S$$

$$V_D = V_{DD} - I_D R_D$$

$$V_{DG} = V_D - V_G$$



**FIG. 7.22**

*Determining the Q-point for the network of Fig. 7.21.*

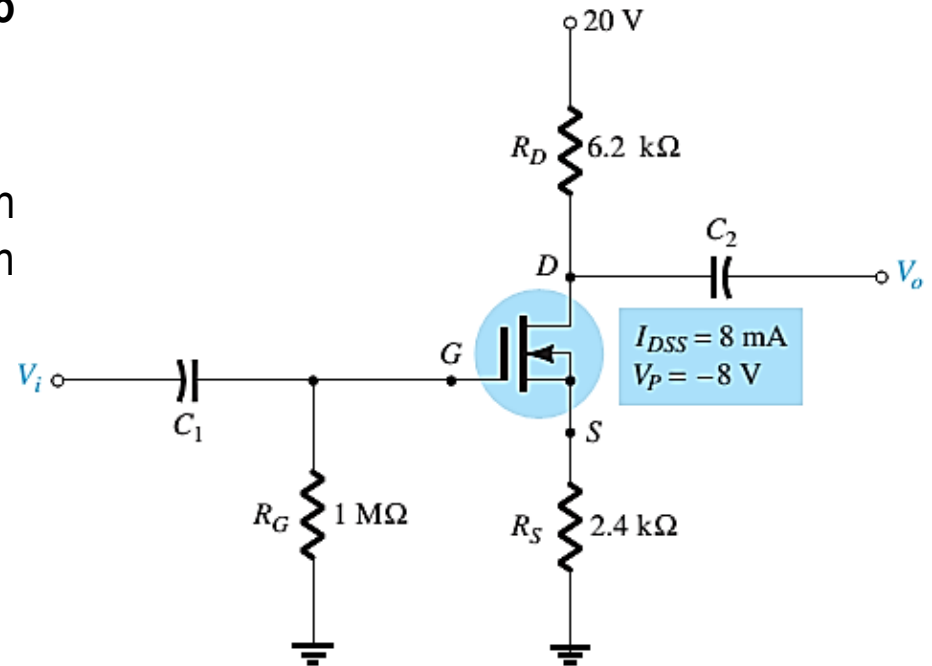
# D-MOSFET SELF-BIAS

- D-MOSFET bias circuits are **similar** to JFETs.
- The only **difference** is that D-MOSFETs can operate with **positive** values of  $V_{GS}$  and with  $I_D$  values that exceed  $I_{DSS}$ .

$$I_G \approx 0A$$

$$I_D = I_S$$

$$I_D = I_{DSS} \left( 1 - \frac{V_{GS}}{V_P} \right)^2$$



**FIG. 7.33**  
Example 7.8.

# D-MOSFET SELF-BIAS

- **Graphical Approach** (to find  $V_{GSQ}$  and  $I_{DQ}$ ):

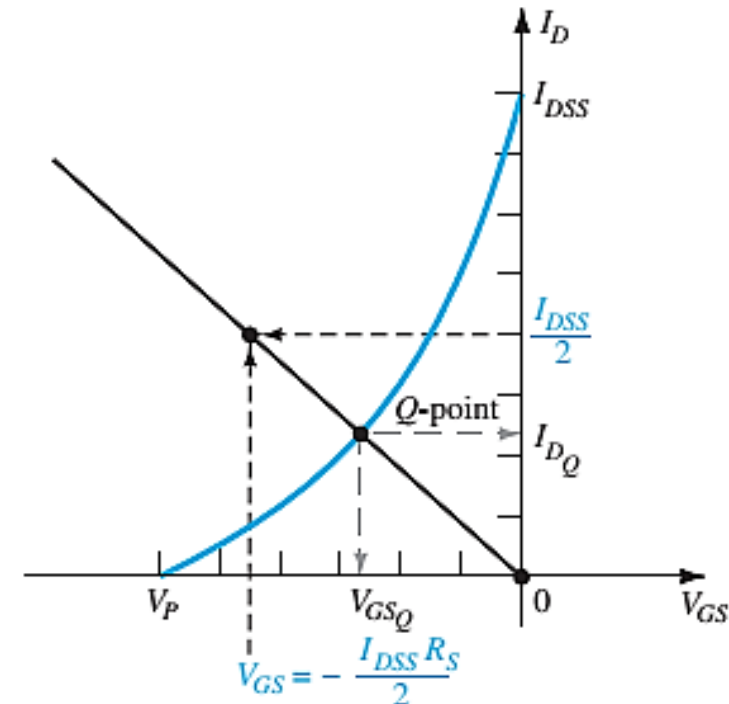
- Plot the **transfer curve** using  $I_{DSS}$  and  $V_P$  using **shorthand method**.

- Plot  $I_D$  vs  $V_{GS}$  using  $V_{GS} = -I_D R_S$ .

- Take a positive value of  $V_{GS}$  and find the  $I_D$  value using

$$I_D = I_{DSS} \left(1 - \frac{V_{GS}}{V_P}\right)^2$$

- The Q-point is located at the intersection.

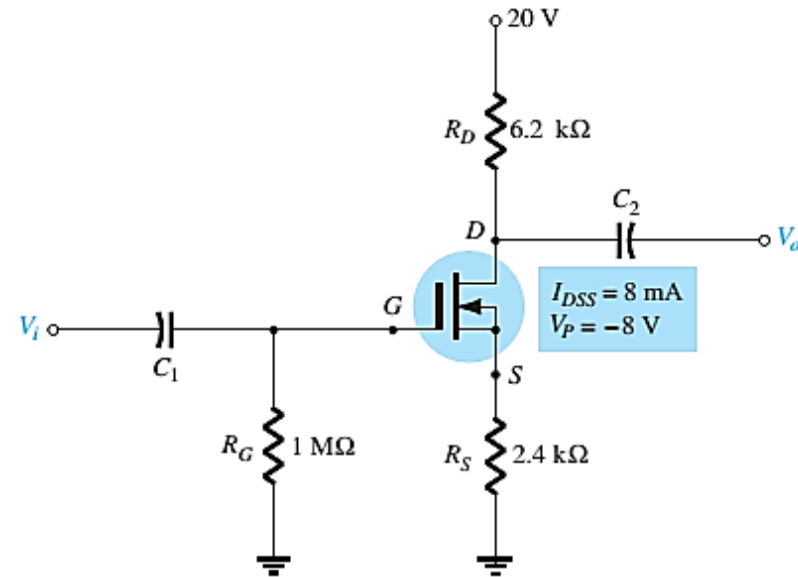


# D-MOSFET SELF-BIAS EXAMPLE

- Determine the  $I_{DQ}$ ,  $V_{GSQ}$  and  $V_D$ .
- Graphical Approach** (to find  $V_{GSQ}$  and  $I_{DQ}$ ):
  - Plot the **transfer curve** using  $I_{DSS}$  and  $V_P$  using **shorthand method**.
  - Take a positive value of  $V_{GS}$  and find the  $I_D$  value using

$$I_D = I_{DSS} \left( 1 - \frac{V_{GS}}{V_P} \right)^2$$

- Plot  $I_D$  vs  $V_{GS}$  using  $V_{GS} = -I_D R_S$ .
- Identify the intersection Q-point.



**FIG. 7.33**  
Example 7.8.

# D-MOSFET SELF-BIAS EXAMPLE

$$V_D = V_{DD} - I_D R_D$$

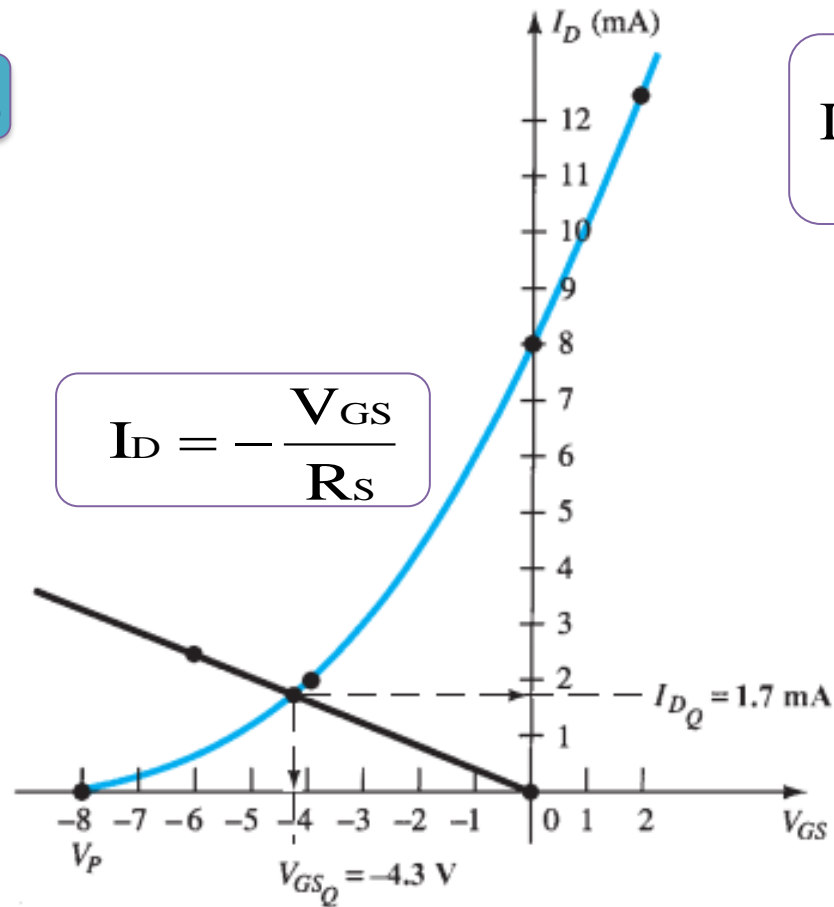
$$V_{GSQ} = -4.3 \text{ V}$$

$$I_{DQ} = 1.7 \text{ mA}$$

$$V_D = 9.46 \text{ V}$$

$$I_D = -\frac{V_{GS}}{R_S}$$

$$I_D = I_{DSS} \left(1 - \frac{V_{GS}}{V_P}\right)^2$$



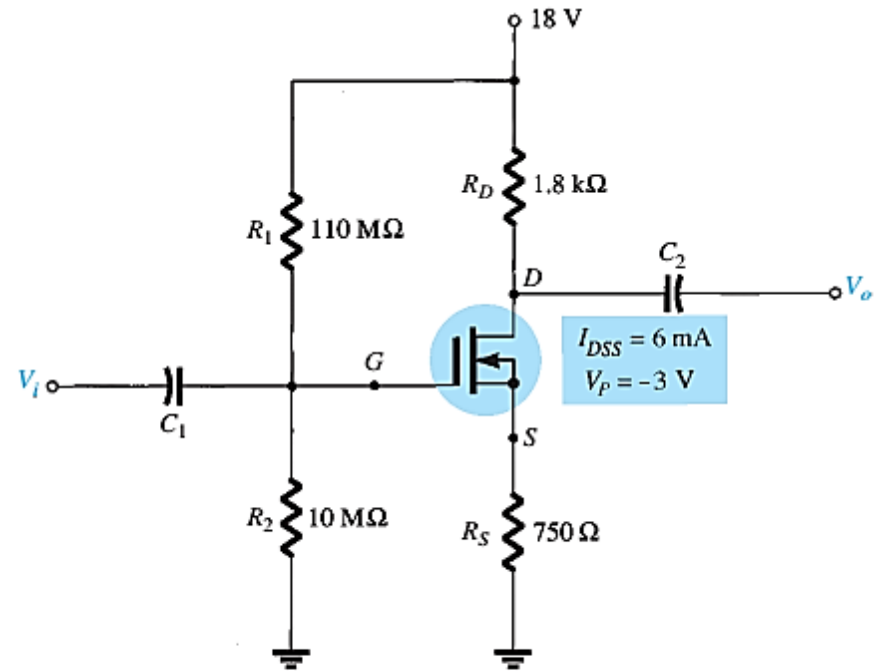
# D-MOSFET VOLTAGE-DIVIDER BIAS

- D-MOSFET bias circuits are similar to **JFETs**.

$$I_G \approx 0A$$

$$I_D = I_S$$

$$I_D = I_{DSS} \left(1 - \frac{V_{GS}}{V_P}\right)^2$$



**FIG. 7.30**

Example 7.6.

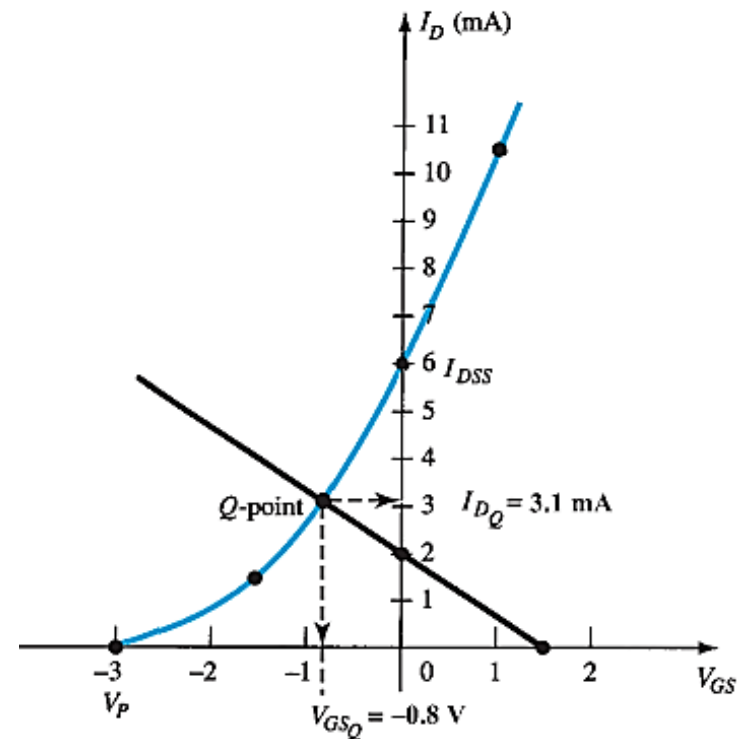
# D-MOSFET VOLTAGE-DIVIDER BIAS

- **Graphical Approach** (to find  $V_{GSQ}$  and  $I_{DQ}$ ):

- Plot the **transfer curve** using  $I_{DSS}$  and  $V_P$  using **shorthand method**.
- Take a positive value of  $V_{GS}$  and find the  $I_D$  value using

$$I_D = I_{DSS} \left( 1 - \frac{V_{GS}}{V_P} \right)^2$$

- Plot  $I_D$  vs  $V_{GS}$  using  $V_{GS} = V_G - I_D R_S$ .
- The Q-point is located at the intersection.



**FIG. 7.31**

*Determining the Q-point for the network of Fig. 7.30.*

# End of Lecture-7

