

**FIG. 6.53**  
Transfer characteristics for the n-channel J2N3819 JFET of Fig. 6.51.

## PROBLEMS

\*Note: Asterisks indicate more difficult problems.

### 6.2 Construction and Characteristics of JFETs

1. a. Draw the basic construction of a *p*-channel JFET.  
b. Apply the proper biasing between drain and source and sketch the depletion region for  $V_{GS} = 0$  V.
2. Using the characteristics of Fig. 6.11, determine  $I_D$  for the following levels of  $V_{GS}$  (with  $V_{DS} > V_P$ ):  
a.  $V_{GS} = 0$  V.  
b.  $V_{GS} = -1$  V.  
c.  $V_{GS} = -1.5$  V.  
d.  $V_{GS} = -1.8$  V.  
e.  $V_{GS} = -4$  V.  
f.  $V_{GS} = -6$  V.
3. Using the results of problem 2 plot the transfer characteristics of  $I_D$  vs.  $V_{GS}$ .
4. a. Determine  $V_{DS}$  for  $V_{GS} = 0$  V and  $I_D = 6$  mA using the characteristics of Fig. 6.11.  
b. Using the results of part (a), calculate the resistance of the JFET for the region  $I_D = 0$  to 6 mA for  $V_{GS} = 0$  V.  
c. Determine  $V_{DS}$  for  $V_{GS} = -1$  V and  $I_D = 3$  mA.  
d. Using the results of part (c), calculate the resistance of the JFET for the region  $I_D = 0$  to 3 mA for  $V_{GS} = -1$  V.  
e. Determine  $V_{DS}$  for  $V_{GS} = -2$  V and  $I_D = 1.5$  mA.  
f. Using the results of part (e), calculate the resistance of the JFET for the region  $I_D = 0$  to 1.5 mA for  $V_{GS} = -2$  V.  
g. Defining the result of part (b) as  $r_o$ , determine the resistance for  $V_{GS} = -1$  V using Eq. (6.1) and compare with the results of part (d).  
h. Repeat part (g) for  $V_{GS} = -2$  V using the same equation, and compare the results with part (f).  
i. Based on the results of parts (g) and (h), does Eq. (6.1) appear to be a valid approximation?
5. Using the characteristics of Fig. 6.11:  
a. Determine the difference in drain current (for  $V_{DS} > V_P$ ) between  $V_{GS} = 0$  V and  $V_{GS} = -1$  V.  
b. Repeat part (a) between  $V_{GS} = -1$  and  $-2$  V.  
c. Repeat part (a) between  $V_{GS} = -2$  and  $-3$  V.  
d. Repeat part (a) between  $V_{GS} = -3$  and  $-4$  V.  
e. Is there a marked change in the difference in current levels as  $V_{GS}$  becomes increasingly negative?

- f. Is the relationship between the change in  $V_{GS}$  and the resulting change in  $I_D$  linear or nonlinear? Explain.
6. What are the major differences between the collector characteristics of a BJT transistor and the drain characteristics of a JFET transistor? Compare the units of each axis and the controlling variable. How does  $I_C$  react to increasing levels of  $I_B$  versus changes in  $I_D$  to increasingly negative values of  $V_{GS}$ ? How does the spacing between steps of  $I_B$  compare to the spacing between steps of  $V_{GS}$ ? Compare  $V_{C_{sat}}$  to  $V_P$  in defining the nonlinear region at low levels of output voltage.
7. a. Describe in your own words why  $I_G$  is effectively 0 A for a JFET transistor.  
 b. Why is the input impedance to a JFET so high?  
 c. Why is the terminology *field effect* appropriate for this important three-terminal device?
8. Given  $I_{DSS} = 12 \text{ mA}$  and  $|V_P| = 6 \text{ V}$ , sketch a probable distribution of characteristic curves for the JFET (similar to Fig. 6.11).
9. In general, comment on the polarity of the various voltages and direction of the currents for an *n*-channel JFET versus a *p*-channel JFET.

### 6.3 Transfer Characteristics

10. Given the characteristics of Fig. 6.54:  
 a. Sketch the transfer characteristics directly from the drain characteristics.  
 b. Using Fig. 6.54 to establish the values of  $I_{DSS}$  and  $V_P$ , sketch the transfer characteristics using Shockley's equation.  
 c. Compare the characteristics of parts (a) and (b). Are there any major differences?

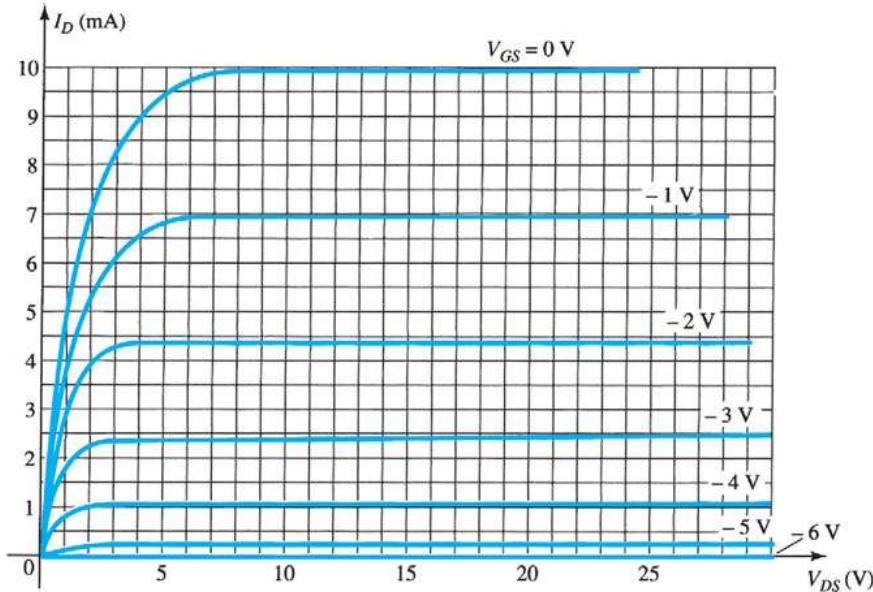


FIG. 6.54  
Problems 10 and 20.

11. a. Given  $I_{DSS} = 12 \text{ mA}$  and  $V_P = -4 \text{ V}$ , sketch the transfer characteristics for the JFET transistor.  
 b. Sketch the drain characteristics for the device of part (a).
12. Given  $I_{DSS} = 9 \text{ mA}$  and  $V_P = -4 \text{ V}$ , determine  $I_D$  when:  
 a.  $V_{GS} = 0 \text{ V}$ .  
 b.  $V_{GS} = -2 \text{ V}$ .  
 c.  $V_{GS} = -4 \text{ V}$ .  
 d.  $V_{GS} = -6 \text{ V}$ .
13. Given  $I_{DSS} = 16 \text{ mA}$  and  $V_P = -5 \text{ V}$ , sketch the transfer characteristics using the data points of Table 6.1. Determine the value of  $I_D$  at  $V_{GS} = -3 \text{ V}$  from the curve, and compare it to the value determined using Shockley's equation. Repeat the above for  $V_{GS} = -1 \text{ V}$ .
14. For a particular JFET if  $I_D = 4 \text{ mA}$  when  $V_{GS} = -3 \text{ V}$ , determine  $V_P$  if  $I_{DSS} = 12 \text{ mA}$ .
15. Given  $I_{DSS} = 6 \text{ mA}$  and  $V_P = -4.5 \text{ V}$ :  
 a. Determine  $I_D$  at  $V_{GS} = -2$  and  $-3.6 \text{ V}$ .  
 b. Determine  $V_{GS}$  at  $I_D = 3$  and  $5.5 \text{ mA}$ .
16. Given a  $Q$ -point of  $I_{DQ} = 3 \text{ mA}$  and  $V_{GS} = -3 \text{ V}$ , determine  $I_{DSS}$  if  $V_P = -6 \text{ V}$ .

17. A *p*-channel JFET has device parameters of  $I_{DSS} = 7.5$  mA and  $V_P = 4$  V. Sketch the transfer characteristics.

#### 6.4 Specification Sheets (JFETs)

18. Define the region of operation for the 2N5457 JFET of Fig. 6.20 using the range of  $I_{DSS}$  and  $V_P$  provided. That is, sketch the transfer curve defined by the maximum  $I_{DSS}$  and  $V_P$  and the transfer curve for the minimum  $I_{DSS}$  and  $V_P$ . Then, shade in the resulting area between the two curves.
19. For the 2N5457 JFET of Fig. 6.20, what is the power rating at a typical operating temperature of 45°C using the 5.0 mW/°C derating factor.
20. Define the region of operation for the JFET of Fig. 6.54 if  $V_{DS_{max}} = 30$  V and  $P_{D_{max}} = 100$  mW.

#### 6.5 Instrumentation

21. Using the characteristics of Fig. 6.22, determine  $I_D$  at  $V_{GS} = -0.7$  V and  $V_{DS} = 10$  V.
22. Referring to Fig. 6.22, is the locus of pinch-off values defined by the region of  $V_{DS} < |V_P| = 3$  V?
23. Determine  $V_P$  for the characteristics of Fig. 6.22 using  $I_{DSS}$  and  $I_D$  at some value of  $V_{GS}$ . That is, simply substitute into Shockley's equation and solve for  $V_P$ . Compare the result to the assumed value of -3 V from the characteristics.
24. Using  $I_{DSS} = 9$  mA and  $V_P = -3$  V for the characteristics of Fig. 6.22, calculate  $I_D$  at  $V_{GS} = -1$  V using Shockley's equation and compare to the level in Fig. 6.22.
25. a. Calculate the resistance associated with the JFET of Fig. 6.22 for  $V_{GS} = 0$  V from  $I_D = 0$  mA to 4 mA.  
 b. Repeat part (a) for  $V_{GS} = -0.5$  V from  $I_D = 0$  to 3 mA.  
 c. Assigning the label  $r_o$  to the result of part (a) and  $r_d$  to that of part (b), use Eq. (6.1) to determine  $r_d$  and compare to the result of part (b).

#### 6.7 Depletion-Type MOSFET

26. a. Sketch the basic construction of a *p*-channel depletion-type MOSFET.  
 b. Apply the proper drain-to-source voltage and sketch the flow of electrons for  $V_{GS} = 0$  V.
27. In what ways is the construction of a depletion-type MOSFET similar to that of a JFET? In what ways is it different?
28. Explain in your own words why the application of a positive voltage to the gate of an *n*-channel depletion-type MOSFET will result in a drain current exceeding  $I_{DSS}$ .
29. Given a depletion-type MOSFET with  $I_{DSS} = 6$  mA and  $V_P = -3$  V, determine the drain current at  $V_{GS} = -1, 0, 1$ , and 2 V. Compare the difference in current levels between -1 V and 0 V with the difference between 1 V and 2 V. In the positive  $V_{GS}$  region, does the drain current increase at a significantly higher rate than for negative values? Does the  $I_D$  curve become more and more vertical with increasing positive values of  $V_{GS}$ ? Is there a linear or a nonlinear relationship between  $I_D$  and  $V_{GS}$ ? Explain.
30. Sketch the transfer and drain characteristics of an *n*-channel depletion-type MOSFET with  $I_{DSS} = 12$  mA and  $V_P = -8$  V for a range of  $V_{GS} = -V_P$  to  $V_{GS} = 1$  V.
31. Given  $I_D = 14$  mA and  $V_{GS} = 1$  V, determine  $V_P$  if  $I_{DSS} = 9.5$  mA for a depletion-type MOSFET.
32. Given  $I_D = 4$  mA at  $V_{GS} = -2$  V, determine  $I_{DSS}$  if  $V_P = -5$  V.
33. Using an average value of 2.9 mA for the  $I_{DSS}$  of the 2N3797 MOSFET of Fig. 6.31, determine the level of  $V_{GS}$  that will result in a maximum drain current of 20 mA if  $V_P = -5$  V.
34. If the drain current for the 2N3797 MOSFET of Fig. 6.31 is 8 mA, what is the maximum permissible value of  $V_{DS}$  utilizing the maximum power rating?

#### 6.8 Enhancement-Type MOSFET

35. a. What is the significant difference between the construction of an enhancement-type MOSFET and a depletion-type MOSFET?  
 b. Sketch a *p*-channel enhancement-type MOSFET with the proper biasing applied ( $V_{DS} > 0$  V,  $V_{GS} > V_T$ ) and indicate the channel, the direction of electron flow, and the resulting depletion region.  
 c. In your own words, briefly describe the basic operation of an enhancement-type MOSFET.
36. a. Sketch the transfer and drain characteristics of an *n*-channel enhancement-type MOSFET if  $V_T = 3.5$  V and  $k = 0.4 \times 10^{-3}$  A/V<sup>2</sup>.  
 b. Repeat part (a) for the transfer characteristics if  $V_T$  is maintained at 3.5 V but  $k$  is increased by 100% to  $0.8 \times 10^{-3}$  A/V<sup>2</sup>.

37. a. Given  $V_{GS(\text{Th})} = 4 \text{ V}$  and  $I_{D(\text{on})} = 4 \text{ mA}$  at  $V_{GS(\text{on})} = 6 \text{ V}$ , determine  $k$  and write the general expression for  $I_D$  in the format of Eq. (6.15).  
 b. Sketch the transfer characteristics for the device of part (a).  
 c. Determine  $I_D$  for the device of part (a) at  $V_{GS} = 2, 5$ , and  $10 \text{ V}$ .
38. Given the transfer characteristics of Fig. 6.55, determine  $V_T$  and  $k$  and write the general equation for  $I_D$ .

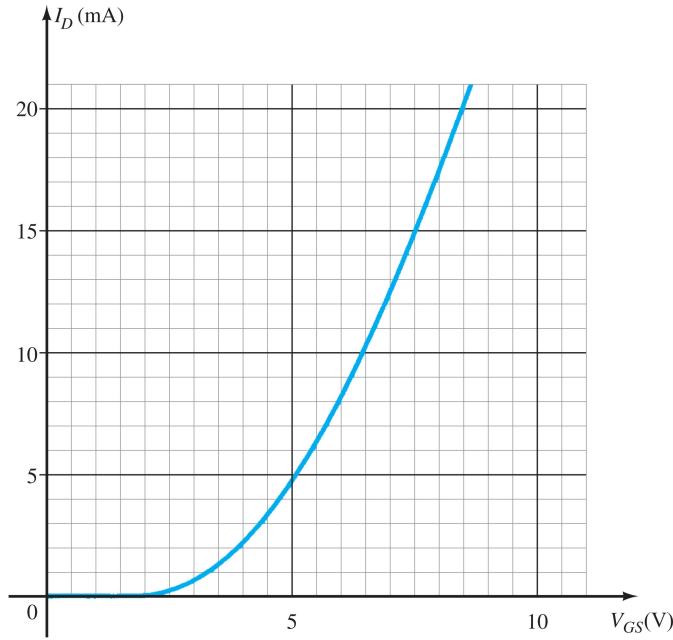


FIG. 6.55

Problem 38.

39. Given  $k = 0.4 \times 10^{-3} \text{ A/V}^2$  and  $I_{D(\text{on})} = 3 \text{ mA}$  with  $V_{GS(\text{on})} = 4 \text{ V}$ , determine  $V_T$ .  
 40. The maximum drain current for the 2N4351 *n*-channel enhancement-type MOSFET is 30 mA. Determine  $V_{GS}$  at this current level if  $k = 0.06 \times 10^{-3} \text{ A/V}^2$  and  $V_T$  is the maximum value.  
 41. Does the current of an enhancement-type MOSFET increase at about the same rate as a depletion-type MOSFET for the conduction region? Carefully review the general format of the equations, and if your mathematics background includes differential calculus, calculate  $dI_D/dV_{GS}$  and compare its magnitude.  
 42. Sketch the transfer characteristics of a *p*-channel enhancement-type MOSFET if  $V_T = -5 \text{ V}$  and  $k = 0.45 \times 10^{-3} \text{ A/V}^2$ .  
 43. Sketch the curve of  $I_D = 0.5 \times 10^{-3}(V_{GS}^2)$  and  $I_D = 0.5 \times 10^{-3}(V_{GS} - 4)^2$  for  $V_{GS}$  from 0 V to 10 V. Does  $V_T = 4 \text{ V}$  have a significant effect on the level of  $I_D$  for this region?

### 6.10 VMOS and UMOS Power MOSFETs

44. a. Describe in your own words why the VMOS FET can withstand a higher current and power rating than devices constructed with standard techniques.  
 b. Why do VMOS FETs have reduced channel resistance levels?  
 c. Why is a positive temperature coefficient desirable?  
 45. What are the relative advantages of the UMOS technology over the VMOS technology?

### 6.11 CMOS

- \*46. a. Describe in your own words the operation of the network of Fig. 6.45 with  $V_i = 0 \text{ V}$ .  
 b. If the “on” MOSFET of Fig. 6.45 (with  $V_i = 0 \text{ V}$ ) has a drain current of 4 mA with  $V_{DS} = 0.1 \text{ V}$ , what is the approximate resistance level of the device? If  $I_D = 0.5 \mu\text{A}$  for the “off” transistor, what is the approximate resistance of the device? Do the resulting resistance levels suggest that the desired output voltage level will result?  
 47. Research CMOS logic at your local or college library, and describe the range of applications and basic advantages of the approach.

by **Edit Model**. An **Edit Model** dialog box will appear in which **Beta** and **V<sub>to</sub>** can be set to **0.222 mA/V<sup>2</sup>** and **-6 V**, respectively. The value of **Beta** is determined using Eq. (6.17) and the parameters of the network as follows:

$$\text{Beta} = \frac{I_{DSS}}{|V_P|^2} = \frac{8 \text{ mA}}{|-6 \text{ V}|^2} = \frac{8 \text{ mA}}{36 \text{ V}^2} = 0.222 \text{ mA/V}^2$$

Once the change is made, be sure to select **Change Part Model** before leaving the dialog box. The **JFET\_N** dialog box will appear again, but an **OK**, and the changes will be made. The labels **IDSS = 8 mA** and **V<sub>p</sub> = -6 V** are added using **Place-Text**. A blinking vertical bar will appear marking the place where the label can be entered. Once entered, it can easily be moved by simply clicking the area and dragging it to the desired position while holding the clicker down.

Using the **Indicator** option on the first vertical toolbar displays the drain and source voltages as shown in Fig. 7.74. In both cases the **VOLTMETER\_V** option was chosen in the **Select a Component** dialog box.

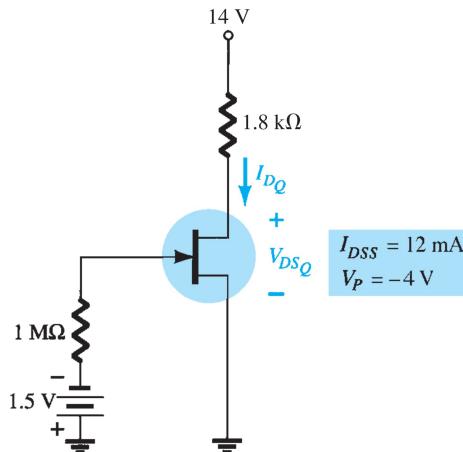
Selecting **Simulate-Run** or moving the switch to the **1** position results in the display of Fig. 7.74. Note that  $V_{GS}$  at  $-2.603 \text{ V}$  is an exact match with the hand-calculated solution of  $-2.6 \text{ V}$ . Although the indicator is connected from source to ground, be aware that this is also the gate-to-source voltage because the voltage drop across the  $1\text{-M}\Omega$  resistor is assumed to be  $0 \text{ V}$ . The level of  $11.405 \text{ V}$  at the drain is very close to the hand-calculated solution of  $11.42 \text{ V}$ —in all, a complete verification of the results of Example 7.2.

## PROBLEMS

\*Note: Asterisks indicate more difficult problems.

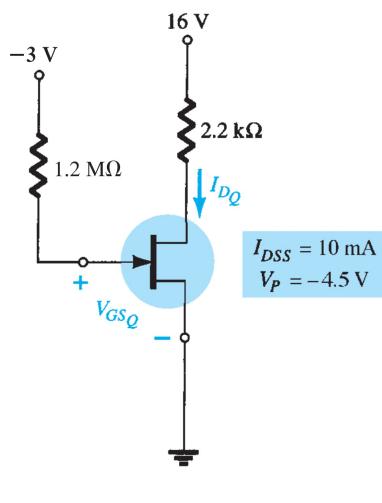
### 7.2 Fixed-Bias Configuration

1. For the fixed-bias configuration of Fig. 7.75:
  - a. Sketch the transfer characteristics of the device.
  - b. Superimpose the network equation on the same graph.
  - c. Determine  $I_{DQ}$  and  $V_{DSQ}$ .
  - d. Using Shockley's equation, solve for  $I_{DQ}$  and then find  $V_{DSQ}$ . Compare with the solutions of part (c).

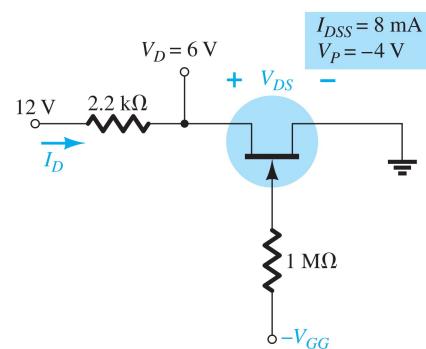


**FIG. 7.75**  
Problems 1 and 37.

2. For the fixed-bias configuration of Fig. 7.76, determine:
  - a.  $I_{DQ}$  and  $V_{GSQ}$  using a purely mathematical approach.
  - b. Repeat part (a) using a graphical approach and compare results.
  - c. Find  $V_{DS}$ ,  $V_D$ ,  $V_G$ , and  $V_S$  using the results of part (a).
3. Given the measured value of  $V_D$  in Fig. 7.77, determine:
  - a.  $I_D$ .
  - b.  $V_{DS}$ .
  - c.  $V_{GG}$ .

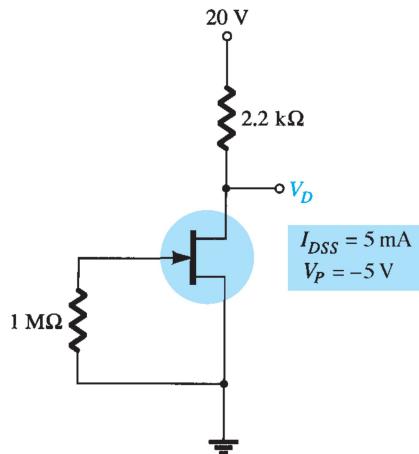


**FIG. 7.76**  
Problem 2.

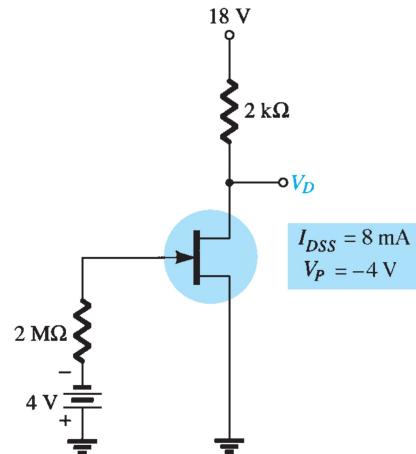


**FIG. 7.77**  
Problem 3.

4. Determine  $V_D$  and  $V_{GS}$  for the fixed-bias configuration of Fig. 7.78.
5. Determine  $V_D$  and  $V_{GS}$  for the fixed-bias configuration of Fig. 7.79.



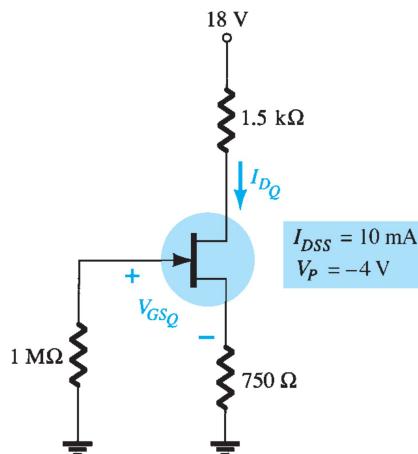
**FIG. 7.78**  
Problem 4.



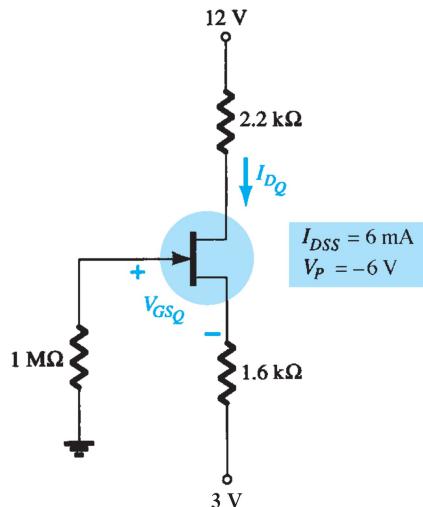
**FIG. 7.79**  
Problem 5.

### 7.3 Self-Bias Configuration

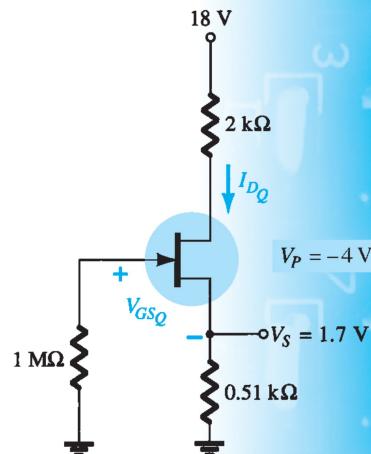
6. For the self-bias configuration of Fig. 7.80:
  - a. Sketch the transfer curve for the device.
  - b. Superimpose the network equation on the same graph.
  - c. Determine  $I_{DQ}$  and  $V_{GSQ}$ .
  - d. Calculate  $V_{DS}$ ,  $V_D$ ,  $V_G$ , and  $V_S$ .
- \*7. Determine  $I_{DQ}$  for the network of Fig. 7.80 using a purely mathematical approach. That is, establish a quadratic equation for  $I_D$  and choose the solution compatible with the network characteristics. Compare to the solution obtained in Problem 6.
8. For the network of Fig. 7.81, determine:
  - a.  $V_{GSQ}$  and  $I_{DQ}$ .
  - b.  $V_{DS}$ ,  $V_D$ ,  $V_G$ , and  $V_S$ .
9. Given the measurement  $V_S = 1.7 \text{ V}$  for the network of Fig. 7.82, determine:
  - a.  $I_{DQ}$ .
  - b.  $V_{GSQ}$ .
  - c.  $I_{DSS}$ .
  - d.  $V_D$ .
  - e.  $V_{DS}$ .



**FIG. 7.80**  
Problems 6, 7, and 38.



**FIG. 7.81**  
Problem 8.

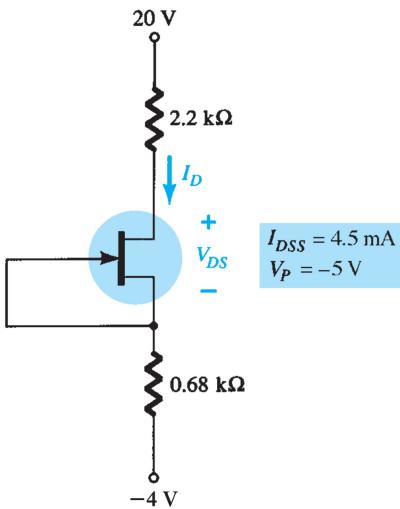


**FIG. 7.82**  
Problem 9.

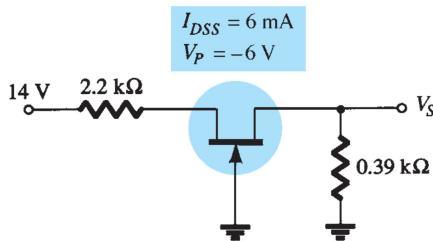
- \*10. For the network of Fig. 7.83, determine:

- $I_D$ .
- $V_{DS}$ .
- $V_D$ .
- $V_S$ .

- \*11. Find  $V_S$  for the network of Fig. 7.84.



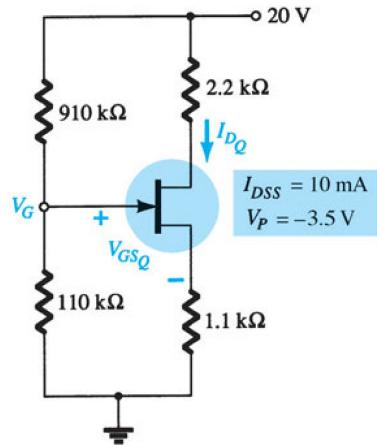
**FIG. 7.83**  
Problem 10.



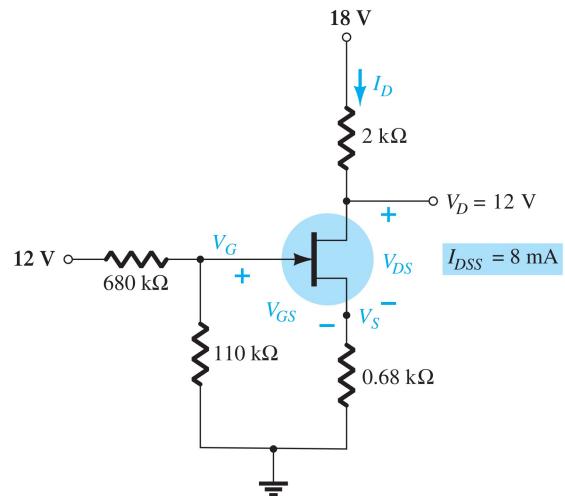
**FIG. 7.84**  
Problem 11.

#### 7.4 Voltage-Divider Biasing

12. For the network of Fig. 7.85, determine:
- $V_G$ .
  - $I_D$  and  $V_{GSQ}$ .
  - $V_D$  and  $V_S$ .
  - $V_{DSQ}$ .
13. a. Repeat Problem 12 with  $R_S = 0.51 \text{ k}\Omega$  (about 50% of the value of that of Problem 12). What is the effect of a smaller  $R_S$  on  $I_{DQ}$  and  $V_{GSQ}$ ?  
b. What is the minimum possible value of  $R_S$  for the network of Fig. 7.85?
14. For the network of Fig. 7.86,  $V_D = 12 \text{ V}$ . Determine:
- $I_D$ .
  - $V_S$  and  $V_{DS}$ .
  - $V_G$  and  $V_{GS}$ .
  - $V_P$ .

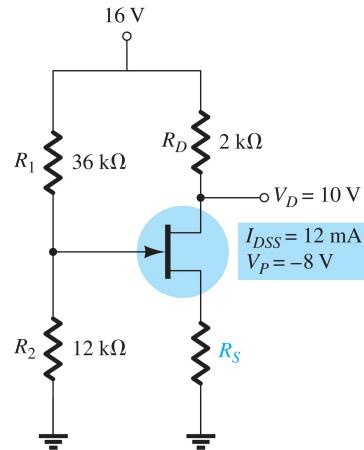


**FIG. 7.85**  
Problems 12 and 13.



**FIG. 7.86**  
Problem 14.

15. Determine the value of  $R_S$  for the network of Fig. 7.87 to establish  $V_D = 10$  V.



**FIG. 7.87**  
Problem 15.

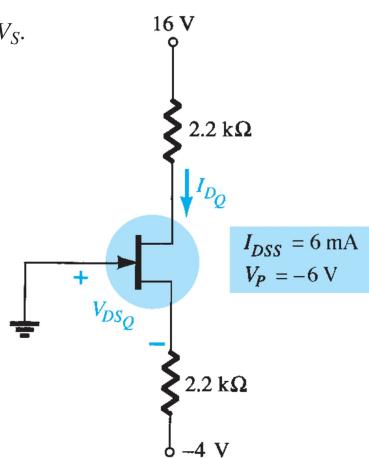
### 7.5 Common-Gate Configuration

- \*16. For the network of Fig. 7.88, determine:

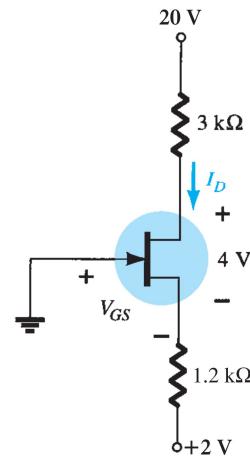
- $I_{DQ}$  and  $V_{GSQ}$ .
- $V_{DS}$  and  $V_S$ .

- \*17. Given  $V_{DS} = 4$  V for the network of Fig. 7.89, determine:

- $I_D$ .
- $V_D$  and  $V_S$ .
- $V_{GS}$ .



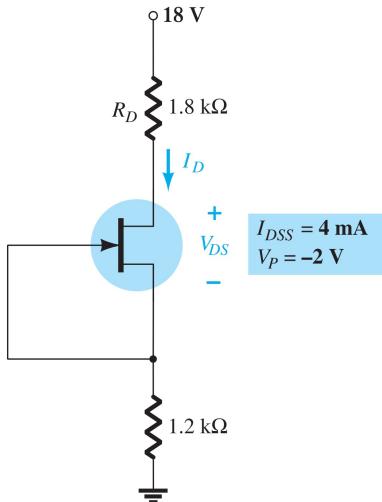
**FIG. 7.88**  
Problems 16 and 39.



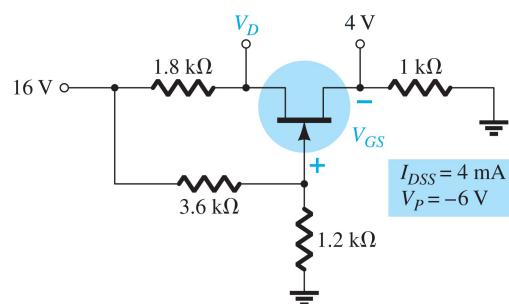
**FIG. 7.89**  
Problem 17.

**7.6 Special Case:  $V_{GSQ} = 0 \text{ V}$** 

18. For the network of Fig. 7.90.
- Find  $I_{DQ}$ .
  - Determine  $V_{DQ}$  and  $V_{DSQ}$ .
  - Find the power supplied by the source and dissipated by the device.
19. Determine  $V_D$  and  $V_{GS}$  for the network of Fig. 7.91 using the provided information.

**FIG. 7.90**

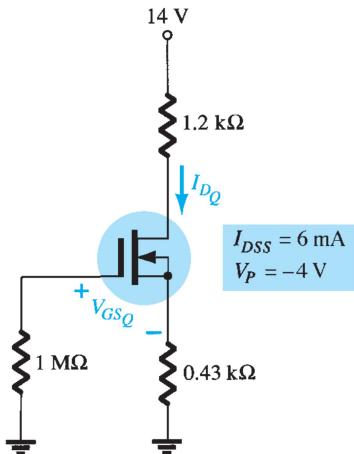
Problem 18.

**FIG. 7.91**

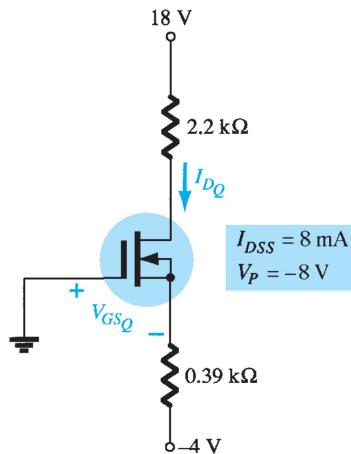
Problem 19.

**7.7 Depletion-Type MOSFETs**

20. For the self-bias configuration of Fig. 7.92, determine:
- $I_{DQ}$  and  $V_{GSQ}$ .
  - $V_{DS}$  and  $V_D$ .
- \*21. For the network of Fig. 7.93, determine:
- $I_{DQ}$  and  $V_{GSQ}$ .
  - $V_{DS}$  and  $V_S$ .

**FIG. 7.92**

Problem 20.

**FIG. 7.93**

Problem 21.

**7.8 Enhancement-Type MOSFETs**

22. For the network of Fig. 7.94, determine:
- $I_{DQ}$ .
  - $V_{GSQ}$  and  $V_{DSQ}$ .
  - $V_D$  and  $V_S$ .
  - $V_{DS}$ .
23. For the voltage-divider configuration of Fig. 7.95, determine:
- $I_{DQ}$  and  $V_{GSQ}$ .
  - $V_D$  and  $V_S$ .

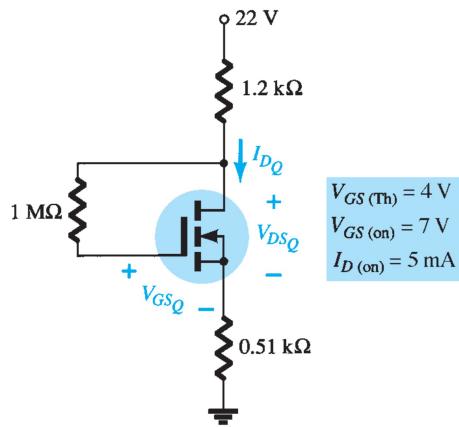


FIG. 7.94

Problem 22.

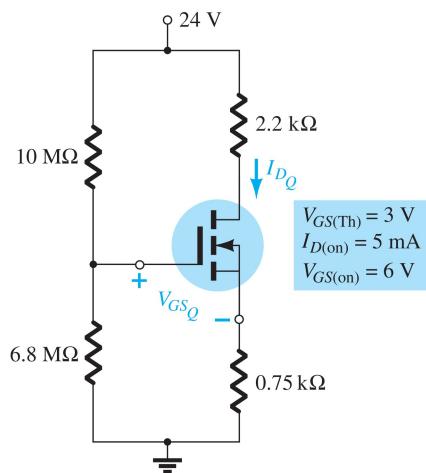


FIG. 7.95

Problem 23.

### 7.10 Combination Networks

\*24. For the network of Fig. 7.96, determine:

- a.  $V_G$ .
- b.  $V_{GSQ}$  and  $I_{DQ}$ .
- c.  $I_E$ .
- d.  $I_B$ .
- e.  $V_D$ .
- f.  $V_C$ .

\*25. For the combination network of Fig. 7.97, determine:

- a.  $V_B$  and  $V_G$ .
- b.  $V_E$ .
- c.  $I_E$ ,  $I_C$ , and  $I_D$ .
- d.  $I_B$ .
- e.  $V_C$ ,  $V_S$ , and  $V_D$ .
- f.  $V_{CE}$ .
- g.  $V_{DS}$ .

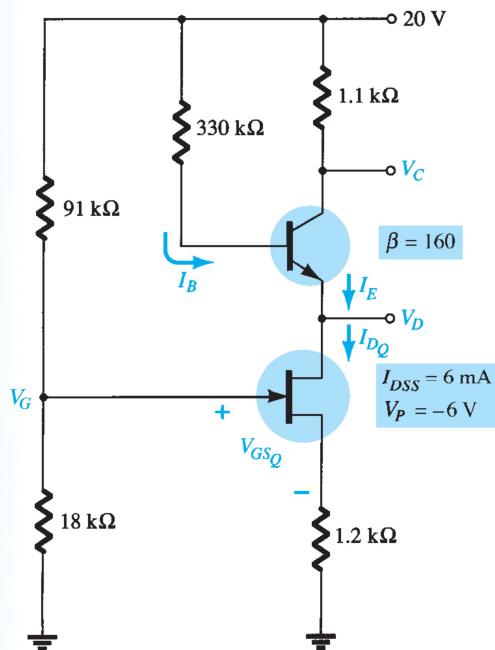


FIG. 7.96

Problem 24.

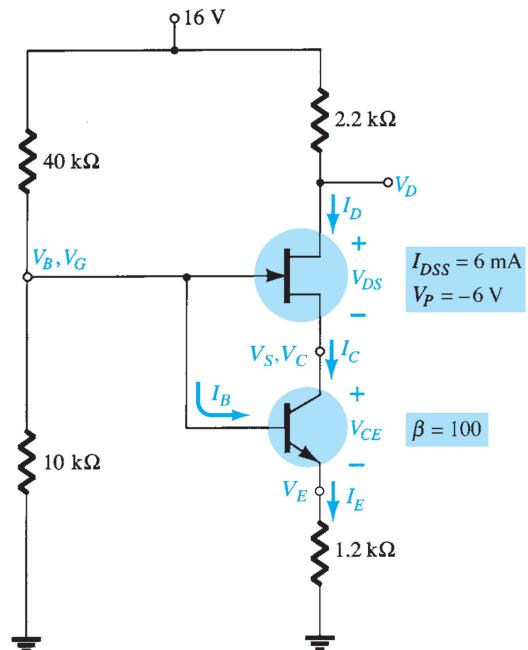


FIG. 7.97

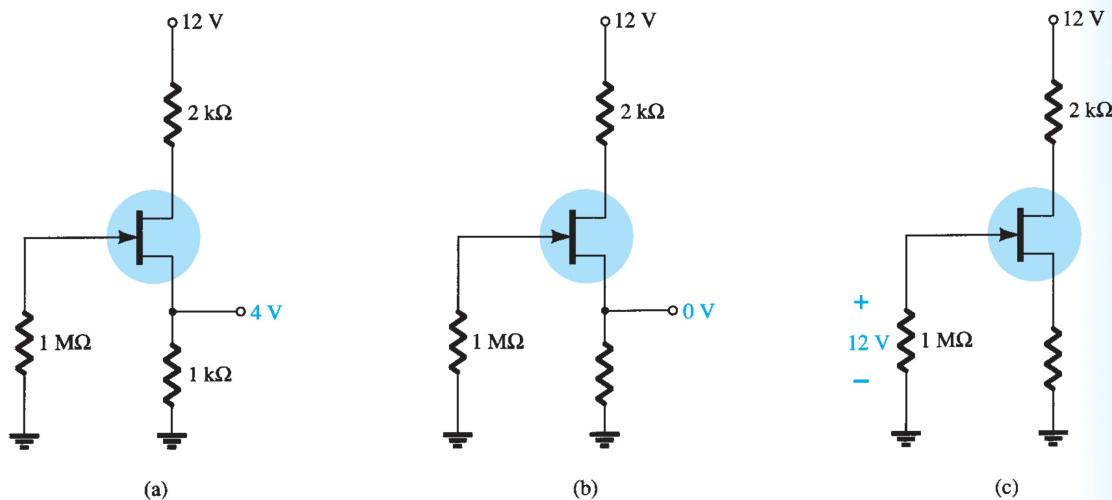
Problem 25.

7.11 Design

- \*26. Design a self-bias network using a JFET transistor with  $I_{DSS} = 8$  mA and  $V_P = -6$  V to have a  $Q$ -point at  $I_{D_Q} = 4$  mA using a supply of 14 V. Assume that  $R_D = 3R_S$  and use standard values.
  - \*27. Design a voltage-divider bias network using a depletion-type MOSFET with  $I_{DSS} = 10$  mA and  $V_P = -4$  V to have a  $Q$ -point at  $I_{D_Q} = 2.5$  mA using a supply of 24 V. In addition, set  $V_G = 4$  V and use  $R_D = 2.5R_S$  with  $R_1 = 22$  M $\Omega$ . Use standard values.
  - 28. Design a network such as appears in Fig. 7.39 using an enhancement-type MOSFET with  $V_{GS(\text{Th})} = 4$  V and  $k = 0.5 \times 10^{-3}$  A/V $^2$  to have a  $Q$ -point of  $I_{D_Q} = 6$  mA. Use a supply of 16 V and standard values.

## 7.12 Troubleshooting

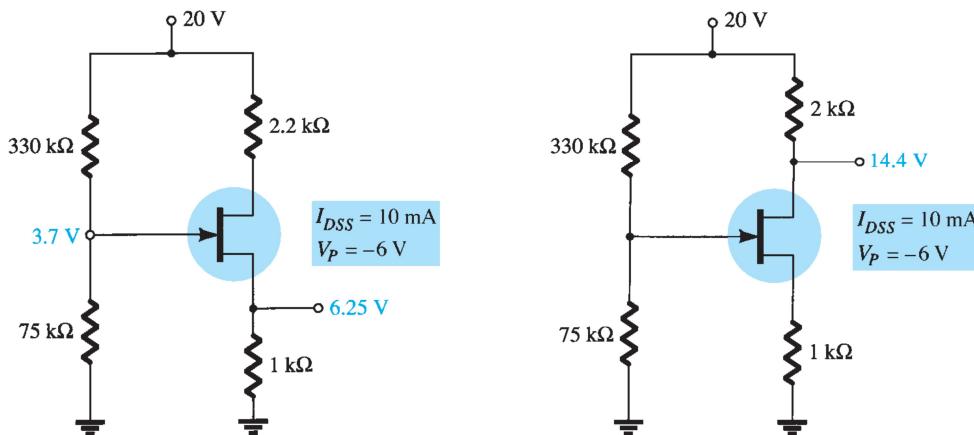
- \*29. What do the readings for each configuration of Fig. 7.98 suggest about the operation of the network?



**FIG. 7.98**  
*Problem 29.*

- \*30. Although the readings of Fig. 7.99 initially suggest that the network is behaving properly, determine a possible cause for the undesirable state of the network.

\*31. The network of Fig. 7.100 is not operating properly. What is the specific cause for its failure?



**FIG. 7.99**  
*Problem 30.*

**FIG. 7.100**  
*Problem 31.*

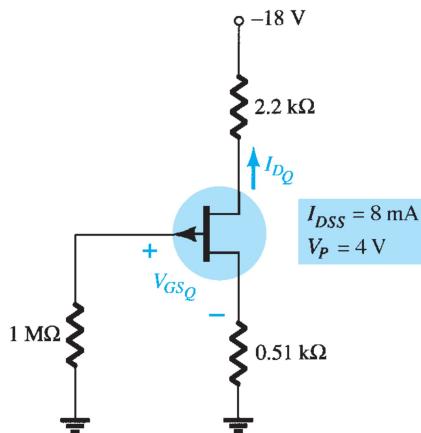
**7.13 p-Channel FETs**

32. For the network of Fig. 7.101, determine:

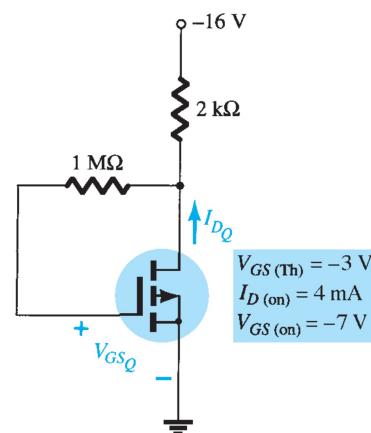
- $I_{DQ}$  and  $V_{GSQ}$ .
- $V_{DS}$ .
- $V_D$ .

33. For the network of Fig. 7.102, determine:

- $I_{DQ}$  and  $V_{GSQ}$ .
- $V_{DS}$ .
- $V_D$ .

**FIG. 7.101**

Problem 32.

**FIG. 7.102**

Problem 33.

**7.14 Universal JFET Bias Curve**

- Repeat Problem 1 using the universal JFET bias curve.
- Repeat Problem 6 using the universal JFET bias curve.
- Repeat Problem 12 using the universal JFET bias curve.
- Repeat Problem 16 using the universal JFET bias curve.

**7.15 Computer Analysis**

- Perform a PSpice Windows analysis of the network of Problem 1.
- Perform a PSpice Windows analysis of the network of Problem 6.
- Perform a Multisim analysis of the network of Problem 16.
- Perform a Multisim analysis of the network of Problem 33.