

Title:

Performance analysis of a common source (CS) E-MOSFET amplifier circuit by varying the loads and justification of the analysis with respect to simulated and experimental data (followed by the given constraints).

Objective:

Design a common source E-MOSFET amplifier circuit and analyze the gain with varying the loads. Finally, a complete analysis will be expected with respect to experimental and simulated data.

Literature review:

MOSFET devices belong to the group of Insulated Gate Field Effect Transistor (IGFETs). MOSFETs like all other IGFETs has three terminals, which are called Gate (G), Source (S), and Drain (D). In PMOS, the body terminal is held at the most positive voltage in the circuit and in NMOS, it is held at the most negative voltage in the circuit.

There are four types of MOSFETs: enhancement n-type MOSFET, enhancement p-type MOSFET, depletion n-type MOSFET, and depletion p-type MOSFET. If the channel between the drain and the source is an induced channel, the transistor is called enhancement transistor. Throughout the handout, we will concentrate on analyzing the enhancement type MOSFET. If we put the drain and source on ground potential and apply a positive voltage to the gate, the free holes (positive charges) are repelled from the region of the substrate under the gate (channel region) due to the positive voltage applied to the gate. The holes are pushed away downwards into the substrate leaving behind a depletion region. At the same time, the positive gate voltage attracts electrons into the channel region. When the concentration of electrons near the surface of the substrate under the gate is higher than the concentration of holes, an n region is created, connecting the source and the drain regions. In the case of an enhancement type NMOS transistor the threshold voltage is positive, whereas an enhancement type PMOS transistor has a negative threshold voltage. So, in order for the current to flow from drain to source, the condition that should be satisfied is $V_G > V_{th}$, where V_G is the gate voltage and V_{th} is the minimum voltage required to form a channel between drain and source so that carriers can flow through the channel. By changing the applied gate voltage, we can modulate the conductance of the channel.

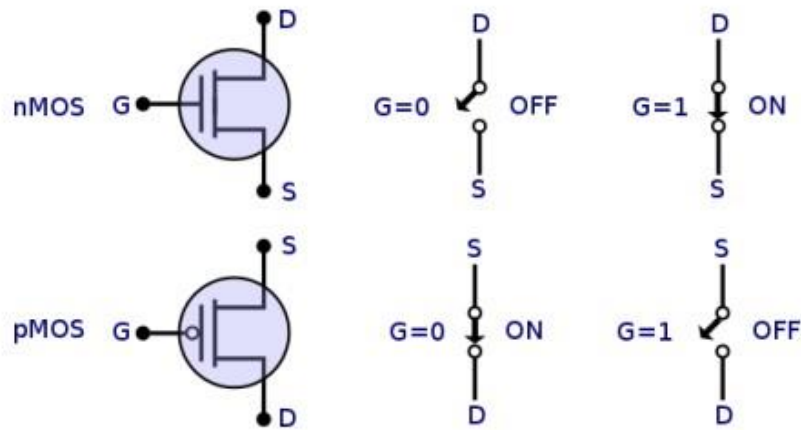


Figure: Symbols for enhancement NMOS and PMOS transistors

Apparatus:

Apparatus	Quantity
MOSFET	1
Trainer board	1
Resistors	8
Oscilloscope	1
Multimeter	1
Signal Generator	1
Capacitors	1
DC Power Supply	1

Experimental data table:

Table 1

V_{DD}	V_D	V_{DD}-V_D	I_D = (V_{DD}-V_D) / R_D	V_{DS}
10 V	95.7 mV	9.91 V	6.67 mA	9.98 V

Table 2

Load resistor	Input voltage	Output voltage	Gain
1k	400 mV	3.9 mV	00.00975
4.7k	420 mV	10.1 mV	0.024
10k	420 mV	9.4 mV	0.022
100k	420 mV	13.1 mV	0.031

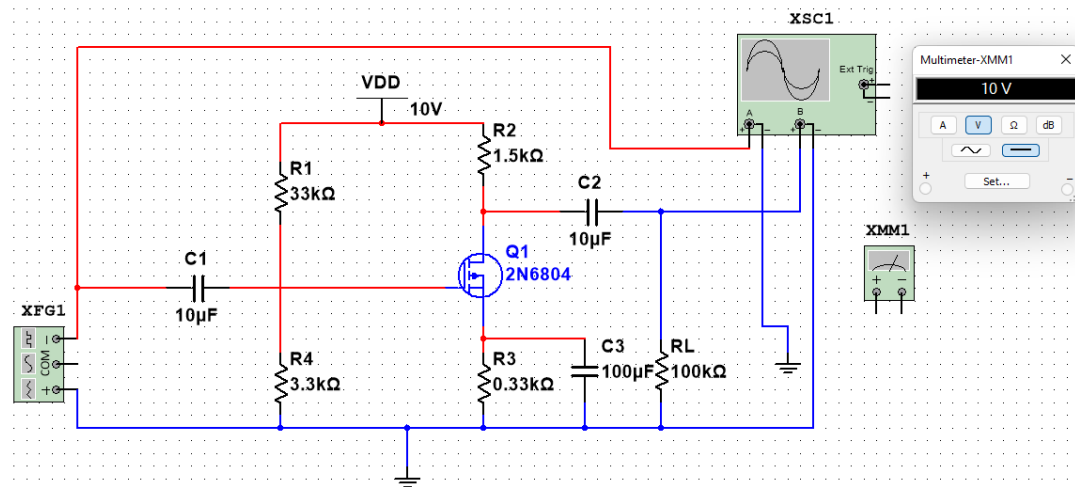
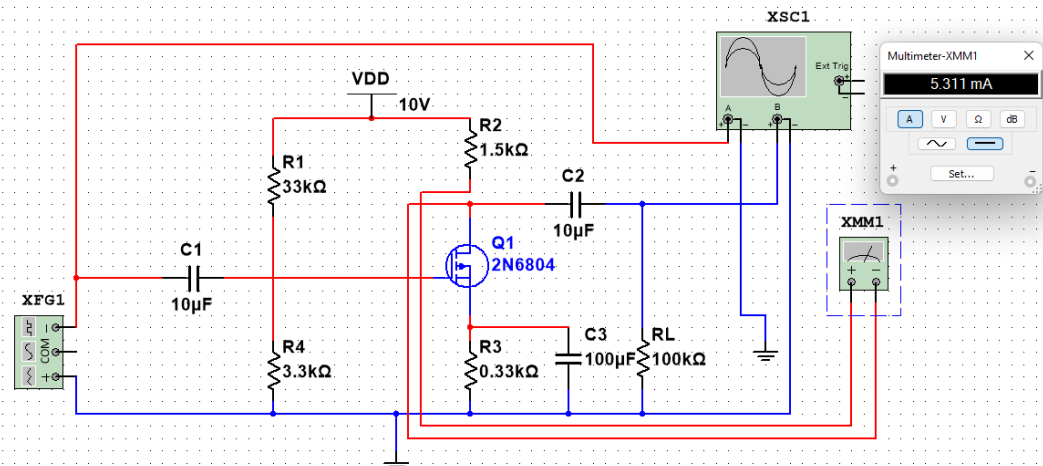
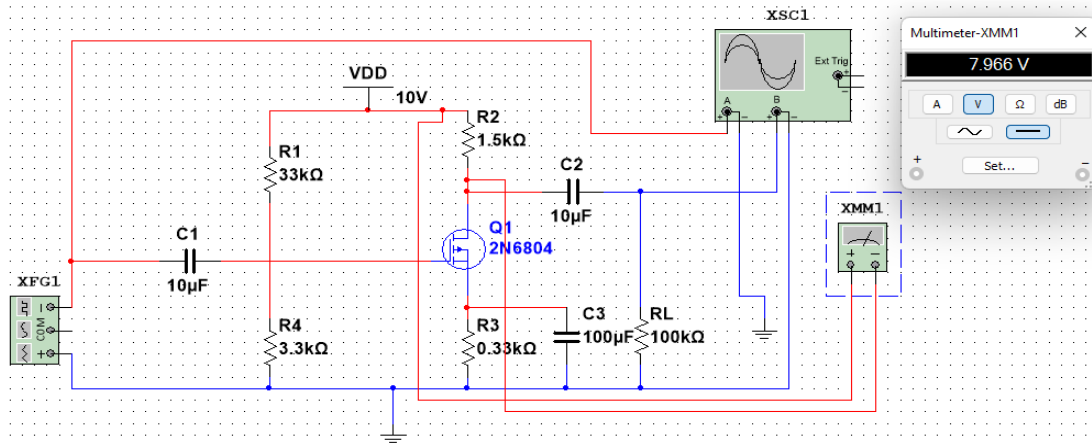
Simulated data table:

Table 3

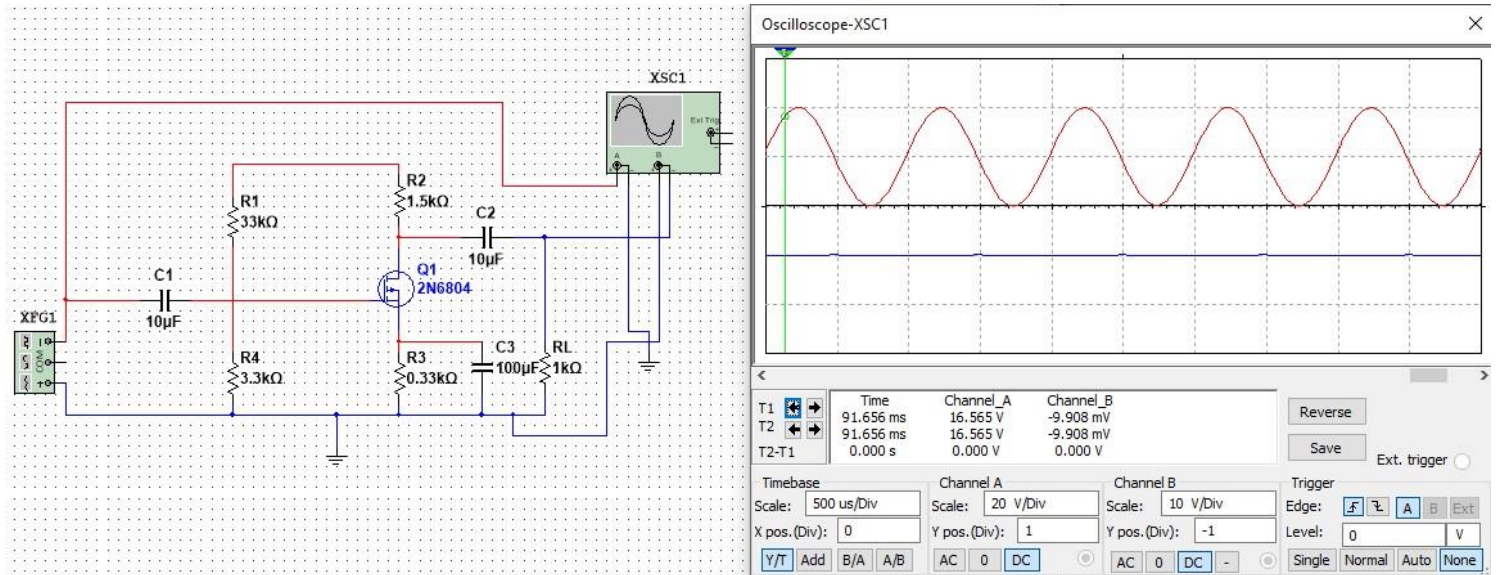
V_{DD}	V_D	V_{DD}-V_D	I_D = (V_{DD}-V_D) / R_D	V_{DS}
10V	7.966 V	2.004	5.311 mA	10 V

Table 4

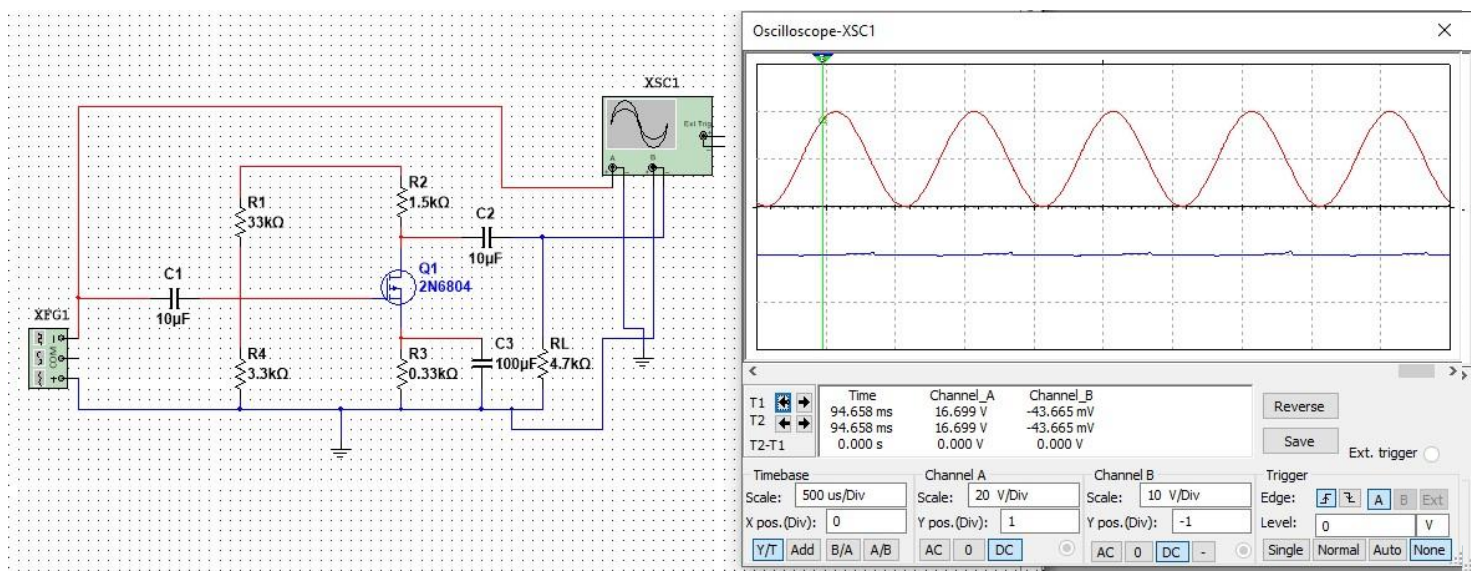
Load resistor	Input voltage	Output voltage	Gain
1k	16.6V	9.91mV	0.597
4.7k	16.7V	43.7mV	2.62
10k	16.03V	95.2mV	5.94
100k	16.2V	258.9mV	15.98



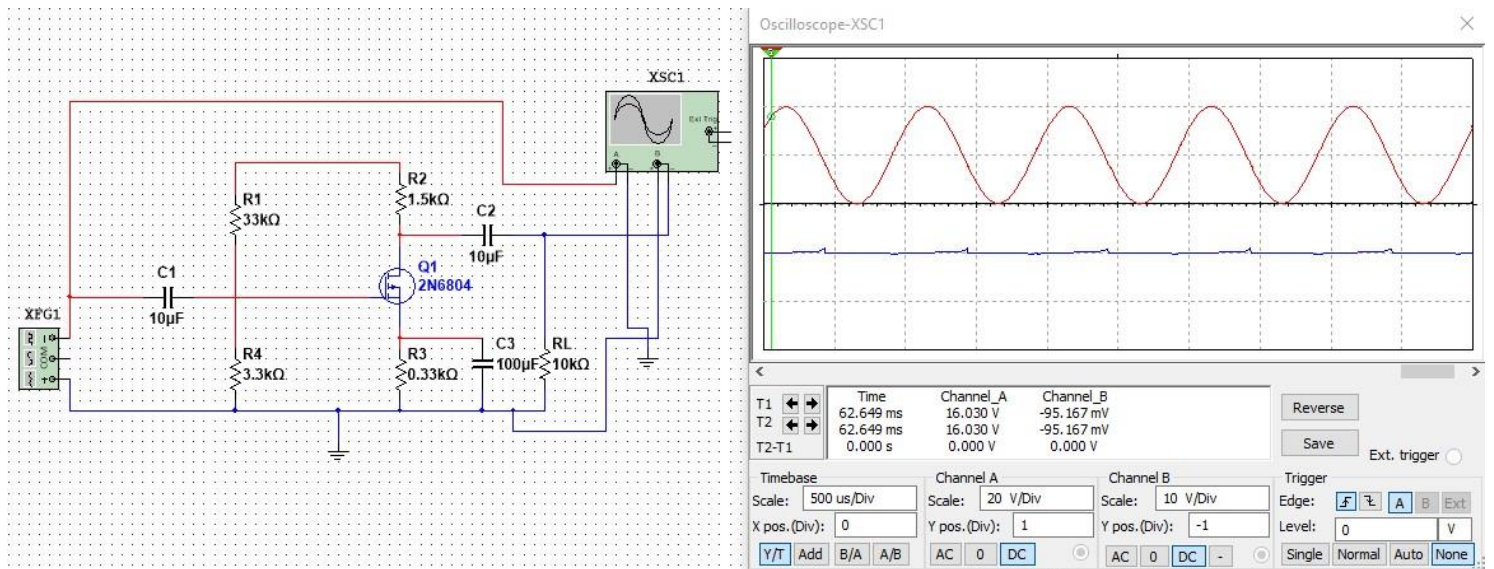
For load resistance 1 kilo ohm:



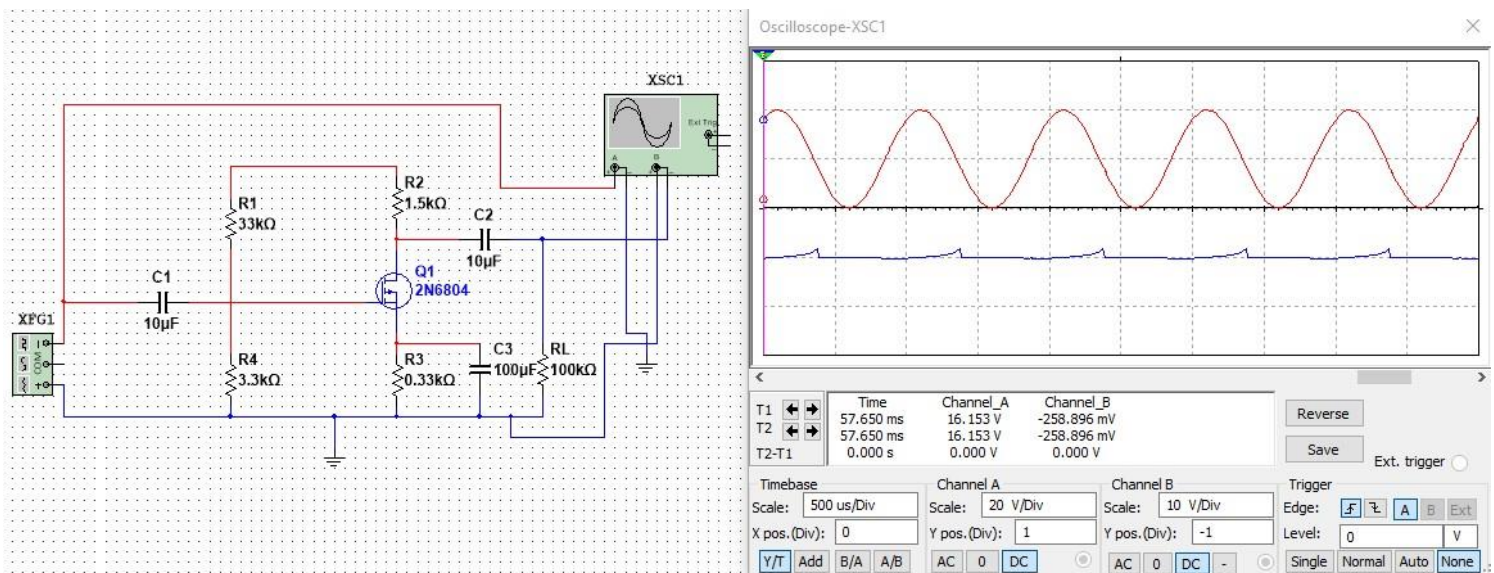
For load resistance 4.7 kilo ohm:



For load resistance 10 kilo ohm:



For load resistance 100 kilo ohm:



Practical images:

