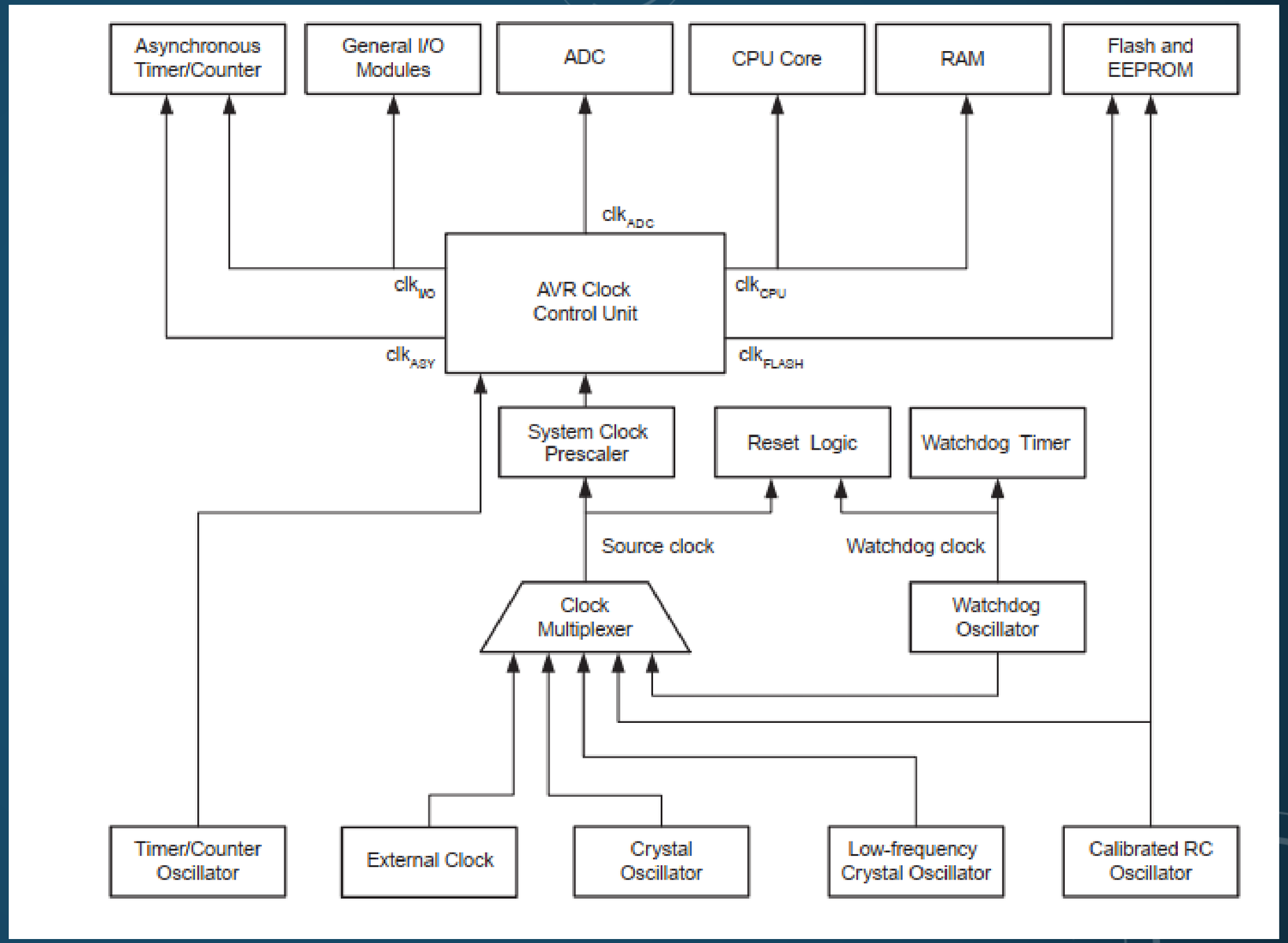
SYSTEM CLOCK OPTIONS

INTRODUCTION:

- The block diagram represents the principal clock systems in the AVR and their distribution. All of the clocks need not be active at a given time. In order to reduce power consumption, the clocks to modules not being used can be halted by using different sleep modes.



CLOCK SOURCES:

The device has the following clock source options, selectable by **Flash Fuse bits** as shown. The clock from the selected source is input to the AVR clock generator, and routed to the appropriate modules

Device Clocking Option	CKSEL3..0
Low Power Crystal Oscillator	1111 - 1000
Full Swing Crystal Oscillator	0111 - 0110
Low Frequency Crystal Oscillator	0101 - 0100
Internal 128 kHz RC Oscillator	0011
Calibrated Internal RC Oscillator	0010
External Clock	0000
Reserved	0001

Note: 1. For all fuses “1” means unprogrammed while “0” means programmed.

DEFAULT CLOCK SOURCE:

The device is shipped with internal RC oscillator at 8.0MHz and with the fuse CKDIV8 programmed, resulting in 1.0MHz system clock. The startup time is set to maximum and time-out period enabled. (CKSEL = "0010", SUT = "10", CKDIV8 = "0"). The default setting ensures that all users can make their desired clock source setting using any available programming interface.

LOW POWER CRYSTAL OSCILLATOR :

Pins XTAL1 and XTAL2 are input and output, respectively, of an inverting amplifier which can be configured for use as an On-chip Oscillator

Frequency Range[1] (MHz)	Recommended Range for Capacitors C1 and C2 (pF)	CKSEL3..1
0.4 - 0.9	–	100[2]
0.9 - 3.0	12 - 22	101
3.0 - 8.0	12 - 22	110
8.0 - 16.0	12 - 22	111

FULL SWING CRYSTAL OSCILLATOR :

This Crystal Oscillator is a full swing oscillator, with rail-to-rail swing on the XTAL2 output. This is useful for driving other clock inputs and in noisy environments.

Frequency Range (MHz)	Recommended Range for Capacitors C1 and C2 (pF)	CKSEL3..1
0.4 - 20	12 - 22	011

LOW FREQUENCY CRYSTAL OSCILLATOR :

The Low-frequency Crystal Oscillator is optimized for use with a 32.768 kHz watch crystal. When selecting crystals, load capacitance and crystal's Equivalent Series Resistance, ESR must be taken into consideration. Both values **are specified by the crystal vendor**.

Crystal CL (pF)	Max ESR [kΩ](1)
6.5	75
9.0	65
12.5	30

Note: 1. Maximum ESR is typical value based on characterization

LOW FREQUENCY CRYSTAL OSCILLATOR :

The Low-frequency Crystal Oscillator provides an **internal load capacitance of typical 6 pF** at each TOSC pin. The **external capacitance (C)** needed at each TOSC pin can be calculated by using:

C= 2*CL-C_S where CL is the load capacitance for a **32.768 kHz crystal** specified by the crystal vendor and C_S is the total stray capacitance for one TOSC pin.

Crystals specifying load capacitance (CL) higher than 6 pF, require external capacitors applied. The Low-frequency Crystal Oscillator must be selected by setting the CKSEL Fuses to “0110” or “0111”. Start-up times are determined by the SUT Fuses.

CKSEL3..0	Start-up Time from Power-down and Power-save	Recommended Usage
0100[1]	1K CK	
0101	32K CK	Stable frequency at start-up

CALIBRATED INTERNAL RC OSCILLATOR :

By default, the Internal RC Oscillator provides an approximate **8.0 MHz clock**. Though voltage and temperature dependent, this clock can be very accurately calibrated by the user. The device is **shipped with the CKDIV8 Fuse programmed. This clock may be selected as the system clock by programming the CKSEL Fuses** .

Frequency Range[1] (MHz)	CKSEL3..0
7.3 - 8.1	0010

Notes:
1. This is the recommended CKSEL settings for the different frequency ranges.
2. If 8 MHz frequency exceeds the specification of the device (depends on V_{CC}), the CKDIV8 Fuse can be programmed in order to divide the internal frequency by 8.

When this Oscillator is selected, start-up times are determined by the SUT Fuses as shown in

If selected, it will operate with no external components. During reset, hardware loads the pre-programmed calibration value into the OSCCAL Register and thereby automatically calibrates the RC Oscillator.

128 KHZ INTERNAL OSCILLATOR :

The 128 kHz internal Oscillator is a low power Oscillator providing a clock of 128 kHz. The frequency is nominal at 3V and 25°C. This clock may be select as the system clock by programming the CKSEL Fuses to “11” .

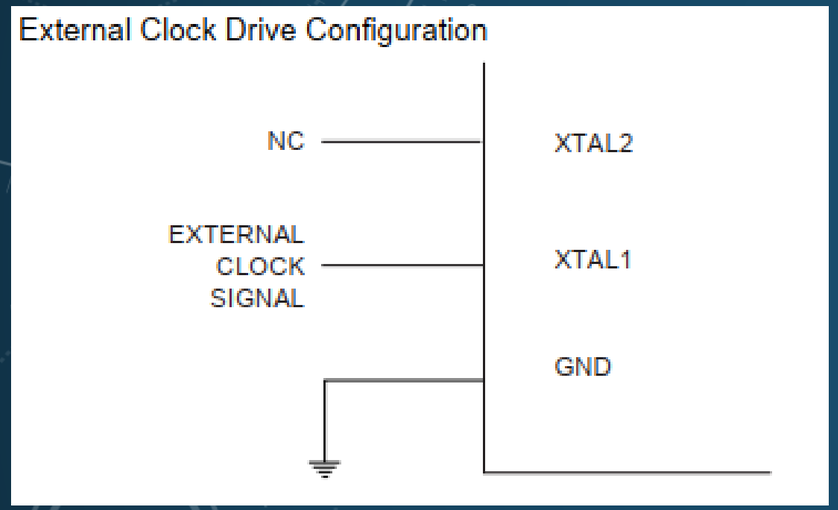
Nominal Frequency(1)	CKSEL3..0
128 kHz	0011

Note: 1. Note that the 128 kHz oscillator is a very low power clock source, and is not designed for a high accuracy.

When this clock source is selected, start-up times are determined by the SUT Fuses as shown in

EXTERNAL CLOCK:

To drive the device from an external clock source, XTAL1 should be driven as shown



To run the device on an external clock, the CKSEL Fuses must be programmed to “0000”

Frequency	CKSEL3..0
0 - 20 MHz	0000

SYSTEM CLOCK PRESCALAR:

- The ATmega48P/88P/168P/328P has a system clock prescaler, and the system clock can be divided by setting the ”CLKPR – Clock Prescale Register”.
- This feature can be used to **decrease the system clock frequency and the power consumption** when the requirement for processing power is low. This can be used with all clock source options, and it will affect the clock frequency of the CPU and all synchronous peripherals.

REGISTER DESCRIPTION:

- CLKPR-Clock Pre-scale Register

Bit	7	6	5	4	3	2	1	0	
(0x61)	CLKPCE	–	–	–	CLKPS3	CLKPS2	CLKPS1	CLKPS0	CLKPR
Read/Write	R/W	R	R	R	R/W	R/W	R/W	R/W	
Initial Value	0	0	0	0	See Bit Description				

- Bit 7 – CLKPCE: Clock Prescaler Change Enable

The CLKPCE bit must be **written to logic one to enable change** of the CLKPS bits. The CLKPCE bit is only updated when the other bits in CLKPR are simultaneously written to zero. CLKPCE is **cleared by hardware four cycles after it is written or when CLKPS bits** are written. Rewriting the CLKPCE bit within this time-out period does neither extend the time-out period, nor clear the CLKPCE bit.

REGISTER DESCRIPTION:

- CLKPR-Clock Prescale Register

Bit	7	6	5	4	3	2	1	0	
(0x61)	CLKPCE	–	–	–	CLKPS3	CLKPS2	CLKPS1	CLKPS0	CLKPR
Read/Write	R/W	R	R	R	R/W	R/W	R/W	R/W	
Initial Value	0	0	0	0	See Bit Description				

- Bits 3..0 – CLKPS3..0: Clock Prescaler Select Bits 3 - 0

These bits define the **division factor between** the selected clock source and the internal system clock. These bits can be written run-time to vary the clock frequency to suit the application requirements. As the divider divides the master clock input to the MCU, the speed of all **synchronous peripherals is reduced** when a division factor is used.

REGISTER DESCRIPTION: CLOCK PRESCALER SELECT

CLKPS3	CLKPS2	CLKPS1	CLKPS0	Clock Division Factor
0	0	0	0	1
0	0	0	1	2
0	0	1	0	4
0	0	1	1	8
0	1	0	0	16
0	1	0	1	32
0	1	1	0	64
0	1	1	1	128
1	0	0	0	256
1	0	0	1	Reserved
1	0	1	0	Reserved
1	0	1	1	Reserved
1	1	0	0	Reserved
1	1	0	1	Reserved
1	1	1	0	Reserved
1	1	1	1	Reserved

POWER MANAGEMENT &SLEEP MODES:

Table 7-1. Active Clock Domains and Wake-up Sources in the Different Sleep Modes.

	Active Clock Domains					Oscillators		Wake-up Sources							
Sleep Mode	clk_{CPU}	clk_{FLASH}	clk_{IO}	clk_{ADC}	clk_{ASY}	Main Clock Source Enabled	Timer Oscillator Enabled	INT1, INT0 and Pin Change	TWI Address Match	Timer2	SPMEEPROM Ready	ADC	WDT	Other/O	Software BOD Disable
Idle			X	X	X	X	X(2)	X	X	X	X	X	X	X	
ADC Noise Reduction				X	X	X	X(2)	X(3)	X	X(2)	X	X	X		
Power-down								X(3)	X				X		X
Power-save					X		X(2)	X(3)	X	X			X		X
Standby(1)						X		X(3)	X				X		X
Extended Standby					X(2)	X	X(2)	X(3)	X	X			X		X

Notes: 1. Only recommended with external crystal or resonator selected as clock source.
2. If Timer/Counter2 is running in asynchronous mode.
3. For INT1 and INT0, only level interrupt.

Sleep modes enable the application to shut down unused modules in the MCU, thereby saving power. The AVR provides various sleep modes allowing the user to tailor the power consumption to the application's requirements.

REGISTER DESCRIPTION:

SMCR – Sleep Mode Control Register
The Sleep Mode Control Register contains control bits for power management.

Bit	7	6	5	4	3	2	1	0	
0x33 (0x53)	–	–	–	–	SM2	SM1	SM0	SE	SMCR
Read/Write	R	R	R	R	R/W	R/W	R/W	R/W	
Initial Value	0	0	0	0	0	0	0	0	

Table 7-2. Sleep Mode Select

SM2	SM1	SM0	Sleep Mode
0	0	0	Idle
0	0	1	ADC Noise Reduction
0	1	0	Power-down
0	1	1	Power-save
1	0	0	Reserved
1	0	1	Reserved
1	1	0	Standby(1)
1	1	1	External Standby(1)

Note: 1. Standby mode is only recommended for use with external crystals or resonators.

PRR-POWER REDUCTION REGISTER:

Bit	7	6	5	4	3	2	1	0	
(0x64)	PRTWI	PRTIM2	PRTIM0	–	PRTIM1	PRSPI	PRUSART0	PRADC	PRR
Read/Write	R/W	R/W	R/W	R	R/W	R/W	R/W	R/W	
Initial Value	0	0	0	0	0	0	0	0	

- **Bit 7 - PRTWI: Power Reduction TWI**
- **Bit 6 - PRTIM2: Power Reduction Timer/Counter2**
- **Bit 5 - PRTIM0: Power Reduction Timer/Counter0**
- **Bit 4 - Res: Reserved bit**
- **Bit 3 - PRTIM1: Power Reduction Timer/Counter1**
- **Bit 2 - PRSPI: Power Reduction Serial Peripheral Interface**
- **Bit 1 - PRUSART0: Power Reduction USART0Bit 0 - PRADC: Power Reduction ADC**

THANKS FOR ATTENDING….