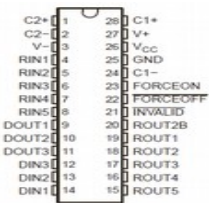
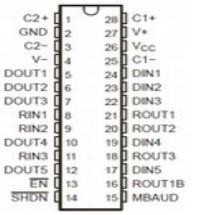
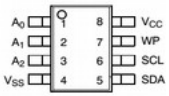
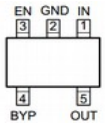
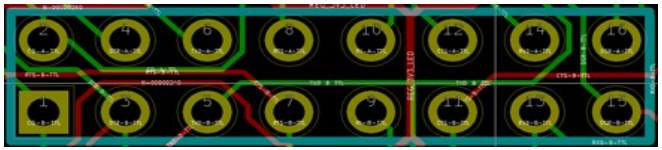
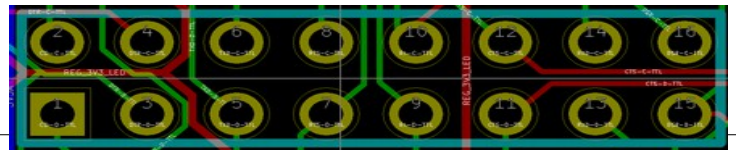
RS-232 Front End Board (By Benjamin Vernoux bvernoux@gmail.com)

RS-232 Front-End Module for Daisho Mother Board		
Functionality	**Detail**	**Pin configuration (TSSOP)**
RS-232 Transceiver Data Terminal Equipment (DTE)	Texas Instrument: 2 x TRSF3243 (DTE) Package: 28-TSSOP Features: 3 OUT(EIA-232) & 5 IN(EIA-232) -> 3 IN(CMOS), 5 OUT(CMOS) Operates: 3V to 5,5V, Up to 1 Mbit/s http://www.ti.com/lit/ds/symlink/trsf3243.pdf **Price: 2.87 USD/1 DigiKey** http://www.digikey.com/product-detail/en/TRSF3243CPWR/296-25102-1-ND/2136639	
RS-232 Transceiver Data Communications Equipment (DCE)	Texas Instrument: 2 x TRS3237E (DCE) Package: 28-TSSOP Features: 5 OUT(EIA-232) & 3 IN(EIA-232) -> 5 IN(CMOS), 3 OUT(CMOS) Operates: 3V to 5,5V, Up to 1 Mbit/s TIA/EIA-232-F ITU v.28 Standards => http://www.ti.com/lit/ds/symlink/trs3237e.pdf **Price: 2.71 USD / 1 DigiKey** http://www.digikey.com/product-detail/en/TRS3237ECPWR/296-25044-1-ND/2136581	
EEPROM to identify the board Type and features Default I2C Addr 7bits = 0x50 I2C Addr Read 8bits = 0xA0 I2C Addr Write 8bits = 0xA1 (A0=A1=A2=0)	CAT24C08WI-GT3 http://www.onsemi.com/pub_link/Collateral/CAT24C08-D.PDF Package: 8-SOIC 0.41 USD / 1 Digikey **http://www.digikey.com/product-detail/en/CAT24C08WI-GT3/CAT24C08WI-GT3CT-ND**	
Connector Front-End to Main Board	Samtech QSH-090-01-F-D-A https://www.samtec.com/technical-specifications/Default.aspx?SeriesMaster=QSH Price: 10.73 USD/1 DigiKey http://www.digikey.com/product-detail/en/QSH-090-01-F-D-A/QSH-090-01-F-D-A-ND/2664439	-
Regulator	1x LDO 300mA 3.3V for all LEDs to have a margin of more than 150mA => MIC5318-3.3YD5 TSOT-23-5 1x LDO 300mA 3.3V for all Transceivers => MIC5318-3.3YD5 TSOT-23-5 http://www.micrel.com/_PDF/mic5318.pdf **Price: 1.46 USD / 1 DigiKey,** http://www.digikey.com/product-detail/en/MIC5318-3.3YD5%20TR/576-2860-1-ND/1822020	
LED for each RS232 signal (Enabled/disabled by FPGA output pin Or by Connector P14)	1 LED per signal on the driver TTL side with transistor NPN MUN5230DW1T1G => TRANS BRT NPN DUAL 50V SOT-363 => replaced by MUN5212DW1T1G (R1/R2=22K) Each led have a resistor of 470 Ohm (Current required on base is about 115uA to drive the LED with the Transceiver) So for a LED current = 3.13mA (simulated with LTSpice) over 3.3V => 8 LEDs per transceivers => 4 Transceivers 32 LEDs x 3.2mA = about 102mA	-

For all signal on Px connected to FPGA, the FPGA signal is always the higher priority.

Connectors description	**Functional description**
P1 I2C EEPROM Write Protect (Manually Enabled with Jumper)	No Jumper: I2C EEPROM is write protected (read only mode). Jumper set(1-2): I2C EEPROM read/write access allowed.
P2 RS232 U3 TRS3237E: !EN: Receiver outputs (ROUT) **- To be enabled by FPGA => Set to 1** **- For test Jumper set(1-2)=1**	Enabled/Disabled by FPGA signal !EN-B-TTL Jumper set(1-2)=1: ROUT Disabled/OFF (hi-Z) (Note: ROUT1B is still Enabled) Jumper set(2-3)=0: ROUT Active Default PullUp=1 (No Jumper, FPGA signal hi-Z)

P3 RS232 U2 TRSF3243: FORCEON: Auto-powerdown	Enabled/Disabled by FPGA signal FORCEON-A-TTL Jumper set(1-2)=1: Normal operation with auto-powerdown disabled (if !FORECEOFF is 1) Jumper set(2-3)=0: Normal operation with auto-powerdown enabled (if !FORECEOFF is 1) Default PullUp=1 (No Jumper, FPGA signal hi-Z)
P4 RS232 U2 TRSF3243: !FORCEOFF: **Powered OFF by default** **- To be enabled by FPGA => Set to 1** **- For test Jumper set(1-2)=1**	Enabled/Disabled by FPGA signal !FORCEOFF-A-TTL Jumper set(1-2)=1: Normal operation Jumper set(2-3)=0: Powered OFF Default PullDown=0 (No Jumper, FPGA signal hi-Z)
P5 RS232 U3 TRS3237E: !SHDN: Outputs (DOUT/ROUT) **DOUT hi-Z(off) by default** **- To be enabled by FPGA => Set to 1** **- For test Jumper set(1-2)=1**	Enabled/Disabled by FPGA signal !SHDN-B-TTL Jumper set(1-2)=1: Shutdown Disabled => DOUT Active Jumper set(2-3)=0: Shutdown Enabled => DOUT hi-Z(off) Default PullDown=0 (No Jumper, FPGA signal hi-Z)
P6 Connector 2x8 pins A-TTL signals on top B-TTL signals on bottom A-TTL=DTE TRSF3243 B-TTL=DCE TRS3237E	
P7 REG_3V3 and GND	For Test purpose to check REG_3V3 Power
P8 REG_3V3_LED and GND	For Test purpose to check REG_3V3_LED Power
P9 RS232 U5 TRS3237E: !EN: Receiver outputs (ROUT) **- To be enabled by FPGA => Set to 1** **- For test Jumper set(1-2)=1**	Enabled/Disabled by FPGA signal !EN-D-TTL Jumper set(1-2)=1: ROUT Disabled/OFF (hi-Z) (Note: ROUT1B is still Enabled) Jumper set(2-3)=0: ROUT Active Default PullUp=1 (No Jumper, FPGA signal hi-Z)
P10 RS232 U4 TRSF3243: FORCEON: Auto-powerdown	Enabled/Disabled by FPGA signal FORCEON-C-TTL Jumper set(1-2)=1: Normal operation with auto-powerdown disabled (if !FORECEOFF is 1) Jumper set(2-3)=0: Normal operation with auto-powerdown enabled (if !FORECEOFF is 1) Default PullUp=1 (No Jumper, FPGA signal hi-Z)
P11 RS232 U4 TRSF3243: !FORCEOFF: **Powered OFF by default** **- To be enabled by FPGA => Set to 1** **- For test Jumper set(1-2)=1**	Enabled/Disabled by FPGA signal !FORCEOFF-C-TTL Jumper set(1-2)=1: Normal operation Jumper set(2-3)=0: Powered OFF Default PullDown=0 (No Jumper, FPGA signal hi-Z)
P12 RS232 U5 TRS3237E: !SHDN: Outputs (DOUT/ROUT) **DOUT hi-Z(off) by default** **- To be enabled by FPGA => Set to 1** **- For test Jumper set(1-2)=1**	Enabled/Disabled by FPGA signal !SHDN-D-TTL Priority on FPGA signal Jumper set(1-2)=1: Shutdown Disabled => DOUT Active Jumper set(2-3)=0: Shutdown Enabled => DOUT hi-Z(off) Default PullDown=0 (No Jumper, FPGA signal hi-Z)
P13 Connector 2x8 pins C-TTL signals on top D-TTL signals on bottom C-TTL=DTE TRSF3243 D-TTL=DCE TRS3237E	
Connector P14 (LEDs Power, also called LEDS_PWR on kicad)	Jumper on POS 1-2: Enable LEDs Power in order to see visually all Transceiver signals on LEDs. No Jumper or Jumper on POS 2-3: Disable LEDs Power.