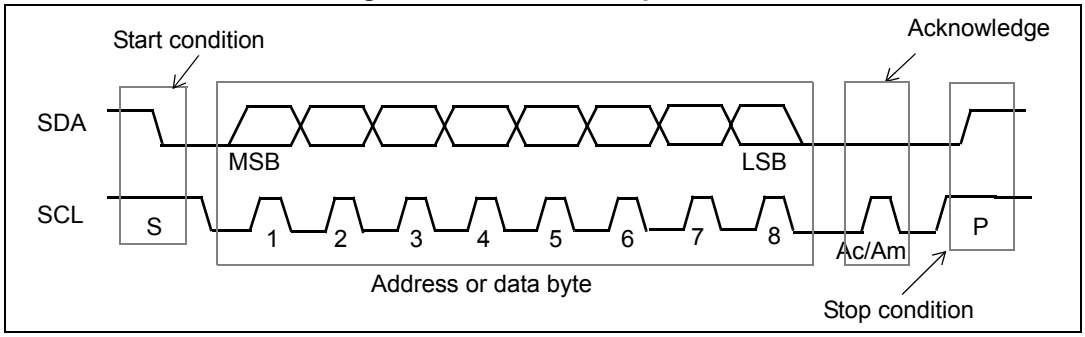
3 Control interface

This section specifies the control interface. The I^2C interface uses two signals: serial data line (SDA) and serial clock line (SCL). Each device connected to the bus is using a unique address and a simple master / slave relationships exists.

Both SDA and SCL lines are connected to a positive supply voltage using pull-up resistors located on the host. Lines are only actively driven low. A high condition occurs when lines are floating and the pull-up resistors pull lines up. When no data is transmitted both lines are high.

Clock signal (SCL) generation is performed by the master device. The master device initiates data transfer. The I^2C bus on the VL53L0X has a maximum speed of 400 kbits/s and uses a device address of 0x52.

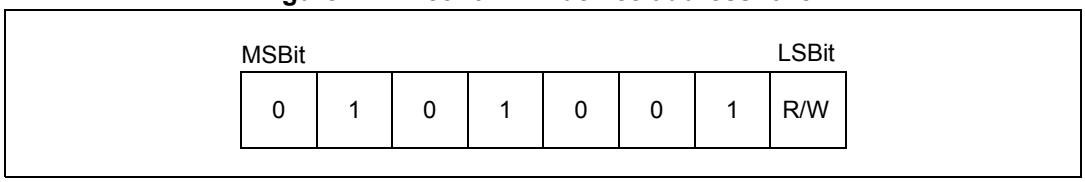
Figure 13. Data transfer protocol



Information is packed in 8-bit packets (bytes) always followed by an acknowledge bit, Ac for VL53L0X acknowledge and Am for master acknowledge (host bus master). The internal data is produced by sampling SDA at a rising edge of SCL. The external data must be stable during the high period of SCL. The exceptions to this are start (S) or stop (P) conditions when SDA falls or rises respectively, while SCL is high.

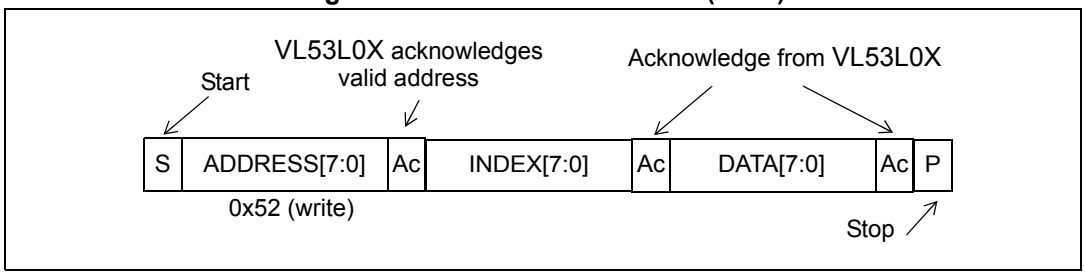
A message contains a series of bytes preceded by a start condition and followed by either a stop or repeated start (another start condition but without a preceding stop condition) followed by another message. The first byte contains the device address (0x52) and also specifies the data direction. If the least significant bit is low (that is, 0x52) the message is a master write to the slave. If the lsb is set (that is, 0x53) then the message is a master read from the slave.

Figure 14. VL53L0X I2C device address: 0x52



All serial interface communications with the camera module must begin with a start condition. The VL53L0X module acknowledges the receipt of a valid address by driving the SDA wire low. The state of the read/write bit (lsb of the address byte) is stored and the next byte of data, sampled from SDA, can be interpreted. During a write sequence the second byte received provide a 8-bit index which points to one of the internal 8-bit registers.

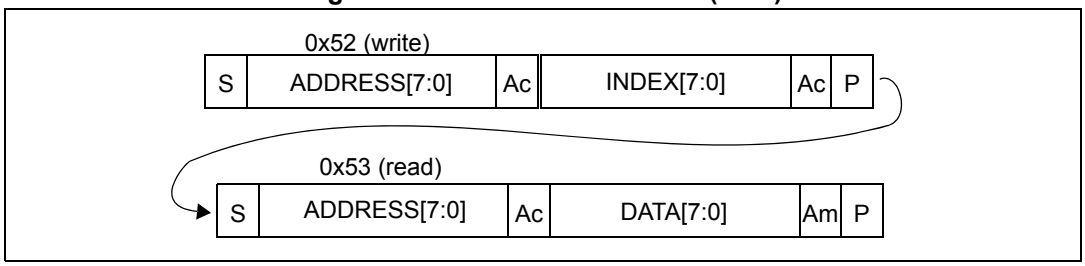
Figure 15. VL53L0X data format (write)



As data is received by the slave it is written bit by bit to a serial/parallel register. After each data byte has been received by the slave, an acknowledge is generated, the data is then stored in the internal register addressed by the current index.

During a read message, the contents of the register addressed by the current index is read out in the byte following the device address byte. The contents of this register are parallel loaded into the serial/parallel register and clocked out of the device by the falling edge of SCL.

Figure 16. VL53L0X data format (read)



At the end of each byte, in both read and write message sequences, an acknowledge is issued by the receiving device (that is, the VL53L0X for a write and the host for a read).

A message can only be terminated by the bus master, either by issuing a stop condition or by a negative acknowledge (that is, **not** pulling the SDA line low) after reading a complete byte during a read operation.

The interface also supports auto-increment indexing. After the first data byte has been transferred, the index is automatically incremented by 1. The master can therefore send data bytes continuously to the slave until the slave fails to provide an acknowledge or the master terminates the write communication with a stop condition. If the auto-increment feature is used the master does **not** have to send address indexes to accompany the data bytes.

Figure 17. VL53L0X data format (sequential write)

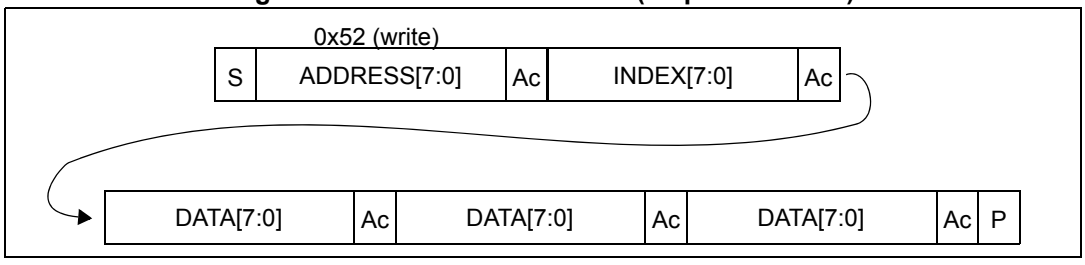
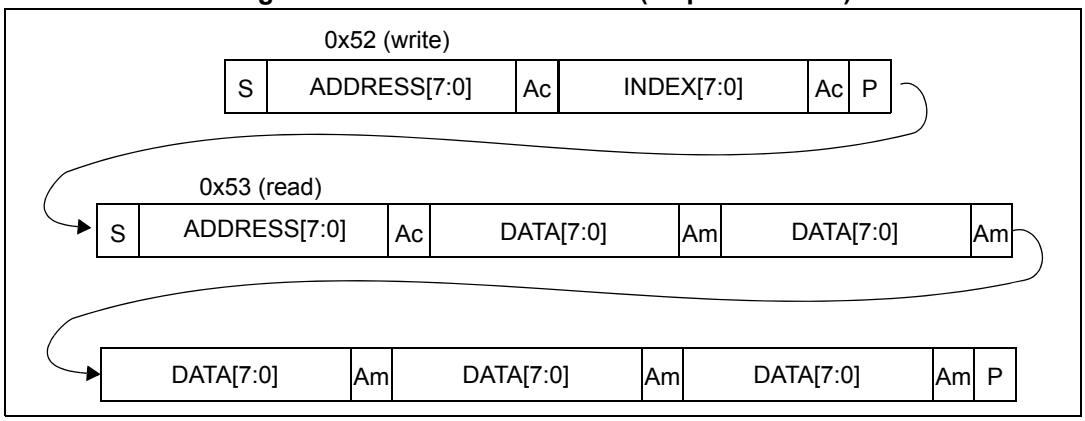


Figure 18. VL53L0X data format (sequential read)



3.1 I²C interface - timing characteristics

Timing characteristics are shown in *Table 3*. Please refer to *Figure 19* for an explanation of the parameters used.

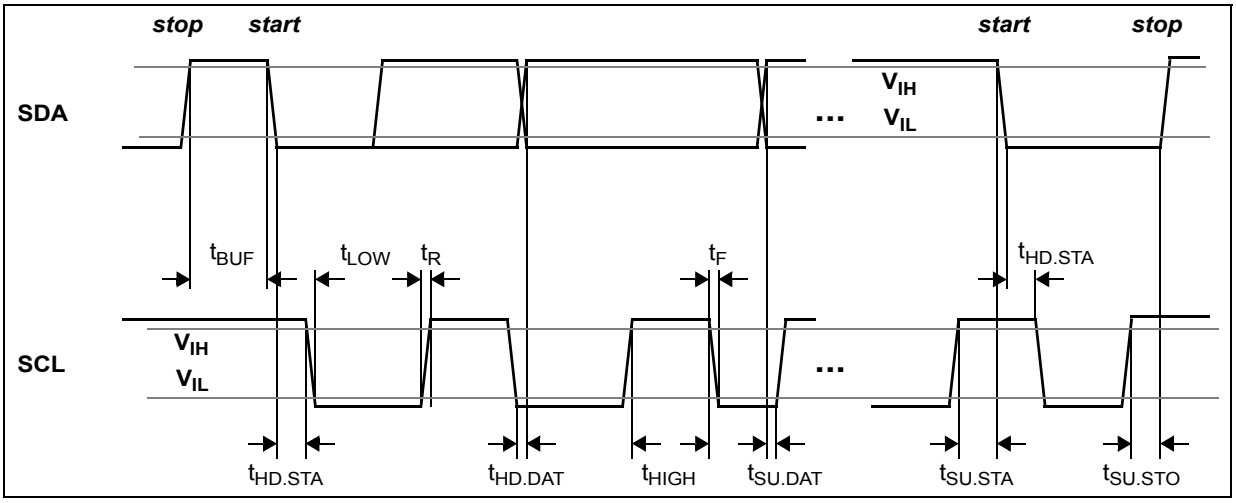
Timings are given for all PVT conditions.

Table 3. I²C interface - timing characteristics

Symbol	Parameter	Minimum	Typical	Maximum	Unit
F_{I2C}	Operating frequency (Standard and Fast mode)	0	-	400(1)	kHz
t_{LOW}	Clock pulse width low	1.3	-	-	µs
t_{HIGH}	Clock pulse width high	0.6	-	-	µs
t_{SP}	Pulse width of spikes which are suppressed by the input filter	-	-	50	ns
t_{BUF}	Bus free time between transmissions	1.3	-	-	ms
$t_{HD.STA}$	Start hold time	0.26	-	-	µs
$t_{SU.STA}$	Start set-up time	0.26	-	-	µs
$t_{HD.DAT}$	Data in hold time	0	-	0.9	µs
$t_{SU.DAT}$	Data in set-up time	50	-	-	ns
t_R	SCL/SDA rise time	-	-	120	ns
t_F	SCL/SDA fall time	-	-	120	ns
$t_{SU.STO}$	Stop set-up time	0.6	-	-	µs
Ci/o	Input/output capacitance (SDA)	-	-	10	pF
Cin	Input capacitance (SCL)	-	-	4	pF
C_L	Load capacitance	-	125	400	pF

1. The maximum bus speed is also limited by the combination of 400pF load capacitance and pull-up resistor. Please refer to the I²C specification for further information.

Figure 19. I²C timing characteristics



All timings are measured from either V_{IL} or V_{IH}.

3.2 I²C interface - reference registers

The registers shown in the table below can be used to validate the user I²C interface.

Table 4. Reference registers

Address	(After fresh reset, without API loaded)
0xC0	0xEE
0xC1	0xAA
0xC2	0x10
0x51	0x0099
0x61	0x0000

Note: I2C read/writes can be 8,16 or 32-bit. Multi-byte reads/writes are always addressed in ascending order with MSB first as shown in Table 5.

Table 5. 32-bit register example

Register address	Byte
Address	MSB
Address + 1	..
Address + 2	..
Address + 3	LSB