Australian National University | ANU College of ENGINEERING, COMPUTING AND CYBERNETICS

ENGN 4213/6213 Digital Systems and Microprocessors

Semester 1, 2023

Tutorial 2

Question 1:

a. Explain and compare **Structural** vs **Behavioral** (also sometimes called *procedural*) design procedure in Verilog with the help of Verilog `assign` statement and `always` block.
b. Use `assign` statement and `always` block to design a 4 to 16 decoder. Explain the advantage and disadvantage of the two designs.

Question 2:

a. Describe the functionality of a blocking and non-blocking assignment in a Verilog `always` block.
b. Explain the functionality of the following two sets of Verilog codes for a module with input signal `wire A` and output signal `reg D`:

Blocking	Non-blocking

`always @(posedge clk)`
`// block triggered on the rising edge of clock`
 	
`begin`
`  B = A;`
`  C = B;`
`  D = C;`
`end`
	`always @(posedge clk)`
	`// block triggered on the rising edge of clock`
	
	`begin`
	`  B <= A;`
	`  C <= B;`
	`  D <= C;`
	`end`

Question 3:

Use Verilog to design the following hardware:

a. 4 to 1 multiplexer
b. 4-bit SIPO register
c. A parallel bank of four D flip-flops with an additional input to disable the output.
d. A clock-divider implementing $1/(2^4)$ division.