Australian National University | ANU College of ENGINEERING, COMPUTING AND CYBERNETICS

ENGN 4213/6213 Digital Systems and Microprocessors

Semester 1, 2023

Tutorial 3 – Worked Solutions

Question 1:

Consider the following Verilog code when answering Question 1:

```
module mymod(
     input wire a,
     input wire b,
     input wire f,
     input wire [3:0] e,
     output wire c);

reg [3:0] d;

   always @(posedge b) begin
      if(a) d <= e;
      else if(f) d <= {1'b0, d[3:1]};
   end

assign c = d[0];

endmodule
```

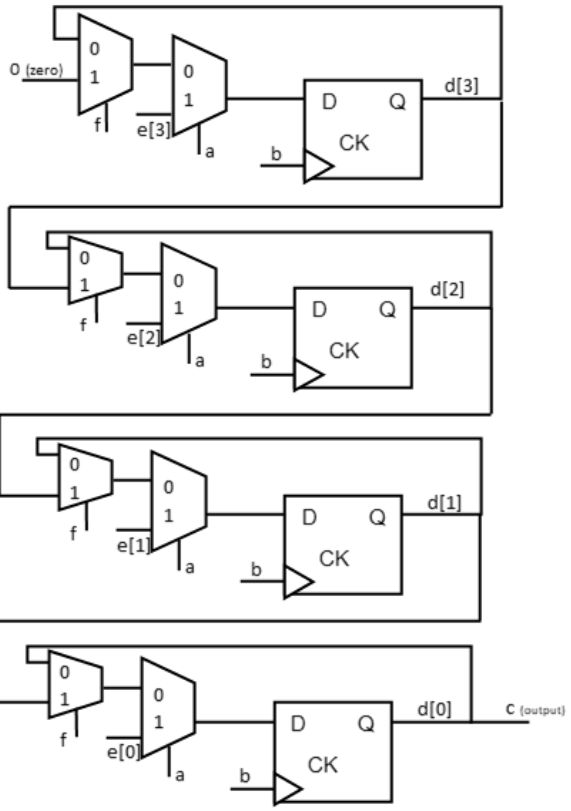
↳ eg. d = 1101

⇓

d = 0110

1'b0 d[3:1]

a. Draw a block diagram detailed to flip-flop level



b. Explain the functional role of entities `a`, `b`, `c`, `d`, `e` and `f`

`a` is a mux selector signal. It can also be called a “parallel write-enable”, “parallel load”, or similarly named

`b` is the clock or edge trigger for the register

`c` is the output, also called serial output or lsb of the register

`d` is the storage register, also called bank of flipflops

`e` is the input data, also called parallel input

`f` is a mux selector signal, can also be called a “push” signal, which serves to shift data along the chain of flipflops

c. Suggest a possible use for the behaviour of this module

PISO shift register

d. Is this design sequential or combinational? Explain your answer

It is sequential since it has memory / timed behaviour.

e. Is this design synchronous or asynchronous? Explain you answer

It is synchronous since all flipflops are driven by the same clock.

Question 2:

You wish to design a circuit with one button and four LEDs such that one LED is on at once, and each press of the button turns the next on the next LED in sequence:

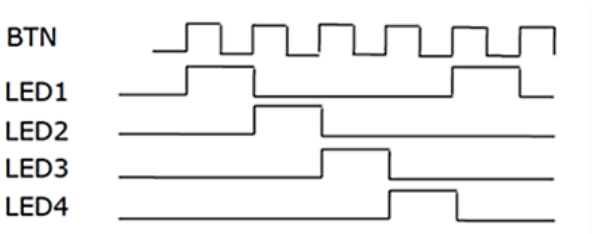
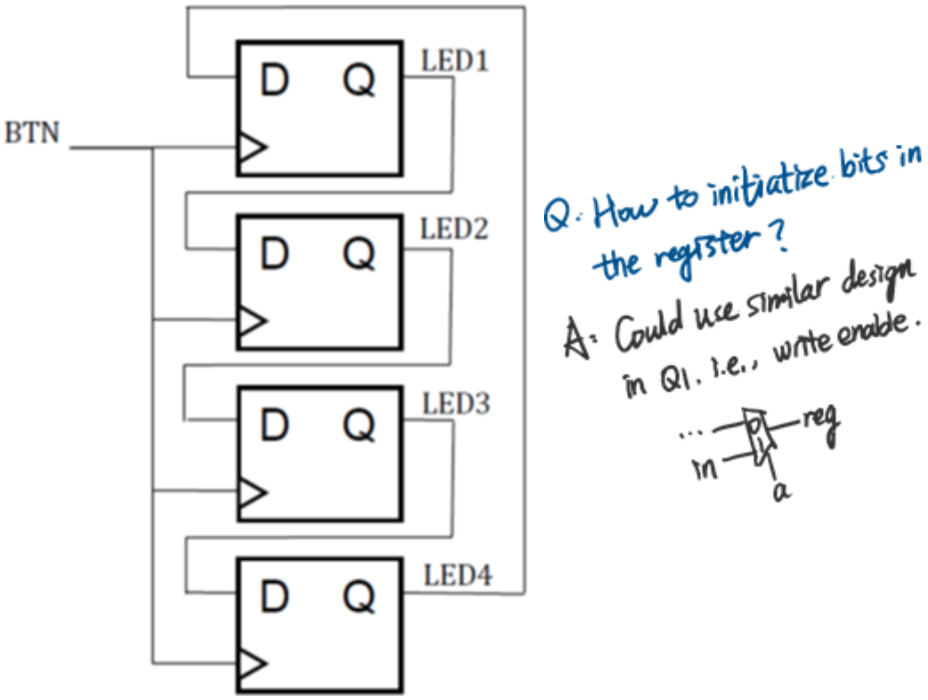


Figure 1

a. What is the name of this type of counter?

One-hot counter: there are n outputs to the device, each delivering a “1” output for one clock cycle only in a rotating fashion

b. Sketch the logic that might be used to implement this behaviour



c. The output of this circuit can be used as a ‘selector’ for down-stream behaviour.
Write a short combinatorial Verilog snippet that takes the outputs of this counter as inputs, and has the following outputs itself:

- A 16-bit bus called `A`
- An 8-bit bus called `D`
- A one-bit line called `LA`
- A one-bit line called `RW`

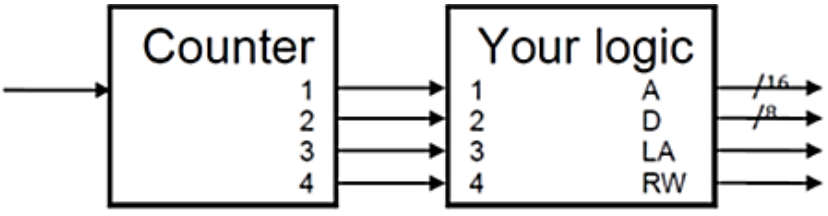


Figure 2

The Verilog code should represent a design which does the following in order:
First state: Set A to '143' (the rest should be '0')
Second state: Set LA to '1'
Third state: Set D to '42', RW to '1', LA to '0'
Fourth state: Set RW to '0'

Congratulations, you just wrote your first state machine! This example would be suitable for storing the value '42' at address '143' in some external RAM.

```
module output_logic(
input wire in1, in2, in3, in4,
output reg [15:0] a,
output reg [7:0] d,
output reg rw,
output reg la);

    always @ (*) begin
        if(in1) begin
            a = 16'd143;
            d = 8'h00;
            rw = 1'b0;
            la = 1'b0;
        end
        else if (in2) begin
            a = 16'd143;
            d = 8'h00;
            rw = 1'b0;
            la = 1'b1;
        end
        else if (in3) begin
            a = 16'd143;
            d = 8'd42;
            rw = 1'b1;
            la = 1'b0;
        end
        else begin // equiv if(in4)
            a = 16'd143;
            d = 8'd42;
            rw = 1'b0;
            la = 1'b0;
        end
    end
endmodule
```