Australian National University

ENGN4213/ENGN6213

Digital Systems and Microprocessors

ANU ENGINEERING & COMPUTER SCIENCE

- Tutorial 8
- MCU ADC

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1. Questions

Assume a 12-bit ADC with $V_{ref} = 3.3V$. The ADC only works for positive voltages, its PCLK2 clock frequency is 16MHz, its prescaler can be configured as 'PCLK divided by 2, 4, 6, or 8'. Assume the ADC sampling time is set to 3 cycles.

1. What is the resolution of this ADC?
2. What is the max quantization error of this ADC?
3. For an input signal $V_{in} = 2V$, what is the corresponding ADC output?
4. How many cycles are required to make one conversion?
5. For an input signal $y = \sin(100\pi t) + \sin(75\pi t) + \sin(1500\pi t)$, what is the minimum sampling frequency that it will not distort its underlying information?
6. To achieve a sampling rate (f_d) of 8KHz, how to configure the trigger of the ADC?
   a) Can we use 'Regular conversion launched by software'? If we can, how to configure the prescaler of the ADC?
   b) If we use a timer (TIM2) to trigger the ADC, assume the clock source of the timer is configured as 'internal clock'. How to configure the timer? Please specify the prescaler (PSC), frequency of the clock source (f_s) and auto-reload (ARR) of the timer.