Video Lecture 1
Non-ideal Behaviour

ENGN 4213/6213

Digital Systems and Microprocessors

What's in this lecture

- The operation of CMOS logic in nonideal conditions or under a load
- Timing and timing hazards

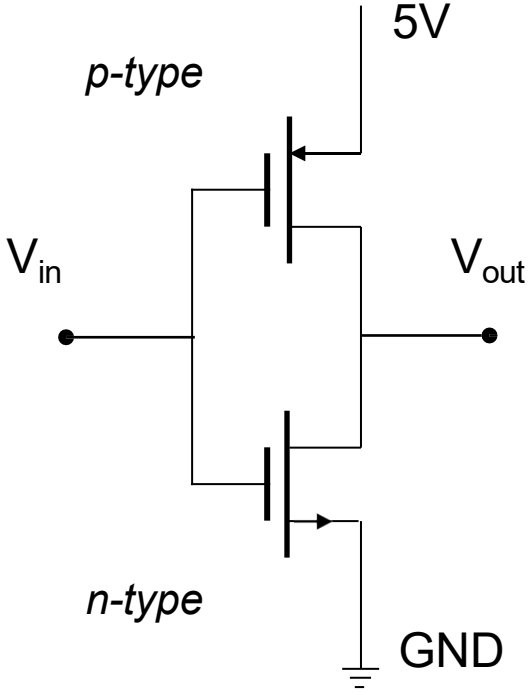
Resources

- Wakerly (5th edition) 14.3 and 14.4 for static and dynamic electrical behaviour of CMOS
  (we do not get into as much detail as the book does)
- Wakerly 4.2 on circuit timing and 3.4 on timing hazards

On MOSFET/CMOS again

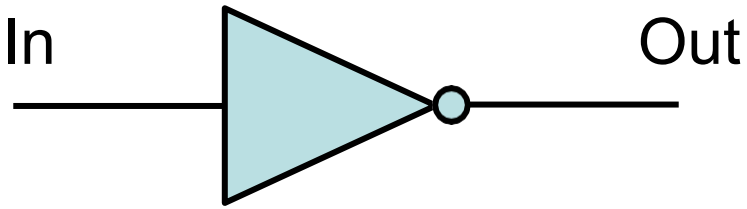
- We remember the following key characteristics
  - MOSFET transistors, when conducting, either behave as a *resistor* (“ohmic” or “triode” mode) or a *current source* (saturation mode), depending on the value of V_{GS} w.r.t. V_{DS}
  - CMOS technology combines n-MOS and p-MOS transistors
  - CMOS components use very little power if no logic switching occurs
  - CMOS logic relies on input/output signals being very close to the upper/lower reference voltages (e.g., 0V/5V)

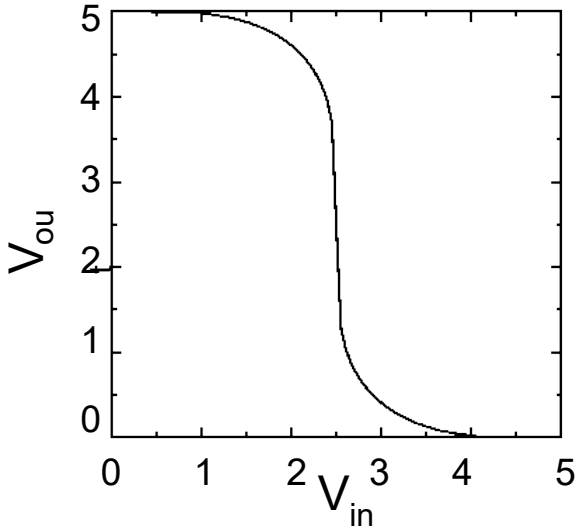
The CMOS inverter



Inverter Truth Table

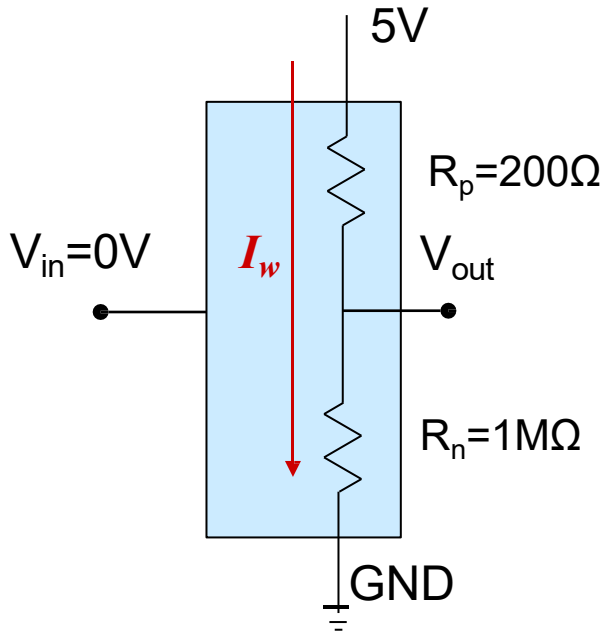
IN	OUT
1	0
0	1





CMOS with nonideal input

Normal operation

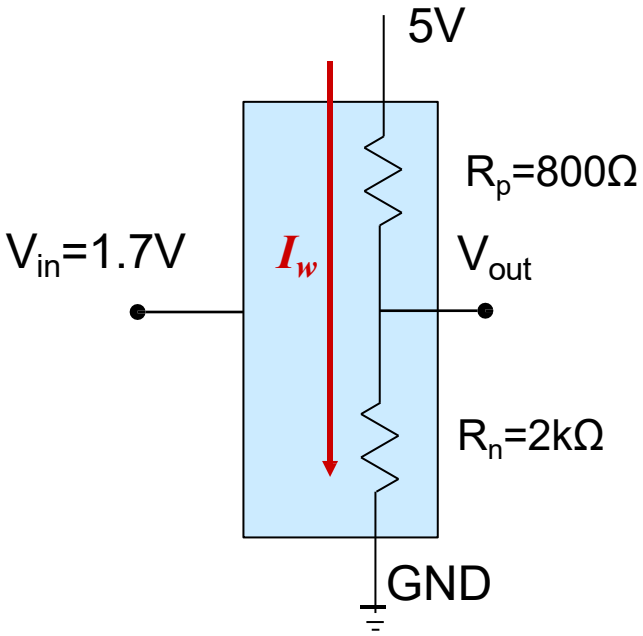


$I_w = 5V/(R_p+R_n) = 5V/(1.0002M\Omega) < 1\mu A$

$P_w = 5V \cdot I_w = 5\mu W$

$V_{out} = 5V - (200\Omega \cdot 1\mu A) = 4.9998V$

Nonideal input



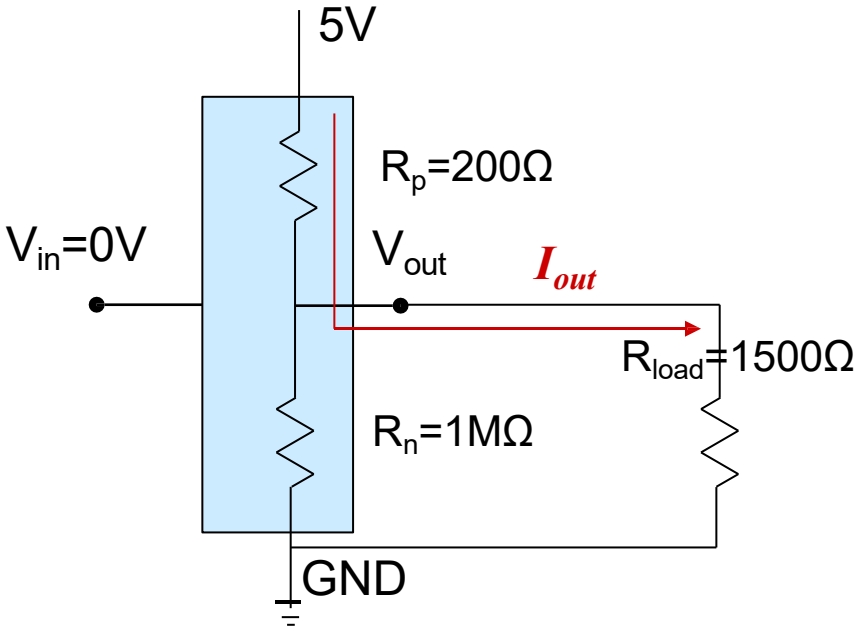
$I_w = 5V/(2.8k\Omega) = 1.79mA$

$P_w = 5V \cdot I_w = 8.93mW$

$V_{out} = 5V - (800\Omega \cdot 1.79mA) = 3.57V$

CMOS with resistive load

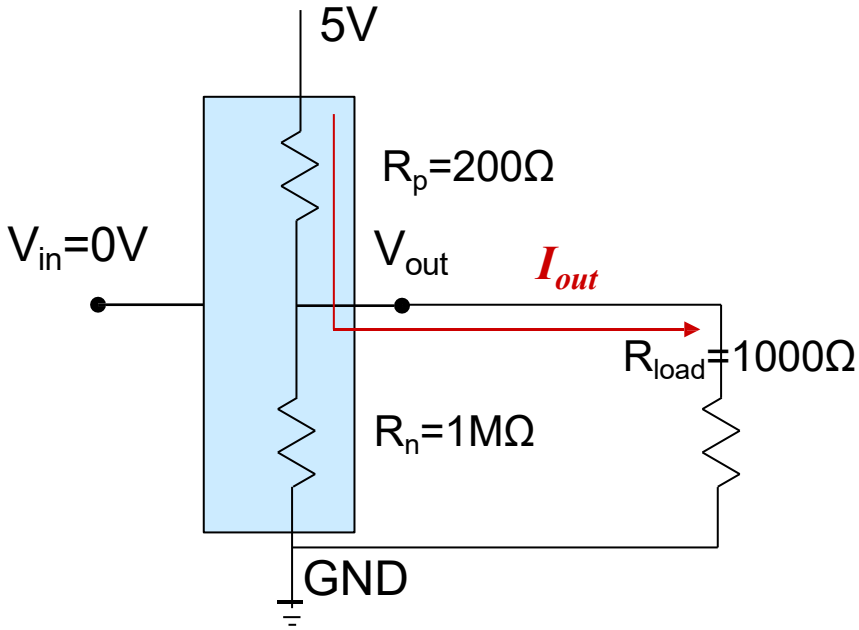
Acceptable load



$I_{out} \approx 5V/(R_p+R_{load}) = 5V/(1.7k\Omega) = 3mA$

$V_{out} = 5V - (200\Omega \cdot 3mA) = 4.4V$

Unacceptable load

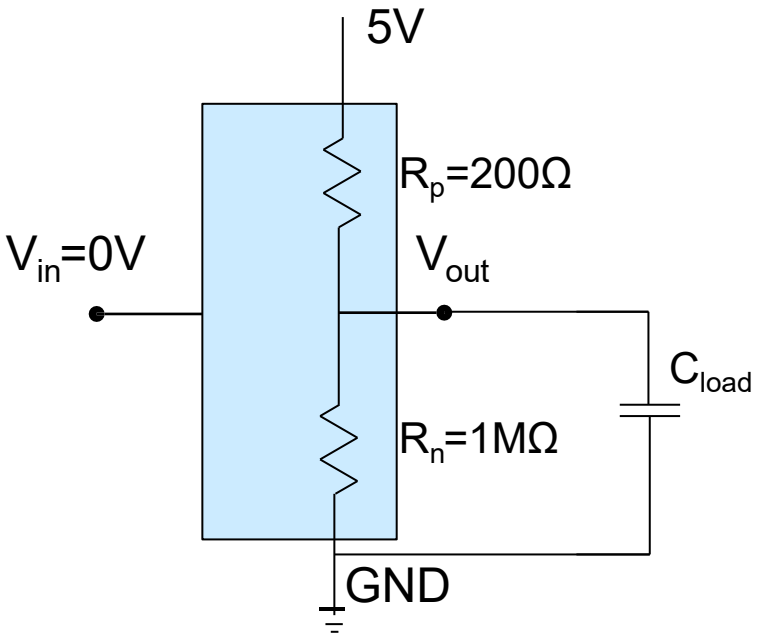


$I_{out} \approx 5V/(R_p+R_{load}) = 5V/(1.2k\Omega) = 4.16mA$

$V_{out} = 5V - (200\Omega \cdot 4.16mA) = 4.17V$

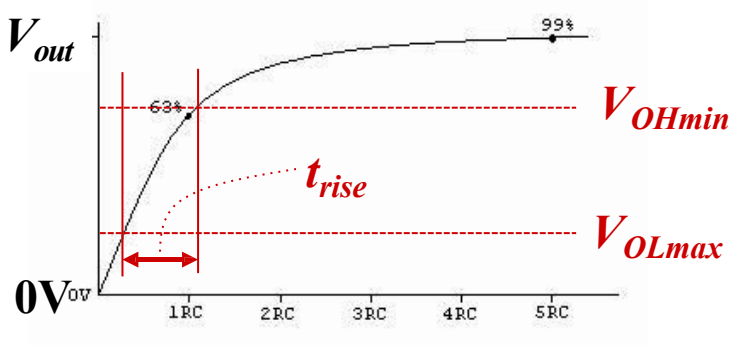
CMOS with a capacitive load

- Capacitive loads are always present.
  - Even the input terminal of a downstream logic stage has capacitance



The charging/discharging of the load capacitance **is not instantaneous**.

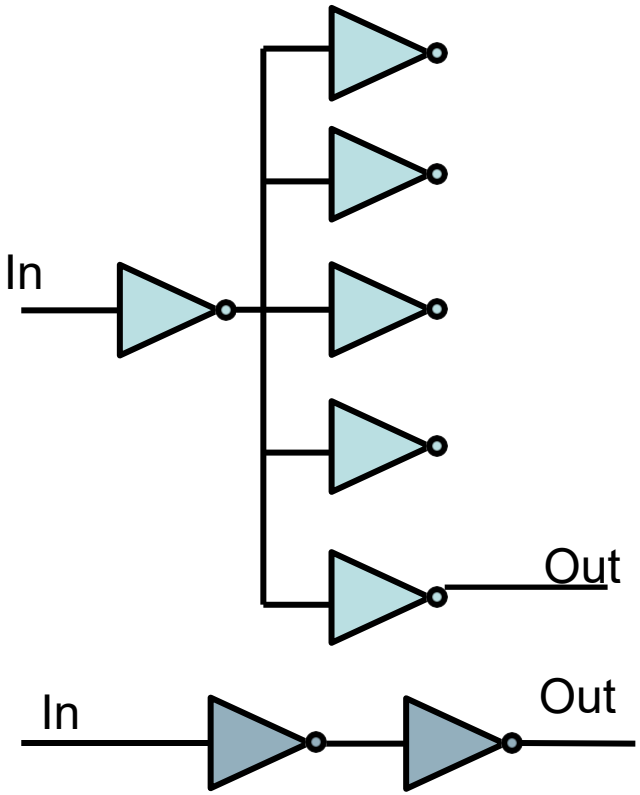
The behaviour can be approximated as a **simple RC network** with a *rise/fall time*



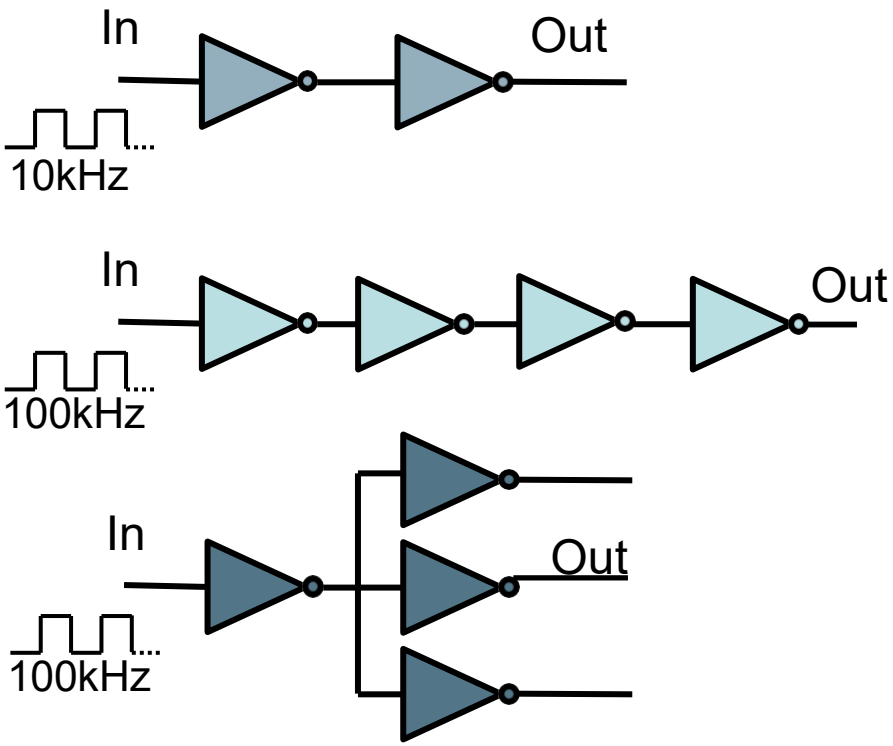
Capacitance can have a big **impact on transition times and delays.**
You will solve a similar exercise in tutorial 1

Visualising some concepts

Will the propagation times be different?

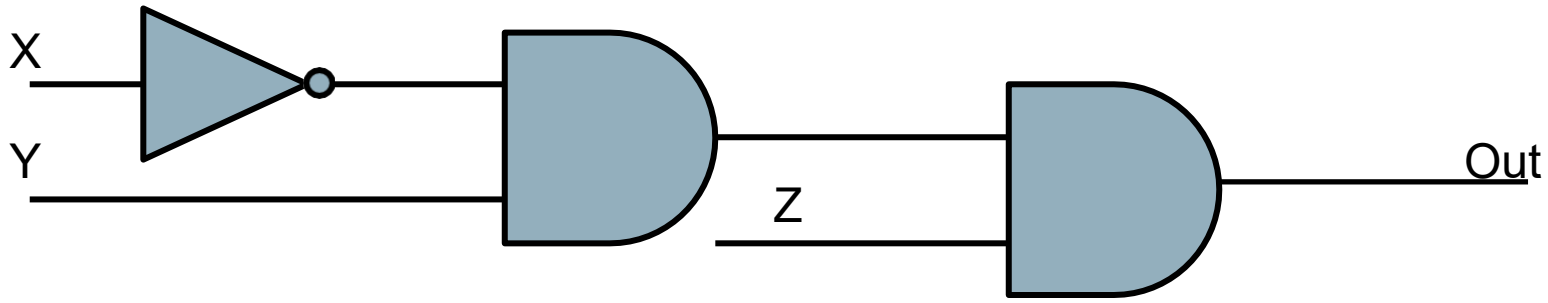


Which schematic is likely to produce the most heat?



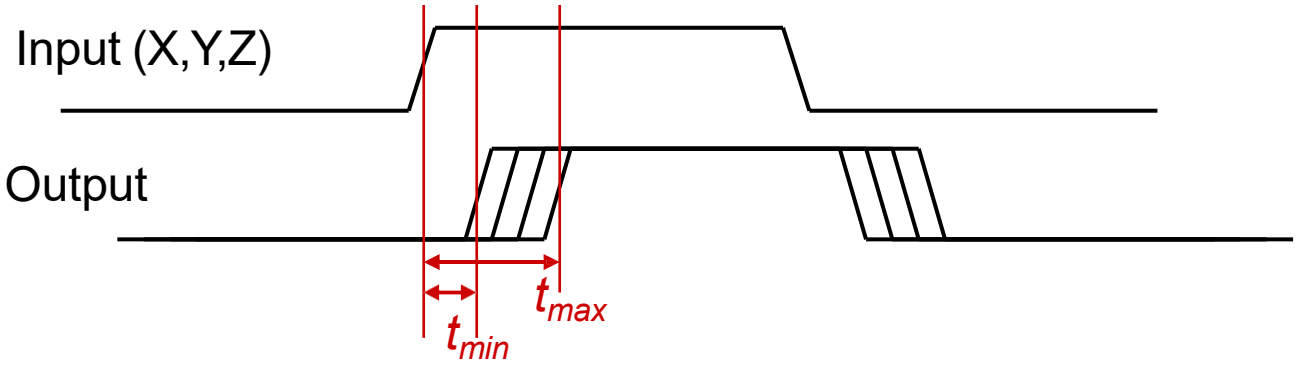
Timing

- We have seen that **load** and **logic complexity** can affect transition times
- It is common to have different propagation delays depending on the signal's pathway.
  - For example, in the circuit below, a change in input Z will show at the output after 1 gate has transitioned, while a change in Y will show after 2 transitions; X after 3 transitions.



Timing (2)

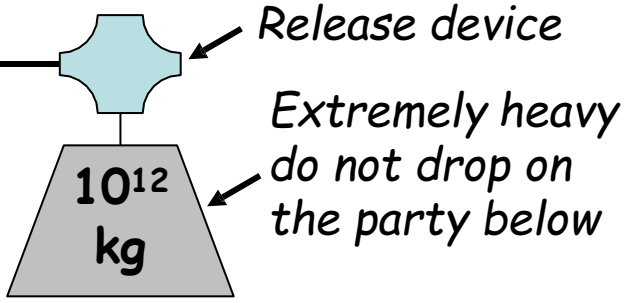
- This uncertainty in the switching timing of the output is reflected in **timing diagrams**. These are a graphical representation which can be useful to the designer in planning/refining a circuit design.
- **Simulation softwares** can be used to generate timing diagrams and you will learn how to do so during the labs.



- A good design should be expected to function for all input combinations. Therefore, considering **worst-case or *maximum* delays** is a safe way to ensure that the system will deliver dependable performance.

Hazards

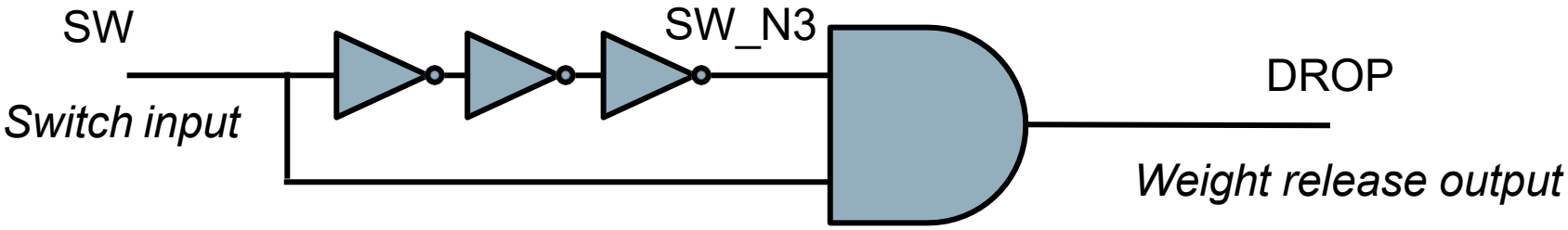
- In some cases paths with different propagation delays can create *hazards.* In purely combinational circuits, these should be avoided.
  - **A hazard is a temporary "glitch" or incorrect output displayed as part of a transition in the circuit.** Since combinational circuits (unlike sequential ones, which we will discuss shortly) react immediately to a change in input, a glitch could initiate a cascade of undesirable transitions. Causing the system to perform poorly.
  - For an example, look at this (silly) system …



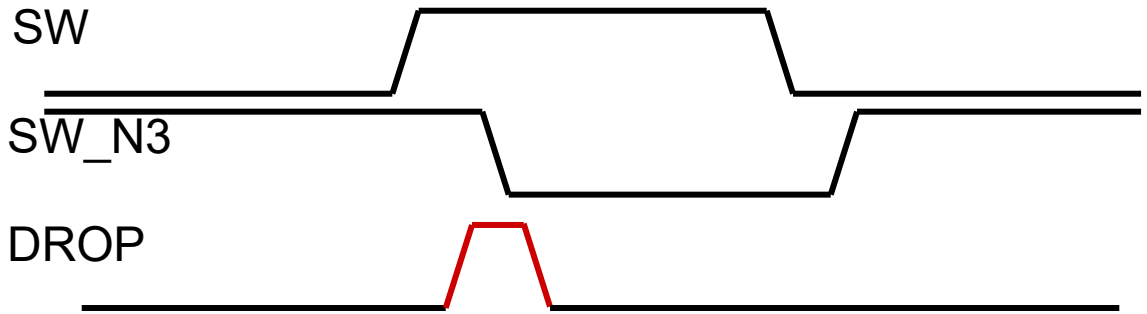
… and assume you want to save them →

Hazards (2)

- **Would this system work?**



- You'd think the partygoers could breathe a sigh of relief, after all **(SW·(((SW)')')') = 0**. Right? Look at the timing diagram below.



Hazards (3)

- Although it might only last a few nanoseconds (transitions of 3 inverters), the glitch in the output *may* prove disastrous. **Steady state analysis is not indicative of dynamic performance.**
- This is a *static type 0 hazard*, where a change in the input which should see the output remain LOW determines a brief "1" glitch. There are also *type 1 hazards* (dual) and *dynamic hazards*.
  - See Wakerly 4.4
- Whether or not you need to worry about hazards depends on **how critical the impact of the glitch is on the output.**
- In sequential circuit design we can use **synchronisation** to neglect hazards. Signals are "sampled" at time intervals which are **far enough in time for all transient behaviour to have settled**.
  - You will see an example of this in CLAB 2

Summing up

- You now know about some non-ideal aspects of digital circuits with a particular focus on CMOS hardware:
  - Importance of correct voltages
    - For digital operation
    - To avoid excessive power dissipation
  - Role of loads in affecting timing
  - Hazards arising from propagation delays

- As you will learn to use computer-assisted design (CAD) tools, the software (ISE WebPACK in our lab activities) will assist you in diagnosing whether your design is at risk of undesirable behaviour.
  - Softwares are no substitute for a good understanding of the underlying principles. You need to have some idea of where to look when the CAD tools “complain” about your design.