Australian National University | ANU College of ENGINEERING, COMPUTING AND CYBERNETICS

ENGN 4213/6213 Digital Systems and Microprocessors

Semester 1, 2023

Tutorial 3

Question 1:

Consider the following Verilog code when answering Question 1:

```
module mymod(
     input wire a,
     input wire b,
     input wire f,
     input wire [3:0] e,
     output wire c);

reg [3:0] d;

   always @(posedge b) begin
      if(a) d <= e;
      else if(f) d <= {1'b0, d[3:1]};
   end

assign c = d[0];

endmodule
```

a. Draw a block diagram detailed to flip-flop level
b. Explain the functional role of entities `a`,`b`,`c`,`d`,`e` and `f`
c. Suggest a possible use for the behaviour of this module
d. Is this design sequential or combinational? Explain your answer
e. Is this design synchronous or asynchronous? Explain you answer

Question 2:

You wish to design a circuit with one button and four LEDs such that one LED is on at once, and each press of the button turns the next on the next LED in sequence:

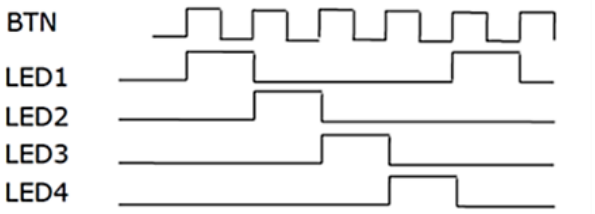

Figure 1

a. What is the name of this type of counter?
b. Sketch the logic that might be used to implement this behaviour
c. The output of this circuit can be used as a 'selector' for down-stream behaviour.
   Write a short combinatorial Verilog snippet that takes the outputs of this counter as inputs, and has the following outputs itself:
   - A 16-bit bus called `A`
   - An 8-bit bus called `D`
   - A one-bit line called `LA`
   - A one-bit line called `RW`

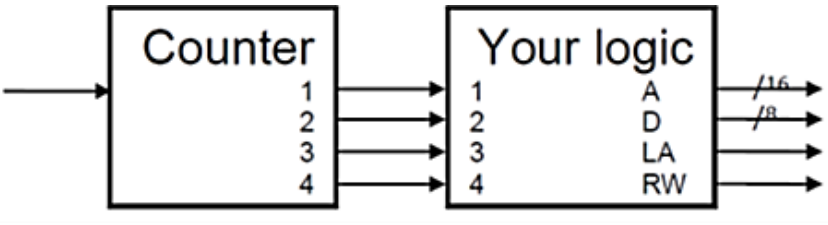

Figure 2

The Verilog code should represent a design which does the following in order:
First state: Set A to '143' (the rest should be '0')
Second state: Set LA to '1'
Third state: Set D to '42', RW to '1', LA to '0'
Fourth state: Set RW to '0'

Congratulations, you just wrote your first state machine! This example would be suitable for storing the value '42' at address '143' in some external RAM.