Lab 2 supplementary material – Finding the logic standard of the clock on Basys 3

The Basys3 board hosts a 100 MHz crystal oscillator, which is a device generating a precisely timed alternating signal. From the Basys3 reference manual, the oscillator connects to the FPGA chip through pin W5. To find the voltage we should inform the implementation tools to expect, check the schematic of Basys3 and search for the pin designator W5. The name of the signal entering W5 is CLK100MHZ (BANK 34 on page 6) which implies it is a clock signal at 100 MHz. On the bottom left corner of page 6, it is shown that CLK100MHZ is generated by a component called DSC1033CC1-100.0000T, which is connected to one of the board's 3.3 V rails (VCC3V3). However, this does **not** guarantee that the oscillator's maximum output voltage is also 3.3 V. Therefore, it is necessary to check the oscillator's datasheet to determine the relationship between the input and output voltages. The minimum voltage level produced by the oscillator is specified to be at worst 0.2 x 3.3 Volts = 0.66 Volts, and the maximum voltage level is specified to be at worst 0.8 x 3.3 Volts = 2.64 Volts, both within the acceptable ranges of the CMOS 3.3 Voltage standards. The I/O standard for the 100 MHz oscillator entering the FPGA is thus LVCMOS33.