Tutorial 8: MCU ADC

Assume a 12-bit ADC, V_{ref} = 3.3V, the ADC only works for positive voltages, PCLK2 clock frequency is 16MHz, prescaler can be configured as 'PCLK divided by 2, 4, 6, or 8'. Assume the ADC sampling time is set to 3 cycles.

1. What is the resolution of this ADC?

$$V_{Resolution} = \frac{V_{ref}}{2^N - 1} = \frac{3.3}{2^{12} - 1} = 0.80586\ mV$$

2. What is the max quantization error of this ADC?

$$Max.quantization\ error = \frac{1}{2} \times V_{Resolution} = \frac{1}{2} \times 0.80586 = \pm 0.40293\ mV$$

3. For an input signal V_{in} = 2V, what is the ADC output?

$$ADC\ output = round\left((2^N - 1) \times \frac{V_{in}}{V_{Ref}}\right) = round\left(\frac{(2^N - 1)}{V_{Ref}} \times V_{in}\right) = round\left(\frac{1}{V_{Res}} \times V_{in}\right)$$

$$\therefore ADC\ output = round\left(\frac{V_{in}}{V_{Resolution}}\right) = round\left(\frac{2\ V}{0.80586\ mV}\right) = round(2481.818) = 2482 = 0x09B2$$

4. How many cycles are required to make one conversion?

	ADC		
Analog ->	Stage 1 Read Analog (A to A) Sampling times $N_s = 3$	Stage 2 Conversion (A to D) Conversion time $N_c = 12$	-> Digital

$$Total\ conversion\ time = N_s + N_c = 3 + 12 = 15\ cycles$$

5. For an input signal $y = \sin(100\pi t) + \sin(75\pi t) + \sin(1500\pi t)$, what is the minimum sampling frequency that it will not distort its underlying information?

$$y_1 = \sin(2\pi f_1 t) = \sin(100\pi t)$$
$$f_1 = 50\ Hz$$
$$y_2 = \sin(2\pi f_2 t) = \sin(75\pi t)$$
$$f_2 = 37.5\ Hz$$
$$y_3 = \sin(2\pi f_3 t) = \sin(1500\pi t)$$
$$f_3 = 750\ Hz$$
$$\therefore f_{max} = f_3 = 750\ Hz$$
$$f_{sampling} \geq 2 \times f_{max} = 2 \times 750 = 1500\ Hz$$

6. To achieve a sampling rate (f_d) of 8KHz, how to configure the trigger of the ADC?

(1) Can we use 'Regular conversion launched by software'? If we can, how to configure the prescaler of the ADC?

The largest prescaler in the list of 'PCLK divided by 2, 4, 6, or 8' is 8. Even if we used it, we have:

$$f_{sampling} = \frac{\left(\frac{16MHz}{8}\right)}{15} = 133.33\ kHz$$

, which is still way larger than *8 kHz* target.

(2) If we use a timer (TIM2) to trigger the ADC, assume the clock source of the timer is configured as 'internal clock'. How to configure the timer? Please specify the prescaler (PSC), frequency of the clock source (f_s), and auto-reload (ARR) of the timer.

From the stm32f411re-datasheet, TIM2 is connected in APB1 bus with a prescaler of 16 bits and an Auto-Reload-Register (ARR) of 32 bits.

$$Total\ scale = \frac{16M}{8K} = 2000 = (PSC + 1)(ARR + 1)$$

If we configure timer clock source (APB1 Timer clocks) $f_s = 16MHz$ and prescaler (PSC) as

$$PSC = 20 - 1 = 19$$

Then for ARR:

$$ARR = \frac{\left(\frac{f_s}{PSC + 1}\right)}{f_d} - 1 = \frac{\left(\frac{16MHz}{20}\right)}{8KHz} - 1 = 100 - 1 = 99$$

Or simply:

$$ARR = \frac{2000}{PSC + 1} - 1 = \frac{2000}{20} - 1 = 99$$

Lastly, we need to double check whether the selected PSC and ARR value are valid choices. That is, whether the chosen value (PSC and ARR) can be represented by 16-bit and 32-bit, respectively.

Please note that the answer is open ended.