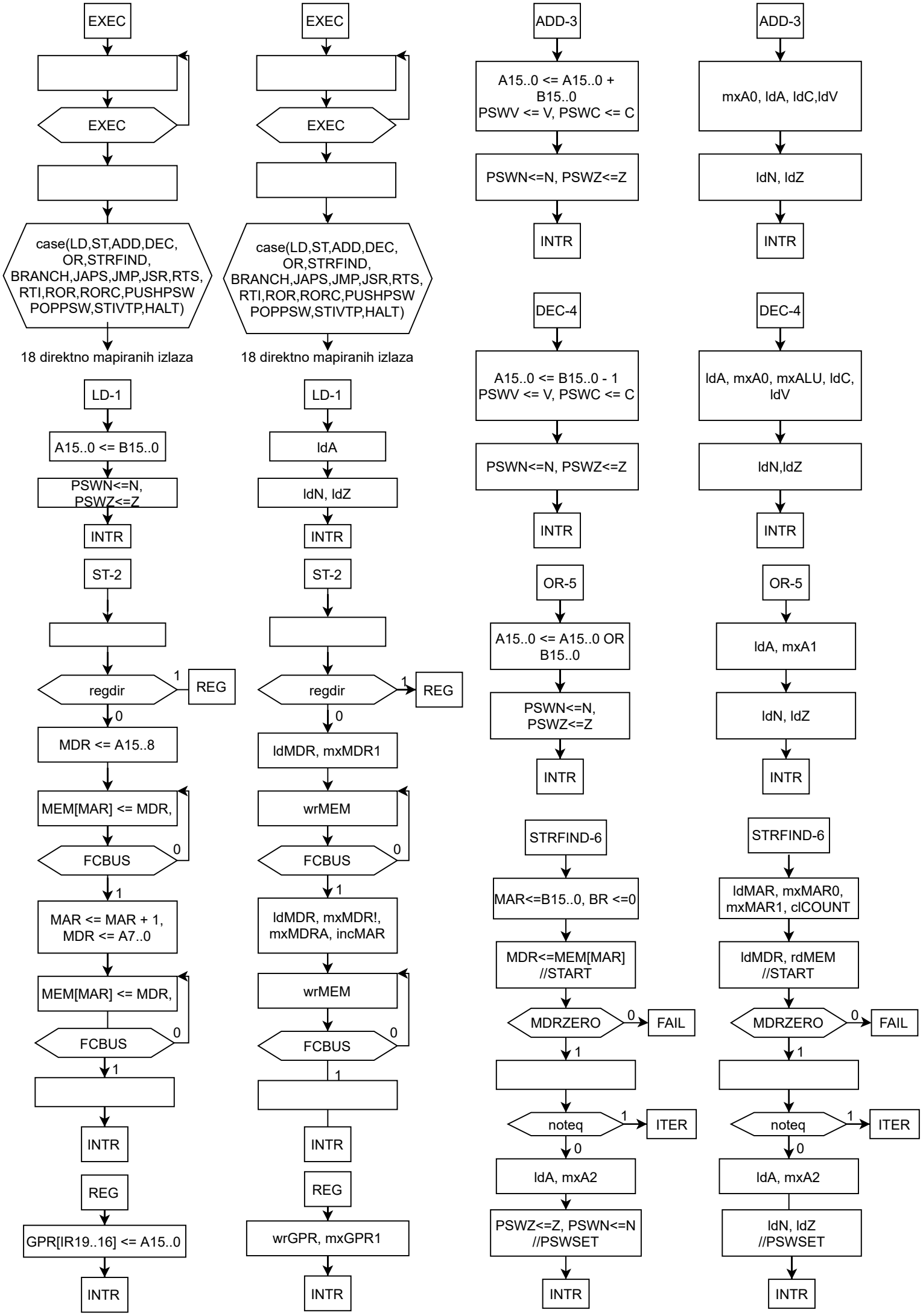
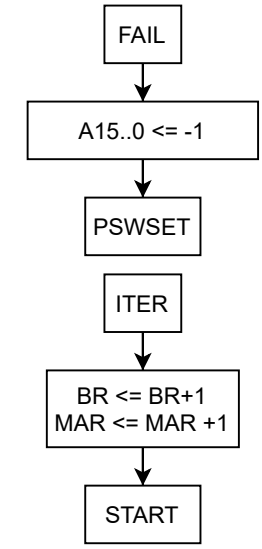
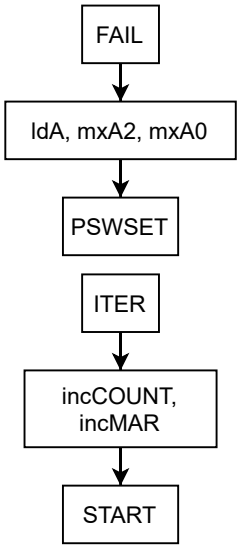
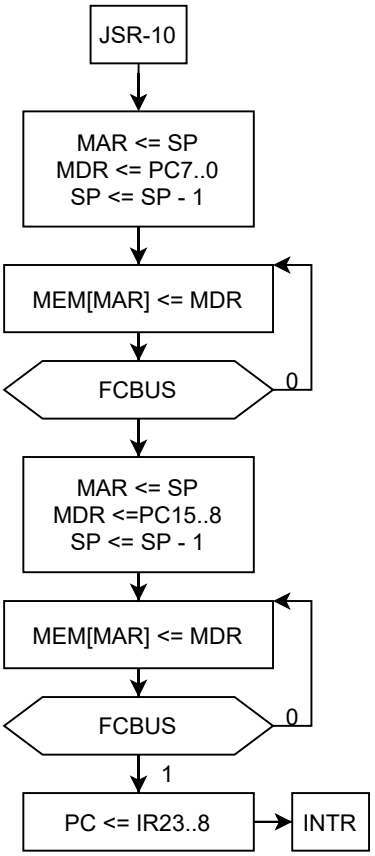
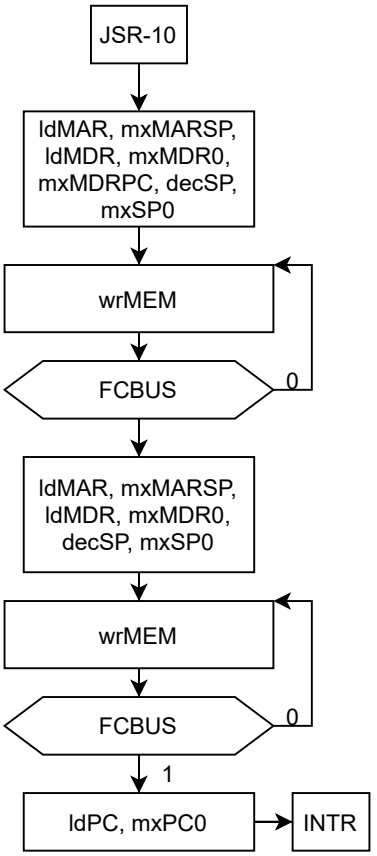
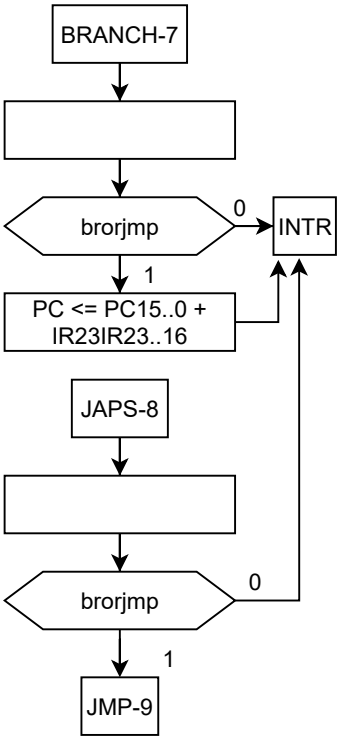

EXEC
EXEC
case(LD,ST,ADD,DEC, OR,STRFIND, BRANCH,JAPS,JMP,JSR,RTS, RTI,ROR,RORC,PUSHPSW POPPSW,STIVTP,HALT)
18 direktno mapiranih izlaza
EXEC
EXEC
case(LD,ST,ADD,DEC, OR,STRFIND, BRANCH,JAPS,JMP,JSR,RTS, RTI,ROR,RORC,PUSHPSW POPPSW,STIVTP,HALT)
18 direktno mapiranih izlaza
ADD-3
A15..0 <= A15..0 + B15..0 PSWV <= V, PSWC <= C
PSWN<=N, PSWZ<=Z
INTR
ADD-3
mxA0, ldA, ldC,ldV
ldN, ldZ
INTR
DEC-4
A15..0 <= B15..0 - 1 PSWV <= V, PSWC <= C
PSWN<=N, PSWZ<=Z
INTR
DEC-4
ldA, mxA0, mxALU, ldC, ldV
ldN,ldZ
INTR
OR-5
A15..0 <= A15..0 OR B15..0
PSWN<=N, PSWZ<=Z
INTR
OR-5
ldA, mxA1
ldN, ldZ
INTR
STRFIND-6
MAR<=B15..0, BR <=0
MDR<=MEM[MAR] //START
MDRZERO
0
FAIL
1
noteq
1
ITER
0
ldA, mxA2
PSWZ<=Z, PSWN<=N //PSWSET
INTR
STRFIND-6
ldMAR, mxMAR0, mxMAR1, clCOUNT
ldMDR, rdMEM //START
MDRZERO
0
FAIL
1
noteq
1
ITER
0
ldA, mxA2
ldN, ldZ //PSWSET
INTR
LD-1
A15..0 <= B15..0
PSWN<=N, PSWZ<=Z
INTR
ST-2
regdir
1
REG
0
MDR <= A15..8
MEM[MAR] <= MDR,
FCBUS
0
1
MAR <= MAR + 1, MDR <= A7..0
MEM[MAR] <= MDR,
FCBUS
0
1
INTR
REG
GPR[IR19..16] <= A15..0
INTR
LD-1
ldA
ldN, ldZ
INTR
ST-2
regdir
1
REG
0
ldMDR, mxMDR1
wrMEM
FCBUS
0
1
ldMDR, mxMDR!, mxMDRA, incMAR
wrMEM
FCBUS
0
1
INTR
REG
wrGPR, mxGPR1
INTR

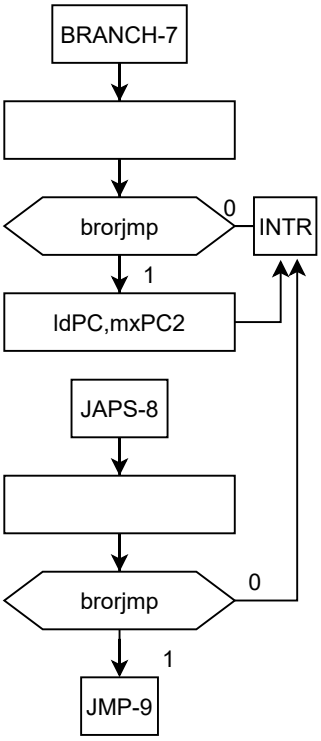

FAIL
A15..0 <= -1
PSWSET
ITER
BR <= BR+1
MAR <= MAR +1
START

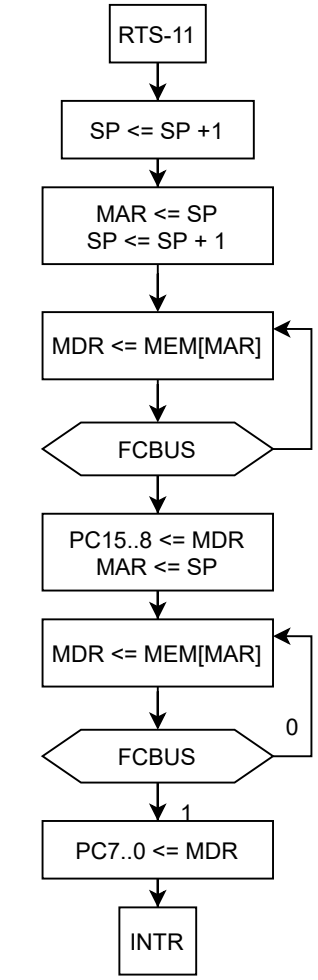

FAIL
ldA, mxA2, mxA0
PSWSET
ITER
incCOUNT,
incMAR
START

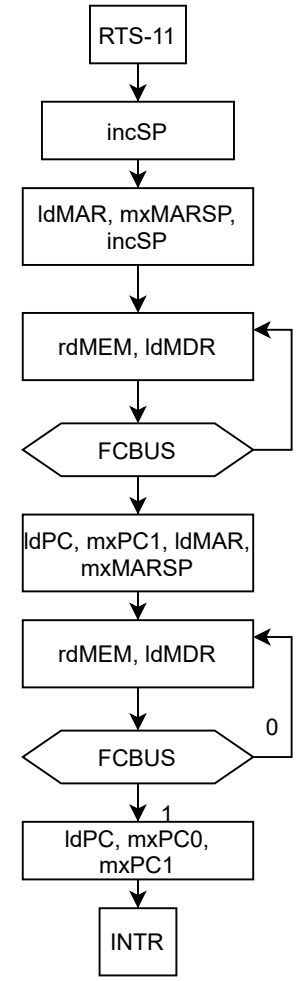

JSR-10
MAR <= SP
MDR <= PC7..0
SP <= SP - 1
MEM[MAR] <= MDR
FCBUS
0
MAR <= SP
MDR <=PC15..8
SP <= SP - 1
MEM[MAR] <= MDR
FCBUS
0
1
PC <= IR23..8
INTR

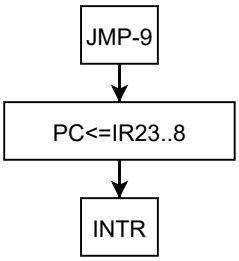

JSR-10
ldMAR, mxMARSP,
ldMDR, mxMDR0,
mxMDRPC, decSP,
mxSP0
wrMEM
FCBUS
0
ldMAR, mxMARSP,
ldMDR, mxMDR0,
decSP, mxSP0
wrMEM
FCBUS
0
1
ldPC, mxPC0
INTR

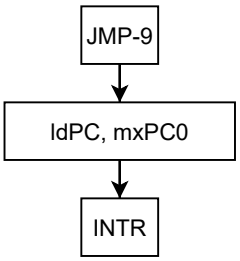

BRANCH-7
brorjmp
0
INTR
1
PC <= PC15..0 +
IR23IR23..16
JAPS-8
brorjmp
0
1
JMP-9

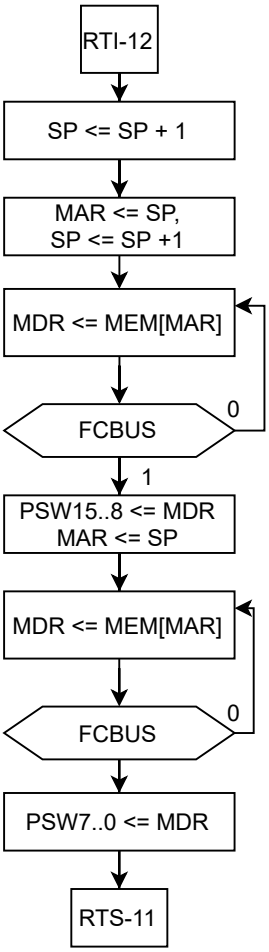

BRANCH-7
brorjmp
0
INTR
1
ldPC,mxPC2
JAPS-8
brorjmp
0
1
JMP-9

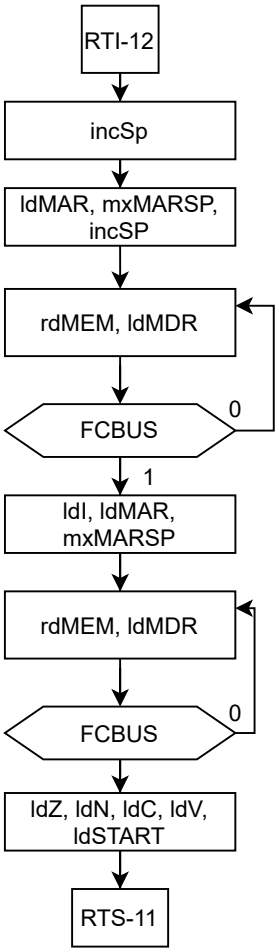

RTS-11
SP <= SP +1
MAR <= SP
SP <= SP + 1
MDR <= MEM[MAR]
FCBUS
PC15..8 <= MDR
MAR <= SP
MDR <= MEM[MAR]
FCBUS
0
1
PC7..0 <= MDR
INTR

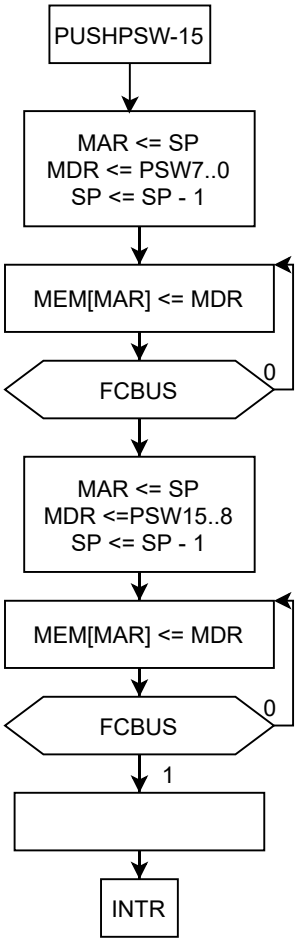

RTS-11
incSP
ldMAR, mxMARSP,
incSP
rdMEM, ldMDR
FCBUS
ldPC, mxPC1, ldMAR,
mxMARSP
rdMEM, ldMDR
FCBUS
0
1
ldPC, mxPC0,
mxPC1
INTR

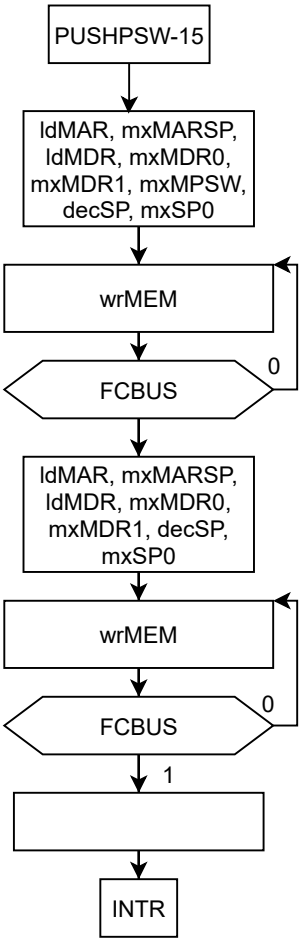

JMP-9
PC<=IR23..8
INTR

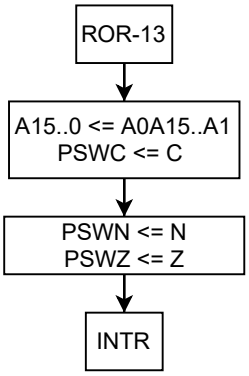

JMP-9
ldPC, mxPC0
INTR

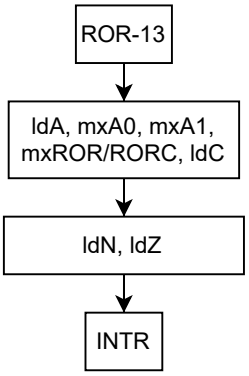

RTI-12
SP <= SP + 1
MAR <= SP,
SP <= SP +1
MDR <= MEM[MAR]
FCBUS
0
1
PSW15..8 <= MDR
MAR <= SP
MDR <= MEM[MAR]
FCBUS
0
PSW7..0 <= MDR
RTS-11

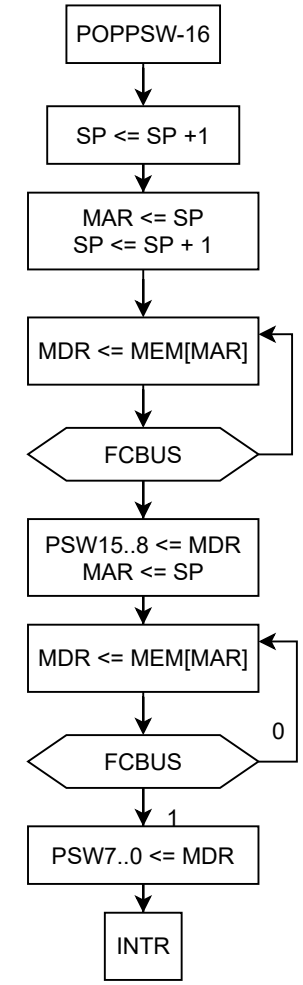

RTI-12
incSp
ldMAR, mxMARSP,
incSP
rdMEM, ldMDR
FCBUS
0
1
ldI, ldMAR,
mxMARSP
rdMEM, ldMDR
FCBUS
0
ldZ, ldN, ldC, ldV,
ldSTART
RTS-11

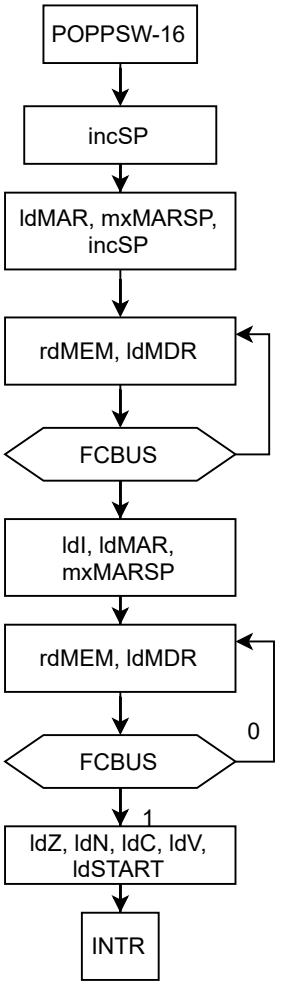

PUSHPSW-15
MAR <= SP
MDR <= PSW7..0
SP <= SP - 1
MEM[MAR] <= MDR
FCBUS
0
MAR <= SP
MDR <=PSW15..8
SP <= SP - 1
MEM[MAR] <= MDR
FCBUS
0
1
INTR

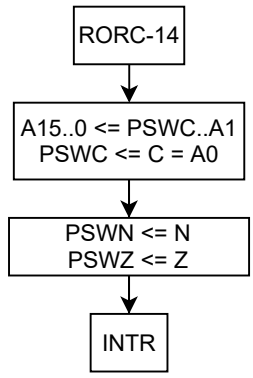

PUSHPSW-15
ldMAR, mxMARSP,
ldMDR, mxMDR0,
mxMDR1, mxMPSW,
decSP, mxSP0
wrMEM
FCBUS
0
ldMAR, mxMARSP,
ldMDR, mxMDR0,
mxMDR1, decSP,
mxSP0
wrMEM
FCBUS
0
1
INTR

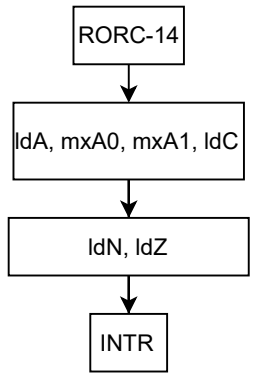

ROR-13
A15..0 <= A0A15..A1
PSWC <= C
PSWN <= N
PSWZ <= Z
INTR

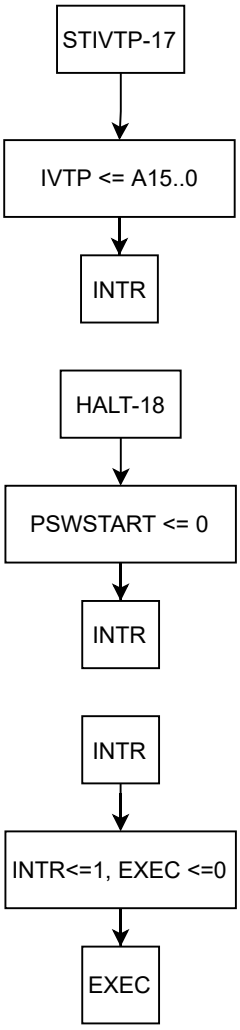

ROR-13
ldA, mxA0, mxA1,
mxROR/RORC, ldC
ldN, ldZ
INTR

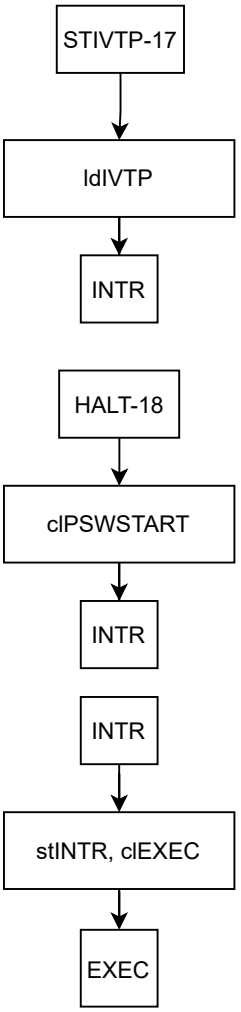

POPPSW-16
SP <= SP +1
MAR <= SP
SP <= SP + 1
MDR <= MEM[MAR]
FCBUS
PSW15..8 <= MDR
MAR <= SP
MDR <= MEM[MAR]
FCBUS
0
1
PSW7..0 <= MDR
INTR


POPPSW-16
incSP
ldMAR, mxMARSP,
incSP
rdMEM, ldMDR
FCBUS
ldI, ldMAR,
mxMARSP
rdMEM, ldMDR
FCBUS
0
1
ldZ, ldN, ldC, ldV,
ldSTART
INTR


RORC-14
A15..0 <= PSWC..A1
PSWC <= C = A0
PSWN <= N
PSWZ <= Z
INTR


RORC-14
ldA, mxA0, mxA1, ldC
ldN, ldZ
INTR


STIVTP-17
IVTP <= A15..0
INTR
HALT-18
PSWSTART <= 0
INTR
INTR
INTR<=1, EXEC <=0
EXEC


STIVTP-17
ldIVTP
INTR
HALT-18
clPSWSTART
INTR
INTR
stINTR, clEXEC
EXEC