DP83822 Robust, low power 10/100 Mbps ethernet physical layer transceiver

1 Features

- IEEE 802.3u compliant: 100BASE-FX, 100BASE-TX and 10BASE-Te
- MII / RMII / RGMII MAC interfaces
- Low power single supply options:
  - 1.8-V AVD < 120 mW
  - 3.3-V AVD < 220 mW
- ±16-kV HBM ESD protection
- ±8-kV IEC 61000-4-2 ESD protection
- Start of frame detect for IEEE 1588 time stamp
- Fast link-down timing
- Auto-crossover in force modes
- Operating temperature: –40°C to +125°C
- I/O voltages: 3.3 V, 2.5 V, and 1.8 V
- Power savings features
  - Energy efficient ethernet (EEE) IEEE 802.3az
  - WoL (Wake-on-LAN) support with magic packet detection
  - Programmable energy savings modes
- Cable diagnostics
- BIST (Built-In Self-Test)
- MDC / MDIO interface

2 Applications

- Industrial networks and factory automation
- Motor and motion control
- IP network cameras
- Building automation

3 Description

The DP83822 is a low power single-port 10/100 Mbps Ethernet PHY. It provides all physical layer functions needed to transmit and receive data over both standard twisted-pair cables or connect to an external fiber optic transceiver. Additionally, the DP83822 provides flexibility to connect to a MAC through a standard MII, RMII, or RGMII interface.

The DP83822 offers integrated cable diagnostic tools, built-in self-test, and loopback capabilities for ease of use. It supports multiple industrial buses with its fast link-down timing as well as Auto-MDIX in forced modes.

The DP83822 offers an innovative and robust approach for reducing power consumption through EEE, WoL and other programmable energy savings modes.

The DP83822 is a feature rich and pin-to-pin upgradeable option for the TLK105, TLK106, TLK105L and TLK106L 10/100 Mbps Ethernet PHYs.

The DP83822 comes in a 32-pin 5.00-mm × 5.00-mm VQFN package.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
DP83822HF	VQFN (32)	5.00 mm × 5.00 mm
DP83822H	VQFN (32)	5.00 mm × 5.00 mm
DP83822IF	VQFN (32)	5.00 mm × 5.00 mm
DP83822I	VQFN (32)	5.00 mm × 5.00 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Simplified Schematic

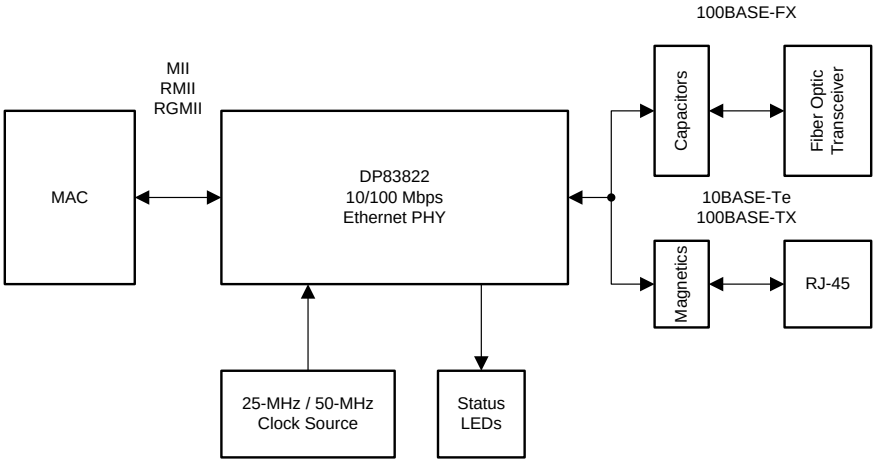


Table of Contents

4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision D (March 2019) to Revision E — **Page**

- Changed to fix typos on Table 1 ... 8

Changes from Revision C (April 2018) to Revision D — **Page**

- Changed the description for LED_1 in Pin Functions table ... 6
- Changed reset pin state for RX_D[3:0] pins in Table 1 ... 8
- Added XO and XI capacitance ... 10
- Added Test Conditions to PMD OUTPUT section of the Electrical Characteristics Table ... 11
- Changed Parameter descriptions and units in Reset Timing Requirements table to match device performance. ... 11
- Changed NOTE for 100BASE-FX Signal Detect pin polarity from Active LOW to Active HIGH. ... 40
- Changed LED_0 strap modes to remove Mode 2 and Mode 3. ... 48
- Changed strap description for SD_EN pin from Active LOW to Active HIGH. ... 48
- Deleted LED_0 configuration table. ... 49
- Changed LED_1 Configuration table to merge LED_0 and LED_1 configuration into a single table for clarity. ... 49
- Changed note in LED Configuration section to clarify LED connections. ... 50
- Added registers 0x0106, 0x0107, 0x01F, 0x0114, 0x0116, 0x0126, 0x04D4, 0x04D5, and 0x04D6 ... 51

- Changed FUNCTION column of bits 3 and 2 in Table 37 to swap '0' and '1' functionality. 64
- Changed SD_EN=0 to SD_EN=1 in Register 0x465 bit 0 Function 79
- Added 100Base-TX MII power consumption data for -40°C and 125°C 98

Changes from Revision B (March 2018) to Revision C **Page**

- Changed TX_D[1:0] back to TX_D[3:0] 29
- Changed RX_D[1:0] back to RX_D[3:0] 29

Changes from Revision A (August 2016) to Revision B **Page**

- Updated data sheet text and format to the latest TI documentation and translations standards 1
- Updated description of pin 24 and changed pin type from: I/O, PD to: I/O 6
- Added *MII: 100BASE-TX Transmit Latency Timing* table 14
- Added *MII: 100BASE-TX Receive Latency Timing* table 14
- Device Power-Up Timing diagram modified to include start voltage limits 15
- Added the *100BASE-TX Transmit Latency Timing* graphic 22
- Added the *100BASE-TX Receive Latency Timing* graphic 22
- Changed the *Functional Block Diagram* 25
- Changed TX_D[3:0] to TX_D[1:0] 29
- Changed RX_D[3:0] to RX_D[1:0] 29
- Added note to the *100BASE-FX Receive* section and changed the SD_DIS pin to SD_EN 40
- Changed RX_ER strap function from: AMDIX_EN (SD_DIS) to: AMDIX_EN (SD_EN) 48
- Changed the default and switched 0 and 1 functions for the RMII Recovered Clock Async FIFO Bypass bit in RCSR register (0X0017) 64
- Changed the 0x7D BIST IPG length from: 125 bytes to: 500 bytes 67
- Added 0 and 1 functions for the MLED Polarity Swap bit in the MLEDCR register (0x0025) 68
- Added Line Driver Class Selection (LDCSEL) register 75
- Changed 0x0465 register from: General Configuration to: Fiber General Configuration and switched the Active HIGH and LOW polarities for 1 and 0 79
- Changed the 100Base-FX Signal Detect Polarity bit description note 79
- Changed Pattern Start Point bit default from: 0 to: 01100 87
- Added the *Detailed Design Procedure* section for the TPI Network Circuit typical application 92
- Added note to the *Oscillator* section 94
- Changed the *Power Connections* graphic 97

Changes from Original (August 2016) to Revision A **Page**

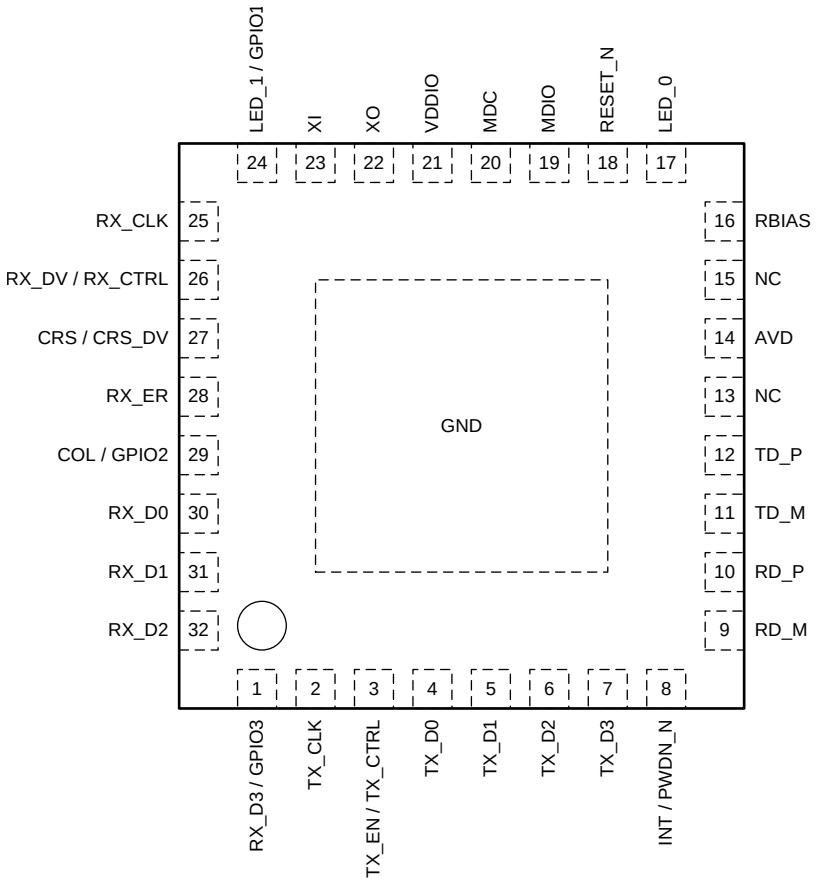
- Changed Product Preview to Production Data release 1

5 Device Comparison Table

PART NUMBER	100BASE-FX SUPPORT	OPERATING TEMPERATURE
DP83822HF	Yes	-40°C to 125°C
DP83822H	No	-40°C to 125°C
DP83822IF	Yes	-40°C to 85°C
DP83822I	No	-40°C to 85°C

6 Pin Configuration and Functions

RHB Package
32-Pin VQFN
Top View



Pin Functions

PIN		TYPE(1)	DESCRIPTION
NAME	NO.		
MAC INTERFACE			
TX_CLK	2	O, Hi-Z	**MII Transmit Clock:** MII Transmit Clock provides a 25-MHz reference clock for 100-Mbps speed and a 2.5-MHz reference clock for 10-Mbps speed. Note that in MII mode, this clock has constant phase referenced to the reference clock. Applications requiring such constant phase may use this feature.
		Hi-Z	**Unused in RMII Mode**
		I, PD	**RGMII Transmit Clock:** The clock is sourced from the MAC layer to the PHY. When operating at 100-Mbps speed, this clock must be 25-MHz. When operating at 10-Mbps speed, this clock must be 2.5-MHz.
TX_EN / TX_CTRL	3	I, PD	**Transmit Enable:** TX_EN is presented on the rising edge of the TX_CLK. TX_EN indicates the presence of valid data inputs on TX_D[3:0] in MII mode and on TX_D[1:0] in RMII mode. TX_EN is an active high signal. **RGMII Transmit Control:** TX_CTRL combines transmit enable and transmit error signals. TX_EN is presented on the rising edge of TX_CLK and TX_ER on the falling edge of TX_CLK.
TX_D0	4	I, PD	**Transmit Data:** In MII mode, the transmit data nibble received from the MAC is synchronous to the rising edge of TX_CLK. In RMII mode, TX_D[1:0] received from the MAC is synchronous to the rising edge of the reference clock. In RGMII mode, the transmit data nibble received from the MAC is synchronous to the rising edge of TX_CLK.
TX_D1	5		
TX_D2	6		
TX_D3	7		
RX_CLK	25	O	**MII Receive Clock:** MII Receive Clock provides a 25-MHz reference clock for 100-Mbps speed and a 2.5-MHz reference clock for 10-Mbps speed, which is derived from the received data stream. **Unused in RMII Mode** **RGMII Receive Clock:**RGMII Receive Clock provides a 25-MHz reference clock for 100-Mbps speed and a 2.5-MHz reference clock for 10-Mbps speed, which is derived from the receive data stream.
RX_DV / RX_CTRL	26	O, S-PD	**Receive Data Valid:** This pin indicates valid data is present on the RX_D[3:0] for MII mode and on RX_D[1:0] in RMII mode, independent from Carrier Sense. **RGMII Receive Control:** RX_CTRL combines receive data valid and receive error signals. RX_DV is presented on the rising edge of RX_CLK and RX_ER on the falling edge of RX_CLK.
RX_ER	28	O, S-PU	**Receive Error:** This pin indicates that an error symbol has been detected within a received packet in both MII and RMII mode. In MII mode, RX_ER is asserted high synchronously to the rising edge of RX_CLK. In RMII mode, RX_ER is asserted high synchronously to the rising edge of the reference clock. This pin is not required to be used by the MAC in MII or RMII because the PHY is corrupting data on a receive error. **Unused in RGMII Mode**
RX_D0	30	O, S-PD	**Receive Data:** Symbols received on the cable are decoded and presented on these pins synchronous to the rising edge of RX_CLK. They contain valid data when RX_DV is asserted. A nibble RX_D[3:0] is received in MII and RGMII modes. 2-bits RX_D[1:0] is received in RMII Mode. PHY address pins PHY_AD[4:1] are multiplexed with RX_D[3:0], and are pulled-down. PHY_AD[0] (LSB of the address) is multiplexed with COL on pin 29, and is pulled up. If no external pullup or pulldown is present, the default PHY address is 0x01.
RX_D1	31		
RX_D2	32		
RX_D3 / GPIO3	1		

(1) The definitions below define the functionality of the I/O cells for each pin.
(a) Type: I - Input
(b) Type: O - Output
(c) Type: I/O - Input/Output
(d) Type OD - Open Drain
(e) Type: PD, PU - Internal Pulldown/Pullup
(f) Type: S-PU, S-PD - Strapping Pin (All strap pins have weak internal pullups or pulldowns. If the default strap value is needed to be changed then an external 2.2-kΩ resistor should be used)

Pin Functions (continued)

PIN		TYPE(1)	DESCRIPTION
NAME	NO.		
CRS / CRS_DV	27	O, S-PU	**Carrier Sense:** In MII mode this pin is asserted high when the receive or transmit medium is non-idle. **Carrier Sense / Receive Data Valid:** In RMII mode, this pin combines the RMII Carrier and Receive Data Valid indications. **Unused in RGMII Mode**
COL / GPIO2	29	I/O, S-PU	**Collision Detect:** For Full-Duplex mode, this pin is always LOW. In Half-Duplex mode, this pin is asserted HIGH only when both transmit and receive media are non-idle. **Unused in RMII Mode**
SERIAL MANAGEMENT INTERFACE			
MDC	20	I	**Management Data Clock:** Synchronous clock to the MDIO serial management input/output data. This clock may be asynchronous to the MAC transmit and receive clocks. The maximum clock rate is 25 MHz. There is no minimum clock rate.
MDIO	19	I/O	**Management Data I/O:** Bidirectional management data signal that may be sourced by the management station or the PHY. This pin requires a 2.2-kΩ pullup resistor.
$\overline{\text{INT/PWDN}}$	8	I/O, OD	**Interrupt / Power Down:** Register access is required for this pin to be configured either as power down or as an interrupt. The default function of this pin is power down. When this pin is configured for a power down function, an active low signal on this pin places the device in power-down mode. When this pin is configured as an interrupt pin, this pin is asserted low when an interrupt condition occurs. The pin has an open-drain output with a weak internal pullup. Some applications may require an external pullup resistor.
$\overline{\text{RESET}}$	18	I, PU	**RESET:** This pin is an active low reset input that initializes or re-initializes all the internal registers of the PHY. Asserting this pin low for at least 1 µs will force a reset process to occur.
CLOCK INTERFACE			
XI	23	I	**Crystal / Oscillator Input** **MII reference clock:** Reference clock 25-MHz ±50 ppm-tolerance crystal or oscillator input. The device supports either an external crystal resonator connected across pins XI and XO, or an external CMOS-level oscillator connected to pin XI only. **RMII reference clock:** Reference clock 50-MHz ±50 ppm-tolerance CMOS-level oscillator in RMII Slave mode. Reference clock 25-MHz ±50 ppm-tolerance crystal or oscillator in RMII Master mode. **RGMII reference clock:**Reference clock 25-MHz ±50 ppm-tolerance crystal or oscillator input. The device supports either an external crystal resonator connected across pins XI and XO, or an external CMOS-level oscillator connected to pin XI only.
XO	22	O	**Crystal Output:** Reference Clock output. XO pin is used for crystal only. This pin should be left floating when a CMOS-level oscillator is connected to XI.
GPIO AND LED INTERFACE			
LED_0	17	O, S-PU	**Mode 1 (Default):** LINK Indication, LED indicates the status of the link. When the link is good, LED is ON. When the link is down, LED is OFF. **Mode 2:** ACT Indication, LED indicates transmit and receive activity in addition to the status of the link. The LED is ON when link is good. The LED blinks when the transmitter or receiver is active.
LED_1 / GPIO1	24	I/O, S-PD	**Mode 1 (Default):** This pin is tri-state. **Mode 2:** SPEED Indication, LED indicates the speed of the link. If speed is 100 Mbps, LED is ON. If speed is 10 Mbps, LED is OFF. External Pull resistors are required when LED is connected to this pin. **GPIO1:** This pin can be used as a GPIO when using register access. **Signal Detect:** This pin acts as Signal Detect in 100BASE-FX mode and shall be connected with Optical Transceiver.

Pin Functions (continued)

PIN		TYPE(1)	DESCRIPTION
NAME	NO.		
COL / GPIO2	29	I/O, S, PU	**MII Mode:** COL pin can be used to drive an LED when operating in Full-Duplex mode. Register access is required for LED configuration. **RMII Mode:** This pin can be used as an LED when using register access. **RGMII Mode:**This pin can be used as an LED when using register access. **GPIO2:** This pin can be used as a GPIO when using register access.
RX_D3 / GPIO3	1	I/O, S-PD	**MII Mode:** RX_D3 will remain as RX_D3 because it is required for MII mode. **RMII Mode:** RX_D3 pin can be configured to drive an LED. Register access is required for LED configuration. **RGMII Mode:**RX_D3 will remain as RX_D3 because it is required for RGMII mode. **GPIO3:** This pin can be used as a GPIO when using register access.
MEDIA DEPENDENT INTERFACE			
TD_M	11	A	**Differential Transmit Output (PMD):** These differential outputs can be automatically configured to either 10BASE-Te, 100BASE-TX, or 100BASE-FX signaling or forced into a specific signaling mode.
TD_P	12		
RD_M	9	A	**Differential Receive Input (PMD):** These differential inputs are automatically configured to accept either 10BASE-Te, 100BASE-TX, or 100BASE-FX signaling or forced into a specific signaling mode.
RD_P	10		
POWER AND GROUND PINS			
VDDIO	21	P	**I/O Supply:** 3.3 V, 2.5 V, or 1.8 V
AVD	14	P	**Analog Supply:** 3.3 V or 1.8 V
GND	Ground Pad	P	**Ground**
RBIAS	16	I	**Bias Resistor Connection**. A 4.87-kΩ ±1% resistor must be connected from RBIAS to GND.
OTHER PINS			
NC	13	NC	**Leave Floating**
NC	15	NC	**Leave Floating**
LED_1 / GPIO1	24	I/O, S-PD	This pin can be left floating when not in used. External Pull resistors are required when LED is connected to this pin.

6.1 IO Pins State During Reset

Table 1. IO Pins State During Reset

PIN NAME	NO.	TYPE	PU/PD/HiZ
MDIO	19	I	Hi-Z
MDC	20	I	PD
INT_N	8	I	PU
RESET_N	18	—	—
TX_CLK	2	O	PD
TX_EN	3	I	PD
TX_D3	7	I	PD
TX_D2	6	I	PD
TX_D1	5	I	PD
TX_D0	4	I	PD
LED_0	17	Strap	PU
LED_1	24	Strap	PD/HiZ (1)
CRS	27	Strap	PU
COL	29	Strap	PU
RX_ER	28	Strap	PU
RX_DV	26	Strap	PD
RX_D3	1	Strap	PD
RX_D2	32	Strap	PD
RX_D1	21	Strap	PD
RX_D0	30	Strap	PD
RX_CLK	25	O	PD

(1) Pull-down present only during power-up. For any subsequent reset pin is HiZ.

7 Specifications

7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

			MIN	MAX	UNIT
	Input voltage	AVD	–0.3	3.8	V
		VDDIO	–0.3	3.8	
		TD–, TD+, RD–, RD+	–0.3	6	
		Other Inputs	–0.3	3.8	
	DC output voltage	All pins	–0.3	3.8	V
T_J	Operating junction temperature			135	°C
T_{stg}	Storage temperature		–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

7.2 ESD Ratings

				VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	All pins except pins 9, 10, 11, and 12	±3000	V
			Pins 9, 10, 11, and 12	±16000	
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	All pins	±1500	
		IEC 61000-4-2(3)	Pins 9, 10, 11, and 12	±8000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.
(3) IEC61000-4-2; 150 pF and 330 Ω, Contact Discharge, Class B.

7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
VDDIO	Supply Voltage I/O (1.8-V Option)	1.71	1.8	1.89	V
	Supply Voltage I/O (2.5-V Option)	2.375	2.5	2.625	
	Supply Voltage I/O (3.3-V Option)	3.15	3.3	3.45	
AVD(1)	Supply Voltage Analog (3.3-V Option)	3.15	3.3	3.45	V
	Supply Voltage Analog (1.8-V Option)	1.71	1.8	1.89	
Center Tap (CT)(1)	Supply Voltage Center Tap (3.3-V Option) *Magnetic Center Tap*	3.15	3.3	3.45	V
	Supply Voltage Analog (1.8V Option) *Magnetic Center Tap*	1.71	1.8	1.89	
T_A	Ambient Temperature: DP83822I and DP83822IF	-40		85	°C
	Ambient Temperature: DP83822H and DP83822HF	-40		125	

(1) Analog supply (AVD) and magnetic center tap must be at the same potential.

7.4 Thermal Information

THERMAL METRIC[1]		DP83822 RHB (VQFN) 32 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	41.0	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	35.5	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	14.1	°C/W
ψ_{JT}	Junction-to-top characterization parameter	0.9	°C/W
ψ_{JB}	Junction-to-board characterization parameter	14.0	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	5.4	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

7.5 Electrical Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
3.3-V VDDIO						
V_{OH}	High level output voltage	I_{OH} = –4 mA VDDIO = 3.3-V ±5%	2.4			V
V_{OL}	low level output voltage	I_{OL} = 4 mA VDDIO = 3.3-V ±5%			0.4	V
V_{IH}	High level input voltage	VDDIO = 3.3-V ±5%	1.7			V
V_{IL}	Low level input voltage	VDDIO = 3.3-V ±5%			0.8	V
2.5-V VDDIO						
V_{OH}	High level output voltage	I_{OH} = –4 mA VDDIO = 2.5-V ±5%	VDDIO × 0.8			V
V_{OL}	Low level output voltage	I_{OL} = 4 mA VDDIO = 2.5-V ±5%			0.4	V
V_{IH}	High level input voltage	VDDIO = 2.5-V ±5%	1.5			V
V_{IL}	Low level input voltage	VDDIO = 2.5-V ±5%			0.7	V
1.8-V VDDIO						
V_{OH}	High level output voltage	I_{OH} = –2 mA VDDIO = 1.8-V ±5%	VDDIO – 0.4			V
V_{OL}	Low level output voltage	I_{OL} = 2 mA VDDIO = 1.8-V ±5%			0.4	V
V_{IH}	High level input voltage	VDDIO = 1.8-V ±5%	1.3			V
V_{IL}	Low level input voltage	VDDIO = 1.8-V ±5%			0.5	V
DC CHARACTERISTICS						
I_{IH}	Input high current (VIN = VCC)	–40°C to 85°C	–10		10	µA
		85°C to 125°C	–20		20	
I_{IL}	Input low current (VIN = GND)	–40°C to 125°C	–10		10	µA
I_{OZ}	TRI-STATE output current (VOUT = VCC, VOUT = GND)	-40°C to 85°C	–10		10	µA
		85°C to 125°C	–20		20	
$C_{XI/XO}$	XO and XI capacitance[1]			0.8		pF
C_{IN}	Input capacitance[1]			5		pF
C_{OUT}	Output capacitance[1]			5		pF
R_{PU-POR}	Integrated pullup resistance during latch-in (RESET and Power-Up)	Pins: RX_ER, LED_0, CRS, and COL	37.5	50	62.5	kΩ
$R_{Pull-Up}$	Integrated pullup resistance		6.75	9	11.25	kΩ

(1) Ensured by production test, characterization or design.

Electrical Characteristics (continued)

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$R_{Pull-Down}$	Integrated pulldown resistance		6.75	9	11.25	kΩ
PMD OUTPUTS						
V_{OD}	MDI 10BASE-Te	VOD can be controlled through Table 74	1.54	1.75	1.96	Vpeak
V_{OD}	MDI 100BASE-TX	VOD can be controlled through Table 74	0.95	1	1.05	Vpeak
V_{ODsym}	MDI 100BASE-TX voltage symmetry		98%	100%	102%	
V_{OD}	MDI 100BASE-FX(1)		0.3	0.5	0.9	Vpeak

7.6 Timing Requirements, Power-Up Timing

See (1)(2).

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
T1	AVD (analog supply) ramp delay post VDDIO (digital supply) ramp. AVD and VDDIO potential must not exceed 0.3 V prior to supply ramp.	Time from start of supply ramp	–100		100	ms
	VDDIO ramp time				100	ms
	AVD ramp time				100	ms
T2	Post power-up stabilization time prior to MDC preamble for register accesses	MDIO is pulled high for 32-bit serial management initialization			200	ms
T3	Hardware configuration latch-in time for power up			200		ms
T4	Hardware configuration pins transition to output drivers			64		ns
T5	Fast Link Pulse transmission delay post power up			1.5		s

(1) Ensured by production test, characterization or design.
(2) See Figure 1.

7.7 Timing Requirements, Reset Timing

See (1)(2).

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
T1	RESET pulse width	X1 clock must be stable for a minimum of 1 μs during RESET pulse low time	10			μs
T2	Post RESET stabilization time prior to MDC preamble for register accesses	MDIO is pulled high for 32-bit serial management initialization			2	ms
T3	Hardware configuration latch-in time for RESET			120		ns
T4	Hardware configuration pins transition to output drivers			64		ns
T5	Fast Link Pulse transmission delay post RESET			1.5		s

(1) Ensured by production test, characterization or design.
(2) See Figure 2.

7.8 Timing Requirements, Serial Management Timing

See (1)(2).

(1) Ensured by production test, characterization or design.
(2) See Figure 3.

Timing Requirements, Serial Management Timing (continued)

See (1)(2).

	PARAMETER	MIN	TYP	MAX	UNIT
T1	MDC to MDIO (Output) Delay Time	0		10	ns
T2	MDIO (Input) to MDC Setup Time	10			ns
T3	MDIO (Input) to MDC Hold Time	10			ns
T4	MDC Frequency		2.5	25	MHz

7.9 Timing Requirements, 100 Mbps MII Transmit Timing

See (1)(2).

	PARAMETER	MIN	TYP	MAX	UNIT
T1	TX_CLK High / Low Time	16	20	24	ns
T2	TX_D[3:0], TX_EN Data Setup to TX_CLK	10			ns
T3	TX_D[3:0], TX_EN Data Hold from TX_CLK	0			ns

(1) Ensured by production test, characterization or design.
(2) See Figure 4.

7.10 Timing Requirements, 100 Mbps MII Receive Timing

See (1)(2).

	PARAMETER	MIN	TYP	MAX	UNIT
T1	RX_CLK High / Low Time	16	20	24	ns
T2	RX_D[3:0], RX_DV and RX_ER Delay from RX_CLK rising	10		30	ns

(1) Ensured by production test, characterization or design.
(2) See Figure 5.

7.11 Timing Requirements, 10 Mbps MII Transmit Timing

See (1)(2).

	PARAMETER	MIN	TYP	MAX	UNIT
T1	TX_CLK High / Low Time	190	200	210	ns
T2	TX_D[3:0], TX_EN Data Setup to TX_CLK	25			ns
T3	TX_D[3:0], TX_EN Data Hold from TX_CLK	0			ns

(1) Ensured by production test, characterization or design.
(2) See Figure 6.

7.12 Timing Requirements, 10 Mbps MII Receive Timing

See (1)(2).

	PARAMETER	MIN	TYP	MAX	UNIT
T1	RX_CLK High / Low Time	160	200	240	ns
T2	RX_D[3:0], RX_DV and RX_ER Delay from RX_CLK rising	100		300	ns

(1) Ensured by production test, characterization or design.
(2) See Figure 7.

7.13 Timing Requirements, RMII Transmit Timing

See (1)(2).

PARAMETER		MIN	TYP	MAX	UNIT
T1	XI Clock Period		20		ns
T2	TX_D[1:0] and TX_EN Data Setup to XI rising	1.4			ns
T3	TX_D[1:0] and TX_EN Data Hold from XI rising	2			ns
T1	RMII Master Clock (RX_D3 Clock) Period		20		ns
	RMII Master Clock (RX_D3 Clock) Duty Cycle	35%		65%	
T2	TX_D[1:0] and TX_EN Data Setup to RMII Master Clock rising	4			ns
T3	TX_D[1:0] and TX_EN Data Hold from RMII Master Clock rising	2			ns

(1) Ensured by production test, characterization or design.
(2) See Figure 8.

7.14 Timing Requirements, RMII Receive Timing

See (1)(2).

PARAMETER		MIN	TYP	MAX	UNIT
T1	XI Clock Period		20		ns
T2	RX_D[1:0], CRS_DV, RX_DV and RX_ER Delay from XI rising	4		14	ns
T1	RX_CLK Clock Period		20		ns
T2	RX_D[1:0], CRS_DV, RX_DV and RX_ER Delay from RX_CLK rising **Note:** While working in 'RMII Receive Clock' mode, bit[0] in register 0x000A	4	10	14	ns
T1	RMII Master Clock (RX_D3 Clock) Period		20		ns
	RMII Master Clock (RX_D3 Clock) Duty Cycle	35%		65%	
T2	RX_D[1:0], CRS_DV, RX_DV and RX_ER Delay from RMII Master Clock rising	4	10	14	ns

(1) Ensured by production test, characterization or design.
(2) See Figure 9.

7.15 Timing Requirements, RGMII

See (1)(2).

PARAMETER		MIN	TYP	MAX	UNIT
SkewT	Data to Clock output Skew (at Transmitter)(3)	–500	0		ps
SkewR	Data to Clock input Skew (at Receiver)(3)	1	1.8		ns
SetupT	Data to Clock output Setup (at Transmitter - integrated delay)(4)	1.2	2		ns
HoldT	Data to Clock output Hold (at Transmitter - integrated delay)(4)	1.2	2		ns
SetupR	Data to Clock input Setup (at Receiver - integrated delay)(4)	1	2		ns
HoldR	Data to Clock input Hold (at Receiver - integrated delay)(4)	1	2		ns
Tcyc_10	Clock Cycle Duration 10 Mbps	360	400	440	ns
Tcyc_100	Clock Cycle Duration 100 Mbps	36	40	44	ns
Duty_T	Duty Cycle for 10/100 Mbps(5)	40%	50%	60%	
Tr / Tf	Rise / Fall Time *(20-80%)*			750	ps

(1) Ensured by production test, characterization or design.
(2) See Figure 10 and Figure 11.
(3) When operating without RGMII internal delay, the PCB design requires clocks to be routed such that an additional trace delay of greater than 1.5 ns is added to the associated clock signal.
(4) Device may operate with or without internal delay.
(5) The duty cycle may be stretched or shrunk during speed changes or while transitioning to a received packet's clock domain as long as minimum duty cycle is not violated and stretching occurs for no more than three Tcyc of the lowest speed transitioned between.

7.16 Normal Link Pulse Timing

See (1)(2).

PARAMETER		MIN	TYP	MAX	UNIT
T1	Pulse Period		16		ms
T2	Pulse Width		100		ns

(1) Ensured by production test, characterization or design.
(2) See Figure 12.

7.17 Auto-Negotiation Fast Link Pulse (FLP) Timing

See (1)(2).

PARAMETER		MIN	TYP	MAX	UNIT
T1	Clock Pulse to Clock Pulse Period		125		µs
T2	Clock Pulse to Data Pulse Period		62		µs
T3	Clock / Data Pulse Width		114		ns
T4	FLP Burst to FLP Burst Period		16		ms
T5	FLP Burst Width		2		ms

(1) Ensured by production test, characterization or design.
(2) See Figure 13.

7.18 10BASE-Te Jabber Timing

See (1)(2).

PARAMETER		MIN	TYP	MAX	UNIT
T1	Jabber activation time		100		ms
T2	Jabber deactivation time		500		ms

(1) Ensured by production test, characterization or design.
(2) See Figure 14.

7.19 MII: 100BASE-TX Transmit Latency Timing

See Figure 15.

PARAMETER			MIN	TYP	MAX	UNIT
T1	TX_CLK rising edge with TX_EN asserted to MDI start of /J/ symbol	100 Mbps		48	56	ns

7.20 MII: 100BASE-TX Receive Latency Timing

See Figure 16.

PARAMETER			MIN	TYP	MAX	UNIT
T2	MDI start of /J/ symbol to RX_CLK rising edge with RX_DV asserted	100 Mbps		194	218	ns

7.21 Timing Diagrams

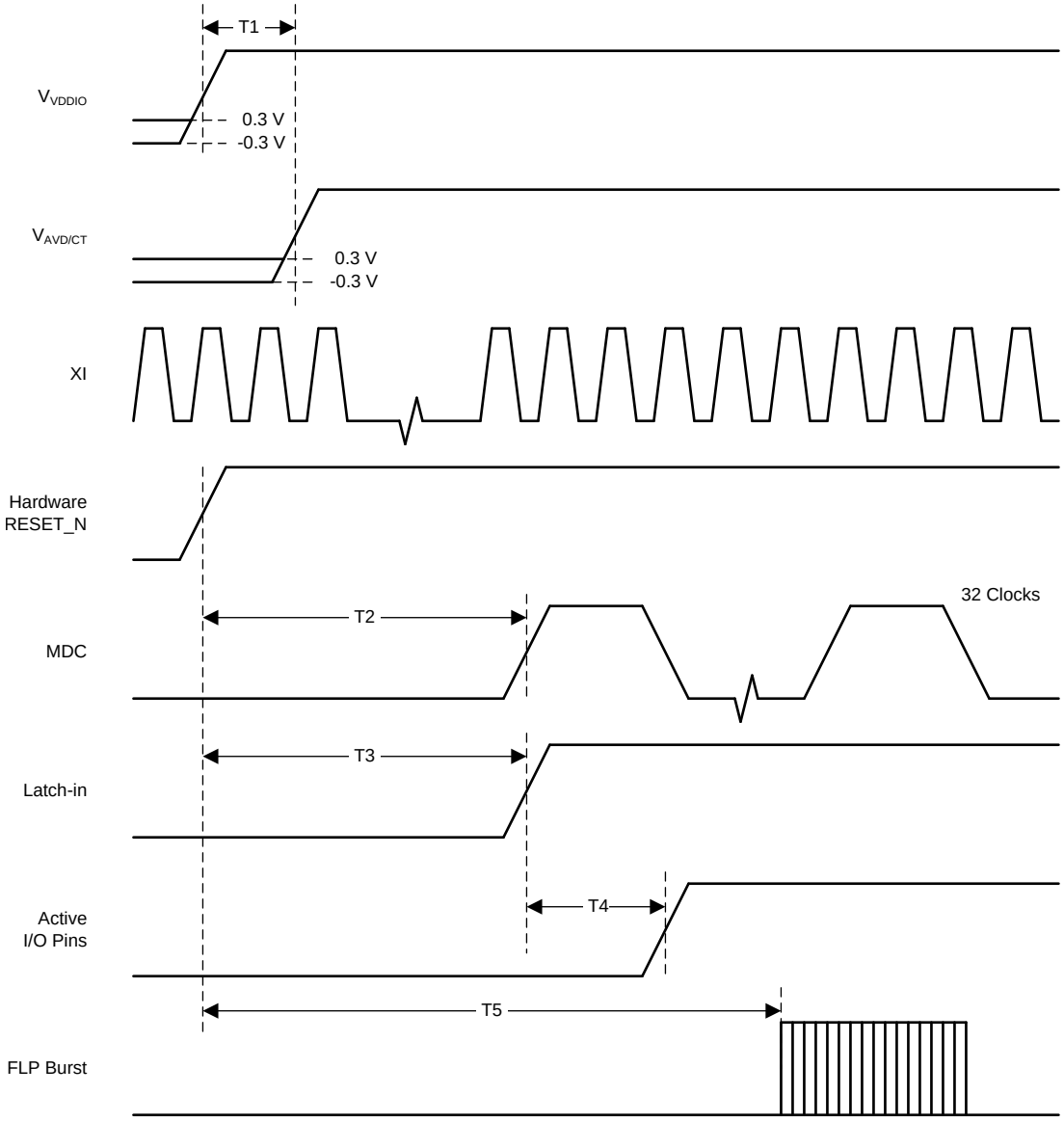


Figure 1. Power-Up Timing

Timing Diagrams (continued)

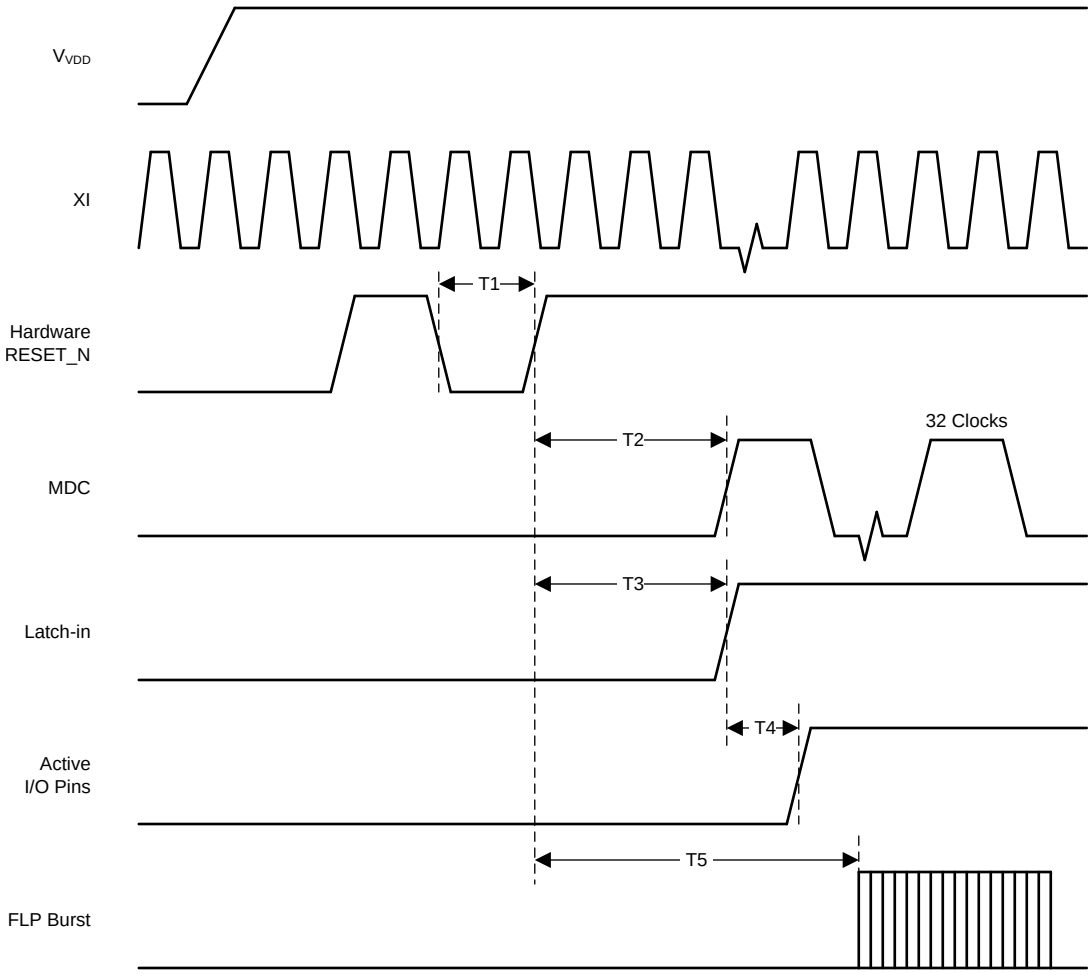


Figure 2. Reset Timing

Timing Diagrams (continued)

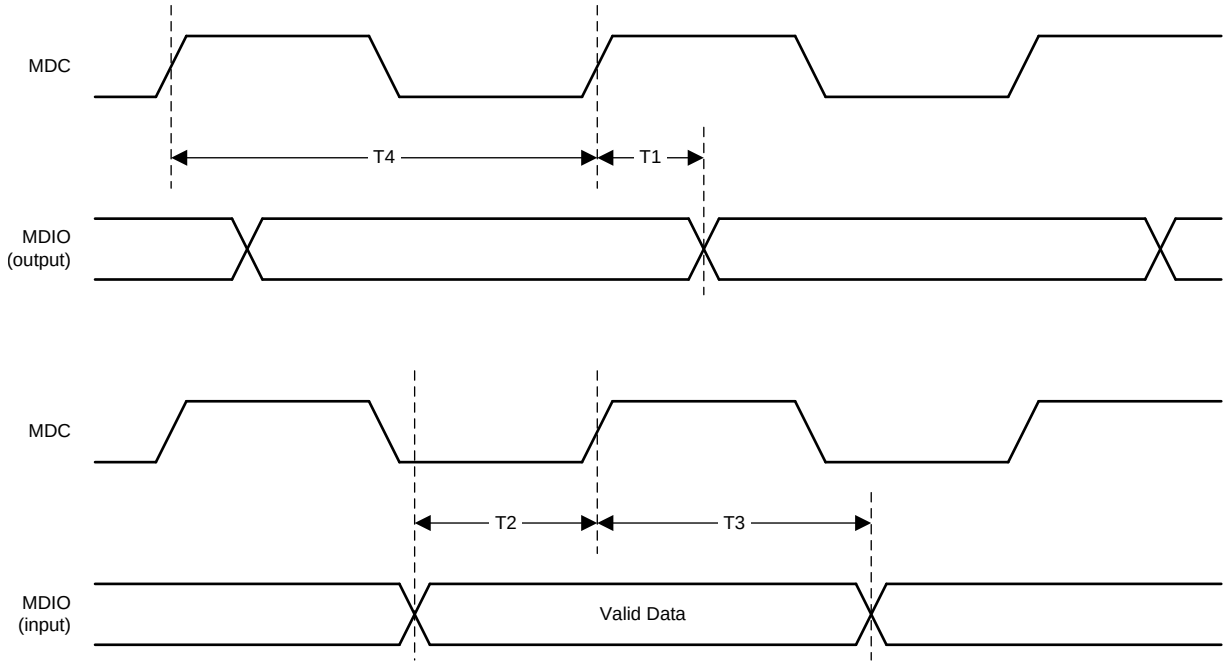


Figure 3. Serial Management Timing

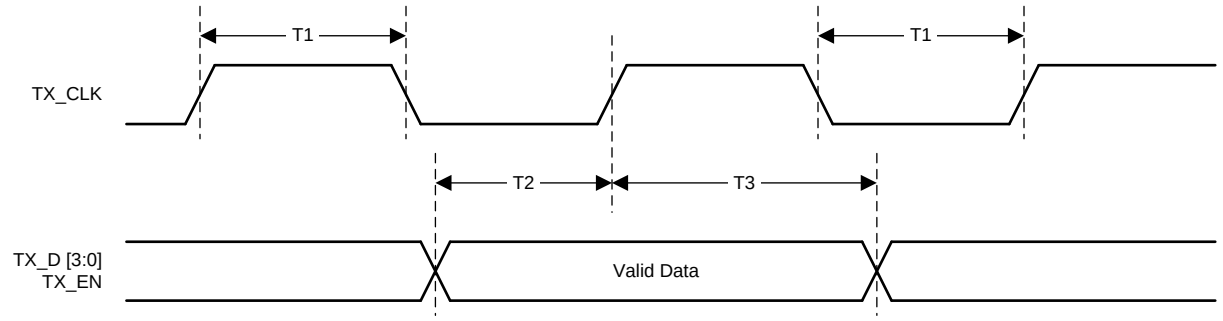


Figure 4. 100-Mbps Transmit Timing

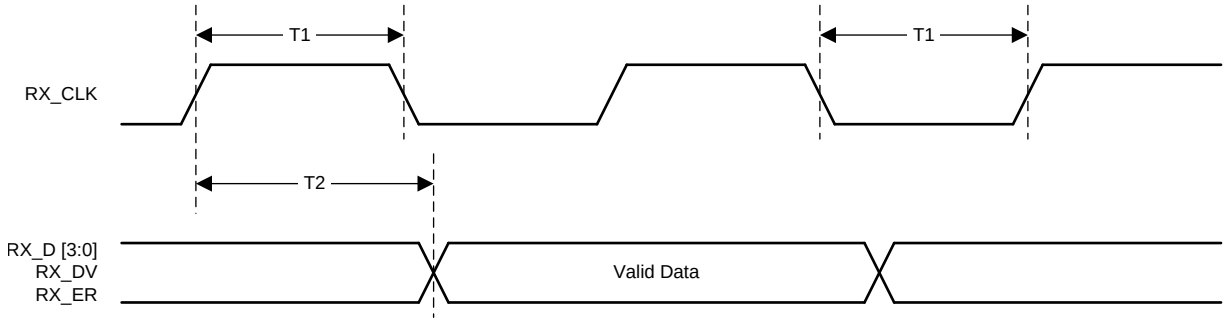


Figure 5. 100-Mbps Receive Timing

Timing Diagrams (continued)

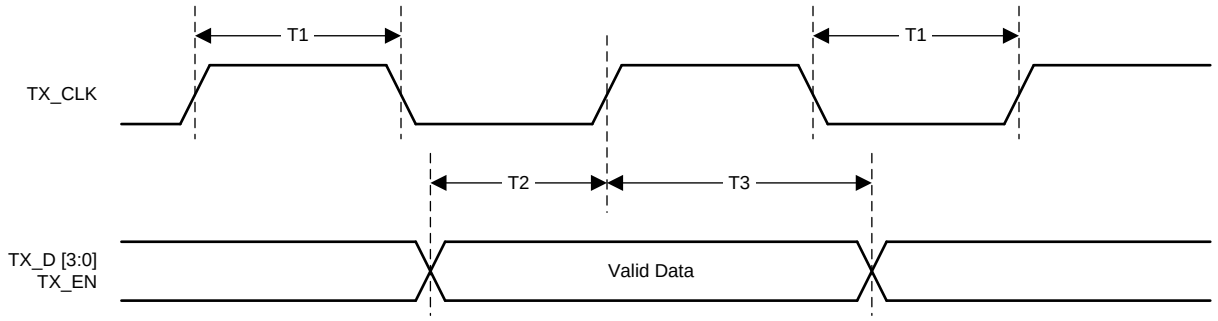


Figure 6. 10-Mbps Transmit Timing

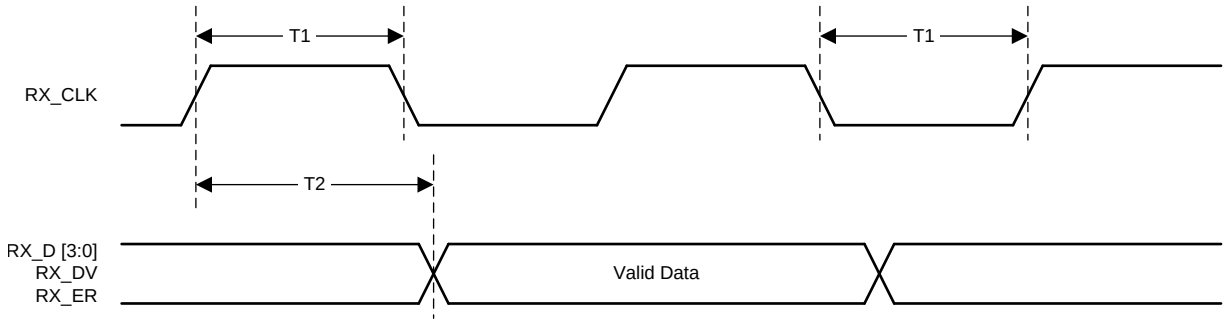


Figure 7. 10-Mbps Receive Timing

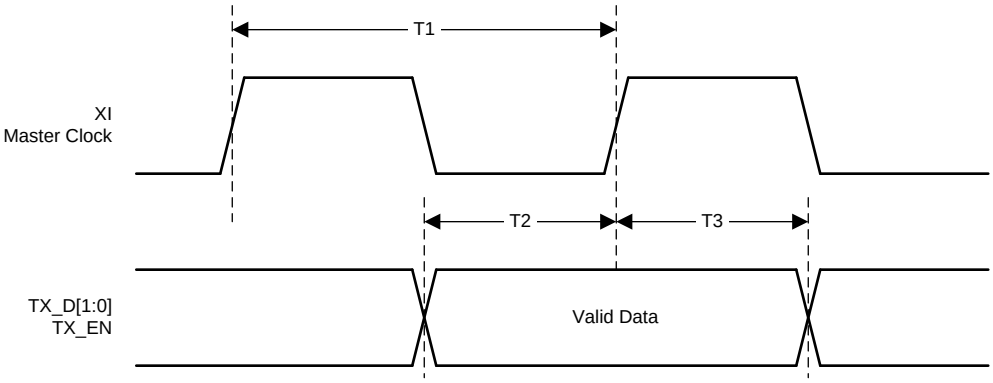


Figure 8. RMII Transmit Timing

Timing Diagrams (continued)

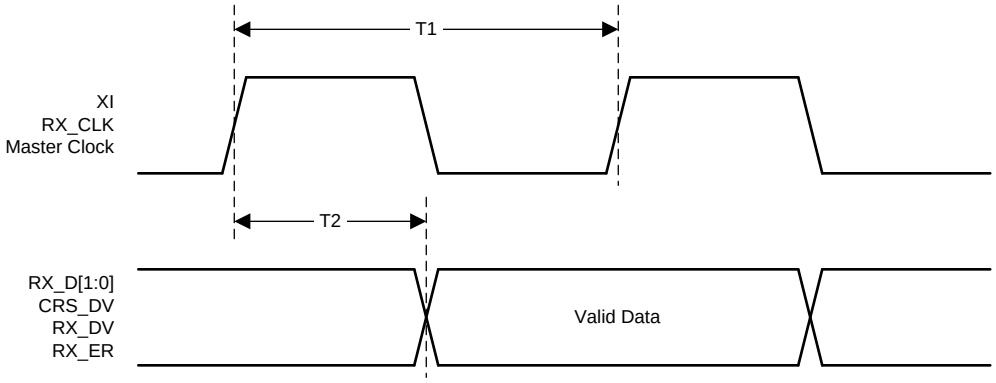


Figure 9. RMII Receive Timing

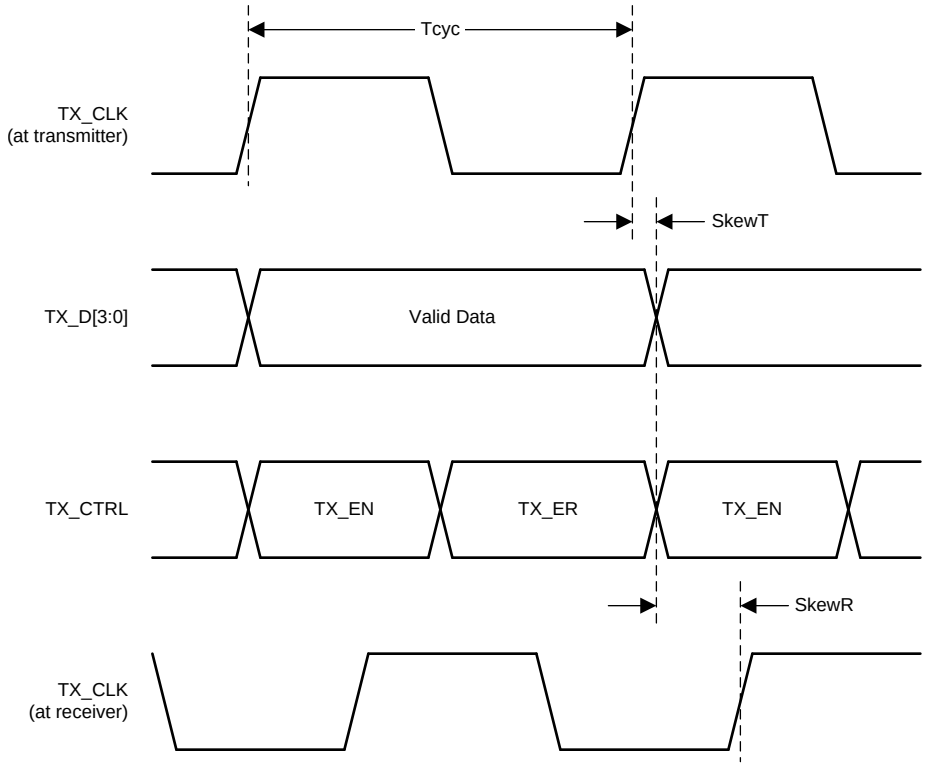


Figure 10. RGMII Transmit Timing

Timing Diagrams (continued)

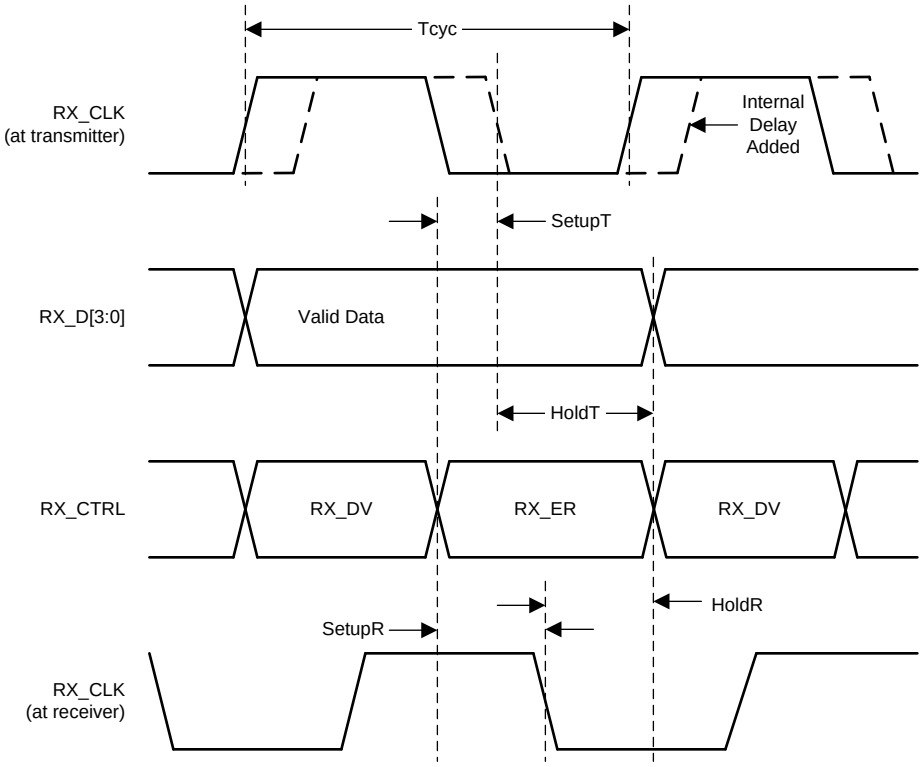


Figure 11. RGMII Receive Timing

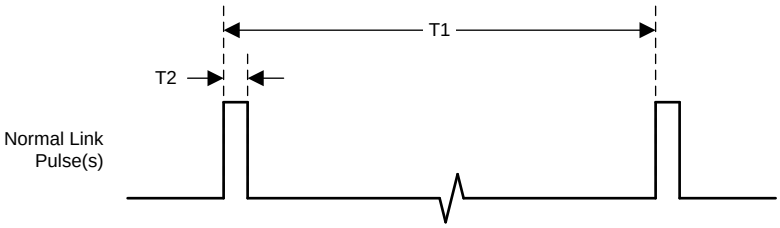


Figure 12. Normal Link Pulse(s) Timing

Timing Diagrams (continued)

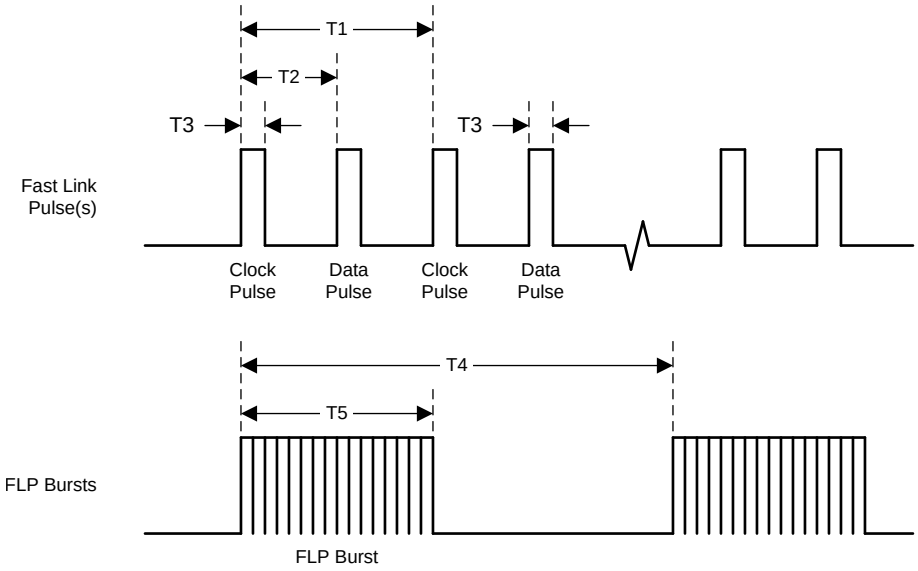


Figure 13. Fast Link Pulse Timing

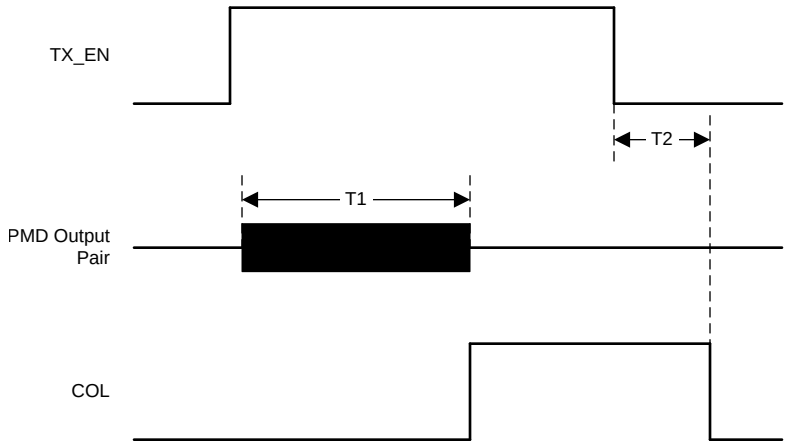


Figure 14. 10BASE-Te Jabber Timing

Timing Diagrams (continued)

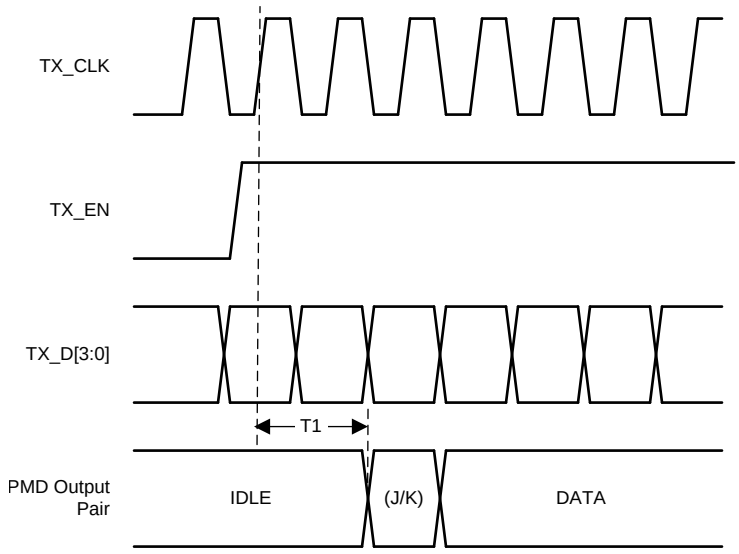


Figure 15. 100BASE-TX Transmit Latency Timing

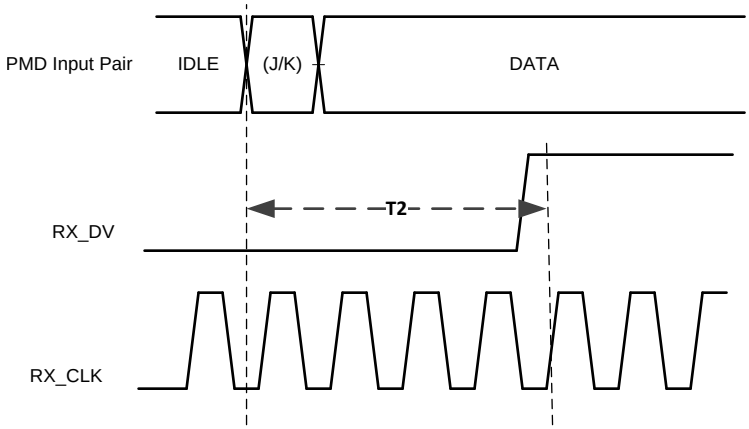
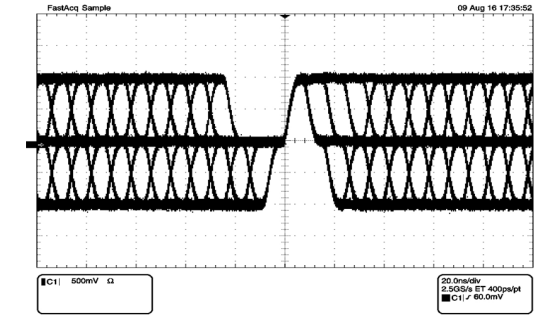


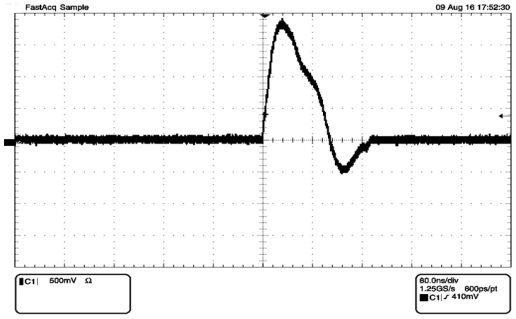
Figure 16. 100BASE-TX Receive Latency Timing

7.22 Typical Characteristics



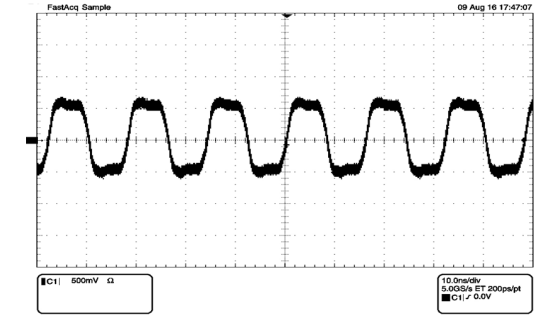
mV per Div	nS per Div
500 mV	20 ns

Figure 17. 100BASE-TX PMD Eye Waveform



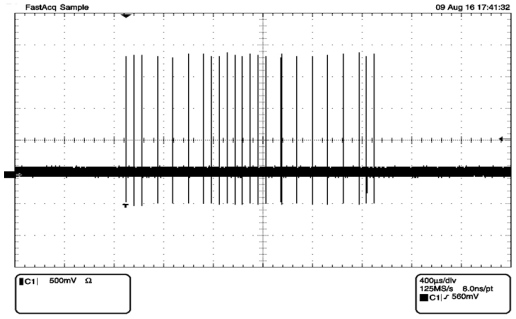
mV per Div	nS per Div
500 mV	80 ns

Figure 18. 10BASE-Te Link Pulse Waveform



mV per Div	nS per Div
500 mV	10 ns

Figure 19. 100BASE-FX Waveform



mV per Div	µS per Div
500 mV	400 µs

Figure 20. Auto-Negotiation Fast Link Pulses Waveform

8 Detailed Description

8.1 Overview

The DP83822 is a fully-featured, single-port Physical Layer transceiver for 10BASE-Te, 100BASE-TX and 100BASE-FX signaling. The device supports the standard Media Independent Interface (MII), Reduced Media Independent Interface (RMII), and Reduced Gigabit Media Independent Interface (RGMII) for direct connection to a Media Access Controller (MAC).

The device is designed for power supply flexibility by allowing for a range of I/O voltage interfaces (3.3 V, 2.5 V, or 1.8 V) and options for analog voltage (1.8 V or 3.3 V) to reduce power consumption. Automatic supply configuration within the DP83822 allows for any combination of VDDIO supply and AVD supply without the need for additional configuration settings. The DP83822 uses mixed-signal processing to perform equalization, data recovery, and error correction to achieve robust operation over CAT5 twisted-pair cable. The DP83822 not only meets the requirements of IEEE 802.3u, but maintains high margins in terms of crosstalk and alien noise.

The DP83822 is also a pin-to-pin upgradeable option for the TLK105, TLK106, TLK105L, and TLK106L 10/100 Mbps Ethernet PHYs.

8.2 Functional Block Diagram

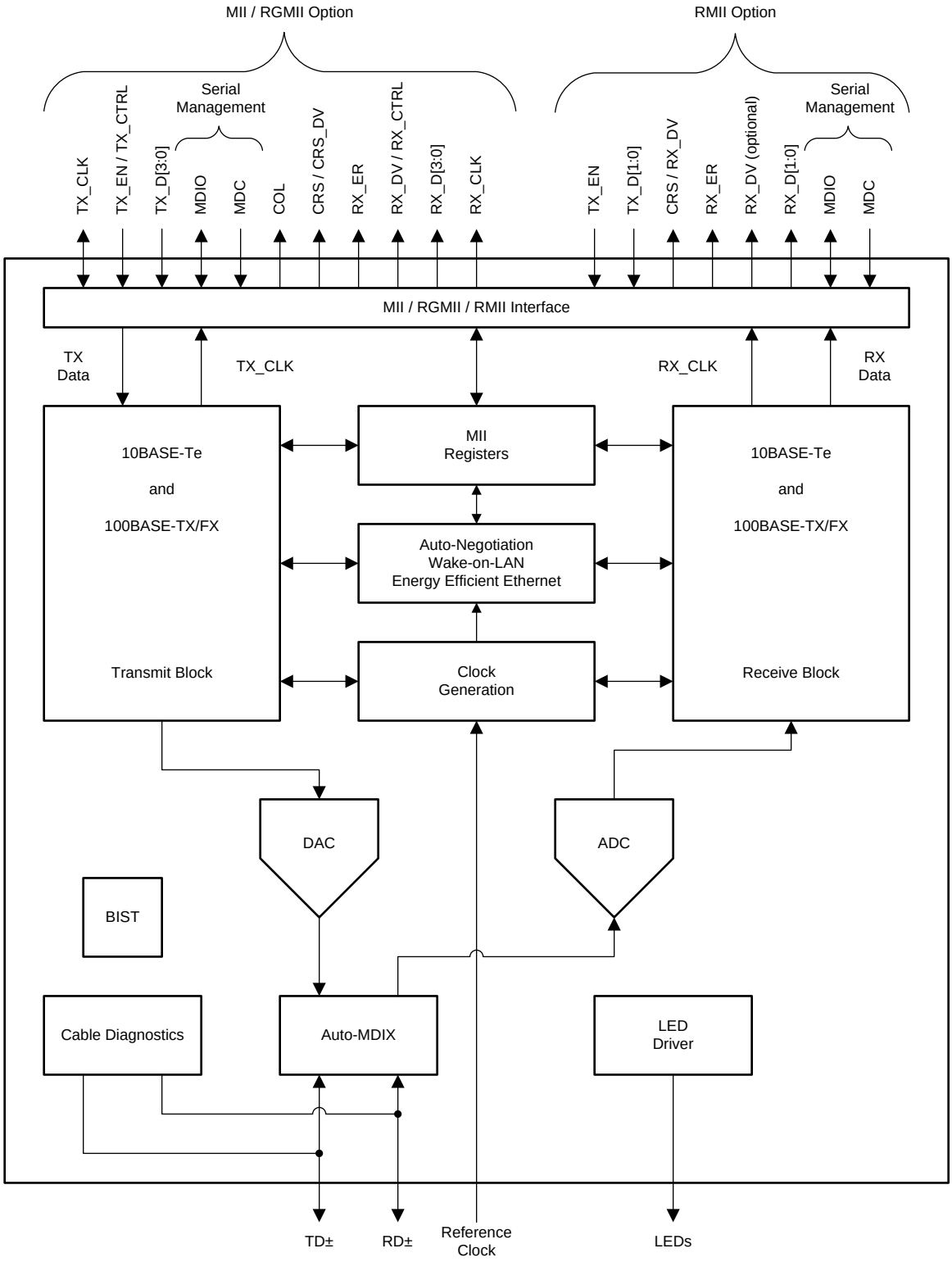


Figure 21. DP83822 Functional Block Diagram

8.3 Feature Description

8.3.1 Energy Efficient Ethernet

8.3.1.1 EEE Overview

Energy Efficient Ethernet (EEE), defined by IEEE 802.3az, is a capability integrated into Layer 1 (Physical Layer) and Layer 2 (Data Link Layer) to operate in Low Power Idle (LPI) mode. In LPI mode, power is saved during periods of low packet utilization. EEE defines the protocol to enter and exit LPI mode without dropping the link or corrupting packets. The transition time into and out of LPI mode is short enough to be transparent to the upper layers within the OSI model.

The DP83822 EEE supports 100 Mbps and 10 Mbps speeds. In 10BASE-Te operation, EEE operates with a reduced transmit amplitude that is fully interoperable with a 10BASE-T PHY.

8.3.1.2 EEE Negotiation

EEE is advertised during Auto-Negotiation. Auto-Negotiation is performed at power up, on management command, after link failure, or due to user intervention. EEE is supported if and only if both link partners advertise EEE capabilities. If EEE is not supported, all EEE functions are disabled and the MAC should not assert LPI. To advertise EEE capabilities, the PHY needs to exchange an additional formatted next page and unformatted next page in sequence.

EEE Negotiation can be activated in two ways:

- Hardware Bootstrapping
- Register Access

EEE Negotiation Advertisements can be activated using RX_D1 pin bootstrap. When RX_D1 is set to strap mode 2 or mode 3, EEE capabilities will be advertised during the Auto-Negotiation process. EEE Negotiation Advertisements can also be activated using regsiter access through the SMI. The DP83822 offers two different ways of accessing EEE control registers within the PHY register set. IEEE 802.3az defines MMD3 and MMD7 as the locations for EEE control and status registers. The MMD3 and MMD7 registers 0x3000, 0x3001, 0x3016, 0x703C, and 0x703D contain all the required controls and status indications for operating EEE. Additionally, the DP83822 supports an EEE configuration bypass option that enables EEE control registers within Texas Instruments' Vendor Specific DEVAD. This helps simplify configuration by allowing for a single DEVAD to be used. The Energy Efficient Ethernet Configuration Register #2 (EEECFG2, address 0x04D0) contains controls for enabling and selecting the pin allocation for TX_ER, which is part of the MAC transmit LPI command. The Energy Efficient Ethernet Configuration Register #3 (EEECFG3, address 0x04D1) contains controls for EEE configuration bypass.

8.3.2 Wake-on-LAN Packet Detection

Wake-on-LAN provides a mechanism to detect specific frames and notify the connected controller through either register status change, GPIO indication or an interrupt flag. The WoL feature within the DP83822 allows for connected devices residing above the Physical Layer to remain in a low power state until frames with the qualifying credentials are detected. Supported WoL frame types include: Magic Packet, Magic Packet with Secure-ON and Custom Pattern Match. When a qualifying WoL frame is received, the DP83822 WoL logic circuit is able to generate a user defined event (either pulses or level change) through any of the GPIO pins or a status interrupt flag to inform a connected controller that a wake event has occurred. Additionally, the DP83822 includes a CRC Gate to prevent invalid packets from triggering a wake-up event.

The Wake-on-LAN feature set includes:

- Identification of WoL frames in all supported speeds (100BASE-FX, 100BASE-TX and 10BASE-Te).
- Wakeup interrupt generation upon reception of a WoL frame.
- CRC error checking of WoL frames to prevent interrupt generation from invalid frames.
- Magic Packets with Secure-ON password and 64-byte Custom Pattern Match for security.

8.3.2.1 Magic Packet Structure

When configured for Magic Packet detection, the DP83822 scans all incoming frames addressed to the node for a specific data sequence. This sequence identifies the frame as a Magic Packet frame.

Feature Description (continued)

A Magic Packet frame must also meet the basic requirements for the LAN technology chosen, such as SOURCE ADDRESS, DESTINATION ADDRESS (which may be the receiving station's IEEE address or a BROADCAST ADDRESS), and CRC.

The specific Magic Packet sequence consists of 16 duplications of the MAC address of this node, with no breaks or interruptions, followed by Secure-ON password if security is enabled. This sequence can be located anywhere within the packet, but must be preceded by a synchronization stream. The synchronization stream is defined as 6-bytes of 0xFF.

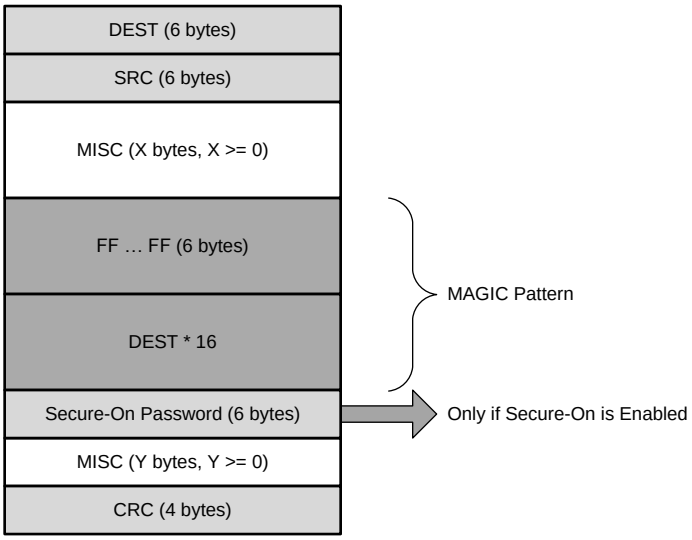


Figure 22. Magic Packet Structure

8.3.2.2 Magic Packet Example

The following is an example Magic Packet for a Destination Address of 11h 22h 33h 44h 55h 66h and a secure-on password 2Ah 2Bh 2Ch 2Dh 2Eh 2Fh:

```
DESTINATION SOURCE MISC FF FF FF FF FF FF
11 22 33 44 55 66 11 22 33 44 55 66 11 22 33 44 55 66
11 22 33 44 55 66 11 22 33 44 55 66 11 22 33 44 55 66
11 22 33 44 55 66 11 22 33 44 55 66 11 22 33 44 55 66
11 22 33 44 55 66 11 22 33 44 55 66 11 22 33 44 55 66
11 22 33 44 55 66 11 22 33 44 55 66 11 22 33 44 55 66
11 22 33 44 55 66 2A 2B 2C 2D 2E 2F MISC CRC
```

8.3.2.3 Wake-on-LAN Configuration and Status

Wake-on-LAN functionality is configured through the Receive Configuration Register (RXFCFG, address 0x04A0). Wake-on-LAN status is reported in the Recieve Status Register (RXFS, address 0x04A1). Wake-on-LAN interrupt flag configuration and status is located in the MII Interrupt Status Register #2 (MISR2, address 0x0013).

Feature Description (continued)

8.3.3 Start of Frame Detect for IEEE 1588 Time Stamp

The DP83822 supports an IEEE 1588 indication pulse at the SFD (start frame delimiter) for receive and transmit paths. The pulse can be delivered to any of the following pins: LED_0, LED_1 (GPIO1), COL (GPIO2), RX_D3 (GPIO3), INT/PWDN_N and CRS. The 1588 Time Stamp pulse indicates the actual time the symbol is presented on the lines (for transmit), or the first symbol received (for receive). The exact timing of the pulse can be adjusted via the IEEE 1588 PTP Configuration Register (PTPCFG, address 0x003F). Each increment of phase value is an 8-ns step.

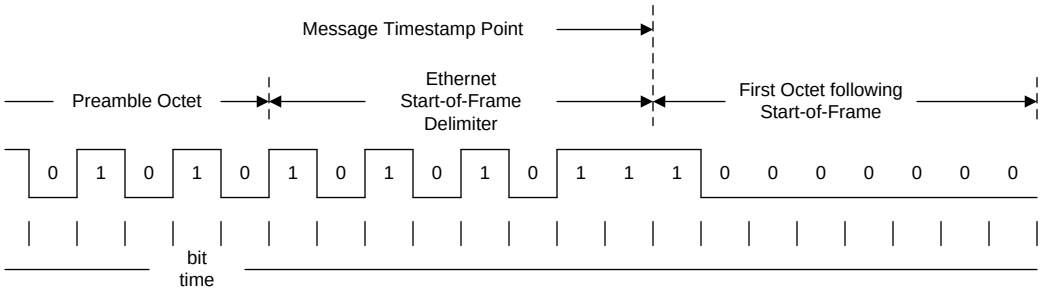


Figure 23. IEEE 1588 Message Timestamp Point

There are three registers that are able to control the routing of the IEEE 1588 transmit and receive indications. The IEEE 1588 PTP Pin Select Register (PTPPSEL, address 0x003E) is able to route both transmit and receive indications to LED_0 (GPIO1), COL (GPIO2), CRS and INT/PWDN_N, which is also found in the TLK105L and TLK106L PHYs. Two additional registers in the DP83822 allow for additional pin selections and a centralized location for GPIO controls through the use of the IO MUX GPIO Control Register #1 and #2 (IOCTRL1 and IOCTRL2, address 0x0462 and address 0x0463).

8.3.4 Clock Output

The DP83822 has several clock configuration options. An external crystal or CMOS-level oscillator provides the stimulus for the internal PHY reference clock. The local reference clock acts as the central source for all clocking within the device, excluding the pass-through clock option.

All clock configuration options are enabled using the DP83822 IO MUX GPIO Control Register #1 and #2 (IOCTRL1 IOCTRL2, address 0x0462 bits[14:12] for RX_D3 (GPIO3), address 0x0462 bits[6:4] for LED_1 (GPIO1), address 0x0463 bits[6:4] for COL (GPIO2)).

Clock options supported by the DP83822 include:

- MAC IF Clock
- XI Clock
- Free-Running Clock
- Recovered Clock

MAC IF Clock will operate at the same rate as the MAC interface selected. For MII operation, MAC IF Clock frequency is 25 MHz. For RMII operation, MAC IF Clock frequency is 50 MHz. For RGMII operation, MAC IF Clock frequency is 25 MHz. XI Clock is a pass-through option, which allows for the XI pin clock to be passed to a GPIO pin. Please note that the clock is buffered prior to transmission out of the GPIOs, and output clock amplitude will be at the selected VDDIO level. Free-Running Clock is an internally generated 125-MHz free-running clock. Recovered Clock is a 125-MHz recovered clock from a connected link partner.

8.4 Device Functional Modes

8.4.1 MAC Interfaces

8.4.1.1 Media Independent Interface (MII)

The Media Independent Interface is a synchronous 4-bit wide nibble data interface that connects the PHY to the MAC in 100BASE-FX, 100BASE-TX and 10BASE-Te modes. The MII is fully compliant with IEEE 802.3-2002 clause 22.

The MII signals are summarized below:

Table 2. MII Signals

FUNCTION	PINS
Data Signals	TX_D[3:0]
	RX_D[3:0]
Transmit and Receive Signals	TX_EN
	RX_DV
Line-Status Signals	CRS
	COL

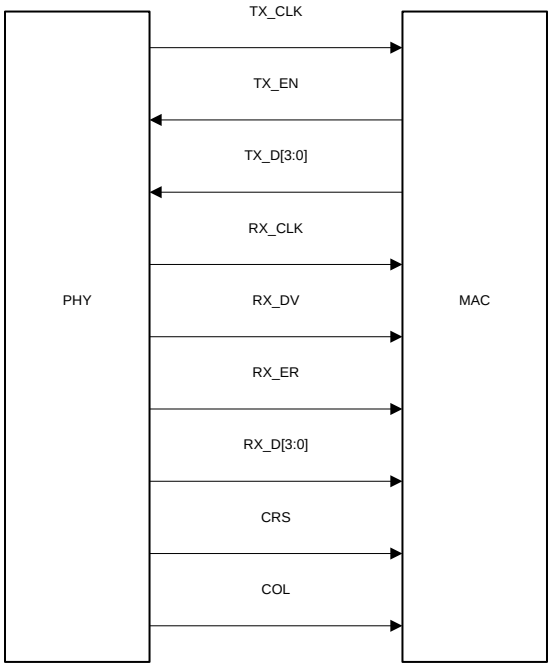


Figure 24. MII Signaling

Additionally, the MII interface includes the carrier sense signal (CRS), as well as a collision detect signal (COL). The CRS signal asserts to indicate the reception or transmission of data. The COL signal asserts as an indication of a collision which can occur during Half-Duplex mode when both transmit and receive operations occur simultaneously.

8.4.1.2 Reduced Media Independent Interface (RMII)

The DP83822 incorporates the Reduced Media Independent Interface (RMII) as specified in the RMII specification from the RMII consortium. The purpose of this interface is to provide a reduced pin count alternative to the IEEE 802.3u MII as specified in Clause 22. Architecturally, the RMII specification provides an additional reconciliation layer on either side of the MII, but can be implemented in the absence of an MII. The DP83822 offers two types of RMII operations: RMII Slave and RMII Master. In RMII Slave operation, the DP83822 operates off of a 50-MHz CMOS-level oscillator connected to the XI pin and shares the same clock as the MAC. In RMII Master operation, the DP83822 operates off of either a 25-MHz CMOS-level oscillator connected to XI pin or a 25-MHz crystal connected across XI and XO pins. A 50-MHz output clock referenced from any of the three DP83822 GPIOs is connected to the MAC.

NOTE

If RMII Master mode is configured through bootstraps, a 50-MHz output clock will automatically be enabled on RX_D3 (GPIO3).

The RMII specification has the following characteristics:

- Supports 100BASE-FX, 100BASE-TX and 10BASE-Te.
- Single clock reference sourced from the MAC to PHY (or from an external source)
- Provides independent 2-bit wide transmit and receive data paths
- Uses CMOS signal levels, the same levels as the MII interface

In this mode, data transfers are two bits for every clock cycle using the internal 50-MHz reference clock for both transmit and receive paths.

The RMII signals are summarized below:

Table 3. RMII Signals

FUNCTION	PINS
Data Signals	TX_D[1:0]
	RX_D[1:0]
Transmit and Receive Signals	TX_EN
	CRS_DV

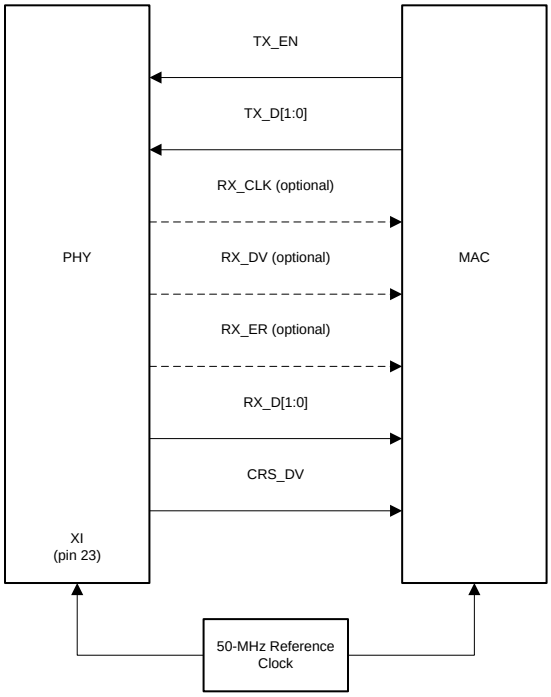


Figure 25. RMII Slave Signaling

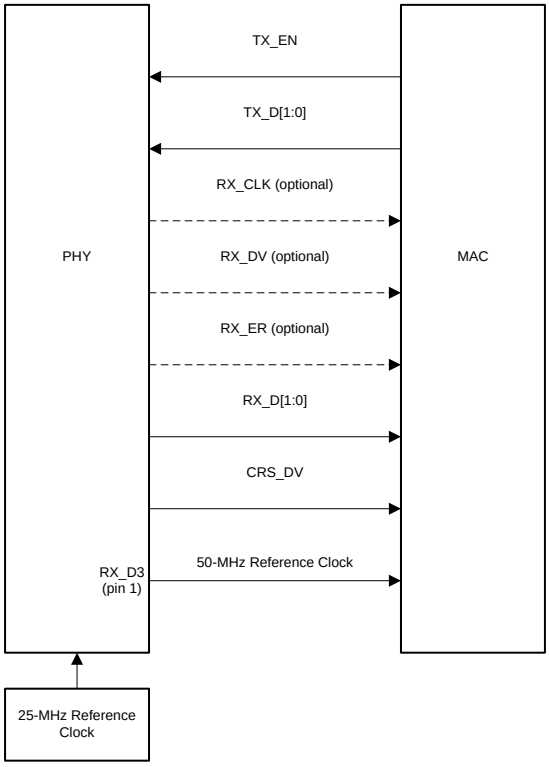


Figure 26. RMII Master Signaling

Data on TX_D[1:0] are latched at the PHY with reference to the clock edges on the XI pin. Data on RX_D[1:0] are latched at the MAC with reference to the same clock edges on the XI pin. RMII operates at the same speed in 10BASE-Te, 100BASE-TX and 100BASE-FX. In 10BASE-Te the data is 10 times slower than the reference clock, so transmit data is sampled every 10 clock cycles. Likewise, receive data is generated on every 10th clock so that an attached MAC device can sample the data every 10 clock cycles.

In addition, RMII mode supplies an RX_DV signal that allows a simpler method of recovering receive data without the need to separate RX_DV from the CRS_DV indication. RX_ER is also supported even though it is not required by the RMII specification.

RMII includes a programmable elastic buffer to adjust for the frequency differences between the reference clock and the recovered receive clock. The programmable elastic buffer minimizes internal propagation delay based on expected maximum packet size and clock accuracy.

Table below indicates how to program the buffer FIFO based on the expected maximum packet size and clock accuracy. It assumes that the RMII reference clock and the far-end transmitter clock have the same accuracy.

Table 4. Recommended RMII Packet Sizes

START THRESHOLD RBR[1:0]	LATENCY TOLERANCE	RECOMMENDED PACKET SIZE AT ±50 ppm	RECOMMENDED PACKET SIZE AT ±100 ppm
1 (4-bits)	2 bits	2400 bytes	1200 bytes
2 (8-bits)	6 bits	7200 bytes	3600 bytes
3 (12-bits)	10 bits	12000 bytes	6000 bytes
4 (16-bits)	14 bits	16800 bytes	8400 bytes

8.4.1.3 Reduced Gigabit Media Independent Interface (RGMII)

The DP83822 also supports Reduced Gigabit Media Independent Interface (RGMII) as specified by RGMII version 2.0. RGMII is designed to reduce the number of pins required to connect the MAC and PHY. To accomplish this goal, the control signals are multiplexed. Both rising and falling edges of the clock are used to sample the control signal pin on the transmit and receive paths. For 10-Mbps operation, RX_CLK and TX_CLK operate at 2.5 MHz. For 100-Mbps operation, RX_CLK and TX_CLK operate at 25 MHz.

The RGMII signals are summarized below:

Table 5. RGMII Signals

FUNCTION	PINS
Data Signals	TX_D[3:0]
	RX_D[3:0]
Transmit and Receive Signals	TX_CTRL
	RX_CTRL

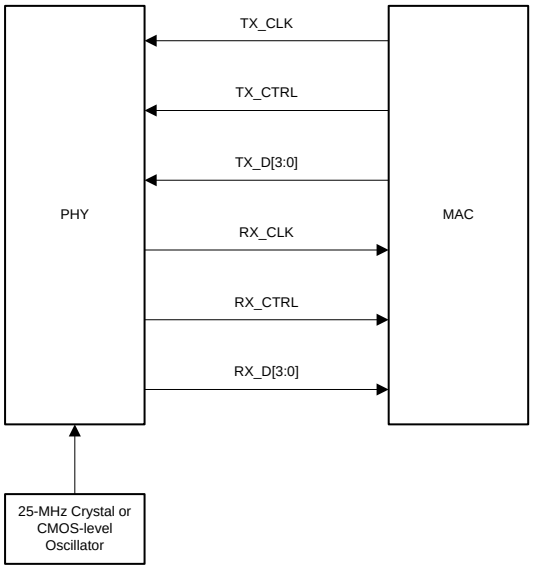


Figure 27. RGMII Signaling

During packet reception, RX_CLK may be stretched on either the positive or negative pulse to accommodate the transition from the internal free running clock to a recovered clock (data synchronous). Additionally, when the speed of the PHY changes, a similar clock stretching of the positive or negative pulses is allowed to prevent clock glitches. Data may be duplicated on the falling edge of the clock because double data rate (DDR) is only required for 1-Gbps operation, which is not supported by the DP83822.

The DP83822 supports in-band status indication. To help simplify detection of link status, speed and duplex, the DP83822 provides inter-frame signals on RX_D[3:0] pins as specified in Table 6 below.

Table 6. RGMII In-Band Status

RX_DV	RX_D3	RX_D[2:1]	RX_D0
0 **Note:** In-band status only valid when RX_DV is low	Duplex Status: 1 = Full-Duplex 0 = Half-Duplex	RX_CLK Clock Speed: 00 = 2.5-MHz (10 Mbps) 01 = 25-MHz (100 Mbps) 10 = Reserved 11 = Reserved	Link Status: 1 = Valid link established 0 = Link not established

8.4.2 Serial Management Interface

The Serial Management Interface provides access to the DP83822 internal register space for status information and configuration. The SMI is compatible with IEEE 802.3 clause 22 and clause 45. The implemented register set consists of the registers required by the IEEE 802.3 plus several others to provide additional visibility and controllability of the DP83822.

The SMI includes the management clock (MDC) and the management input/output data pin (MDIO). MDC is sourced by the external management entity, also called Station (STA), and can run at a maximum clock rate of 25 MHz. MDC is not expected to be continuous, and can be turned off by the external management entity when the bus is idle.

MDIO is sourced by the external management entity and by the PHY. The data on the MDIO pin is latched on the rising edge of the MDC. MDIO pin requires a pullup resistor (2.2 KΩ), which pulls MDIO high during IDLE and turnaround.

Up to 32 PHYs can share a common SMI bus. To distinguish between the PHYs, a 5-bit address is used. During power up or hardware reset, the DP83822 latches the PHY_AD[4:0] configuration pins to determine its address.

The management entity must not start an SMI transaction in the first cycle after power up or hardware reset. To maintain valid operation, the SMI bus must remain inactive at least one MDC cycle after reset is deasserted. In normal MDIO transactions, the register address is taken directly from the management-frame reg_addr field, thus allowing direct access to 32 16-bit registers (including those defined in IEEE 802.3 and vendor specific). The data field is used for both reading and writing. The Start code is indicated by a <01> pattern. This pattern makes sure that the MDIO line transitions from the default idle line state. Turnaround is defined as an idle bit time inserted between the Register Address field and the Data field. To avoid contention during a read transaction, no device may actively drive the MDIO signal during the first bit of Turnaround. The addressed DP83822 drives the MDIO with a zero for the second bit of turnaround and follows this with the required data.

For write transactions, the station-management entity writes data to the addressed DP83822, thus eliminating the requirement for MDIO Turnaround. The Turnaround time is filled by the management entity by inserting <10>.

Table 7. SMI Protocol

SMI PROTOCOL	<idle><start><op code><device addr><reg addr><turnaround><data><idle>
Read Operation	<idle><01><10><AAAAA><RRRRR><Z0><XXXX XXXX XXXX XXXX><idle>
Write Operation	<idle><01><01><AAAAA><RRRRR><10><XXXX XXXX XXXX XXXX><idle>

8.4.2.1 Extended Register Space Access

The DP83822 SMI function supports read and write access to the extended register set using the Register Control Register (REGCR, address 0x000D), the Data Register (ADDAR, address 0x000E), and the MDIO Manageable Device (MMD) indirect method defined in IEEE 802.3ah Draft for Clause 22 for accessing the Clause 45 extended register set.

The standard register set, MDIO registers 0 to 31, is accessed using the normal direct-MDIO access or the indirect method, except for register REGCR and register ADDAR, which are accessed only using the normal MDIO transaction. The SMI function will ignore indirect access to these registers.

REGCR is the MMD access control. In general, register REGCR[4:0] is the device address DEVAD that directs any accesses of the ADDAR register to the appropriate MMD.

The DP83822 supports three MMD device addresses:

1. The Vendor-Specific device address DEVAD[4:0] = 11111 is used for general MMD register accesses.
2. DEVAD[4:0] = 00011 is used for Energy Efficient Ethernet MMD register accesses. Register names for registers accessible at this device address are preceded by MMD3.
3. DEVAD[4:0] = 00111 is used for Energy Efficient Ethernet MMD registers accesses. Register names for registers accessible at this device address are preceded by MMD7.

All accesses through register REGCR and ADDAR must use the correct DEVAD. Transactions with other DEVAD are ignored. REGCR[15:14] holds the access function: address (00), data with no post increment (01), data with post increment on read and writes (10) and data with post increment on writes only (11).

- ADDAR is the address/data MMD register. ADDAR is used in conjunction with REGCR to provide the access to the extended register set. If register REGCR[15:14] is (00), then ADDAR holds the address of the extended address space register. Otherwise, ADDAR holds the data as indicated by the contents of its address register. When REGCR[15:14] is set to (00), accesses to register ADDAR modify the extended register set address register. This address register must always be initialized in order to access any of the registers within the extended register set.
- When REGCR[15:14] is set to (01), accesses to register ADDAR access the register within the extended register set selected by the value in the address register.
- When REGCR[15:14] is set to (10), access to register ADDAR access the register within the extended register set selected by the value in the address register. After that access is complete, for both reads and writes, the value in the address register is incremented.
- When REGCR[15:14] is set to (11), access to register ADDAR access the register within the extended register set selected by the value in the address register. After that access is complete, for write access only, the value in the address register is incremented. For read accesses, the value of the address register remains unchanged.

The following sections describe how to perform operations on the extended register set using register REGCR and ADDAR. The descriptions use the device address for general MMD register accesses (DEVAD[4:0] = 11111). For register accesses to the MMD3 or MMD7 registers the corresponding device address would be used.

8.4.2.2 Write Address Operation

To set the address register:

1. Write the value 0x001F (address function field = 00, DEVAD = 31) to register REGCR.
2. Write the register address to register ADDAR.

Subsequent writes to register ADDAR (step 2) continue to write the address register.

8.4.2.3 Read Address Operation

To read the address register:

1. Write the value 0x001F (address function field = 00, DEVAD = 31) to register REGCR.
2. Read the register address from register ADDAR.

Subsequent reads to register ADDAR (step 2) continue to read the address register.

8.4.2.4 Write (No Post Increment) Operation

To write a register in the extended register set:

1. Write the value 0x001F (address function field = 00, DEVAD = 31) to register REGCR.
2. Write the desired register address to register ADDAR.
3. Write the value 0x401F (data, no post increment function field = 01, DEVAD = 31) to register REGCR.
4. Write the content of the desired extended register set to register ADDAR.

Subsequent writes to register ADDAR (step 4) continue to rewrite the register selected by the value in the address register.

NOTE

Steps (1) and (2) can be skipped if the address register was previously configured.

8.4.2.5 Read (No Post Increment) Operation

To read a register in the extended register set:

1. Write the value 0x001F (address function field = 00, DEVAD = 31) to register REGCR.
2. Write the desired register address to register ADDAR.
3. Write the value 0x401F (data, no post increment function field = 01, DEVAD = 31) to register REGCR.
4. Read the content of the desired extended register set in register ADDAR.

Subsequent reads to register ADDAR (step 4) continue to reading the register selected by the value in the address register.

NOTE

Steps (1) and (2) can be skipped if the address register was previously configured.

8.4.2.6 Write (Post Increment) Operation

1. Write the value 0x001F (address function field = 00, DEVAD = 31) to register REGCR.
2. Write the desired register address to register ADDAR.
3. Write the value 0x801F (data, post increment function field = 10, DEVAD = 31) or the value 0xC01F (data, post increment on writes function field = 11, DEVAD = 31) to register REGCR.
4. Write the content of the desired extended register set to register ADDAR.

Subsequent writes to register ADDAR (step 4) write the next higher addressed data register selected by the value of the address register; the address register is incremented after each access.

8.4.2.7 Read (Post Increment) Operation

To read a register in the extended register set and automatically increment the address register to the next higher value following the write operation:

1. Write the value 0x001F (address function field = 00, DEVAD = 31) to register REGCR.
2. Write the desired register address to register ADDAR.
3. Write the value 0x801F (data, post increment function field = 10, DEVAD = 31) to register REGCR.
4. Read the content of the desired extended register set in register ADDAR.

Subsequent reads to register ADDAR (step 4) read the next higher addressed data register selected by the value of the address register; the address register is incremented after each access.

8.4.2.8 Example Write Operation (No Post Increment)

The following example will demonstrate a write operation with no post increment. In this example, the MAC impedance will be adjusted to 99.25 Ω using the IO MUX GPIO Control Register (IOCTRL, address 0x0461).

1. Write the value 0x001F to register 0x000D.
2. Write the value 0x0461 to register 0x000E. (Sets desired register to the IOCTRL)
3. Write the value 0x401F to register 0x000D.
4. Write the value 0x0400 to register 0x000E. (Sets MAC impedance to 99.25 Ω)

8.4.2.9 Example Read Operation (No Post Increment)

The following example will demonstrate a read operation with no post increment. In this example, the MMD7 Energy Efficient Ethernet Link Partner Ability Register (MMD7_EEE_LP_ABILITY, address 0x703D) will be read.

1. Write the value 0x0007 to register 0x000D.
2. Write the value 0x003D to register 0x000E. (Sets desired register to the MMD7_EEE_LP_ABILITY)
3. Write the value 0x4007 to register 0x000D.
4. Read the value of register 0x000E. (Data read is the value contained within the MMD7_EEE_LP_ABILITY)

8.4.3 100BASE-TX

8.4.3.1 100BASE-TX Transmitter

The 100BASE-TX transmitter consists of several functional blocks which convert synchronous 4-bit nibble data, as provided by the MII, to a scrambled MLT-3 125 Mbps serial data stream on the MDI. 4B5B encoding and decoding is detailed in Table 8 below.

The transmitter section consists of the following funcitonal blocks:

1. Code-Group Encoder and Injection Block
2. Scrambler Block with Bypass Option
3. NRZ to NRZI Encoder Block
4. Binary to MLT-3 Converter / Common Driver Block

The bypass option for the functional blocks within the 100BASE-TX transmitter provides flexibility for applications where data conversion is not always required. The DP83822 implements the 100BASE-TX transmit state machine diagram as specified in the IEEE 802.3u Standard, Clause 24.

Table 8. 4B5B Code-Group Encoding / Decoding

NAME	PCS 5B CODE-GROUP	MII 4B NIBBLE CODE
DATA CODES		
0	11110	0000
1	01001	0001
2	10100	0010
3	10101	0011
4	01010	0100
5	01011	0101
6	01110	0110
7	01111	0111
8	10010	1000
9	10011	1001
A	10110	1010
B	10111	1011
C	11010	1100
D	11011	1101
E	11100	1110
F	11101	1111
IDLE AND CONTROL CODES(1)		
H	00100	HALT code-group - Error code
I	11111	Inter-Packet IDLE - 0000
J	11000	First Start of Packet - 0101
K	10001	Second Start of Packet - 0101
T	01101	First End of Packet - 0000
R	00111	Second End of Packet - 0000
P	00000	EEE LPI - 0001(2)
INVALID CODES		
V	00001	
V	00010	
V	00011	
V	00101	
V	00110	
V	01000	
V	01100	
V	10000	
V	11001	

(1) Control code-groups I, J, K, T and R in data fields will be mapped as invalid codes, together with RX_ER asserted.
(2) Energy Efficient Ethernet LPI must also have TX_ER / RX_ER asserted and TX_EN / RX_DV deasserted.

8.4.3.1.1 Code-Group Encoding and Injection

The code-group encoder converts 4-bit (4B) nibble data generated by the MAC into 5-bit (5B) code-groups for transmission. This conversion is required to allow control data to be combined with packet data code-groups. Refer to Table 8 for 4B to 5B code-group mapping details.

The code-group encoder substitutes the first 8-bits of the MAC preamble with a J/K code-group pair (11000 10001) upon transmission. The code-group encoder continues to replace subsequent 4B preamble and data nibbles with corresponding 5B code-groups. At the end of the transmit packet, upon the deassertion of transmit enable (TX_EN) signal from the MAC, the code-group encoder injects the T/R code-group pair (01101 00111) indicating the end of the frame.

After the T/R code-group pair, the code-group encoder continuously injects IDLEs into the transmit data stream until the next transmit packet is detected (reassertion of transmit enable).

8.4.3.1.2 Scrambler

The scrambler is required to control the radiated emissions at the media connector and on the twisted-pair cable. By scrambling the data, the total energy launched onto the cable is randomly distributed over a wide frequency range. Without the scrambler, energy levels at the MDI and on the cable could peak beyond FCC limitations at frequencies related to repeating 5B sequences (that is, continuous transmission of IDLEs).

The scrambler is configured as a closed loop linear feedback shift register (LFSR) with an 11-bit polynomial. The output of the closed loop LFSR is X-ORd with the serial NRZ data from the code-group encoder. The result is a scrambled data stream with sufficient randomization to decrease radiated emissions at certain frequencies by as much as 20 dB.

8.4.3.1.3 NRZ to NRZI Encoder

After the transmit data stream has been serialized and scrambled, the data must be NRZI encoded in order to comply with the TP-PMD standard for 100BASE-TX transmission over Category-5 Unshielded twisted pair cable. There is no ability to bypass this block within the DP83822. The NRZI data is sent to the 100 Mbps Driver.

8.4.3.1.4 Binary to MLT-3 Converter

The Binary to MLT-3 conversion is accomplished by converting the serial binary data stream output from the NRZI encoder into two binary data streams with alternately phased logic one events. These two binary streams are then fed to the twisted pair output driver which converts the voltage to current and alternately drives either side of the transmit transformer primary winding, resulting in a minimal current MLT-3 signal.

The 100BASE-TX MLT-3 signal sourced by the PMD Output Pair common driver is slew rate controlled. This should be considered when selecting AC coupling magnetics to ensure TP-PMD Standard compliant transition times (3 ns < Trise/fall < 5 ns).

The 100BASE-TX transmit TP-PMD function within the DP83822 is capable of sourcing only MLT-3 encoded data. Binary output from the PMD Output Pair is not possible in 100 Mbps mode. Fully encoded MLT-3 on both Tx+ and Tx- and can be configured by configuring Register 0x0404h (for example, in transformer-less designs).

8.4.3.2 100BASE-TX Receiver

The 100BASE-TX receiver consists of several functional blocks which convert the scrambled MLT-3 125 Mbps serial data stream to synchronous 4-bit nibble data that is provided to the MII.

The receive section consists of the following functional blocks:

1. Input and BLW Compensation
2. Signal Detect
3. Digital Adaptive Equalization
4. MLT-3 to Binary Decoder
5. Clock Recovery Module
6. NRZI to NRZ Decoder
7. Serial to Parallel
8. Descrambler
9. Code-Group Alignment

10. 4B/5B Decoder
11. Link Integrity Monitor
12. Bad SSD Detection

8.4.4 100BASE-FX

The DP83822 provides IEEE 802.3 compliant 100BASE-FX operation. Hardware bootstrap or register configuration can be used to enable 100BASE-FX operation.

8.4.4.1 100BASE-FX Transmit

In 100BASE-FX mode, the DP83822 transmit pins connect to an industry standard fiber transceiver through a capacitively coupled circuit. During 100BASE-FX operation, the DP83822 transmit path will bypass the scrambler and MLT-3 encoder so that only serialized 4B5B encoded NRZI data is transmitted at 125-MHz.

8.4.4.2 100BASE-FX Receive

In 100BASE-FX mode, the DP83822 receive pins connect to an industry standard fiber transceiver through a capacitively coupled circuit. During 100BASE-FX operation, the DP83822 receive path will bypass the MLT-3 decoder and scrambler. This allows for reception of serialized 4B5B encoded NRZI data at 125 MHz.

The DP83822 also has the added feature of a signal detection pin for direct connection to an industry standard fiber transceiver. When enabling 100BASE-FX operation using the FX_EN bootstrap, AMDIX_EN bootstrap turns into SD_EN bootstrap. If 100BASE-FX operation is enabled by setting FX_EN to either bootstrap mode 2 or 3, SD_EN will enable signal detection pin, LED_1, when SD_EN is set to either bootstrap mode 3 or 4. Please see Table 11 for mode information regarding hardware bootstraps.

NOTE

100BASE-FX signal detect pin (LED_1) polarity is controlled by bit[0] in the General Configuration Register (GENCFG, address 0x0465). By default, signal detect is an active HIGH polarity.

NOTE

TI recommends connecting Signal Detect pin from the Optical Transceiver to the LED_1 pin and enable it using SD_EN bootstrap pin in 100BASE-FX mode. The LED_1 pin is not used in design and that, if the electrical link between the fiber module and the DP83822 is broken, disconnected or otherwise disrupted, the link will recover only by initiating a soft reset through MDIO/MDC interface.

8.4.5 10BASE-Te

The 10BASE-Te transceiver module is IEEE 802.3 compliant. It includes the receiver, transmitter, collision, heartbeat, loopback, jabber, and link integrity functions, as defined in the standard.

8.4.5.1 Squelch

Squelch is responsible for determining when valid data is present on the differential receive inputs. The squelch circuitry employs a combination of amplitude and timing measurements (as specified in the IEEE 802.3 10BASE-Te standard) to determine the validity of data on the twisted-pair inputs.

The signal at the start of a packet is checked by the squelch, and any pulses not exceeding the squelch level (either positive or negative, depending upon polarity) are rejected. When this first squelch level is exceeded correctly, the opposite squelch level must then be exceeded no earlier than 50ns. Finally, the signal must again exceed the original squelch level no earlier than 50ns to qualify as a valid input waveform, and not be rejected. This checking procedure results in the typical loss of three preamble bits at the beginning of each packet. When the transmitter is operating, five consecutive transitions are checked before indicating that valid data is present. At this time, the squelch circuitry is reset.

8.4.5.2 Normal Link Pulse Detection and Generation

The link pulse generator produces pulses as defined in the IEEE 802.3 10BASE-Te standard. Each link pulse is nominally 100 ns in duration and transmitted every 16 ms in the absence of transmit data. Link pulses are used to check the integrity of the connection with the remote end.

8.4.5.3 Jabber

Jabber is a condition in which a station transmits for a period of time longer than the maximum permissible packet length, usually due to a fault condition. The jabber function monitors the DP83822 output and disables the transmitter if it attempts to transmit a packet of longer than legal size. A jabber timer monitors the transmitter and disables the transmission if the transmitter is active for approximately 100ms. When disabled by the Jabber function, the transmitter stays disabled for the entire time that the module's internal transmit enable is asserted. This signal must be de-asserted for approximately 500ms (unjab time) before the Jabber function re-enables the transmit outputs. The Jabber function is only available and active in 10BASE-Te mode.

8.4.5.4 Active Link Polarity Detection and Correction

Swapping the wires within the twisted-pair causes polarity errors. Wrong polarity affects 10BASE-Te connections. 100BASE-TX is immune to polarity problems because it uses MLT-3 encoding. 10BASE-Te receive block automatically detects reversed polarity.

8.4.6 Auto-Negotiation (Speed / Duplex Selection)

Auto-Negotiation provides a mechanism for exchanging configuration information between the two ends of a link segment. This mechanism is implemented by exchanging Fast Link Pulses (FLP). FLPs are burst pulses that provide the information used to communicate the abilities between two devices at each end of a link segment. The DP83822 supports 100BASE-TX and 10BASE-Te modes of operation for Auto-Negotiation. 100BASE-FX is not included in the Auto-Negotiation process. Auto-Negotiation ensures that the highest performance protocol is selected based on the advertised abilities of the Link Partner and the local device. Auto-Negotiation can be enabled or disabled in hardware, using the AN_EN bootstrap, or by regsiter configuration, using bit[12] in the Basic Mode Control Register (BMCR, address 0x0000). For further details regarding Auto-Negotiation, refer to Clause 28 of the IEEE 802.3 specification.

8.4.7 Auto-MDIX Resolution

The DP83822 can determine if a “straight” or “crossover” cable is used to connect to the Link Partner. It can automatically re-assign channel A and B to establish link with the Link Partner. Auto-MDIX resolution precedes the actual Auto-Negotiation process that involves exchange of FLPs to advertise capabilities. Automatic MDI/MDIX is described in IEEE 802.3 Clause 40, section 40.8.2. It is not a required implementation for 10BASE-Te and 100BASE-TX. Auto-MDIX can also be used when operating the PHY in Forced modes.

Auto-MDIX can be enabled or disabled in hardware, using the AMDIX bootstrap, or by register configuration, using bit[15] of the PHY Control Register (PHYCR, address 0x0019). When Auto-MDIX is disabled, the PMA is forced to either MDI (“straight”) or MDIX (“crossover”). Manual configuration of MDI or MDIX can also be accomplished in hardware, using the AMDIX bootstrap, or by register configuration, using bit[14] of the PHYCR. Additionally, the DP83822 supports Fast Auto-MDIX configuration via register configuration to enable faster MDIX resolution for link establishment. Fast Auto-MDIX can be enabled using bit[6] in the Control Register #1 (CR1, address 0x0009).

8.4.8 Loopback Modes

There are several loopback options within the DP83822 that test and verify various functional blocks within the PHY. Enabling loopback modes allow for in-circuit testing of the digital and analog data paths. The DP83822 may be configured to any one of the Near-End Loopback modes or to the Far-End (reverse) Loopback mode. MII Loopback is configured using the Basic Mode Control Register (BMCR, address 0x0000). All other loopback modes are enabled using the BIST Control Register (BISCR, address 0x0016). Except where otherwise noted, loopback modes are supported for all speeds (10/100 Mbps and all MAC interfaces).

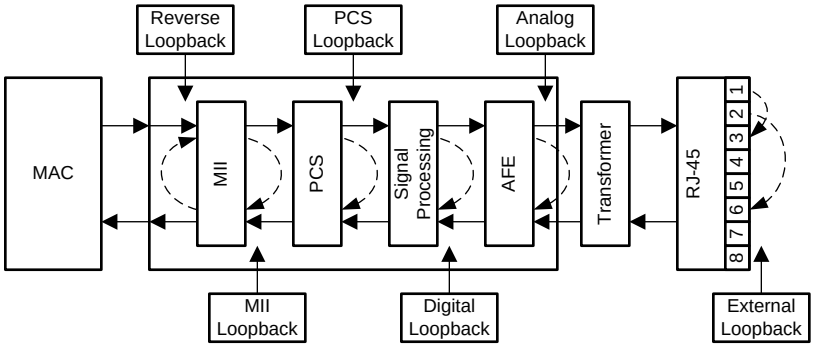


Figure 28. Loopback Test Modes

8.4.8.1 Near-End Loopback

Near-End Loopback provides the ability to loop the transmitted data back to the receiver via the digital or analog circuitry. The point at which the signal is looped back is selected using loopback control bits[3:0] in the BISCR register. Auto-Negotiation and Auto-MDIX should be disabled before selecting the Near-End Loopback modes. This constraint does not apply for external-loopback mode.

8.4.8.2 MII Loopback

MII Loopback is the shallowest loop through the PHY. It is a useful test mode to validate communications between the MAC and the PHY. When in MII Loopback, data transmitted from a connected MAC on the TX path is internally looped back in the DP83822 to the RX pins where it can be checked by the MAC.

MII Loopback is enabled by setting bit[14] in the BMCR.

8.4.8.3 PCS Loopback

PCS Loopback occurs in the PCS layer of the PHY. No signal processing is performed when using PCS Loopback.

PCS Input Loopback is enabled by setting bit[0] in the BISCR.

PCS Output Loopback is enabled by setting bit[1] in the BISCR.

8.4.8.4 Digital Loopback

Digital Loopback includes the entire digital transmit and receive paths. Data is looped back prior to the analog circuity.

Digital Loopback is enabled by setting bit[2] in the BISCR.

8.4.8.5 Analog Loopback

When operating in 10BASE-Te or 100BASE-TX mode, signals can be looped back after the analog front-end. Analog Loopback requires 100-Ω terminations accross pins #1 and #2 as well as 100-Ω terminations accross pins #3 and #6 at the RJ45.

Analog Loopback is enabled by setting bit[3] in the BISCR.

8.4.8.6 Far-End (Reverse) Loopback

Far-End (Reverse) loopback is a special test mode to allow PHY testing with a link partner. In this mode, data that is received from the Link Partner passes through the PHY's receiver, is looped back at the MAC interface and then transmitted back to the Link Partner. While in Reverse Loopback mode, all data signals that come from the MAC are ignored.

Reverse Loopback is enabled by setting bit[4] in the BISCR.

8.4.9 BIST Configurations

The DP83822 incorporates an internal PRBS Built-in Self-Test (BIST) circuit to accommodate in-circuit testing and diagnostics. The BIST circuit can be used to test the integrity of transmit and receive data paths. The BIST can be performed using both internal loopbacks (digital or analog) or external loopback using a cable fixture. The BIST simulates pseudo-random data transfer scenarios in format of real packets and Inter-Packet Gap (IPG) on the lines. The BIST allows full control of the packet lengths and the IPG.

The BIST Packet Length is controlled using bits[10:0] in the BIST Control and Status Register #2 (BICSR2, address 0x001C). The BIST IPG Length is controlled using bits[7:0] in the BIST Control and Status Register #1 (BICSR1, address 0x001B).

The BIST is implemented with independent transmit and receive paths, with the transmit clock generating a continuous stream of a pseudo-random sequence. The device generates a 15-bit pseudo-random sequence for BIST. Received data is compared to the generated pseudo-random data to determine pass/fail status. The number of error bytes that the PRBS checker received is stored in bits[15:8] of the BICSR1. PRBS lock status and sync can be read from the BIST Control Register (BISCR, address 0x0016).

The PRBS test can be put in a continuous mode by using bit[14] in the BISCR. In continuous mode, when the BIST error counter reaches the maximum value, the counter starts counting from zero again. To read the BIST error count, bit[15] in the BICSR1 must be set to '1'. This will lock the current value of the BIST errors for reading. Please note that setting bit[15] also clears the BIST Error Counter.

8.4.10 Cable Diagnostics

With the vast deployment of Ethernet devices, the need for a reliable, comprehensive and user-friendly cable diagnostic tool is more important than ever. The wide variety of cables, topologies and connectors deployed results in the need to non-intrusively identify and report cable faults. The TI cable-diagnostic unit provides extensive information about cable integrity. The DP83822 offers the following capabilities in its Cable Diagnostic tool kit:

- Time Domain Reflectometry (TDR)

8.4.10.1 TDR

The DP83822 uses Time Domain Reflectometry (TDR) to determine the quality of the cables, connectors and terminations in addition to estimating the cable length. Some of the possible problems that can be diagnosed include opens, shorts, cable impedance mismatch, bad connectors, termination mismatches, cross faults, cross shorts and any other discontinuities along the cable.

The DP83822 transmits a test pulse of known amplitude (1 V) down each of the two pairs of an attached cable. The transmitted signal continues down the cable and reflects from each cable imperfection, fault, connector and from the end of the cable itself. After the pulse transmission, the DP83822 measures the return time and amplitude of all these reflected pulses. This technique enables measuring the distance and magnitude (impedance) of non-terminated cables (open or short), discontinuities (bad connectors) and improperly terminated cables with ±1m accuracy.

For all TDR measurements, the transformation between time of arrival and physical distance is done by the external host using minor computations (such as multiplication, addition and lookup tables). The host must know the expected propagation delay of the cable, which depends, among other things, on the cable category (for example, CAT5, CAT5e, or CAT6).

TDR measurement is allowed in the following scenarios:

- While the Link Partner is disconnected – cable is unplugged at the other side
- Link Partner is connected but remains “quiet” (for example, in power down mode)
- TDR could be automatically activated when the link fails or is dropped

TDR Auto-Run can be enabled by using bit[8] in the Control Regsiter #1 (CR1, address 0x0009). When a link drops, TDR will automatically execute and store the results in the respective TDR Cable Diagnostic Location Result Registers #1 - #5 (CDLRR, addresses 0x0180 to 0x0184) and the Cable Diagnostic Amplitude Result Registers #1 - #5 (CDLAR, addresses 0x0185 to 0x0189). TDR can also be run manually using bit[15] in the Cable Diagnostic Control Register (CDCR, address 0x001E). Cable diagnostic status is obtained by reading bits[1:0] in the CDCR. Additional TDR functions including cycle averaging, bypass channel and crossover disable can be found in the Cable Diagnostic Specific Control Register (CDSCR, address 0x0170).

8.4.11 Fast Link Down Functionality

The DP83822 includes advanced link-down capabilities that support various real-time applications. The link-down mechanism is configurable and includes enhanced modes that allow extremely fast link-drop reaction times.

The DP83822 supports an enhanced link drop mechanism, also called Fast Link Drop (FLD), which shortens the observation window for determining link. There are multiple ways of determining link status, which can be enabled or disabled based on user preference. Fast Link Drop can be enabled in hardware with bootstrapping or in software using register configuration. RX_D2 when strapped to either mode 2 or mode 3 will enable FLD at power up or hardware reset. Additionally, FLD can be configured using the Control Register #3 (CR3, address 0x000B). Bits[3:0] and bit[10] allow for various FLD conditions to be enabled. When link drop occurs, indication of a particular fault condition can be read from the Fast Link Down Status Register (FLDS, address 0x000F).

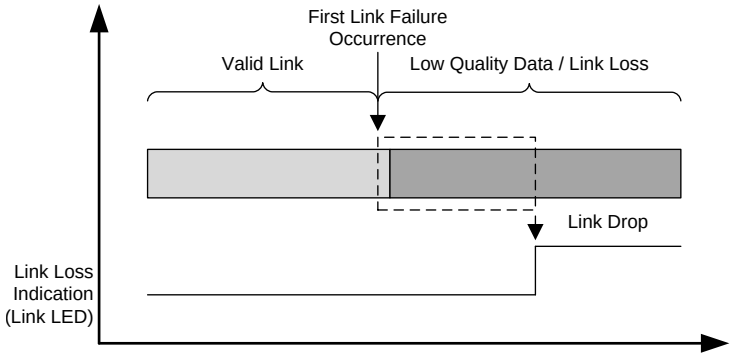


Figure 29. Fast Link Down

Fast Link Down criteria include:

- RX Error Count - when a predefined number of 32 RX_ERs occur in a 10μs window, the link will be dropped.
- MLT3 Error Count - when a predefined number of 20 MLT3 errors occur in a 10μs window, the link will be dropped.
- Low SNR Threshold - when a predefined number of 20 threshold crossings occur in a 10μs window, the link will be dropped.
- Signal/Energy Loss - when the energy detector indicates energy loss, the link will be dropped.

The Fast Link Down functionality allows the use of each of these options separately or in any combination.

NOTE

Because this mode enables extremely quick reaction time, it is more exposed to temporary bad link-quality scenarios.

8.5 Programming

8.5.1 Hardware Bootstrap Configurations

The DP83822 uses the receive path functional pins as bootstrap options to place the device into specific modes of operation. The values of these pins are sampled at power up or hardware reset, through either the RESET pin or bit[15] in the PHY Reset Control Register (PHYRCR, address 0x001F).

The DP83822 bootstrap pins are 4-level, which are described in greater detail below.

NOTE

Because bootstrap pins may have alternate functions after reset is de-asserted, they should not be connected directly to VCC or GND. pullup and pulldown resistors are required for proper operation.

Pins: COL, LED_0, CRS and RX_ER have internal pullup resistors. All other pins with bootstraps have internal pulldown resistors. To account for the difference between the internal pullup and pulldown, please reference Table 9 and Table 10 below for proper implementation.

LED_0 and LED_1 require parallel pullup or pulldown resistors when using the pin in conjunction with an LED and current limiting resistor.

Configuration of the device may be done via 4-level strapping or via serial management interface. A pullup resistor and a pulldown resistor of suggested values should be used to set the voltage ratio of the bootstrap pin input and the supply to select one of the possible modes.

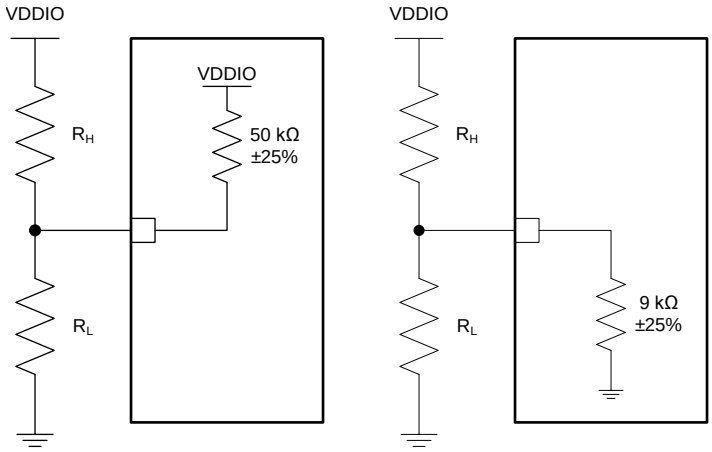


Figure 30. Bootstrap Circuits

Programming (continued)

Table 9. Recommended 4-Level Strap Resistor Ratios(1)

MODE	IDEAL $R_{H\ (k\Omega)}$	IDEAL $R_{L\ (k\Omega)}$
PULLDOWN PINS (9 kΩ)		
1 (Default)	**OPEN**	**OPEN**
2	10	2.49
3	5.76	2.49
4	2.49	OPEN
PULLUP PINS (50 kΩ)		
1	OPEN	1.96
2	13	1.96
3	6.2	1.96
4 (Default)	**OPEN**	**OPEN**

(1) Strap resistors with 1% tolerance are recommended.

Table 10. 4-Level Strap Voltage Ratios(1)

TARGET VOLTAGE	MODE 1	MODE 2	MODE 3	MODE 4
V_{max} (V)	0.098 x VDDIO	0.181 x VDDIO	0.277 x VDDIO	VDDIO
V_{typ} (V)	0	0.165 x VDDIO	0.252 x VDDIO	VDDIO
V_{min} (V)	0	0.148 x VDDIO	0.227 x VDDIO	0.694 x VDDIO

(1) Ensured by production test, characterization or design.

Table 11 describes the DP83822 configuration bootstraps:

Table 11. 4-Level Strap Pins

PIN NAME	PIN #	DEFAULT	STRAP FUNCTION			DESCRIPTION
COL	29	[01]	**MODE**	**FX_EN**	**PHY_AD0**	**FX_EN:** Enables 100BASE-FX when set to '1' **PHY_AD0:** PHY Address bit[0]
			1	0	0	
			2	1	0	
			3	1	1	
			4 (Default)	**0**	**1**	
RX_D0	30	[10]	**MODE**	**AN_1**	**PHY_AD1**	**AN_1:** See Table 12 below **PHY_AD1:** PHY Address bit[1]
			1 (Default)	**1**	**0**	
			2	0	0	
			3	0	1	
			4	1	1	
RX_D1	31	[00]	**MODE**	**EEE_EN**	**PHY_AD2**	**EEE_EN:** Enables EEE operation when set to '1' **PHY_AD2:** PHY Address bit [2]
			1 (Default)	**0**	**0**	
			2	1	0	
			3	1	1	
			4	0	1	
RX_D2	32	[00]	**MODE**	**FLD_EN**	**PHY_AD3**	**FLD_EN:** Enables Fast Link Drop when set to '1'. Energy Detection, Low SNR threshold and RX_ER will be enabled. **PHY_AD3:** PHY Address bit[3]
			1 (Default)	**0**	**0**	
			2	1	0	
			3	1	1	
			4	0	1	
RX_D3	1	[10]	**MODE**	**AN_EN**	**PHY_AD4**	**AN_EN:** See Table 12 below **PHY_AD4:** PHY Address bit[4]
			1 (Default)	**1**	**0**	
			2	0	0	
			3	0	1	
			4	1	1	
LED_0	17	[X1]	**MODE**	**RESERVED**	**AN_0**	**AN_0:** See Table 12 below
			1	X	0	
			2	X	Not Applicable	
			3	X	Not Applicable	
			4 (Default)	X	**1**	
CRS	27	[01]	**MODE**	**LED_SPEED**	**LED_CFG**	**LED_CFG:** See below **LED_SPEED:** See Table 13 below
			1	0	0	
			2	1	0	
			3	1	1	
			4 (Default)	**0**	**1**	
RX_ER	28	[01]	**MODE**	**RGMII_EN**	**AMDIX_EN *(SD_EN)***	**AMDIX_EN:** Enables Auto-MDIX when set to '1' **RGMII_EN:** See Table 14 below **SD_EN:** Enables 100BASE-FX Signal Detection on LED_1 when set to '1'. FX_EN strap must be enabled for SD_EN strap to be functional. Signal Detection is Active HIGH, but polarity can be changed using the General Configuration Register (GENCFG, address 0x0465).
			1	0	0	
			2	1	0	
			3	1	1	
			4 (Default)	**0**	**1**	

Table 11. 4-Level Strap Pins (continued)

PIN NAME	PIN #	DEFAULT	STRAP FUNCTION			DESCRIPTION
RX_DV	26	[00]	**MODE**	**XI_50**	**RMII_EN**	**XI_50:** See Table 14 below **RMII_EN:** See Table 14 below
			1 (Default)	**0**	**0**	
			2	1	0	
			3	0	1	
			4	1	1	

Table 12. Modes of Operation

FX_EN	AN_EN	AN_1	AN_0	Description
Force Modes				
0	0	0	0	10BASE-Te, Half-Duplex
0	0	0	1	10BASE-Te, Full-Duplex
0	0	1	0	100BASE-TX, Half-Duplex
0	0	1	1	100BASE-TX, Full-Duplex
Advertised Modes				
0	1	0	0	10BASE-Te, Half-Duplex
0	1	0	1	10BASE-Te, Half/Full-Duplex
0	1	1	0	10BASE-Te, Half-Duplex 100BASE-TX, Half-Duplex
0	1	1	1	10BASE-Te, Half/Full-Duplex 100BASE-TX, Half/Full-Duplex
Fiber Modes				
1	X	X	0	100BASE-FX, Half Duplex
1	X	X	1	100BASE-FX, Full Duplex

Table 13. LED Configuration

CRS Strap Mode	LED_SPEED	LED_CFG[0]	LED_0	LED_1
1	0	0	ON for Good Link BLINK for TX/RX Activity	LED_1 in Tri-State
2	1	0	ON for Good Link BLINK for TX/RX Activity	ON for 100 Mbps SPEED OFF for 10 Mbps SPEED
3	1	1	ON for Good Link OFF for No Link	ON for 100 Mbps SPEED OFF for 10 Mbps SPEED
4	0	1	ON for Good Link OFF for No Link	LED_1 in Tri-State

Table 14. MAC Interface Configuration

RGMII_EN	RMII_EN	XI_50	Description
0	0	0	MII, 25-MHz Reference Clock
0	0	1	**Reserved**
0	1	0	RMII, 25-MHz Reference Clock
0	1	1	RMII, 50-MHz Reference Clock
1	X	0	RGMII, 25-MHz Reference Clock
1	X	1	**Reserved**

8.5.2 LED Configuration

The DP83822 supports up to three configurable Light Emitting Diode (LED) pins: LED_0, LED_1 (GPIO1), COL (GPIO2) and RX_D3 (GPIO3). Several functions can be multiplexed onto the LEDs for different modes of operation. The LED configuration modes are selected using the LEDs Configuration Register (LEDCFG1, register 0x0460) and the Multi-LED Control Register (MLEDCR, register 0x0025). LED_0 and COL (GPIO2) use the MLED function found in register 0x0025. MLED can be routed to only one of these two pins at a time. MLED routing is determined by bits[1:0] in register 0x0025.

Because LED pins are also used as bootstrap pins, external components must be considered in order to avoid contention. LED pins are automatically configured for the proper polarity based on the bootstrap configuration at power up or hardware reset. If an LED pin is resistively pulled low, the corresponding output will be configured as an active high driver. Conversely, if a given bootstrap input is resistively pulled high, the corresponding output will be configured as an active low driver.

An example below shows proper bootstrap connections for LED pins using either pullup or pulldown configurations.

Note: LED_0 and LED_1 require parallel pullup or pulldown resistors when using the pin in conjunction with an LED and current limiting resistor. A 1.96kΩ to 2.49kΩ resistor should be used as the parallel pull resistor. When LED pins are not used, they can be left floating.

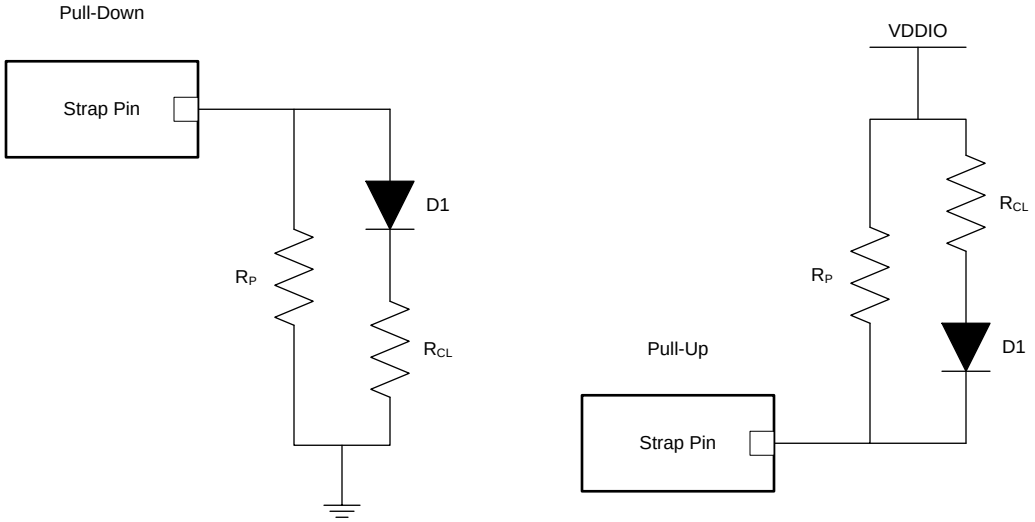


Figure 31. Example Strap Connections

8.5.3 PHY Address Configuration

The DP83822 can be configured for any of the 32 possible PHY addresses available through bootstrap configuration. The PHY address is latched into the device upon power up or hardware reset. Each DP83822 or port sharing PHY on the serial management bus in the system must have a unique PHY address. The DP83822 supports PHY address strapping values 0x0000 (0b00000) through 0x001F (0b11111).

By default, the DP83822 will latch-in PHY address 0x0001 (0b00001). This address can be changed by adding the required pullup or pulldown resistors defined in the bootstrap section above.

8.6 Register Maps

In the register definitions under the “TYPE” heading, the following definitions apply:

COR Clear on Read

Strap Default value loads from bootstrap pin after reset

LH Latched high and held until read

LL Latched low and held until read

RO Read Only Access

RO/COR Read Only, Clear on Read

RO/P Read Only, Permanently set to a default value

RW Read Write access

RW/SC Read Write access, Self Clearing bit

SC Register sets on event occurrence and Self-Clears when event ends

Table 15. 0x0000 Basic Mode Control Register (BMCR)

BIT	NAME	TYPE	DEFAULT	FUNCTION
15	Reset	RW, SC	0	**PHY Software Reset:** 1 = Initiate software Reset / Reset in Progress 0 = Normal Operation Writing a 1 to this bit resets the PHY PCS registers. When the reset operation is done, this bit is cleared to 0 automatically. PHY Vendor Specific registers will not be cleared.
14	MII Loopback	RW	0	**MII Loopback:** 1 = MII Loopback enabled 0 = Normal Operation When MII loopback mode is activated, the transmitted data presented on MII TXD is looped back to MII RXD internally.
13	Speed Selection	RW, Strap	1	**Speed Select:** 1 = 100 Mbps 0 = 10 Mbps When Auto-Negotiation is disabled (bit[12] = 0 in Register 0x0000), writing to this bit allows the port speed to be selected.
12	Auto-Negotiation Enable	RW, Strap	1	**Auto-Negotiation Enable:** 1 = Enable Auto-Negotiation 0 = Disable Auto-Negotiation If Auto-Negotiation is disabled, bit[8] and bit[13] of this register determine the port speed and duplex mode.
11	IEEE Power Down	RW	0	**Power Down:** 1 = IEEE Power Down 0 = Normal Operation The PHY is powered down after this bit is set. Only register access is enabled during this power down condition. To control the power down mechanism, this bit is OR'ed with the input from the INT/PWDN_N pin. When the active low INT/PWDN_N is asserted, this bit is set.
10	Isolate	RW	0	**Isolate:** 1 = Isolates the port from the MII with the exception of the SMI 0 = Normal Operation
9	Restart Auto-Negotiation	RW, SC	0	**Restart Auto-Negotiation:** 1 = Restarts Auto-Negotiation 0 = Normal Operation If Auto-Negotiation is disabled (bit[12] = 0), bit[9] is ignored. This bit is self-clearing and will return a value of 1 until Auto-Negotiation is initiated, whereupon it will self-clear. Operation of the Auto-Negotiation process is not affected by the management entity clearing this bit.

Register Maps (continued)

Table 15. 0x0000 Basic Mode Control Register (BMCR) (continued)

BIT	NAME	TYPE	DEFAULT	FUNCTION
8	Duplex Mode	RW, Strap	1	**Duplex Mode:** 1 = Full-Duplex 0 = Half-Duplex When Auto-Negotiation is disabled, writing to this bit allows the port Duplex capability to be selected.
7	Collision Test	RW	0	**Collision Test:** 1 = Enable COL Signal Test 0 = Normal Operation When set, this bit causes the COL signal to be asserted in response to the assertion of TX_EN within 512 bit times. The COL signal is de-asserted within 4 bit times in response to the de-assertion to TX_EN.
6:0	Reserved	RO	0	Reserved

Table 16. 0x0001 Basic Mode Status Register (BMSR)

BIT	NAME	TYPE	DEFAULT	FUNCTION
15	100Base-T4	RO	0	**100Base-T4 Capable:** This protocol is not available. Always reads as 0.
14	100Base-TX Full-Duplex	RO	1	**100Base-TX Full-Duplex Capable:** 1 = Device able to perform Full-Duplex 100Base-TX 0 = Device not able to perform Full-Duplex 100Base-TX
13	100Base-TX Half-Duplex	RO	1	**100Base-TX Half-Duplex Capable:** 1 = Device able to perform Half-Duplex 100Base-TX 0 = Device not able to perform Half-Duplex 100Base-TX
12	10Base-Te Full-Duplex	RO	1	**10Base-Te Full-Duplex Capable:** 1 = Device able to perform Full-Duplex 10Base-Te 0 = Device not able to perform Full-Duplex 10Base-Te
11	10Base-Te Half-Duplex	RO	1	**10Base-Te Half-Duplex Capable:** 1 = Device able to perform Half-Duplex 10Base-Te 0 = Device not able to perform Half-Duplex 10Base-Te
10:7	Reserved	RO	0	Reserved
6	SMI Preamble Suppression	RO	1	**Preamble Suppression Capable:** 1 = Device able to perform SMI transaction with preamble suppressed 0 = Device not able to perform SMI transaction with preamble suppressed If this bit is set to 1, 32-bits of preamble needed only once after reset, invalid opcode or invalid turnaround.
5	Auto-Negotiation Complete	RO	0	**Auto-Negotiation Complete:** 1 = Auto-Negotiation process completed 0 = Auto Negotiation process not completed (either still in process, disabled or reset)
4	Remote Fault	RO, LH	0	**Remote Fault:** 1 = Remote fault condition detected 0 = No remote fault condition detected Far End Fault indication or notification from Link Partner of Remote Fault. This bit is cleared on read or reset.
3	Auto-Negotiation Ability	RO	1	**Auto-Negotiation Ability:** 1 = Device is able to perform Auto-Negotiation 0 = Device is not able to perform Auto-Negotiation
2	Link Status	RO, LL	0	**Link Status:** 1 = Valid link established (for either 10 Mbps or 100 Mbps operation) 0 = Link not established
1	Jabber Detect	RO, LH	0	**Jabber Detect:** 1 = Jabber condition detected 0 = No jabber condition detected This bit only has meaning for 10Base-Te operation.

Table 16. 0x0001 Basic Mode Status Register (BMSR) (continued)

BIT	NAME	TYPE	DEFAULT	FUNCTION
0	Extended Capability	RO	1	**Extended Capability:** 1 = Extended register capabilities 0 = Basic register set capabilities only

Table 17. 0x0002 PHY Identifier Register #1 (PHYIDR1)

BIT	NAME	TYPE	DEFAULT	FUNCTION
15:0	Organizationally Unique Identifier Bits 21:6	RO	0010 0000 0000 0000	

Table 18. 0x0003 PHY Identifier Register #2 (PHYIDR2)

BIT	NAME	TYPE	DEFAULT	FUNCTION
15:10	Organizationally Unique Identifier Bits 5:0	RO	1010 00	
9:4	Model Number	RO	10 0100	**Vendor Model Number:** The six bits of vendor model number are mapped from bits [9] to [4]
3:0	Revision Number	RO	0000	**Model Revision Number:** Four bits of the vendor model revision number are mapped from bits [3:0]. This field is incremented for all major device changes.

Table 19. 0x0004 Auto-Negotiation Advertisement Register (ANAR)

BIT	NAME	TYPE	DEFAULT	FUNCTION
15	Next Page	RW	0	**Next Page Indication:** 1 = Next Page Transfer desired 0 = Next Page Transfer not desired
14	Reserved	RO	0	Reserved
13	Remote Fault	RW	0	**Remote Fault:** 1 = Advertises that this device has detected a Remote Fault 0 = No Remote Fault detected
12	Reserved	RO	0	Reserved
11	Asymmetric Pause	RW	0	**Asymmetric Pause Support For Full-Duplex Links:** 1 = Advertise asymmetric pause ability 0 = Do not advertise asymmetric pause ability
10	Pause	RW	0	**Pause Support for Full-Duplex Links:** 1 = Advertise pause ability 0 = Do not advertise pause ability
9	100Base-T4	RO	0	**100Base-T4 Support:** 1 = Advertise 100Base-T4 ability 0 = Do not advertise 100Base-T4 ability
8	100Base-TX Full-Duplex	RW, Strap	1	**100Base-TX Full-Duplex Support:** 1 = Advertise 100Base-TX Full-Duplex ability 0 = Do not advertise 100Base-TX Full-Duplex ability
7	100Base-TX Half-Duplex	RW, Strap	1	**100Base-TX Half-Duplex Support:** 1 = Advertise 100Base-TX Half-Duplex ability 0 = Do not advertise 100Base-TX Half-Duplex ability
6	10Base-Te Full-Duplex	RW, Strap	1	**10Base-Te Full-Duplex Support:** 1 = Advertise 10Base-Te Full-Duplex ability 0 = Do not advertise 10Base-Te Full-Duplex ability
5	10Base-Te Half-Duplex	RW, Strap	1	**10Base-Te Half-Duplex Support:** 1 = Advertise 10Base-Te Half-Duplex ability 0 = Do not advertise 10Base-Te Half-Duplex ability
4:0	Selector Field	RW	0 0001	**Protocol Selection Bits:** Technology selector field (IEEE802.3u <00001>)

Table 20. 0x0005 Auto-Negotiation Link Partner Ability Register (ANLPAR)

BIT	NAME	TYPE	DEFAULT	FUNCTION
15	Next Page	RO	0	**Next Page Indication:** 1 = Link partner desires Next Page Transfer 0 = Link partner does not desire Next Page Transfer
14	Acknowledge	RO	0	**Acknowledge:** 1 = Link partner acknowledges reception of link code word 0 = Link partner does not acknowledge reception of link code word
13	Remote Fault	RO	0	**Remote Fault:** 1 = Link partner advertises remote fault event detection 0 = Link partner does not advertise remote fault event detection
12	Reserved	RO	0	Reserved
11	Asymmetric Pause	RO	0	**Asymmetric Pause:** 1 = Link partner advertises asymmetric pause ability 0 = Link partner does not advertise asymmetric pause ability
10	Pause	RO	0	**Pause:** 1 = Link partner advertises pause ability 0 = Link partner does not advertise pause ability
9	100Base-T4	RO	0	**100Base-T4 Support:** 1 = Link partner advertises 100Base-T4 ability 0 = Link partner does not advertise 100Base-T4 ability
8	100Base-TX Full-Duplex	RO	0	**100Base-TX Full-Duplex Support:** 1 = Link partner advertises 100Base-TX Full-Duplex ability 0 = Link partner does not advertise 100Base-TX Full-Duplex ability
7	100Base-TX Half-Duplex	RO	0	**100Base-TX Half-Duplex Support:** 1 = Link partner advertises 100Base-TX Half-Duplex ability 0 = Link partner does not advertise 100Base-TX Half-Duplex ability
6	10Base-Te Full-Duplex	RO	0	**10Base-Te Full-Duplex Support:** 1 = Link partner advertises 10Base-Te Full-Duplex ability 0 = Link partner does not advertise 10Base-Te Full-Duplex ability
5	10Base-Te Half-Duplex	RO	0	**10Base-Te Half-Duplex Support:** 1 = Link partner advertises 10Base-Te Half-Duplex ability 0 = Link partner does not advertise 10Base-Te Half-Duplex ability
4:0	Selector Field	RO	0 0000	**Protocol Selection Bits:** Technology selector field (IEEE802.3 <00001>)

Table 21. 0x0006 Auto-Negotiation Expansion Register (ANER)

BIT	NAME	TYPE	DEFAULT	FUNCTION
15:5	Reserved	RO	0	Reserved
4	Parallel Detection Fault	RO, LH	0	**Parallel Detection Fault:** 1 = A fault has been detected during the parallel detection process 0 = No fault detected
3	Link Partner Next Page Able	RO	0	**Link Partner Next Page Ability:** 1 = Link partner is able to exchange next pages 0 = Link partner is not able to exchange next pages
2	Local Device Next Page Able	RO	1	**Next Page Ability:** 1 = Local device is able to exchange next pages 0 = Local device is not able to exchange next pages
1	Page Received	RO, LH	0	**Link Code Word Page Received:** 1 = A new page has been received 0 = A new page has not been received
0	Link Partner Auto-Negotiation Able	RO	0	**Link Partner Auto-Negotiation Ability:** 1 = Link partner supports Auto-Negotiation 0 = Link partner does not support Auto-Negotiation

Table 22. 0x0007 Auto-Negotiation Next Page Register (ANNPTR)

BIT	NAME	TYPE	DEFAULT	FUNCTION
15	Next Page	RW	0	**Next Page Indication:** 1 = Advertise desire to send additional next pages 0 = Do not advertise desire to send additional next pages

Table 22. 0x0007 Auto-Negotiation Next Page Register (ANNPTR) (continued)

BIT	NAME	TYPE	DEFAULT	FUNCTION
14	Reserved	RO	0	Reserved
13	Message Page	RW	1	**Message Page:** 1 = Current page is a message page 0 = Current page is an unformatted page
12	Acknowledge 2	RW	0	**Acknowledge2:** 1 = Will comply with message 0 = Cannot comply with message Acknowledge2 is used by the next page function to indicate that Local Device has the ability to comply with the message received.
11	Toggle	RO	0	**Toggle:** 1 = Toggle bit in previously transmitted Link Code Word was 0 0 = Toggle bit in previously transmitted Link Code Word was 1 Toggle is used by the Arbiitration function within Auto-Negotiation to synchronize with the Link Parnter during Next Page exchange. This bit always takes the opposite value of the Toggle bit in the previously exchanged Link Code Word.
10:0	CODE	RW	000 0000 0001	This field represents the code field of the next page transmission. If the Message Page bit is set (bit [13] of this register), then the code is interpreted as a Message Page, as defined in annex 28C of IEEE 802.3u. Otherwise, the code is interperated as an Unformatted Page, and the interpretation is application specific. The default value of the CODE represents a Null Page as defined in Annex 28C of IEEE 802.3u.

Table 23. 0x0008 Auto-Negotiation Link Partner Ability Next Page Register (ANLNPTR)

BIT	NAME	TYPE	DEFAULT	FUNCTION
15	Next Page	RO	0	**Next Page Indication:** 1 = Advertise desire to send additional next pages 0 = Do not advertise desire to send additional next pages
14	Acknowledge	RO	0	**Acknowledge:** 1 = Link partner acknowledges reception of link code word 0 = Link partner does not acknowledge reception of link code work
13	Message Page	RO	0	**Message Page:** 1 = Current page is a message page 0 = Current page is an unformatted page
12	Acknowledge 2	RO	0	**Acknowledge2:** 1 = Will comply with message 0 = Cannot comply with message Acknowledge2 is used by the next page function to indicate that Local Device has the ability to comply with the message received.
11	Toggle	RO	0	**Toggle:** 1 = Toggle bit in previously transmitted Link Code Word was 0 0 = Toggle bit in previously transmitted Link Code Word was 1 Toggle is used by the Arbiitration function within Auto-Negotiation to synchronize with the Link Parnter during Next Page exchange. This bit always takes the opposite value of the Toggle bit in the previously exchanged Link Code Word.
10:0	Message/ Unformatted Field	RO	0 0000 0001	This field represents the code field of the next page transmission. If the Message Page bit is set (bit 13 of this register), then the code is interpreted as a Message Page, as defined in annex 28C of IEEE 802.3u. Otherwise, the code is interperated as an Unformatted Page, and the interpretation is application specific. The default value of the CODE represents a Null Page as defined in Annex 28C of IEEE 802.3u.

Table 24. 0x0009 Control Register #1 (CR1)

BIT	NAME	TYPE	DEFAULT	FUNCTION
15:10	Reserved	RO	0	Reserved
9	RMII Enhanced Mode	RW	0	**RMII Enhanced Mode:** 1 = Enable RMII Enhanced Mode 0 = RMII operated in normal mode In normal RMII mode, if the line is not idle, CRS_DV goes high. As soon as the False Carrier is detected, RX_ER is asserted and RXD is set to "2" (0010). This situation remains for the duration of the receive event. While in enhanced mode, CRS_DV is disqualified and de-asserted when the False Carrier is detected. This status also remains for the duration of the receive event. In addition, in normal mode, the start of the packet is intact. Each symbol error is indicatied by setting RX_ER high. The data on RXD is replaced with "1" starting with the first symbol error. While in enhanced mode, the CRS_DV is de-asserted with the first symbol error.
8	TDR Auto-Run	RW	0	**TDR Auto-Run at Link Down:** 1 = Enable execution of TDR procedure after link down event 0 = Disable automatic execution of TDR
7	Link Loss Recovery	RW	0	**Link Loss Recovery:** 1 = Enable Link Loss Recovery mechanism 0 = Normal Link Loss operation This mode allows recovery from short interference and continue to hold the link up for a few additional mSec until the short interference is gone and the signal is OK. Under Normal Link Loss operation, Link status will go down approximately 250μs from signal loss.
6	Fast Auto MDIX	RW	0	**Fast Auto-MDIX:** 1 = Enable Fast Auto-MDIX 0 = Normal Auto-MDIX If both link partners are configured to work in Force 100Base-TX mode (Auto-Negotiation disabled), this mode enables Automatic MDI/MDIX resolution in a shortened time.
5	Robust Auto MDIX	RW	0	**Robust Auto-MDIX:** 1 = Enable Robust Auto-MDIX 0 = Disable Auto-MDIX If link partners are configured for operational modes that are not supported by normal Auto-MDIX, Robust Auto-MDIX allows MDI/MDIX resolution and prevents deadlock. When the DP83822 is strapped for 100 Mbps operation with Auto-MDIX capabilities, Robust Auto-MDIX will be automatically set to aid in MDI/MDIX resolution and deadlock prevention.
4	Fast Auto-Negotiation Enable	RW	0	**Fast Auto-Negotiation Enable:** 1 = Enable Fast Auto-Negotiation 0 = Disable Fast Auto-Negotiation The PHY Auto-Negotiaties using timer setting according to Fast Auto-Negotiation Select bits (bits[3:2] in this register).
3:2	Fast Auto-Negotiation Select	RW	0	**Fast Auto-Negotiation Select Bits:** Adjusting these bits reduces the time it takes to Auto-Negotiate between two PHYs. In Fast Auto-Negotiation, both PHYs should be set to the same configuration. These 2 bits define the duration for each state of the Auto-Negotiation process according to the table above. The new duration time must be enabled by setting "Fast Auto Negotiation Enable" (bit [4] of this register). Note: Using this mode in cases where both link partners are not configured to the same Fast-Autonegotiation configuration might produce scenarios with unexpected behavior.

Fast Auto-Negotiation Select	Break Link Timer	Link Fail Inhibit Timer	Auto-Negotitation Wait Timer
<00>	80	50	35
<01>	120	75	50
<10>	240	150	100
<11>	NA	NA	NA

Table 24. 0x0009 Control Register #1 (CR1) (continued)

BIT	NAME	TYPE	DEFAULT	FUNCTION
1	Fast RX_DV Detection	RW	0	**Fast RX_DV Detection:** 1 = Enable Fast RX_DV detection 0 = Diable Fast RX_DV detection When Fast RX_DV is enabled, RX_DV will assert high on receive packet due to detection of the /J/ symbol only. If a consecutive /K/ does not appear, RX_ER is generated. In normal mode, RX_DV will only be asserted after detection of /JK/.
0	Reserved	RO	0	**Reserved**

Table 25. 0x000A Control Register #2 (CR2)

BIT	NAME	TYPE	DEFAULT	FUNCTION
15	100Base-TX Force Far-End Link drop	RW	0	**100Base-TX Force Far-End Link Drop:** Writing a 1 asserts the 100Base-TX Force Far-End link drop mode. In this mode (only valid for 100 Mbps), the PHY disables the TX upon link drop to allow the far-end peer to drop its link as well, thus allowing both link partners to be aware of the system link failure. This mode exceeds the standard definition of force 100 Mbps.
14	100Base-FX Enable	RW, Strap	0	**100Base-FX Enable:** 1 = 100Base-FX mode enabled 0 = 100Base-FX mode disabled
13:7	Reserved	RW	00 0001 0	**Reserved**
6	Fast Link-Up in Parallel Detect	RW	0	**Fast Link-Up in Parallel Detect Mode:** 1 = Enable Fast Link-Up time during Paralled Detection 0 = Normal Parallel Detection Link establishment In Fast Auto MDIX and in Robust Auto-MDIX modes (bit[6] and bit[5] in register CR1), this bit is automatically set.
5	Extended Full-Duplex Ability	RW	0	**Extended Full-Duplex Ability:** 1 = Enable Extended Full-Duplex Ability 0 = Diable Extended Full-Duplex Ability In Extended Full-Duplex ability, when the PHY is set to Auto-Negotiation or Force 100Base-TX and the link partner is operated in Force 100Base-TX, the link is always Full-Duplex. When disabled, the decision to work in Full-Duplex or Half-Duplex mode follows IEEE specification.
4	Enhanced LED Link	RW	0	**Enhanced LED Link:** 1 = LED ON only when link is 100Base-TX Full-Duplex mode 0 = LED ON when link is established In Enhanced LED Link mode, TX/RX BLINK on activity is disabled for this LED pin. LED will only indicate LINK for established 100Base-TX Full-Duplex links.
3	Isolate MII in 100Base-TX Half-Duplex or 10Base-Te	RW	0	**Isolate MII:** 1 = Isolate MII Enabled 0 = Normal MII output operation In Isolate MII, MII outputs are isolated when Half-Duplex link established for 100Base-TX or when Half-Duplex or Full-Duplex link established for 10Base-Te.
2	RX_ER During IDLE	RW	1	**Detection of Receive Symbol Error During IDLE State:** 1 = Enable detection of Receive symbol error during IDLE state 0 = Disable detection of Receive symbol error during IDLE state
1	Odd-Nibble Detection Disable	RW	0	**Detection of Transmit Error:** 1 = Disable detection of transmit error in odd-nibble boundary 0 = Enable detection of transmit error in odd-nibble boundary Detection of odd-nibble will extend TX_EN by one additional TX_CLK cycle and behaves as if TX_ER were asserted during that additional cycle
0	RMII Receive Clock	RW	0	**RMII Receive Clock:** 1 = RMII Data (RXD[1:0]) is sampled and referenced to RX_CLK 0 = RMII Data (RXD[1:0]) is sampled and referenced to XI

Table 26. 0x000B Control Register #3 (CR3)

BIT	NAME	TYPE	DEFAULT	FUNCTION
15:11	Reserved	RW	0001 0	**Reserved**
10	Descrambler Fast Link Down Mode	RW	0	**Descrambler Fast Link Drop:** 1 = Drop the link on descrambler link loss 0 = Do not drop the link on descrambler link loss This option can be enabled in parallel to the other fast link down modes in bits[3:0].
9:7	Reserved	RW	0	**Reserved**
6	Polarity Swap	RW	0	**Polarity Swap:** 1 = Inverted polarity on both pairs: TD+ and TD-, RD+ and RD- 0 = Normal polarity **Port Mirror Function:** To enable port mirroring, set this bit and bit [5] high.
5	MDI/MDIX Swap	RW	0	**MDI/MDIX Swap:** 1 = Swap MDI pairs (Receive on TD pair, Transmit on RD pair) 0 = MDI pairs normal (Receive on RD pair, Transmit on TD pair) **Port Mirror Function:** To enable port mirroring, set this bit and bit[6] high.
4	Reserved	RW	0	**Reserved**
3:0	Fast Link Down Mode	RW	0000	**Fast Link Down Modes:** **Bit 3** Drop the link based on **RX Error count** of the MII interface. When a predefined number of 32 RX Error occurences in a 10µs interval is reached, the link will be dropped. **Bit 2** Drop the link based on **MLT3 Error count** (Violation of the MLT3 coding in the DSP output). When a predefined number of 20 MLT3 Error occurences in a 10µs interval is reached, the link will be dropped. **Bit 1** Drop the link based on **Low SNR Threshold**. When a predefined number of 20 Threshold crossing occurences in a 10µs interval is reached, the link will be dropped. **Bit 0** Drop the link based on **Signal/Energy Loss** indication. When the Energy detector indicates Energy Loss, the link will be dropped. Typical reaction time is 10µs. The Fast Link Down function is an OR of all 5 options (bit[10] and bits[3:0]), the designer can enable any combination of these conditions.

Table 27. 0x000D Register Control Register (REGCR)

BIT	NAME	TYPE	DEFAULT	FUNCTION
15:14	Extended Register Command	RW	0	**Extended Register Command:** 00 = Address 01 = Data, no post increment 10 = Data, post increment on read and write 11 = Data, post increment on write only
13:5	Reserved	RO	0	**Reserved**
4:0	DEVAD	RW	0	**Device Address:** Bits[4:0] are the device address, DEVAD, that directs any accesses of ADDAR register (0x000E) to the appropriate MMD. Specifically, the DP83822 uses the vendor specific DEVAD [4:0] = "11111" for accesses to registers 0x04D1 and lower. For MMD3 access, the DEVAD[4:0] = '00011'. For MMD7 access, the DEVAD[4:0] = '00111'. All accesses through registers REGCR and ADDAR should use the DEVAD for either MMD, MMD3 or MMD7. Transactions with other DEVAD are ignored.

Table 28. 0x000E Data Register (ADDAR)

BIT	NAME	TYPE	DEFAULT	FUNCTION
15:0	Address/Data	RW	0	If REGCR register bits[15:14] = '00', holds the MMD DEVAD's address register, otherwise holds the MMD DEVAD's data.

Table 29. 0x000F Fast Link Down Status Register (FLDS)

BIT	NAME	TYPE	DEFAULT	FUNCTION
15:9	Reserved	RO	0	**Reserved**
8:4	Fast Link Down Status	RO, LH	0	**Fast Link Down Status:** 1 0000 = Descrambler Loss Sync 0 1000 = RX Errors 0 0100 = MLT3 Errors 0 0010 = SNR Level 0 0001 = Signal/Energy Lost Status Registers that latch high each time a given Fast Link Down mode is activated and causes a link drop (assuming the modes were enabled)
3:0	Reserved	RO	0	**Reserved**

Table 30. 0x0010 PHY Status Register (PHYSTS)

BIT	NAME	TYPE	DEFAULT	FUNCTION
15	Reserved	RO	0	**Reserved**
14	MDI/MDIX Mode	RO	0	**MDI/MDIX Mode Status:** 1 = MDI Pairs swapped (Receive on TD pair, Transmit on RD pair) 0 = MDI Pairs normal (Receive on RD pair, Transmit on TD pair)
13	Receive Error Latch	RO, LH	0	**Receive Error Latch:** 1 = Receive error event has occurred 0 = No receive error event has occurred Receive error event has occured since last read of RECR register (address 0x0015). This bit will be cleared upon a read of the RECR register.
12	Polarity Status	RO, LH	0	**Polarity Status**: 1 = Inverted Polarity detected 0 = Correct Polarity detected This bit is a duplication of bit[4] in the 10BTSCR register (address 0x001A). This bit will be cleared upon a read of the 10BTSCR register, but not upon a read of the PHYSTS register.
11	False Carrier Sense Latch	RO, LH	0	**False Carrier Sense Latch:** 1 = False Carrier event has occurred 0 = No False Carrier event has occurred False Carrier event has occurred since last read of FCSCR register (address 0x0014). This bit will be cleared upon a read of the FCSR register.
10	Signal Detect	RO, LL	0	**Signal Detect:** Active high 100Base-TX unconditional Signal Detect indication from PMD **Note:** During EEE_LPI the value of this register bit should be ignored
9	Descrambler Lock	RO, LL	0	**Descrambler Lock:** Active high 100Base-TX Descrambler Lock indication from PMD **Note:** During EEE_LPI the value of this register bit should be ignored
8	Page Received	RO	0	**Link Code Word Page Received:** 1 = A new Link Code Word Page has been received 0 = Link Code Word Page has not been received This bit is a duplicate of Page Received (bit[1]) in the ANER register and it is cleared on read of the ANER register (address 0x0006).
7	MII Interrupt	RO, LH	0	**MII Interrupt Pending:** 1 = Indicates that an internal interrupt is pending 0 = No interrupt pending Interrupt source can be determined by reading the MISR register (0x0012). Reading the MISR will clear this interrupt bit indication.
6	Remote Fault	RO	0	**Remote Fault:** 1 = Remote Fault condition detected 0 = No Remote Fault condition detected Fault criteria: notification from link partner of Remote Fault via Auto-Negotiation. Cleared on read of BMSR register (address 0x0001) or by reset.

Table 30. 0x0010 PHY Status Register (PHYSTS) (continued)

BIT	NAME	TYPE	DEFAULT	FUNCTION
5	Jabber Detect	RO	0	**Jabber Detection:** 1 = Jabber condition detected 0 = No Jabber This bit is only for 10 Mbps operation. This bit is a duplicate of the Jabber Detect bit in the BMSR register (address 0x0001) and will not be cleared upon a read of the PHYSTS register.
4	Auto-Negotiation Status	RO	0	**Auto-Negotiation Status:** 1 = Auto-Negotiation complete 0 = Auto-Negotiation not complete
3	MII Loopback Status	RO	0	**MII Loopback Status:** 1 = Loopback enabled 0 = Normal operation
2	Duplex Status	RO	0	**Duplex Status:** 1 = Full-Duplex mode 0 = Half-Duplex mode
1	Speed Status	RO	0	**Speed Status:** 1 = 10 Mbps mode 0 = 100 Mbps mode
0	Link Status	RO	0	**Link Status:** 1 = Valid link established (for either 10 Mbps or 100 Mbps) 0 = No link established This bit is duplicated from the Link Status bit in the BMSR register (address 0x0001) and will not be cleared upon a read of the PHYSTS register.

Table 31. 0x0011 PHY Specific Control Register (PHYSCR)

BIT	NAME	TYPE	DEFAULT	FUNCTION
15	Disable PLL	RW	0	**Disable PLL:** 1 = Disable internal clocks circuitry 0 = Normal operation **Note:** clock circuitry can be disabled only in IEEE power down mode.
14	Power Save Mode Enable	RW	0	**Power Save Mode Enable:** 1 = Enable power save modes 0 = Normal operation
13:12	Power Save Modes	RW	00	**Power Saving Modes Selection Field:** Power Save Mode Enable (bit[14]) must be set to '1' for power save modes to be enabled.

Power Mode	Name	Description
<00>	Normal	Normal operation mode. PHY is fully functional.
<01>	Reserved	Reserved
<10>	Active Sleep	Low Power Active Energy Saving mode that shuts down all internal circuitry besides SMI and energy detect functionalities. In this mode the PHY sends NLP every 1.4 seconds to wake up link partner. Automatic power-up is done when link partner is detected.
<11>	Passive Sleep	Low Power Passive Energy Saving mode that shuts down all internal circuitry besides SMI and energy detect functionalities. Automatic power-up is done when link partner is detected.

11	Scrambler Bypass	RW	0	**Scrambler Bypass:** 1 = Scrambler bypass enabled 0 = Scrambler bypass disabled
10	Reserved	RW	0	**Reserved**

Table 31. 0x0011 PHY Specific Control Register (PHYSCR) (continued)

BIT	NAME	TYPE	DEFAULT	FUNCTION
9:8	Loopback FIFO Depth	RW	01	**Far-End Loopback FIFO Depth:** 00 = 4 nibbles FIFO 01 = 5 nibbles FIFO 10 = 6 nibbles FIFO 11 = 8 nibbles FIFO This FIFO is used to adjust RX (receive) clock rate to TX clock rate. FIFO depth needs to be set based on expected maximum packet size and clock accuracy. Default value sets to 5 nibbles.
7:5	Reserved	RO	0	**Reserved**
4	COL Full-Duplex Enable	RW	0	**Collision in Full-Duplex Mode:** 1 = Enable Collision generation signaling in Full-Duplex mode 0 = Disable Collision in Full-Duplex mode **Note:** When in Half-Duplex mode, Collision will always be active.
3	Interrupt Polarity	RW	1	**Interrupt Polarity:** 1 = Normal operation is 1 logic and during interrupt is 0 logic 0 = Normal operation is 0 logic and during interrupt is 1 logic
2	Test Interrupt	RW	0	**Test Interrupt:** 1 = Generate an interrupt 0 = Do not generate interrupt Forces the PHY to generate an interrupt to facilitate interrupt testing. Interrupts will continue to be generated as long as this bit remains set.
1	Interrupt Enable	RW	0	**Interrupt Enable:** 1 = Enable event based interrupts 0 = Disable event based interrupts Enable interrupt dependent on the event enables in the MISR register (address 0x0012).
0	Interrupt Output Enable	RW	0	**Interrupt Output Enable:** 1 = INT/PWDN_N is an interrupt output 0 = INT/PWDN_N is a Power Down pin Enable active low interrupt events via the INT/PWDN_N pin by configuring the INT/PWDN_N pin as an output.

Table 32. 0x0012 MII Interrupt Status Register #1 (MISR1)

BIT	NAME	TYPE	DEFAULT	FUNCTION
15	Link Quality Interrupt	RO, LH	0	**Change of Link Quality Status Interrupt:** 1 = Change of link quality when link is ON 0 = Link quality is Good
14	Energy Detect Interrupt	RO, LH	0	**Change of Energy Detection Status Interrupt:** 1 = Change of energy detected 0 = No change of energy detected
13	Link Status Changed Interrupt	RO, LH	0	**Change of Link Status Interrupt:** 1 = Change of link status interrupt is pending 0 = No change of link status
12	Speed Changed Interrupt	RO, LH	0	**Change of Speed Status Interrupt:** 1 = Change of speed status interrupt is pending 0 = No change of speed status
11	Duplex Mode Changed Interrupt	RO, LH	0	**Change of Duplex Status Interrupt:** 1 = Change of duplex status interrupt is pending 0 = No change of duplex status
10	Auto-Negotiation Completed Interrupt	RO, LH	0	**Auto-Negotiation Complete Interrupt:** 1 = Auto-Negotiation complete interrupt is pending 0 = No Auto-Negotiation complete event is pending
9	False Carrier Counter Half-Full Interrupt	RO, LH	0	**False Carrier Counter Half-Full Interrupt:** 1 = False Carrier HF interrupt is pending 0 = False Carrier HF event is not pending False Carrier counter (Register FCSCR, address 0x0014) exceeds half-full interrupt is pending.

Table 32. 0x0012 MII Interrupt Status Register #1 (MISR1) (continued)

BIT	NAME	TYPE	DEFAULT	FUNCTION
8	Receive Error Counter Half-Full Interrupt	RO, LH	0	**Receiver Error Counter Half-Full Interrupt:** 1 = Receive Error HF interrupt is pending 0 = Receive Error HF event is not pending Receiver Error counter (Register RECR, address 0x0015) exceeds half-full interrupt is pending.
7	Link Quality Interrupt Enable	RW	0	**Enable** interrupt on change of link quality
6	Energy Detect Interrupt Enable	RW	0	**Enable** interrupt on change of energy detection
5	Link Status Changed Enable	RW	0	**Enable** interrupt on change of link status
4	Speed Changed Interrupt Enable	RW	0	**Enable** Interrupt on change of speed status
3	Duplex Mode Changed Interrupt Enable	RW	0	**Enable** Interrupt on change of duplex status
2	Auto-Negotiation Completed Enable	RW	0	**Enable** Interrupt on Auto-negotiation complete event
1	False Carrier HF Enable	RW	0	**Enable** Interrupt on False Carrier Counter Register half-full event
0	Receive Error HF Enable	RW	0	**Enable** Interrupt on Receive Error Counter Register half-full event

Table 33. 0x0013 MII Interrupt Status Register #2 (MISR2)

BIT	NAME	TYPE	DEFAULT	FUNCTION
15	EEE Error Interrupt	RO, LH	0	**Energy Efficient Ethernet Error Interrupt:** 1 = EEE error has occurred 0 = EEE error has not occurred
14	Auto-Negotiation Error Interrupt	RO, LH	0	**Auto-Negotiation Error Interrupt:** 1 = Auto-Negotiation error interrupt is pending 0 = No Auto-Negotiation error event pending
13	Page Received Interrupt	RO, LH	0	**Page Receiver Interrupt:** 1 = Page has been received 0 = Page has not been received
12	Loopback FIFO OF/UF Event Interrupt	RO, LH	0	**Loopback FIFO Overflow/Underflow Event Interrupt:** 1 = FIFO Overflow/Underflow event interrupt pending 0 = No FIFO Overflow/Underflow event pending
11	MDI Crossover Change Interrupt	RO, LH	0	**MDI/MDIX Crossover Status Change Interrupt:** 1 = MDI crossover status changed interrupt is pending 0 = MDI crossover status has not changed
10	Sleep Mode Interrupt	RO, LH	0	**Sleep Mode Event Interrupt:** 1 = Sleep mode event interrupt is pending 0 = No Sleep mode event pending
9	Polarity Changed Interrupt / WoL Packet Received Interrupt	RO, LH	0	**Polarity Change Interrupt / WoL Packet Received Interrupt:** 1 = Data polarity interrupt pending / WoL packet was recieved 0 = No Data polarity pending / No WoL packet received
8	Jabber Detect Interrupt	RO, LH	0	**Jabber Detect Event Interrupt:** 1 = Jabber detect event interrupt pending 0 = No Jabber detect event pending
7	EEE Error Interrupt Enable	RW	0	**Enable** interrupt on EEE Error
6	Auto-Negotiation Error Interrupt Enable	RW	0	**Enable** Interrupt on Auto-Negotiation error event
5	Page Received Interrupt Enable	RW	0	**Enable** Interrupt on page receive event
4	Loopback FIFO OF/UF Enable	RW	0	**Enable** Interrupt on loopback FIFO Overflow/Underflow event
3	MDI Crossover Change Enable	RW	0	**Enable** Interrupt on change of MDI/X status
2	Sleep Mode Event Enable	RW	0	**Enable** Interrupt on sleep mode event
1	Polarity Changed / WoL Packet Enable	RW	0	**Enable** Interrupt on change of polarity status
0	Jabber Detect Enable	RW	0	**Enable** Interrupt on Jabber detection event

Table 34. 0x0014 False Carrier Sense Counter Register (FCSCR)

BIT	NAME	TYPE	DEFAULT	FUNCTION
15:8	Reserved	RO	0	**Reserved**
7:0	False Carrier Event Counter	RO, COR	0	**False Carrier Event Counter:** This 8-bit counter increments on every false carrier event. This counter stops when it reaches its maximum count (FFh). When the counter exceeds half-full (7Fh), an interrupt event is generated. This register is cleared on read.

Table 35. 0x0015 Receive Error Count Register (RECR)

BIT	NAME	TYPE	DEFAULT	FUNCTION
15:0	Receive Error Counter	RO, COR	0	**RX_ER Counter:** When a valid carrier is presented (only while RXDV is set), and there is at least one occurrence of an invalid data symbol, this 16-bit counter increments for each receive error detected. The RX_ER counter does not count in MII loopback mode. The counter stops when it reaches its maximum count (FFh). When the counter exceeds half-full (7Fh), an interrupt is generated. This register is cleared on read.

Table 36. 0x0016 BIST Control Register (BISCR)

BIT	NAME	TYPE	DEFAULT	FUNCTION
15	Reserved	RO	0	**Reserved**
14	BIST Error Counter Mode	RW	0	**BIST Error Counter Mode:** 1 = Continuous mode 0 = Single mode Continuous mode, when the BIST Error counter reaches its max value, a pulse is generated and the counter starts counting from zero again. When in Single mode, if the BIST Error Counter reaches its max value, PRBS checker will stop counting.
13	PRBS Checker	RW	0	**PRBS Checker:** 1 = PRBS Checker Enabled 0 = PRBS Checker Disabled When PRBS checker is enabled, DP83822 will check PRBS data received.
12	Packet Generation Enable	RW	0	**Packet Generation Enable:** 1 = Enable packet generator with PRBS data 0 = Disable packet generator
11	PRBS Checker Lock/Sync	RO	0	**PRBS Checker Lock/Sync Indication:** 1 = PRBS checker is locked and synced on received bit stream 0 = PRBS checker is not locked
10	PRBS Checker Sync Loss	RO, LH	0	**PRBS Checker Sync Loss Indication:** 1 = PRBS checker has lost sync 0 = PRBS checker has not lost sync
9	Packet Generator Status	RO	0	**Packet Generation Status Indication:** 1 = Packet Generator is active and generating packets 0 = Packet Generator is off
8	Power Mode	RO	1	**Sleep Mode Indication:** 1 = Indicates that the PHY is in normal power mode 0 = Indicates that the PHY is in one of the sleep modes
7	Reserved	RO	0	**Reserved**
6	Transmit in MII Loopback	RW	0	**Transmit Data in MII Loopback Mode (valid only at 100 Mbps):** 1 = Enable transmission 0 = Disable transmission When enabled, data received from the MAC on the TX pins will be routed to the MDI in parallel to the MII loopback (to RX pins). This bit may be set only in MII Loopback mode - setting bit[14] in in BMCR register (address 0x0000). When disabled, data from the MAC is not transmitted to the MDI.
5	Reserved	RO	0	**Reserved**

Table 36. 0x0016 BIST Control Register (BISCR) (continued)

BIT	NAME	TYPE	DEFAULT	FUNCTION
4:0	Loopback Mode	RW	0	**Loopback Mode Select:** The PHY provides several options for loopback that test and verify various functional blocks within the PHY. Enabling loopback mode allows in-circuit testing of the DP83822 digital and analog data paths **Near-end Loopback** 00001 = PCS Input Loopback 00010 = PCS Output Loopback 00100 = Digital Loopback 01000 = Analog Loopback (requires 100-Ω termination) **Far-end Loopback** 10000 = Reverse Loopback

Table 37. 0x0017 RMII and Status Register (RCSR)

BIT	NAME	TYPE	DEFAULT	FUNCTION
15:13	Reserved	RO	0	**Reserved**
12	RGMII RX Clock Shift	RW	0	**RGMII RX Clock Shift:** 1 = Receive path internal clock shift is enabled 0 = Receive path internal clock shift is disabled When enabled, receive path internal clock (RX_CLK) is delayed by 3.5ns relative to recieve data. When disabled, data and clock are in align mode.
11	RGMII TX Clock Shift	RW	0	**RGMII TX Clock Shift:** 1 = Transmit path internal clock shift is disabled 0 = Transmit path internal clock shift is enabled When enabled, transmit path internal clock (TX_CLK) is delayed by 3.5ns relative to transmit data.
10	RGMII TX Synced	RW	0	**RGMII TX Clock Sync:** 1 = PHY and MAC share same clock reference 0 = PHY operates from same or independent clock source as MAC This mode, when enabled, reduces latency since both MAC and PHY are synchronized to the same clock source. This mode can also be used when enabling the PHY Clock Output by connecting the MAC to the PHY Output Clock.
9	RGMII Mode	RW, Strap	0	**RGMII Mode Enable:** 1 = Enable RGMII mode of operation 0 = Mode determined by bit[5]
8	RMII TX Clock Shift	RW	0	**RMII TX Clock Shift:** 1 = Transmit path internal clock shift is enabled 0 = Transmit path internal clock shift is disabled
7	RMII Clock Select	RW, Strap	0	**RMII Reference Clock Select:** Strap XI_50 determines the clock reference requirement. 1 = 50-MHz clock reference, CMOS-level oscillator 0 = 25-MHz clock reference, crystal or CMOS-level oscillator
6	RMII Recovered Clock Async FIFO Bypass	RW	0	**RMII Recovered Clock Async FIFO Bypass:** 0 = Bypass Asynchronous FIFO 1 = Normal operation When in RMII Recovered Clock mode, the asynchronous FIFO can be bypassed to reduce the receive path latency within the DP83822. 50-MHz clock is outputted on RX_CLK when in Async fifo bypass
5	RMII Mode	RW	0	**RMII Mode Enable:** 1 = Enable RMII mode of operation 0 = Enable MII mode of operation
4	RMII Revision Select	RW	0	**RMII Revision Select:** 1 = RMII revision 1.0 0 = RMII revision 1.2 RMII revision 1.0, CRS_DV will remain asserted until final data is transferred. CRS_DV will not toggle at the end of a packet. RMII revision 1.2, CRS_DV will toggle at the end of a packet to indicate de-assertion of CRS.

Table 37. 0x0017 RMII and Status Register (RCSR) (continued)

BIT	NAME	TYPE	DEFAULT	FUNCTION
3	RMII Overflow Status	RO, COR	0	**RX FIFO Overflow Status:** 1 = Overflow detected 0 = Normal
2	RMII Underflow Status	RO, COR	0	**RX FIFO Underflow Status:** 1 = Underflow detected 0 = Normal
1:0	Receive Elasticity Buffer Size	RW	01	**Receive Elasticity Buffer Size:** This field controls the Receive Elasticity Buffer which allows for frequency variation tolerance between the 50-MHz RMII clock and the recovered data. The following values indicate the tolerance in bits for a single packet. The minimum setting allows for standard Ethernet frame sizes at ±50ppm accuracy. For greater frequency tolerance, the packet lengths may be scaled (for ±100ppm), divide the packet lengths by 2). 00 = 14 bit tolerance (up to 16800 byte packets) 01 = 2 bit tolerance (up to 2400 byte packets) 10 = 6 bit tolerance (up to 7200 byte packets) 11 = 10 bit tolerance (up to 12000 byte packets)

Table 38. 0x0018 LED Control Register (LEDCR)

BIT	NAME	TYPE	DEFAULT	FUNCTION
15:11	Reserved	RO	0	**Reserved**
10:9	Blink Rate	RW	10	**LED_0 Blinking Rate (ON/OFF duration):** 00 = 20Hz (50 ms) 01 = 10Hz (100 ms) 10 = 5Hz (200 ms) 11 = 2Hz (500 ms)
8	Reserved	RW	0	**Reserved**
7	LED_0 Polarity	RW, Strap	0	**LED_0 Link Polarity Setting:** 1 = Active High polarity setting 0 = Active Low polarity setting LED_0 polarity defined by strapping value of this pin. This register allows for override of this strap value.
6:5	Reserved	RW	0	**Reserved**
4	Drive LED_0	RW	0	**Drive Link LED_0 Select:** 1 = Drive value of ON/OFF bit[1] onto LED_0 output pin 0 = Normal operation
3:2	Reserved	RW	0	**Reserved**
1	LED_0 ON/OFF Setting	RW	0	Value to force LED_0 output
0	Reserved	RW	0	**Reserved**

Table 39. 0x0019 PHY Control Register (PHYCR)

BIT	NAME	TYPE	DEFAULT	FUNCTION
15	Auto MDI/X Enable	RW, Strap	0	**Auto-MDIX Enable:** 1 = Enable Auto-Negotiation Auto-MDIX capability 0 = Disable Auto-Negotiation Auto-MDIX capability
14	Force MDI/X	RW	0	**Force MDIX:** 1 = Force MDI pairs to cross (MDIX) 0 = Normal operation (MDI) When Force MDI/X is enabled, receive data is on the TD pair and transmit data is on the RD pair. When disabled, receive data is on the RD pair and transmit data is on the TD pair.
13	Pause RX Status	RO	0	**Pause Receive Negotiation Status:** Indicates that pause receive should be enabled in the MAC. Based on bits[11:10] in ANAR register and bits[11:10] in ANLPAR register settings. The function shall be enabled according to IEEE 802.3 Annex 28B Table 28B-3, "Pause Resolution", only if the Auto-Negotiation highest common denominator is a Full-Duplex technology.

Table 39. 0x0019 PHY Control Register (PHYCR) (continued)

BIT	NAME	TYPE	DEFAULT	FUNCTION
12	Pause TX Status	RO	0	**Pause Transmit Negotiated Status:** Indicates that pause should be enabled in the MAC. Based on bits[11:10] in ANAR register and bits[11:10] in ANLPAR register settings. This function shall be enabled according to IEEE 802.3 Annex 28B Table 28B-3, "Pause Resolution", only if the Auto-Negotiation highest common denominator is a Full-Duplex technology.
11	MII Link Status	RO	0	**MII Link Status:** 1 = 100Base-TX Full-Duplex link is active 0 = No active 100Base-TX Full-Duplex link
10:8	Reserved	RO	0	**Reserved**
7	Bypass LED Stretching	RW	0	**Bypass LED Stretching:** 1 = Bypass LED stretching 0 = Normal LED operation Set this bit to '1' to bypass the LED stretching, the LED reflects the internal value.
6	Reserved	RW	0	**Reserved**
5	LED Configuration	RW, Strap	1	**Configuration** / **LED_CFG** / **LED_0** 1 / 1 / ON for LINK, OFF for no LINK 2 / 0 / ON for LINK, BLINK for TX/RX Activity
4:0	PHY Address	RO, Strap	0000 1	**PHY Address:** Strapping configuration for PHY Address

Table 40. 0x001A 10Base-Te Status/Control Register (10BTSCR)

BIT	NAME	TYPE	DEFAULT	FUNCTION
15:14	Reserved	RO	0	**Reserved**
13	Receiver Threshold Enable	RW	0	**Lower Receiver Threshold Enable:** 1 = Enable 10Base-Te lower receiver threshold 0 = Normal 10Base-Te operation When enabled, receiver threshold is lowered to allow for operation with longer cables.
12:9	Squelch	RW	0000	**Squelch Configuration:** Used to set the Peak Squelch 'ON' threshold for the 10Base-Te receiver. Starting from 200mV to 600mV, step size of 50mV with some overlapping as shown below: 0000 = 200mV 0001 = 250mV 0010 = 300mV 0011 = 350mV 0100 = 400mV 0101 = 450mV 0110 = 500mV 0111 = 550mV 1000 = 600mV
8	Reserved	RW	0	**Reserved**
7	NLP Disable	RW	0	**NLP Transmission Control:** 1 = Disable transmission of NLPs 0 = Enable transmission of NLPs
6:5	Reserved	RO	0	**Reserved**
4	Polarity Status	RO	0	**Polarity Status:** 1 = Inverted Polarity detected 0 = Correct Polarity detected This bit is a duplication of bit[12] in the PHYSTS register (0x0010). Both bits will be cleared upon a read of 10BTSCR register, but not upon a read of the PHYSTS register.
3:1	Reserved	RO	0	**Reserved**

Table 40. 0x001A 10Base-Te Status/Control Register (10BTSCR) (continued)

BIT	NAME	TYPE	DEFAULT	FUNCTION
0	Jabber Disable	RW	0	**Jabber Disable:** 1 = Jabber function disabled 0 = Jabber function enabled **Note:** This function is only applicable in 10Base-Te operation.

Table 41. 0x001B BIST Control and Status Register #1 (BICSR1)

BIT	NAME	TYPE	DEFAULT	FUNCTION
15:8	BIST Error Count	RO	0x0	**BIST Error Count:** Holds number of errored bytes received by the PRBS checker. Value in this register is locked and cleared when write is done to bit[15]. When BIST Error Counter Mode is set to '0', count stops on 0xFF (see register 0x0016) **Note:** Writing '1' to bit[15] will lock the counter's value for successive read operation and clear the BIST Error Counter.
7:0	BIST IPG Length	RW	0111 1101	**BIST IPG Length:** Inter Packet Gap (IPG) Length defines the size of the gap (in bytes) between any 2 successive packets generated by the BIST. Default value is 0x7D (equal to 500 bytes).

Table 42. 0x001C BIST Control and Status Register #2 (BICSR2)

BIT	NAME	TYPE	DEFAULT	FUNCTION
15:11	Reserved	RO	0	**Reserved**
10:0	BIST Packet Length	RW	101 1111 1111	**BIST Packet Length:** Length of the generated BIST packets. The value of this register defines the size (in bytes) of every packet that is generated by the BIST. Default value is 0x5EE, which is equal to 1518 bytes.

Table 43. 0x001E Cable Diagnostic Control Register (CDCR)

BIT	NAME	TYPE	DEFAULT	FUNCTION
15	Cable Diagnostic Start	RW	0	**Cable Diagnostic Process Start:** 1 = Start cable measurement 0 = Cable Diagnostic is disabled Diagnostic Start bit is cleared once Diagnostic Done indication bit is triggered.
14:2	Reserved	RO	0	**Reserved**
1	Cable Diagnostic Status	RO	0	**Cable Diagnostic Process Done:** 1 = Indication that cable measurement process is complete 0 = Cable Diagnostic had not completed
0	Cable Diagnostic Test Fail	RO	0	**Cable Diagnostic Process Fail:** 1 = Indication that cable measurement process failed 0 = Cable Diagnostic has not failed

Table 44. 0x001F PHY Reset Control Register (PHYRCR)

BIT	NAME	TYPE	DEFAULT	FUNCTION
15	Software Reset	RW, SC	0	**Software Reset:** 1 = Reset PHY 0 = Normal Operation This bit is self cleared and has the same effect as Hardware reset pin.
14	Digital Restart	RW, SC	0	**Digital Restart:** 1 = Restart PHY 0 = Normal Operation This bit is self cleared and resets all PHY digital circuitry except the registers.
13:0	Reserved	RW	0	**Reserved**

Table 45. 0x0025 Multi-LED Control Register (MLEDCR)

BIT	NAME	TYPE	DEFAULT	FUNCTION
15:10	Reserved	RW	0	**Reserved**
9	MLED Polarity Swap	RW	Strap	**MLED Polarity Swap:** The polarity of MLED depends on the routing configuration and the strap on COL pin. If the pin strap is Pull-Up then polarity is active low. If the pin strap is Pull-Down then polarity is active high. 0 = Active Low (default when pin strapped HIGH) 1 = Active High (default when pin strapped LOW)
8:7	Reserved	RW	0	**Reserved**
6:3	MLED Configuration (COL Pin)	RW	000 0	**MLED Configurations:** 000 0 = LINK OK 000 1 = RX/TX Activity 001 0 = TX Activity 001 1 = RX Activity 010 0 = Collision 010 1 = Speed, High for 100Base-TX 011 0 = Speed, High for 10Base-Te 011 1 = Full-Duplex 100 0 = LINK OK / BLINK on TX/RX Activity 100 1 = Active Stretch Signal 101 0 = MII LINK (100BT+FD) 101 1 = LPI Mode (EEE) 110 0 = TX/RX MII Error 110 1 = Link Lost 111 0 = Blink for PRBS error 111 1 = Reserved Link Lost, LED remains ON until BMCR register (address 0x0001) is read. Blink for PRBS Errors, LED remains ON for single error and remains until BICSR1 register (address 0x001B) is cleared.
2	Reserved	RW	0	**Reserved**
1:0	MLED Route to LED_0	RW	00	**MLED Route to LED_0:** 00 = MLED routed to COL 01 = Reserved 10 = Reserved 11 = MLED routed to LED_0

Table 46. 0x0027 Compliance Test Register (COMPT)

BIT	NAME	TYPE	DEFAULT	FUNCTION
15:5	Reserved	RW	0	**Reserved**
4	10Base-Te Test Patterns Enable	RW	0	**10Base-Te Test Pattern Enable:** 1 = Enable 10Base-Te Test Patterns 0 = Disable 10Base-Te Test Patterns

Table 46. 0x0027 Compliance Test Register (COMPT) (continued)

BIT	NAME	TYPE	DEFAULT	FUNCTION
3:0	Compliance Test Configuration	RW	0000	**Compliance Test Configuration Select:** Bit[4] in Register 0x0027 = 1, Enables 10Base-Te Test Patterns. Bit[4] in Register 0x0428 = 1, Enables 100Base-TX Test Modes Bits[3:0] select the **10Base-Te** test pattern, as follows: 0000 = Single NLP 0001 = Single Pulse 1 0010 = Single Pulse 0 0011 = Repetitive 1 0100 = Repetitive 0 0101 = Preamble (repetitive '10') 0110 = Single 1 followed by TP_IDLE 0111 = Single 0 followed by TP_IDLE 1000 = Repetitive '1001' sequence 1001 = Random 10Base-Te data 1010 = TP_IDLE_00 1011 = TP_IDLE_01 1100 = TP_IDLE_10 1101 = TP_IDLE_11 **100Base-TX** Test Mode is determined by bits {[5] in register 0x0428, [3:0] in register 0x0027}. The bits determine the number of 0's to follow a '1'. 0,0001 = Single '0' after a '1' 0,0010 = Two '0' after a '1' 0,0011 = Three '0' after a '1' 0,0100 = Four '0' after a '1' 0,0101 = Five '0' after a '1' 0,0110 = Six '0' after a '1' 0,0111 = Seven '0' after a '1' ... 1,1111 = Thirty one '0' after a '1' 0,0000 = Clears the shift register **Note 1:** To reconfigure the 100Base-TX Test Mode, bit[4] must be cleared in register 0x0428 and then reset to '1' to configure the new pattern. **Note 2:** When performing 100Base-TX or 10Base-Te tests modes, the speed must be forced using the Basic Mode Control Register (BMCR), address 0x0000.

Table 47. 0x003E IEEE 1588 PTP Pin Select Register (PTPPSEL)

BIT	NAME	TYPE	DEFAULT	FUNCTION
15:7	Reserved	RO	0	**Reserved**
6:4	IEEE 1588 TX Pin Select	RW	000	**IEEE 1588 TX Pin Select:** Assigns transmit SFD pulse indication to pin selected by value 001 = Reserved 010 = Reserved 011 = LED_0 Pin 100 = CRS Pin 101 = COL Pin 110 = INT/PWDN_N Pin 111 = No pulse output
3	Reserved	RO	0	**Reserved**
2:0	IEEE 1588 RX Pin Select	RW	000	**IEEE 1588 RX Pin Select:** Assigns receive SFD pulse indication to pin selected by value 001 = Reserved 010 = Reserved 011 = LED_0 Pin 100 = CRS Pin 101 = COL Pin 110 = INT/PWDN_N Pin 111 = No pulse output

Table 48. 0x003F IEEE 1588 PTP Configuration Register IEEE 1588 Precision Timing Configuration Register (PTPCFG)

BIT	NAME	TYPE	DEFAULT	FUNCTION
15:13	PTP Transmit Timing	RW	101	**PTP Transmit Timing:** Set IEEE 1588 indication for TX path (8ns step)
12:10	PTP Receive Timing	RW	101	**PTP Receive Timing:** Set IEEE 1588 indication for RX path (8ns step)
9:8	TX Error Input Pin	RW	00	**Configure TX Error Input Pin:** 00 = No TX Error 01 = Reserved 10 = Use INT/PWDN_N pin as TX error 11 = Use COL pin as TX error
7:0	Reserved	RW	1111 1111	**Reserved**

Table 49. 0x0042 TX_CLK Phase Shift Register (TXCPSR)

BIT	NAME	TYPE	DEFAULT	FUNCTION
15:5	Reserved	RO	0	**Reserved**
4	Phase Shift Enable	RW, SC	0	**TX Clock Phase Shift Enable:** 1 = Perform Phase Shift to TX_CLK 0 = No change in TX_CLK phase When enabled, TX_CLK phase shift is according to the value written to TX Clock Phase Shift Value (bits[4:0]).
3:0	Phase Shift Value	RW	0000	**TX Clock Phase Shift Value:** The value of this register represents the current phase shift between Reference clock at XI and MII tramsmit clock at TX_CLK. Any different value that will be written to these bits will shift TX_CLK by 4 times the difference (in ns). Example: If the value of the register is 0x0002, writing 0x0009 to this register will shift TX_CLK by 28ns. (4 times 7ns)

Table 50. 0x0106 Digital Filter Configuration Register 1 (DFCR1)

BIT	NAME	TYPE	DEFAULT	FUNCTION
15:0	Reserved	RW	1011 0000 1011 1011	**Reserved**

Table 51. 0x0107 Digital Filter Configuration Register 2 (DFCR2)

BIT	NAME	TYPE	DEFAULT	FUNCTION
15:0	Reserved	RW	0000 0110 0000 0101	**Reserved**

Table 52. 0x010F DSP Configuration Registers (DSPCR)

BIT	NAME	TYPE	DEFAULT	FUNCTION
15:0	Reserved	RW	0000 0011 0000 0000	**Reserved**

Table 53. 0x0114 Digital Feedback Equalizer Control Register (DFECR)

BIT	NAME	TYPE	DEFAULT	FUNCTION
15:0	Reserved	RW	0100 0000 0000 1010	**Reserved**

Table 54. 0x0116 AGC Bandwidth Control Register (AGCBCR)

BIT	NAME	TYPE	DEFAULT	FUNCTION
15:0	Reserved	RW	0000 0001 0100 1010	**Reserved**

Table 55. 0x0126 Digital Equalizer Timer Register (DETR)

BIT	NAME	TYPE	DEFAULT	FUNCTION
15:0	Reserved	RW	0100 0110 0001 1011	**Reserved**

Table 56. 0x0155 ALCD Control and Results 1 Register (ALCDRR1)

BIT	NAME	TYPE	DEFAULT	FUNCTION
15	ALCD Start Test	SC	0	**Active Link Cable Diagnostic Start:** 1 = Start ALCD test 0 = Do not start ALCD test
14:13	Reserved	RO	00	**Reserved**
12	ALCD Test Status	RO	1	**Active Link Cable Diagnostic Status:** 1 = ALCD is not complete 0 = ALCD is complete
11:4	ALCD Sum Out	RO	1111 0100	
3:0	Reserved	RW	0001	**Reserved**

Table 57. 0x0170 Cable Diagnostic Specific Control Register (CDSCR)

BIT	NAME	TYPE	DEFAULT	FUNCTION
15	Reserved	RO	0	**Reserved**
14	Cable Diagnostic Cross Disable	RW	0	**Cross TDR Diagnostic Mode:** 1 = Disable TDR Cross Mode 0 = Enable TDR Cross Mode When enabled, the TDR mechanism is looking for reflection on the other pair to check for shorts between pairs.
13	Cable Diagnostic TD Bypass	RW	0	**TD Diagnostic Bypass:** 1 = Bypass TD pair diagnostic 0 = TDR is executed on TD pair When enabled, TDR on TD pair will not be executed.
12	Cable Diagnostic RD Bypass	RW	0	**RD Diganostic Bypass:** 1= Bypass RD pair diagnostic 0 = TDR is executed on RD pair When enabled, TDR on RD pair will not be executed.
11	Reserved	RW	1	**Reserved**
10:8	Cable Diagnostic Average Cycles	RW	110	**Number of TDR Cycles to Average:** 000 = 1 TDR cycle 001 = 2 TDR cycles 010 = 4 TDR cycles 011 = 8 TDR cycles 100 = 16 TDR cycles 101 = 32 TDR cycles 110 = 64 TDR cycles 111 = Reserved
7:0	Reserved	RW	0101 0010	**Reserved**

Table 58. 0x0171 Cable Diagnostic Specific Control Register 2 (CDSCR2)

BIT	NAME	TYPE	DEFAULT	FUNCTION
15:4	Reserved	RW	1100 1000 0101	**Reserved**
3:0	TDR Pulse Control	RW	1100	Configure expected self reflection in TDR

Table 59. 0x0173 Cable Diagnostic Specific Control Register 3 (CDSCR3)

BIT	NAME	TYPE	DEFAULT	FUNCTION
15:8	Cable Length Configuration	RW	1111 1111	Configure duration of listening to detect long cable reflections
7:0	Reserved	RW	0001 1110	**Reserved**

Table 60. 0x0177 Cable Diagnostic Specific Control Register 4 (CDSCR4)

BIT	NAME	TYPE	DEFAULT	FUNCTION
15:13	Reserved	RW	000	**Reserved**
12:8	Short Cables Threshold	RW	1 1000	Threshold to compensate for strong reflections in short cables
7:0	Reserved	RW	1001 1011	**Reserved**

Table 61. 0x0180 Cable Diagnostic Location Result Register #1 (CDLRR1)

BIT	NAME	TYPE	DEFAULT	FUNCTION
15:8	TD Peak Location 2	RO	0000 0000	Location of the **Second** peak discovered by the TDR mechanism on Transmit Channel (TD). The value of these bits need to be translated into distance from the PHY.
7:0	TD Peak Location 1	RO	0000 0000	Location of the **First** peak discovered by the TDR mechanism on Transmit Channel (TD). The value of these bits need to be translated into distance from the PHY.

Table 62. 0x0181 Cable Diagnostic Location Result Register #2 (CDLRR2)

BIT	NAME	TYPE	DEFAULT	FUNCTION
15:8	TD Peak Location 4	RO	0000 0000	Location of the **Fourth** peak discovered by the TDR mechanism on Transmit Channel (TD). The value of these bits need to be translated into distance from the PHY.
7:0	TD Peak Location 3	RO	0000 0000	Location of the **Third** peak discovered by the TDR mechanism on Transmit Channel (TD). The value of these bits need to be translated into distance from the PHY.

Table 63. 0x0182 Cable Diagnostic Location Result Register #3 (CDLRR3)

BIT	NAME	TYPE	DEFAULT	FUNCTION
15:8	RD Peak Location 1	RO	0000 0000	Location of the **First** peak discovered by the TDR mechanism on Receive Channel (RD). The value of these bits need to be translated into distance from the PHY.
7:0	TD Peak Location 5	RO	0000 0000	Location of the **Fifth** peak discovered by the TDR mechanism on Transmit Channel (TD). The value of these bits need to be translated into distance from the PHY.

Table 64. 0x0183 Cable Diagnostic Location Result Register #4 (CDLRR4)

BIT	NAME	TYPE	DEFAULT	FUNCTION
15:8	RD Peak Location 3	RO	0000 0000	Location of the **Third** peak discovered by the TDR mechanism on Receive Channel (RD). The value of these bits need to be translated into distance from the PHY.
7:0	RD Peak Location 2	RO	0000 0000	Location of the **Second** peak discovered by the TDR mechanism on Receive Channel (RD). The value of these bits need to be translated into distance from the PHY.

Table 65. 0x0184 Cable Diagnostic Location Result Register #5 (CDLRR5)

BIT	NAME	TYPE	DEFAULT	FUNCTION
15:8	RD Peak Location 5	RO	0000 0000	Location of the **Fifth** peak discovered by the TDR mechanism on Receive Channel (RD). The value of these bits need to be translated into distance from the PHY.
7:0	RD Peak Location 4	RO	0000 0000	Location of the **Fourth** peak discovered by the TDR mechanism on Receive Channel (RD). The value of these bits need to be translated into distance from the PHY.

Table 66. 0x0185 Cable Diagnostic Amplitude Result Register #1 (CDLAR1)

BIT	NAME	TYPE	DEFAULT	FUNCTION
15	Reserved	RO	0	**Reserved**
14:8	TD Peak Amplitude 2	RO	000 0000	Amplitude of the **Second** peak discovered by the TDR mechanism on Transmit Channel (TD). The value of these bits is translated into type of cable fault and/or interference.
7	Reserved	RO	0	**Reserved**
6:0	TD Peak Amplitude 1	RO	000 0000	Amplitude of the **First** peak discovered by the TDR mechanism on Transmit Channel (TD). The value of these bits is translated into type of cable fault and/or interference.

Table 67. 0x0186 Cable Diagnostic Amplitude Result Register #2 (CDLAR2)

BIT	NAME	TYPE	DEFAULT	FUNCTION
15	Reserved	RO	0	**Reserved**
14:8	TD Peak Amplitude 4	RO	000 0000	Amplitude of the **Fourth** peak discovered by the TDR mechanism on Transmit Channel (TD). The value of these bits is translated into type of cable fault and/or interference.
7	Reserved	RO	0	**Reserved**
6:0	TD Peak Amplitude 3	RO	000 0000	Amplitude of the **Third** peak discovered by the TDR mechanism on Transmit Channel (TD). The value of these bits is translated into type of cable fault and/or interference.

Table 68. 0x0187 Cable Diagnostic Amplitude Result Register #3 (CDLAR3)

BIT	NAME	TYPE	DEFAULT	FUNCTION
15	Reserved	RO	0	**Reserved**
14:8	RD Peak Amplitude 1	RO	000 0000	Amplitude of the **First** peak discovered by the TDR mechanism on Receive Channel (RD). The value of these bits is translated into type of cable fault and/or interference.
7	Reserved	RO	0	**Reserved**
6:0	TD Peak Amplitude 5	RO	000 0000	Amplitude of the **Fifth** peak discovered by the TDR mechanism on Transmit Channel (TD). The value of these bits is translated into type of cable fault and/or interference.

Table 69. 0x0188 Cable Diagnostic Amplitude Result Register #4 (CDLAR4)

BIT	NAME	TYPE	DEFAULT	FUNCTION
15	Reserved	RO	0	**Reserved**
14:8	RD Peak Amplitude 3	RO	000 0000	Amplitude of the **Third** peak discovered by the TDR mechanism on Receive Channel (RD). The value of these bits is translated into type of cable fault and/or interference.
7	Reserved	RO	0	**Reserved**
6:0	RD Peak Amplitude 2	RO	000 0000	Amplitude of the **Second** peak discovered by the TDR mechanism on Receive Channel (RD). The value of these bits is translated into type of cable fault and/or interference.

Table 70. 0x0189 Cable Diagnostic Amplitude Result Register #5 (CDLAR5)

BIT	NAME	TYPE	DEFAULT	FUNCTION
15	Reserved	RO	0	**Reserved**
14:8	RD Peak Amplitude 5	RO	000 0000	Amplitude of the **Fifth** peak discovered by the TDR mechanism on Receive Channel (RD). The value of these bits is translated into type of cable fault and/or interference.
7	Reserved	RO	0	**Reserved**
6:0	RD Peak Amplitude 4	RO	000 0000	Amplitude of the **Fourth** peak discovered by the TDR mechanism on Receive Channel (RD). The value of these bits is translated into type of cable fault and/or interference.

Table 71. 0x018A Cable Diagnostic General Result Register (CDLGR)

BIT	NAME	TYPE	DEFAULT	FUNCTION
15	TD Peak Polarity 5	RO	0	Polarity of the **Fifth** peak discovered by the TDR mechanism on Transmit Channel (TD).
14	TD Peak Polarity 4	RO	0	Polarity of the **Fourth** peak discovered by the TDR mechanism on Transmit Channel (TD).
13	TD Peak Polarity 3	RO	0	Polarity of the **Third** peak discovered by the TDR mechanism on Transmit Channel (TD).
12	TD Peak Polarity 2	RO	0	Polarity of the **Second** peak discovered by the TDR mechanism on Transmit Channel (TD).
11	TD Peak Polarity 1	RO	0	Polarity of the **First** peak discovered by the TDR mechanism on Transmit Channel (TD).
10	RD Peak Polarity 5	RO	0	Polarity of the **Fifth** peak discovered by the TDR mechanism on Receive Channel (RD).
9	RD Peak Polarity 4	RO	0	Polarity of the **Fourth** peak discovered by the TDR mechanism on Receive Channel (RD).
8	RD Peak Polarity 3	RO	0	Polarity of the **Third** peak discovered by the TDR mechanism on Receive Channel (RD).
7	RD Peak Polarity 2	RO	0	Polarity of the **Second** peak discovered by the TDR mechanism on Receive Channel (RD).
6	RD Peak Polarity 1	RO	0	Polarity of the **First** peak discovered by the TDR mechanism on Receive Channel (RD).
5	Cross Detect on TD	RO	0	Cross Reflections were detected on TD. Indicate on Short between TD and TD
4	Cross Detect on RD	RO	0	Cross Reflections were detected on RD. Indicate on Short between TD and RD
3	Above 5 TD Peaks	RO	0	More than 5 reflections were detected on TD
2	Above 5 RD Peaks	RO	0	More than 5 reflections were detected on RD
1:0	Reserved	RO	0	**Reserved**

Table 72. 0x0215 ALCD Control and Results 2 Register (ALCDRR2)

BIT	NAME	TYPE	DEFAULT	FUNCTION
15:4	Reserved	RO	0	**Reserved**
3:0	PGA Control	RO	0011	Control word to analog PGA

Table 73. 0x021D ALCD Control and Results 3 Register (ALCDRR3)

BIT	NAME	TYPE	DEFAULT	FUNCTION
15:12	Reserved	RO	0	**Reserved**
11:0	FAGC Accumulator	RW	0110 0000 0000	FAGC Accumulator

Table 74. 0x0403 Line Driver Control Register (LDCTRL)

BIT	NAME	TYPE	DEFAULT	FUNCTION
15:12	Reserved	RW	1001	**Reserved**
11:8	100Base-FX Line Driver Swing Select	RW	1111	**100Base-FX Line Driver Swing Select (peak-to-peak):** 0000 = 0.533-V 0001 = 0.567-V 0010 = 0.600-V 0011 = 0.633-V 0100 = 0.667-V 0101 = 0.700-V 0110 = 0.733-V 0111 = 0.767-V 1000 = 0.800-V 1001 = 0.833-V 1010 = 0.867-V 1011 = 0.900-V 1100 = 0.933-V 1101 = 0.976-V 1110 = 1.000-V 1111 = 1.033-V (Default Setting)
7:4	100Base-TX Line Driver Swing Select	RW	1100	**100Base-TX Line Driver Swing Select (peak-to-peak):** 0000 = 1.600-V 0001 = 1.633-V 0010 = 1.667-V 0011 = 1.700-V 0100 = 1.733-V 0101 = 1.767-V 0110 = 1.800-V 0111 = 1.833-V 1000 = 1.867-V 1001 = 1.900-V 1010 = 1.933-V 1011 = 1.967-V 1100 = 2.000-V (Default Setting) 1101 = 2.033-V 1110 = 2.067-V 1111 = 2.100-V
3:0	10Base-Te Line Driver Swing Select	RW	1111	**10Base-Te Line Driver Swing Select:** 0000 = 3.200-V 0001 = 3.233-V 0010 = 3.267-V 0011 = 3.300-V 0100 = 3.333-V 0101 = 3.367-V 0110 =3.400-V 0111 = 3.433-V 1000 = 3.467-V 1001 = 3.500-V 1010 = 3.533-V 1011 = 3.567-V 1100 = 3.600-V 1101 = 3.633-V 1110 = 3.667-V 1111 = 3.700-V (Default Setting)

Table 75. 0x0404 Line Driver Class Selection (LDCSEL)

BIT	NAME	TYPE	DEFAULT	FUNCTION
15:0	Line Driver Class Selection	RW	0020	0x0020 : Reduced MLT-3 (Class B) 0x0024 : To program full MLT-3 on both Tx+ and Tx– (Class A)

Table 76. 0x0428 Deep Power Down Control Register (DPDWN)

BIT	NAME	TYPE	DEFAULT	FUNCTION
15:6	Reserved	RO	0	**Reserved**
5	MSB 100Base-TX Idle Pattern	RW	0	**MSB 100Base-TX Idle Pattern:** 100Base-TX Test Mode is determined by bits {[5] in register 0x0428, [3:0] in register 0x0027}. The bits determine the number of 0's to follow a '1'. 0,0001 = Single '0' after a '1' 0,0010 = Two '0' after a '1' 0,0011 = Three '0' after a '1' 0,0100 = Four '0' after a '1' 0,0101 = Five '0' after a '1' 0,0110 = Six '0' after a '1' 0,0111 = Seven '0' after a '1' . .. 1,1111 = Thirty one '0' after a '1' 0,0000 = Clears the shift register
4	100Base-TX Idle Pattern Test Mode	RW	0	**100Base-TX Idle Pattern Test Mode:** 1 = 100Base-TX Idle Pattern Enable 0 = Normal operation When enabled, 100Base-TX Idle Pattern is determined by bit[5] in register 0x0428 and bits[3:0] in register 0x0027.
3	Deep Power Down Speed	RW	0	**Deep Power Down Speed Selection:** 1 = 50ms duration to exit Deep Power Down 0 = 100ms duration to exit Deep Power Down
2	Deep Power Down Enable	RW	0	**Deep Power Down Enable:** 1 = Deep Power Down activated 0 = Normal operation **Note:** If set, the DP83822 enters into deep power down mode. Deep power down mode requires that IEEE Power Down be enabled first by either register access (set bit[11] = '1' in register 0x0000) or using INT/PWDN pin.
1:0	Reserved	RW	0	**Reserved**

Table 77. 0x0456 General Configuration Register (GENCFG)

BIT	NAME	TYPE	DEFAULT	FUNCTION
15:4	Reserved	RW	0	**Reserved**
3	Min IPG Enable	RW	1	**Min IPG Enable:** 1 = Enable Minimum Inter-Packet Gap (IPG is set to 120ns) 0 = IPG set to 0.20µs **Note:** IPGs <200ns should only be used when operating with a MII MAC IF configuration.
2:0	Reserved	RW	0	**Reserved**

Table 78. 0x0460 LEDs Configuration Register #1 (LEDCFG1)

BIT	NAME	TYPE	DEFAULT	FUNCTION
15:12	Reserved	RO	0	**Reserved**
11:8	LED_1 Control	RW	0101	**LED_1 Control:** Selects the source for LED_1. 0000 = LINK OK 0001 = RX/TX Activity 0010 = TX Activity 0011 = RX Activity 0100 = Collision 0101 = Speed, High for 100Base-TX 0110 = Speed, High for 10Base-Te 0111 = Full-Duplex 1000 = LINK OK / BLINK on TX/RX Activity 1001 = Active Stretch Signal 1010 = MII LINK (100BT+FD) 1011 = LPI Mode (EEE) 1100 = TX/RX MII Error 1101 = Link Lost 1110 = Blink for PRBS error 1111 = Reserved Link Lost, LED remains ON until BMCR register (address 0x0001) is read. Blink for PRBS Errors, LED remains ON for single error and remains until BICSR1 register (address 0x001B) is cleared.
7:4	LED_3 Control (RX_D3)	RW	0101	**LED_3 Control:** Selects the source for RX_D3. Please reference bits[11:8] for list of sources.
3:0	Reserved	RW	0001	**Reserved**

Table 79. 0x0461 IO MUX GPIO Control Register (IOCTRL)

BIT	NAME	TYPE	DEFAULT	FUNCTION
15:5	Reserved	RW	0000 0100 000	**Reserved**
4:1	MAC Impedance Control	RW	1 000	**MAC Impedance Control:** MAC interface impedance control sets the series termination for the digital pins. 0 000 = 99.25 Ω 0 001 = 91.13 Ω 0 010 = 84.24 Ω 0 011 = 78.31 Ω 0 100 = 73.17 Ω 0 101 = 68.65 Ω 0 110 = 64.66 Ω 0 111 = 61.11 Ω 1 000 = 58.07 Ω (Default Setting) 1 001 = 55.18 Ω 1 010 = 52.57 Ω 1 011 = 50.20 Ω 1 100 = 48.03 Ω 1 101 = 46.04 Ω 1 110 = 44.20 Ω 1 111 = 42.51 Ω
0	Reserved	RW	0	**Reserved**

Table 80. 0x0462 IO MUX GPIO Control Register #1 (IOCTRL1)

BIT	NAME	TYPE	DEFAULT	FUNCTION
15	Reserved	RO	0	**Reserved**
14:12	RX_D3 / GPIO_3 Clock Source	RW	000	**Clock Source:** If RX_D3 is configured as a clock source from bits[10:8] the following field determines the reference 000 = MAC IF Clock 001 = XI Clock (Pass-Through Clock from XI pin) 010 = Internal Reference Clock: 25-MHz 011 = Reserved 100 = RMII Master Mode Reference Clock: 50-MHz 101 = Reserved 110 = Free Running Clock: 125-MHz 111 = Recovered Clock: 125-MHz MAC IF Clock: MII Mode the clock frequency is 25-MHz, RMII Mode the clock frequency is 50-MHz; RGMII Mode the clock frequency is 25-MHz. RMII Master Mode Reference Clock: Identical to MAC IF Clock in RMII Master Mode.
11	Reserved	RO	0	**Reserved**
10:8	RX_D3 / GPIO_3 Control	RW	000	**RX_D3 GPIO Configuration:** 000 = Normal operation 001 = LED_3 (Default: Speed, High for 100Base-TX) 010 = WoL 011 = Clock reference according to bits[14:12] 100 = IEEE 1588 TX Indication 101 = IEEE 1588 RX Indication 110 = Constant '0' 111 = Constand '1'
7	Reserved	RO	0	**Reserved**
6:4	LED_1 / GPIO_1 Clock Source	RW	000	**Clock Source:** If LED_1 is configured as a clock source from bits[2:0] the following field determines the reference 000 = MAC IF Clock 001 = XI Clock (Pass-Through Clock from XI pin) 010 = Internal Reference Clock: 25-MHz 011 = Reserved 100 = RMII Master Mode Reference Clock: 50-MHz 101 = Reserved 110 = Free Running Clock: 125-MHz 111 = Recovered Clock: 125-MHz MAC IF Clock: MII Mode the clock frequency is 25-MHz, RMII Mode the clock frequency is 50-MHz; RGMII Mode the clock frequency is 25-MHz. RMII Master Mode Reference Clock: Identical to MAC IF Clock in RMII Master Mode.
3	Reserved	RO	0	**Reserved**
2:0	LED_1 / GPIO_1 Control	RW	000	**LED_1 GPIO Configuration:** 000 = Tri-state 001 = LED_1 (Default: Speed, High for 100Base-TX) 010 = WoL 011 = Clock reference according to bits[6:4] 100 = IEEE 1588 TX Indication 101 = IEEE 1588 RX Indication 110 = Constant '0' 111 = Constand '1'

Table 81. 0x0463 IO MUX GPIO Control Register #2 (IOCTRL2)

BIT	NAME	TYPE	DEFAULT	FUNCTION
15:7	Reserved	RO	0	**Reserved**
6:4	COL / GPIO_2 Clock Source	RW	000	**Clock Source:** If COL is configured as a clock source from bits[2:0] the following field determines the reference 000 = MAC IF Clock 001 = XI Clock (Pass-Through Clock from XI pin) 010 = Internal Reference Clock: 25-MHz 011 = Reserved 100 = RMII Master Mode Reference Clock: 50-MHz 101 = Reserved 110 = Free Running Clock: 125-MHz 111 = Recovered Clock: 125-MHz MAC IF Clock: MII Mode the clock frequency is 25-MHz, RMII Mode the clock frequency is 50-MHz; RGMII Mode the clock frequency is 25-MHz. RMII Master Mode Reference Clock: Identical to MAC IF Clock in RMII Master Mode.
3	Reserved	RO	0	**Reserved**
2:0	COL / GPIO_2 Control	RW	000	**COL GPIO Configuration:** 000 = Normal operation 001 = MLED (Register 0x0025) 010 = WoL 011 = Clock reference according to bits[6:4] 100 = IEEE 1588 TX Indication 101 = IEEE 1588 RX Indication 110 = Constant '0' 111 = Constand '1'

Table 82. 0x0465 Fiber General Configuration Register (FIBER GENCFG)

BIT	NAME	TYPE	DEFAULT	FUNCTION
15:1	Reserved	RW	1111 1111 0000 000	**Reserved**
0	100Base-FX Signal Detect Polarity	RW	0	**100Base-FX Signal Detect Polarity:** 1 = Signal Detect is Active LOW 0 = Signal Detect is Active HIGH When set to Active HIGH, Link drop will occur if SD pin senses a LOW state (SD = '0'). When set to Active LOW, Link drop will occur if SD pin senses a HIGH state (SD = '1'). **Note:** To enable 100Base-FX Signal Detection on LED_1 (pin #24), strap SD_EN = '1'

Table 83. 0x0467 Strap Latch-In Register #1 (SOR1)

BIT	NAME	TYPE	DEFAULT	FUNCTION
15:14	RX_D1 Strap Mode	RO, Strap	00	**RX_D1 Strap Mode:** 00 = Mode 1 01 = Mode 2 10 = Mode 3 11 = Mode 4 Please refer to the strap section in the datasheet for information regarding PHY configuration. **Note:** Bit values ('00', '01', '10', '11') are just used to indicate the Strap Mode and do not reflect the same bit sequence that is defined in the strap section of the datasheet.
13:12	RX_D0 Strap Mode	RO, Strap	00	**RX_D0 Strap Mode:** Use same reference as defined by bits[15:14] in this register.
11:10	COL Strap Mode	RO, Strap	11	**COL Strap Mode:** Use same reference as defined by bits[15:14] in this register.

Table 83. 0x0467 Strap Latch-In Register #1 (SOR1) (continued)

BIT	NAME	TYPE	DEFAULT	FUNCTION
9:8	RX_ER Strap Mode	RO, Strap	11	**RX_ER Strap Mode:** Use same reference as defined by bits[15:14] in this register.
7:6	CRS Strap Mode	RO, Strap	11	**CRS Strap Mode:** Use same reference as defined by bits[15:14] in this register.
5:4	RX_DV Strap Mode	RO, Strap	00	**RX_DV Strap Mode:** Use same reference as defined by bits[15:14] in this register.
3:2	Reserved	RO	00	**Reserved**
1:0	LED_0 Strap Mode	RO, Strap	11	**LED_0 Strap Mode:** 00 = Mode 1 01 = Reserved 10 = Reserved 11 = Mode 4 Please refer to the strap section in the datasheet for information regarding PHY configuration. **Note:** Bit values ('00', '01', '10', '11') are just used to indicate the Strap Mode and do not reflect the same bit sequence that is defined in the strap section of the datasheet.

Table 84. 0x0468 Strap Latch-In Register #2 (SOR2)

BIT	NAME	TYPE	DEFAULT	FUNCTION
15:4	Reserved	RO	0	**Reserved**
3:2	RX_D3 Strap Mode	RO, Strap	00	**RX_D3 Strap Mode:** Use same reference as defined by bits[15:14] in register 0x0467.
1:0	RX_D2 Strap Mode	RO, Strap	00	**RX_D2 Strap Mode:** Use same reference as defined by bits[15:14] in register 0x0467.

Table 85. 0x0469 LEDs Configuration Register #2 (LEDCFG2)

BIT	NAME	TYPE	DEFAULT	FUNCTION
15:11	Reserved	RO	0	**Reserved**
10	LED_1 Polarity	RW	0	**LED_1 Polarity:** 1 = Active High 0 = Active Low
9	LED_1 Force Override Value	RW	0	**LED_1 Force Override Value:** 1 = LED_1 forced High 0 = LED_1 forced Low
8	LED_1 Force Override Enable	RW	0	**LED_1 Force Override Enable:** 1 = Enable Force Override 0 = Disable Force Override When enabled, bit[9] in this register determines state of LED_1.
7	Reserved	RO	0	**Reserved**
6	LED_3 Polarity	RW	1	**LED_3 Polarity:** 1 = Active High 0 = Active Low
5	LED_3 Force Override Value	RW	0	**LED_3 Force Override Value:** 1 = RX_D3 forced High 0 = RX_D3 forced Low
4	LED_3 Force Override Enable	RW	0	**LED_3 Force Override Enable:** 1 = Enable Force Override 0 = Disable Force Override When enabled, bit[5] in this register determines state of RX_D3.
3:0	Reserved	RO	0	**Reserved**

Table 86. 0x04A0 Receive Configuration Register (RXFCFG)

BIT	NAME	TYPE	DEFAULT	FUNCTION
15:14	Bit Nibble Swap	RW	00	**Bit Nibble Swap:** 00 = Normal order, no swap (RXD[3:0]) 01 = Swap bits order (RXD[0:3]) 10 = Swap nibbles order (RXD[3:0] , RXD[7:4]) 11 = Swap bits order in each nibble (RXD[4:7] , RXD[0:3])
13	SFD Byte	RW	0	**SFD Byte Search:** 1 = SFD is 0x5D (i.e. Receive module searches for 0x5D) 0 = SFD is 0xD5 (i.e. Receive module searches for 0xD5)
12	CRC Gate	RW	1	**CRC Gate:** 1 = Bad CRC gates Magic Packet and Pattern Indications 0 = Bad CRC does not gate Magic Packet or Pattern Indications If Magic Packet has Bad CRC there will be no indication (status, interrupt, GPIO) when enabled.
11	WoL Level Change Indication Clear	W, SC	0	**WoL Level Change Indication Clear:** If WoL Indication is set for Level change mode, this bit clears the level upon a write.
10:9	WoL Pulse Indication Select	RW	00	**WoL Pulse Indication Select:** Only valid when WoL Indication is set for Pulse mode. 00 = 8 clock cycles (of 125-MHz clock) 01 = 16 clock cycles 10 = 32 clock cycles 11 = 64 clock cycles
8	WoL Indication Select	RW	0	**WoL Indication Select:** 1 = Level change mode 0 = Pulse mode
7	WoL Enable	RW	0	**WoL Enable:** 1 = Enable Wake-on-LAN (WoL) 0 = Normal operation
6	Bit Mask Flag	RW	0	**Bit Mask Flag**
5	Secure-ON Enable	RW	0	**Enable** Secure-ON password for Magic Packets
4:2	Reserved	RW	0	**Reserved**
1	WoL Pattern Enable	RW	0	**Enable** Interrupt upon reception of packet with configured pattern
0	WoL Magic Packet Enable	RW	0	**Enable** Interrupt upon reception of Magic Packet

Table 87. 0x04A1 Receive Status Register (RXFS)

BIT	NAME	TYPE	DEFAULT	FUNCTION
15:13	Reserved	RO	0	**Reserved**
12	WoL Interrupt Source	RW	0	**WoL Interrupt Source:** Source of Interrupt for bit[1] of register 0x0013. 1 = WoL Interrupt 0 = Data Polarity Interrupt When enabling WoL, this bit is automatically set to WoL Interrupt.
11:8	Reserved	RO	0	**Reserved**
7	SFD Error	RO, LH, SC	0	**SFD Error:** 1 = Packet with SFD error 0 = No SFD error
6	Bad CRC	RO, LH, SC	0	**Bad CRC:** 1 = Bad CRC was received 0 = No bad CRC received
5	Secure-On Hack Flag	RO, LH, SC	0	**Secure-ON Hack Flag:** 1 = Invalid Password detected in Magic Packet 0 = Valid Secure-ON Password
4:2	Reserved	RO, LH, SC	0	**Reserved**
1	WoL Pattern Status	RO, LH, SC	0	**WoL Pattern Status:** 1 = Valid packet with configured pattern received 0 = No valid packet with configured pattern received

Table 87. 0x04A1 Receive Status Register (RXFS) (continued)

BIT	NAME	TYPE	DEFAULT	FUNCTION
0	WoL Magic Packet Status	RO, LH, SC	0	**WoL Magic Packet Status:** 1 = Valid Magic Packet received 0 = No valid Magic Packet received

Table 88. 0x04A2 Receive Perfect Match Data Register #1 (RXFPMD1)

BIT	NAME	TYPE	DEFAULT	FUNCTION
15:8	MAC Destination Address Byte 4	RW	0	**Perfect Match Data:** Configured for MAC Destination Address
7:0	MAC Destination Address Byte 5	RW	0	**Perfect Match Data:** Configured for MAC Destination Address

Table 89. 0x04A3 Receive Perfect Match Data Register #2 (RXFPMD2)

BIT	NAME	TYPE	DEFAULT	FUNCTION
15:8	MAC Destination Address Byte 2	RW	0	**Perfect Match Data:** Configured for MAC Destination Address
7:0	MAC Destination Address Byte 3	RW	0	**Perfect Match Data:** Configured for MAC Destination Address

Table 90. 0x04A4 Receive Perfect Match Data Register #3 (RXFPMD3)

BIT	NAME	TYPE	DEFAULT	FUNCTION
15:8	MAC Destination Address Byte 0	RW	0	**Perfect Match Data:** Configured for MAC Destination Address
7:0	MAC Destination Address Byte 1	RW	0	**Perfect Match Data:** Configured for MAC Destination Address

Table 91. 0x04A5 Receive Secure-ON Password Register #1 (RXFSOP1)

BIT	NAME	TYPE	DEFAULT	FUNCTION
15:8	Secure-ON Password Byte 1	RW	0	**Secure-ON Password Select:** Secure-ON password for Magic Packets
7:0	Secure-ON Password Byte 0	RW	0	**Secure-ON Password Select:** Secure-ON password for Magic Packets

Table 92. 0x04A6 Receive Secure-ON Password Register #2 (RXFSOP2)

BIT	NAME	TYPE	DEFAULT	FUNCTION
15:8	Secure-ON Password Byte 3	RW	0	**Secure-ON Password Select:** Secure-ON password for Magic Packets
7:0	Secure-ON Password Byte 2	RW	0	**Secure-ON Password Select:** Secure-ON password for Magic Packets

Table 93. 0x04A7 Receive Secure-ON Password Register #3 (RXFSOP3)

BIT	NAME	TYPE	DEFAULT	FUNCTION
15:8	Secure-ON Password Byte 5	RW	0	**Secure-ON Password Select:** Secure-ON password for Magic Packets
7:0	Secure-ON Password Byte 4	RW	0	**Secure-ON Password Select:** Secure-ON password for Magic Packets

Table 94. 0x04A8 Receive Pattern Register #1 (RXFPAT1)

BIT	NAME	TYPE	DEFAULT	FUNCTION
15:8	Pattern Byte 1	RW	0	**Pattern Configuration:** Configures byte 1 of the pattern
7:0	Pattern Byte 0	RW	0	**Pattern Configuration:** Configures byte 0 of the pattern

Table 95. 0x04A9 Receive Pattern Register #2 (RXFPAT2)

BIT	NAME	TYPE	DEFAULT	FUNCTION
15:8	Pattern Byte 3	RW	0	**Pattern Configuration:** Configures byte 3 of the pattern
7:0	Pattern Byte 2	RW	0	**Pattern Configuration:** Configures byte 2 of the pattern

Table 96. 0x04AA Receive Pattern Register #3 (RXFPAT3)

BIT	NAME	TYPE	DEFAULT	FUNCTION
15:8	Pattern Byte 5	RW	0	**Pattern Configuration:** Configures byte 5 of the pattern
7:0	Pattern Byte 4	RW	0	**Pattern Configuration:** Configures byte 4 of the pattern

Table 97. 0x04AB Receive Pattern Register #4 (RXFPAT4)

BIT	NAME	TYPE	DEFAULT	FUNCTION
15:8	Pattern Byte 7	RW	0	**Pattern Configuration:** Configures byte 7 of the pattern
7:0	Pattern Byte 6	RW	0	**Pattern Configuration:** Configures byte 6 of the pattern

Table 98. 0x04AC Receive Pattern Register #5 (RXFPAT5)

BIT	NAME	TYPE	DEFAULT	FUNCTION
15:8	Pattern Byte 9	RW	0	**Pattern Configuration:** Configures byte 9 of the pattern
7:0	Pattern Byte 8	RW	0	**Pattern Configuration:** Configures byte 8 of the pattern

Table 99. 0x04AD Receive Pattern Register #6 (RXFPAT6)

BIT	NAME	TYPE	DEFAULT	FUNCTION
15:8	Pattern Byte 11	RW	0	**Pattern Configuration:** Configures byte 11 of the pattern
7:0	Pattern Byte 10	RW	0	**Pattern Configuration:** Configures byte 10 of the pattern

Table 100. 0x04AE Receive Pattern Register #7 (RXFPAT7)

BIT	NAME	TYPE	DEFAULT	FUNCTION
15:8	Pattern Byte 13	RW	0	**Pattern Configuration:** Configures byte 13 of the pattern
7:0	Pattern Byte 12	RW	0	**Pattern Configuration:** Configures byte 12 of the pattern

Table 101. 0x04AF Receive Pattern Register #8 (RXFPAT8)

BIT	NAME	TYPE	DEFAULT	FUNCTION
15:8	Pattern Byte 15	RW	0	**Pattern Configuration:** Configures byte 15 of the pattern
7:0	Pattern Byte 14	RW	0	**Pattern Configuration:** Configures byte 14 of the pattern

Table 102. 0x04B0 Receive Pattern Register #9 (RXFPAT9)

BIT	NAME	TYPE	DEFAULT	FUNCTION
15:8	Pattern Byte 17	RW	0	**Pattern Configuration:** Configures byte 17 of the pattern

Table 102. 0x04B0 Receive Pattern Register #9 (RXFPAT9) (continued)

BIT	NAME	TYPE	DEFAULT	FUNCTION
7:0	Pattern Byte 16	RW	0	**Pattern Configuration:** Configures byte 16 of the pattern

Table 103. 0x04B1 Receive Pattern Register #10 (RXFPAT10)

BIT	NAME	TYPE	DEFAULT	FUNCTION
15:8	Pattern Byte 19	RW	0	**Pattern Configuration:** Configures byte 19 of the pattern
7:0	Pattern Byte 18	RW	0	**Pattern Configuration:** Configures byte 18 of the pattern

Table 104. 0x04B2 Receive Pattern Register #11 (RXFPAT11)

BIT	NAME	TYPE	DEFAULT	FUNCTION
15:8	Pattern Byte 21	RW	0	**Pattern Configuration:** Configures byte 21 of the pattern
7:0	Pattern Byte 20	RW	0	**Pattern Configuration:** Configures byte 20 of the pattern

Table 105. 0x04B3 Receive Pattern Register #12 (RXFPAT12)

BIT	NAME	TYPE	DEFAULT	FUNCTION
15:8	Pattern Byte 23	RW	0	**Pattern Configuration:** Configures byte 23 of the pattern
7:0	Pattern Byte 22	RW	0	**Pattern Configuration:** Configures byte 22 of the pattern

Table 106. 0x04B4 Receive Pattern Register #13 (RXFPAT13)

BIT	NAME	TYPE	DEFAULT	FUNCTION
15:8	Pattern Byte 25	RW	0	**Pattern Configuration:** Configures byte 25 of the pattern
7:0	Pattern Byte 24	RW	0	**Pattern Configuration:** Configures byte 24 of the pattern

Table 107. 0x04B5 Receive Pattern Register #14 (RXFPAT14)

BIT	NAME	TYPE	DEFAULT	FUNCTION
15:8	Pattern Byte 27	RW	0	**Pattern Configuration:** Configures byte 27 of the pattern
7:0	Pattern Byte 26	RW	0	**Pattern Configuration:** Configures byte 26 of the pattern

Table 108. 0x04B6 Receive Pattern Register #15 (RXFPAT15)

BIT	NAME	TYPE	DEFAULT	FUNCTION
15:8	Pattern Byte 29	RW	0	**Pattern Configuration:** Configures byte 29 of the pattern
7:0	Pattern Byte 28	RW	0	**Pattern Configuration:** Configures byte 28 of the pattern

Table 109. 0x04B7 Receive Pattern Register #16 (RXFPAT16)

BIT	NAME	TYPE	DEFAULT	FUNCTION
15:8	Pattern Byte 31	RW	0	**Pattern Configuration:** Configures byte 31 of the pattern
7:0	Pattern Byte 30	RW	0	**Pattern Configuration:** Configures byte 30 of the pattern

Table 110. 0x04B8 Receive Pattern Register #17 (RXFPAT17)

BIT	NAME	TYPE	DEFAULT	FUNCTION
15:8	Pattern Byte 33	RW	0	**Pattern Configuration:** Configures byte 33 of the pattern
7:0	Pattern Byte 32	RW	0	**Pattern Configuration:** Configures byte 32 of the pattern

Table 111. 0x04B9 Receive Pattern Register #18 (RXFPAT18)

BIT	NAME	TYPE	DEFAULT	FUNCTION
15:8	Pattern Byte 35	RW	0	**Pattern Configuration:** Configures byte 35 of the pattern
7:0	Pattern Byte 34	RW	0	**Pattern Configuration:** Configures byte 34 of the pattern

Table 112. 0x04BA Receive Pattern Register #19 (RXFPAT19)

BIT	NAME	TYPE	DEFAULT	FUNCTION
15:8	Pattern Byte 37	RW	0	**Pattern Configuration:** Configures byte 37 of the pattern
7:0	Pattern Byte 36	RW	0	**Pattern Configuration:** Configures byte 36 of the pattern

Table 113. 0x04BB Receive Pattern Register #20 (RXFPAT20)

BIT	NAME	TYPE	DEFAULT	FUNCTION
15:8	Pattern Byte 39	RW	0	**Pattern Configuration:** Configures byte 39 of the pattern
7:0	Pattern Byte 38	RW	0	**Pattern Configuration:** Configures byte 38 of the pattern

Table 114. 0x04BC Receive Pattern Register #21 (RXFPAT21)

BIT	NAME	TYPE	DEFAULT	FUNCTION
15:8	Pattern Byte 41	RW	0	**Pattern Configuration:** Configures byte 41 of the pattern
7:0	Pattern Byte 40	RW	0	**Pattern Configuration:** Configures byte 40 of the pattern

Table 115. 0x04BD Receive Pattern Register #22 (RXFPAT22)

BIT	NAME	TYPE	DEFAULT	FUNCTION
15:8	Pattern Byte 43	RW	0	**Pattern Configuration:** Configures byte 43 of the pattern
7:0	Pattern Byte 42	RW	0	**Pattern Configuration:** Configures byte 42 of the pattern

Table 116. 0x04BE Receive Pattern Register #23 (RXFPAT23)

BIT	NAME	TYPE	DEFAULT	FUNCTION
15:8	Pattern Byte 45	RW	0	**Pattern Configuration:** Configures byte 45 of the pattern
7:0	Pattern Byte 44	RW	0	**Pattern Configuration:** Configures byte 44 of the pattern

Table 117. 0x04BF Receive Pattern Register #24 (RXFPAT24)

BIT	NAME	TYPE	DEFAULT	FUNCTION
15:8	Pattern Byte 47	RW	0	**Pattern Configuration:** Configures byte 47 of the pattern

Table 117. 0x04BF Receive Pattern Register #24 (RXFPAT24) (continued)

BIT	NAME	TYPE	DEFAULT	FUNCTION
7:0	Pattern Byte 46	RW	0	**Pattern Configuration:** Configures byte 46 of the pattern

Table 118. 0x04C0 Receive Pattern Register #25 (RXFPAT25)

BIT	NAME	TYPE	DEFAULT	FUNCTION
15:8	Pattern Byte 49	RW	0	**Pattern Configuration:** Configures byte 49 of the pattern
7:0	Pattern Byte 48	RW	0	**Pattern Configuration:** Configures byte 48 of the pattern

Table 119. 0x04C1 Receive Pattern Register #26 (RXFPAT26)

BIT	NAME	TYPE	DEFAULT	FUNCTION
15:8	Pattern Byte 51	RW	0	**Pattern Configuration:** Configures byte 51 of the pattern
7:0	Pattern Byte 50	RW	0	**Pattern Configuration:** Configures byte 50 of the pattern

Table 120. 0x04C2 Receive Pattern Register #27 (RXFPAT27)

BIT	NAME	TYPE	DEFAULT	FUNCTION
15:8	Pattern Byte 53	RW	0	**Pattern Configuration:** Configures byte 53 of the pattern
7:0	Pattern Byte 52	RW	0	**Pattern Configuration:** Configures byte 52 of the pattern

Table 121. 0x04C3 Receive Pattern Register #28 (RXFPAT28)

BIT	NAME	TYPE	DEFAULT	FUNCTION
15:8	Pattern Byte 55	RW	0	**Pattern Configuration:** Configures byte 55 of the pattern
7:0	Pattern Byte 54	RW	0	**Pattern Configuration:** Configures byte 54 of the pattern

Table 122. 0x04C4 Receive Pattern Register #29 (RXFPAT29)

BIT	NAME	TYPE	DEFAULT	FUNCTION
15:8	Pattern Byte 57	RW	0	**Pattern Configuration:** Configures byte 57 of the pattern
7:0	Pattern Byte 56	RW	0	**Pattern Configuration:** Configures byte 56 of the pattern

Table 123. 0x04C5 Receive Pattern Register #30 (RXFPAT30)

BIT	NAME	TYPE	DEFAULT	FUNCTION
15:8	Pattern Byte 59	RW	0	**Pattern Configuration:** Configures byte 59 of the pattern
7:0	Pattern Byte 58	RW	0	**Pattern Configuration:** Configures byte 58 of the pattern

Table 124. 0x04C6 Receive Pattern Register #31 (RXFPAT31)

BIT	NAME	TYPE	DEFAULT	FUNCTION
15:8	Pattern Byte 61	RW	0	**Pattern Configuration:** Configures byte 61 of the pattern
7:0	Pattern Byte 60	RW	0	**Pattern Configuration:** Configures byte 60 of the pattern

Table 125. 0x04C7 Receive Pattern Register #32 (RXFPAT32)

BIT	NAME	TYPE	DEFAULT	FUNCTION
15:8	Pattern Byte 63	RW	0	**Pattern Configuration:** Configures byte 63 of the pattern
7:0	Pattern Byte 62	RW	0	**Pattern Configuration:** Configures byte 62 of the pattern

Table 126. 0x04C8 Receive Pattern Byte Mask Register #1 (RXFPBM1)

BIT	NAME	TYPE	DEFAULT	FUNCTION
15:0	Mask Bytes 0 to 15	RW	0	**Pattern Byte Mask Configuration:** Configures masks for bytes 0 to 15. For each byte '1' means it is masked.

Table 127. 0x04C9 Receive Pattern Byte Mask Register #2 (RXFPBM2)

BIT	NAME	TYPE	DEFAULT	FUNCTION
15:0	Mask Bytes 16 to 31	RW	0	**Pattern Byte Mask Configuration:** Configures masks for bytes 16 to 31. For each byte '1' means it is masked.

Table 128. 0x04CA Receive Pattern Byte Mask Register #3 (RXFPBM3)

BIT	NAME	TYPE	DEFAULT	FUNCTION
15:0	Mask Bytes 32 to 47	RW	0	**Pattern Byte Mask Configuration:** Configures masks for bytes 32 to 47. For each byte '1' means it is masked.

Table 129. 0x04CB Receive Pattern Byte Mask Register #4 (RXFPBM4)

BIT	NAME	TYPE	DEFAULT	FUNCTION
15:0	Mask Bytes 48 to 63	RW	0	**Pattern Byte Mask Configuration:** Configures masks for bytes 48 to 63. For each byte '1' means it is masked.

Table 130. 0x04CC Receive Pattern Control Register (RXFPATC)

BIT	NAME	TYPE	DEFAULT	FUNCTION
15:6	Reserved	RO	0	**Reserved**
5:0	Pattern Start Point	RW	01100	**Pattern Start Point:** Number of bytes after SFD where comparison begins on RX packets to the configured pattern. 00000 = Start compare on 1st byte after SFD 00001 = Start compare on 2nd byte after SFD ... 01100 = Start compare on 13th byte (Default) Default setting is 0xC, which means the pattern comparision will begin after source and destination addresses since they are each 6 bytes.

Table 131. 0x04D0 Energy Efficient Ethernet Configuration Register #2 (EEECFG2)

BIT	NAME	TYPE	DEFAULT	FUNCTION
15	Reserved	RO	0	**Reserved**
14	TX_ER for LPI Request	RW	0	**TX_ER for LPI Request:** 1 = TX_ER used for LPI Request 0 = TX_ER not used for LPI Request
13:7	Reserved	RO	00 0011 0	**Reserved**
6:5	TX_ER Pin Select	RW	00	**TX_ER Pin Select:** 00 = No Pin Selected 01 = INT/PWDN 10 = COL/GPIO 11 = No Pin Selected

Table 131. 0x04D0 Energy Efficient Ethernet Configuration Register #2 (EEECFG2) (continued)

BIT	NAME	TYPE	DEFAULT	FUNCTION
4:0	Reserved	RO	0 0010	**Reserved**

Table 132. 0x04D1 Energy Efficient Ethernet Configuration Register #2 (EEECFG3)

BIT	NAME	TYPE	DEFAULT	FUNCTION
15:4	Reserved	RW	0000 0001 1000	**Reserved**
3	EEE Capabilities Bypass	RW	1	**EEE Advertise Bypass:** 1 = Bit [0] determines EEE Auto-Negotiation Abilities 0 = MMD3 and MMD7 determine EEE Auto-Negotiation Abilities Allows for EEE Advertisment during Auto-Negotiation to be determined by bit[0] in register 0x04D1 rather than the Next Page Registers (Register 0x003C and Register 0x003D in MMD7).
2	EEE Next Page Disable	RW	0	**EEE Next Page Disable:** 1 = Reception of EEE Next Pages is disabled 0 = Reception of EEE Next Pages is enabled
1	EEE RX Path Shutdown	RW	1	**EEE RX Path Shutdown:** 1= Enable shutdown of Analog RX path at LPI_Quiet 0 = Analog RX path is active during LPI_Quiet
0	EEE Capabilities Enable	RW, Strap	0	**EEE Capabilities Enable:** 1 = PHY supports EEE capabilities 0 = PHY does not support EEE When enabled, Auto-Negotiation will negotiate to EEE as defined by register 0x003C and register 0x003D in MMD7. When disabled, register 0x0014 in MMD3, register 0x003C and register 0x003D in MMD7 are ignored.

Table 133. 0x04D4 TLOOP Bandwidth Control Register 1 (TLBCR1)

BIT	NAME	TYPE	DEFAULT	FUNCTION
15:0	Reserved	RW	0111 0010 0010 0000	**Reserved**

Table 134. 0x04D5 TLOOP Bandwidth Control Register 2 (TLBCR2)

BIT	NAME	TYPE	DEFAULT	FUNCTION
15:0	Reserved	RW	1111 1011 1100 0001	**Reserved**

Table 135. 0x04D6 TLOOP Bandwidth Control Register 3 (TLBCR3)

BIT	NAME	TYPE	DEFAULT	FUNCTION
15:0	Reserved	RW	0000 0001 1100 0001	**Reserved**

Table 136. 0x3000 MMD3 PCS Control Register #1 (MMD3_PCS_CTRL_1)

BIT	NAME	TYPE	DEFAULT	FUNCTION
15	PCS Reset	RW, SC	0	**PCS Reset:** 1 = Soft Reset of MMD3, MMD7 and PCS registers 0 = Normal operation Reset clears MMD3, MMD7 and PCS registers. Reset does not clear Vendor Specific Registers (DEVAD = 31).
14:11	Reserved	RO	0	**Reserved**
10	RX Clock Stoppable	RW	0	**RX Clock Stoppable:** 1 = Receive Clock stoppable during LPI 0 = Receive Clock not stoppable
9:0	Reserved	RO	0	**Reserved**

Table 137. 0x3001 MMD3 PCS Status Register #1 (MMD3_PCS_STATUS_1)

BIT	NAME	TYPE	DEFAULT	FUNCTION
15:12	Reserved	RO	0	**Reserved**
11	TX LPI Received	RO	0	**TX LPI Received:** 1 = TX PCS has received LPI 0 = LPI not received
10	RX LPI Received	RO	0	**RX LPI Received:** 1 = RX PCS has received LPI 0 = LPI not received
9	TX LPI Indication	RO	0	**TX LPI Indication:** 1 = TX PCS is currently receiving LPI 0 = TX PCS is not currently receiving LPI
8	RX LPI Indication	RO	0	**RX LPI Indication:** 1 = RX PCS is currently receiving LPI 0 = RX PCS is not currenly receiving LPI
7	Reserved	RO	0	**Reserved**
6	TX Clock Stoppable	RO	0	**TX Clock Stoppable:** 1 = MAC may stop clock during LPI 0 = TX Clock is not stoppable
5:0	Reserved	RO	0	**Reserved**

Table 138. 0x3014 MMD3 Energy Efficient Ethernet Capability Register (MMD3_EEE_CAPABILITY)

BIT	NAME	TYPE	DEFAULT	FUNCTION
15:3	Reserved	RO	0	**Reserved**
2	EEE 1Gbps Enable	RO	0	**EEE 1Gbps Enable:** 1 = EEE is supported for 1000Base-T 0 = EEE is not supported for 1000Base-T
1	EEE 100Mbps Enable	RO	0	**EEE 100Mbps Enable:** 1 = EEE is supported for 100Base-TX 0 = EEE is not supported for 100Base-TX
0	Reserved	RO	0	**Reserved**

Table 139. 0x3016 MMD3 Wake Error Counter Register (MMD3_WAKE_ERR_CNT)

BIT	NAME	TYPE	DEFAULT	FUNCTION
15:0	EEE Wake Error Counter	RO, LH	0	**EEE Wake Error Counter:** This register counts the wake time faults where the PHY fails to complete its normal wake sequence within the time required for the specific PHY type. This counter is cleared after a read and holds at all ones in the case of overflow. PCS Reset also clears this register.

Table 140. 0x703C MMD7 Energy Efficient Ethernet Advertisement Register (MMD7_EEE_ADVERTISEMENT)

BIT	NAME	TYPE	DEFAULT	FUNCTION
15:2	Reserved	RO	0	**Reserved**
1	Advertise 100Base-TX EEE	RW	1	**Advertise 100Base-TX EEE:** 1 = Energy Efficient Ethernet is advertised for 100Base-TX 0 = Energy Efficient Ethernet is not advertised
0	Reserved	RO	0	**Reserved**

Table 141. 0x703D MMD7 Energy Efficient Ethernet Link Partner Ability Register (MMD7_EEE_LP_ABILITY)

BIT	NAME	TYPE	DEFAULT	FUNCTION
15:2	Reserved	RO	0	**Reserved**

Table 141. 0x703D MMD7 Energy Efficient Ethernet Link Partner Ability Register (MMD7_EEE_LP_ABILITY) (continued)

BIT	NAME	TYPE	DEFAULT	FUNCTION
1	Link Partner EEE Capability	RO	0	**Link Partner EEE Capability:** 1 = Link Partner is advertising EEE capability for 100Base-TX 0 = Link Partner is not advertising EEE capability for 100Base-TX
0	Reserved	RO	0	**Reserved**

9 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

The DP83822 is a single-port 10/100 Mbps Ethernet PHY. It supports connections to an Ethernet MAC through MII, RMII, or RGMII. Connections to the Ethernet media are made via the IEEE 802.3 defined Media Dependent Interface.

When using the device for Ethernet applications, it is necessary to meet certain requirements for normal operation. The following subsections are intended to assist in appropriate component selection and required circuit connections.

9.2 Typical Applications

Figure 32 shows a typical application for the DP83822. More typical application examples are given in this section.

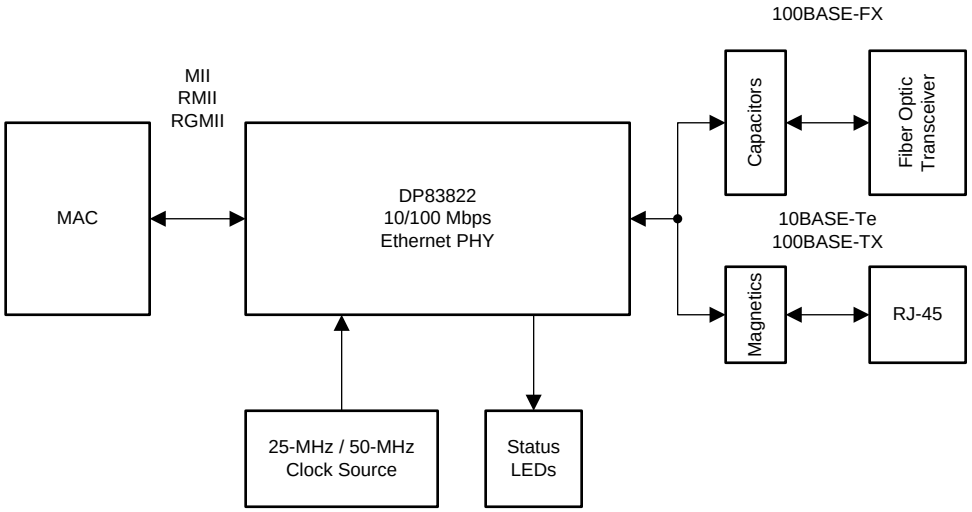


Figure 32. Typical DP83822 Application

Typical Applications (continued)

9.2.1 TPI Network Circuit

Figure 33 shows the recommended twisted-pair interface network circuit for 10/100 Mbps. Variations with PCB and component characteristics require that the application be tested to verify that the circuit meets the requirements of the intended application.

Center tap of the transformer must be connected to analog supply rail (AVD) with decoupling capacitors close to the transformer. All resistors and capacitors should be placed as close to the device as possible.

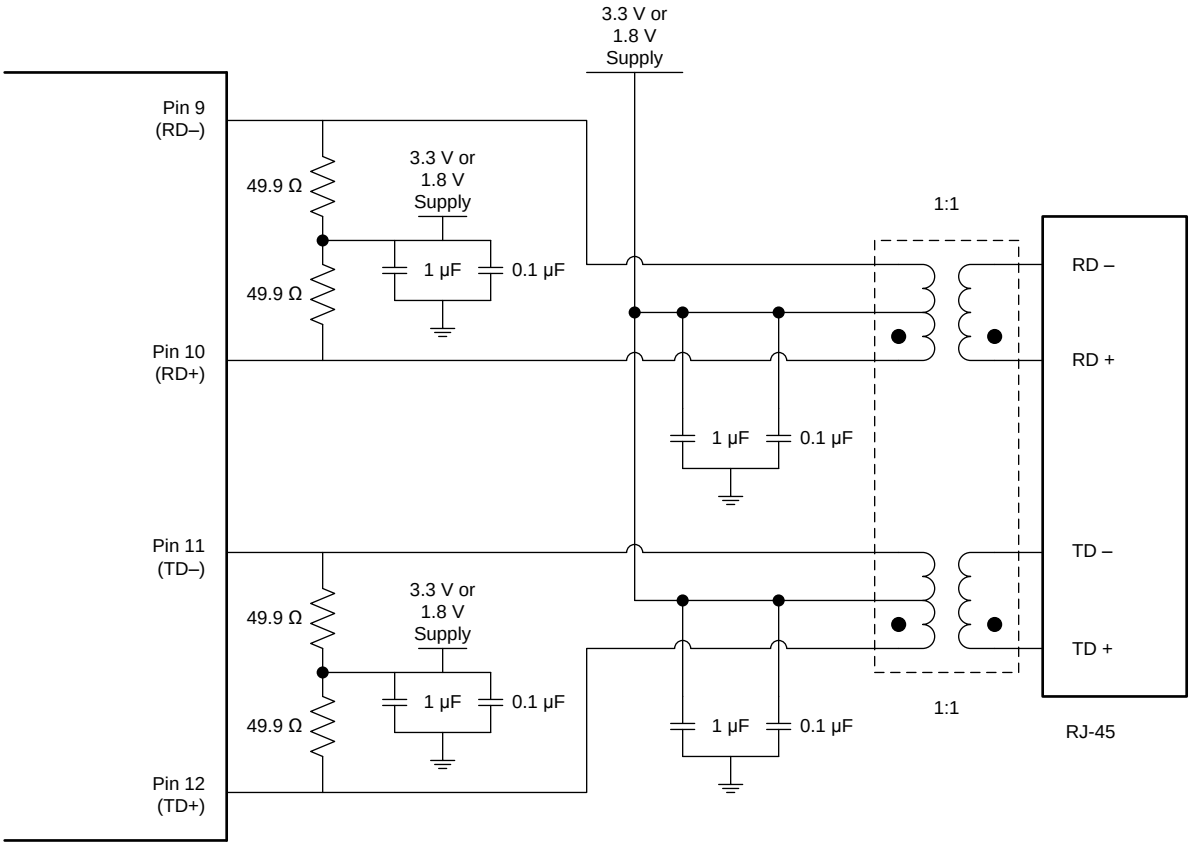


Figure 33. TPI Network Circuit

9.2.1.1 Design Requirements

The design requirements for the DP83822 in TPI operation (100BASE-TX or 10BASE-Te) are:

1. AVD Suppy = 3.3 V or 1.8 V
2. Center Tap Supply = AVD Supply
3. VDDIO Supply = 3.3 V, 2.5 V, or 1.8 V
4. Reference Clock Input = 25-MHz or 50-MHz (RMII Slave)

9.2.1.2 Detailed Design Procedure

For the detailed design procedure of the TPI network circuit, see *Detailed Design Procedure*.

9.2.1.3 Application Curves

For expected TPI network MDI curves, see Figure 17 and Figure 18 and Figure 20.

Typical Applications (continued)

9.2.2 Fiber Network Circuit

Figure 34 shows the recommended circuit for a 100-Mbps fiber network. Variations with PCB and component characteristics require that the application be tested to verify that the circuit meets the requirements of the intended application.

All resistors and capacitors should be placed as close to the fiber transceiver as possible.

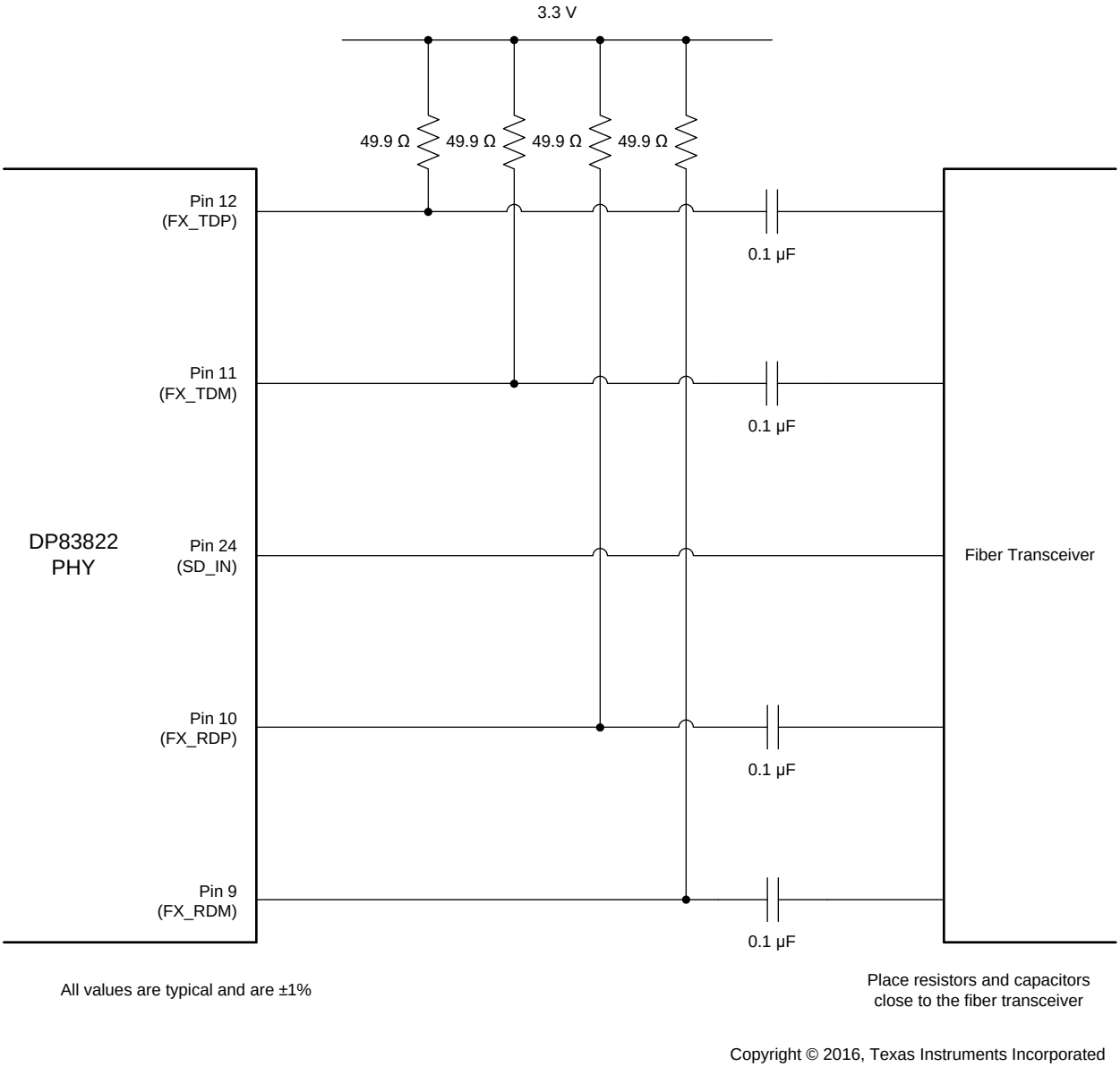


Figure 34. Fiber Network Circuit

9.2.2.1 Design Requirements

9.2.2.1.1 Clock Requirements

The DP83822 supports an external CMOS-level oscillator source or an internal oscillator with an external crystal.

Typical Applications (continued)

9.2.2.1.1.1 Oscillator

If an external clock source is used, XI should be tied to the clock source and XO should be left floating. The amplitude of the oscillator should be a nominal voltage of VDDIO.

NOTE

The DP83822 requires Clock to be present at PoR. In case clock is delayed, pull-down on XI is recommended to avoid spurious signal latch-up.

9.2.2.1.1.2 Crystal

The use of a 25-MHz, parallel, 20-pF load crystal is recommended if operating with a crystal. A typical connection diagram is shown below for a crystal resonator circuit. The load capacitor values will vary with the crystal vendors; check with the vendor for the recommended loads.

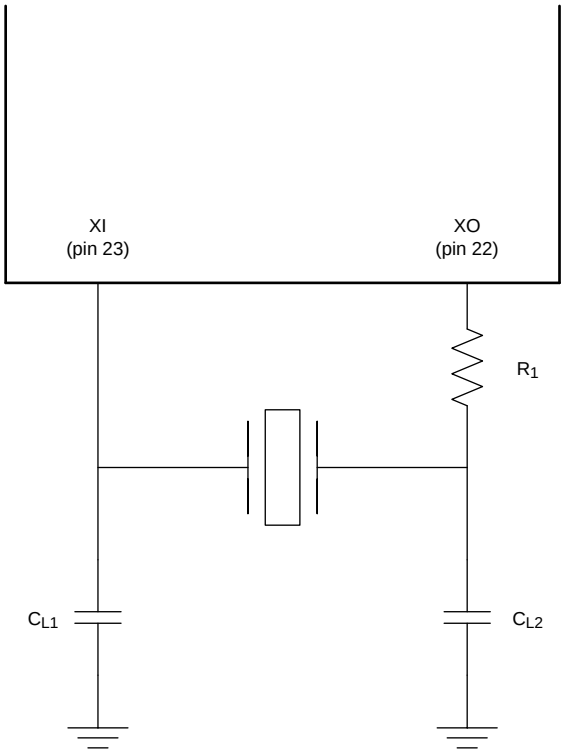


Figure 35. Crystal Oscillator Circuit

Typical Applications (continued)

Table 142. 25-MHz Oscillator Specification

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Frequency			25		MHz
Frequency Tolerance	Operational Temperature	-50		50	ppm
Frequency Stability	1 year aging	-50		50	ppm
Rise / Fall Time	10% - 90%			8	nsec
Jitter (Short Term)	Cycle-to-cycle		50		psec
Jitter (Long Term)	Accumulative over 10 ms			1	nsec
Symmetry	Duty Cycle	40		60	%
Load Capacitance			15	30	pF

Table 143. 50-MHz Oscillator Specification

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Frequency			50		MHz
Frequency Tolerance	Operational Temperature	-50		50	ppm
Frequency Stability	1 year aging	-50		50	ppm
Rise / Fall Time	10% - 90%			8	nsec
Jitter (Short Term)	Cycle-to-cycle		50		psec
Jitter (Long Term)	Accumulative over 10 ms			1	nsec
Symmetry	Duty Cycle	40		60	%
Load Capacitance			15	30	pF

Table 144. 25-MHz Crystal Specification

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Frequency			25		MHz
Frequency Tolerance	Operational Temperature	-50		50	ppm
	At 25°C	-50		50	ppm
Frequency Stability	1 year aging	-5		5	ppm
Load Capacitance		10		40	pF

9.2.2.2 Detailed Design Procedure

The Media Independent Interface (MII / RMII / RGMII) connects the DP83822 to the Media Access Controller (MAC). The MAC may in-fact be a discrete device or integrated into a microprocessor, CPU, FPGA, or ASIC. The Media Dependent Interface (MDI) connects the DP83822 to the transformer of the Ethernet network or to AC isolation capacitors when interfacing with a fiber transceiver.

9.2.2.2.1 MII Layout Guidelines

1. MII signals are single-ended signals
2. Traces should be routed with 50-Ω impedance to ground
3. Keep trace lengths as short as possible, less than two inches is recommended and less than six inches maximum

9.2.2.2.2 RMII Layout Guidelines

1. RMII signals are single-ended signals
2. Traces should be routed with 50-Ω impedance to ground
3. Keep trace lengths as short as possible, less than two inches is recommended and less than six inches maximum

9.2.2.2.3 RGMII Layout Guidelines

1. RGMII signals are single-ended signals
2. Traces should be routed with 50-Ω impedance to ground
3. Keep trace lengths as short as possible, less than two inches is recommended and less than six inches maximum
4. Internal Clock Delay can be enabled on the transmit and receive path independently within the DP83822 using register access

9.2.2.2.4 MDI Layout Guidelines

1. MDI signals are differential
2. Traces should be routed with 50-Ω impedance to ground and 100-Ω differential controlled impedance
3. Route MDI traces to the transformer on the same layer
4. Use a metal shielded RJ-45 connector and electrically connect the shield to chassis ground
5. Avoid supplies and ground beneath the magnetics
6. Do not overlap the circuit ground and chassis ground planes. Keep chassis ground and circuit ground isolated by turning chassis ground into an isolated island by leaving a gap between the planes. Connecting a 1206 (size) capacitor between chassis ground and circuit ground is recommended to avoid floating metal. Capacitors less than 805 (size) can create an arching path for ESD due to a small air-gap.

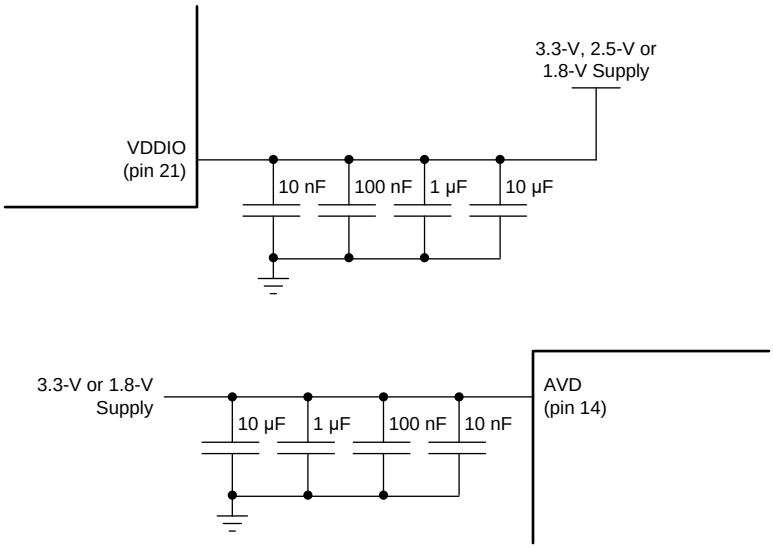
9.2.2.3 Application Curves

For expected Fiber network MDI curve, see Figure 19.

10 Power Supply Recommendations

The DP83822 is capable of operating with a wide range of I/O supply voltages (3.3 V, 2.5 V, or 1.8 V) along with any of the two analog supply options (3.3 V or 1.8 V).

The recommended power supply de-coupling network is shown below:



(1) The smallest value is placed closest to the pin

Figure 36. Power Connections

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

10.1 Power Supply Characteristics

The following data was measured using a DP83822 evaluation module. All the power dissipation numbers are measured at nominal voltage under typical temperature of 25°C. Center tap must be connected to the same potential as the analog supply rail (AVD).

Table 145. Power Supply Characteristics(1)

PARAMETER	TEST CONDITIONS	MAGNETIC SUPPLY (mA)	AVD SUPPLY (mA)	VDDIO SUPPLY (mA)	TOTAL POWER (mW)
3.3-V AVD/CT AND 3.3-V VDDIO					

(1) Ensured by production test, characterization, or design.

Power Supply Characteristics (continued)

Table 145. Power Supply Characteristics[1] (continued)

PARAMETER	TEST CONDITIONS	MAGNETIC SUPPLY (mA)	AVD SUPPLY (mA)	VDDIO SUPPLY (mA)	TOTAL POWER (mW)
100BASE-TX	MII, Link-Up, No Traffic	22	36	15	241
	MII, Link-Up, 960-ns IPG (100% Utilization), 1514-byte Packets, 25°C	22	36	21	261
	MII, Link-Up, 960-ns IPG (100% Utilization), 1514-byte Packets, -40°C	22	25	20	221
	MII, Link-Up, 960-ns IPG (100% Utilization), 1514-byte Packets, 125°C	22	52	22	317
	RMII, Link-Up, No Traffic	22	36	6	211
	RMII, Link-Up, 960-ns IPG (100% Utilization), 1514-byte Packets	22	36	7	215
	RGMII, Link-Up, No Traffic	22	36	8	218
	RGMII, Link-Up, 960-ns IPG (100% Utilization), 1514-byte Packets	22	36	9	221
10BASE-Te	MII, Link-Up, No Traffic	2	18	7	89
	MII, Link-Up, 960-ns IPG (100% Utilization), 1514-byte Packets	49	18	7	244
	RMII, Link-Up, No Traffic	2	18	6	86
	RMII, Link-Up, 960ns IPG (100% Utilization), 1514-byte Packets	49	18	6	241
	RGMII, Link-Up, No Traffic	2	18	7	89
	RGMII, Link-Up, 960-ns IPG (100% Utilization), 1514-byte Packets	49	18	7	244
Passive Sleep	RMII, bits[15:12] = 0b0111 in register 0x0011	2	16	6	79
Active Sleep	RMII, bits[15:12] = 0b0110 in register 0x0011	2	16	6	79
IEEE Power Down	RMII, bits[11] = 1 in register 0x0000	2	4	6	40
Deep Power Down	RMII, bits[11] = 1 in register 0x0000 and bit[2] = 1 in register 0x0428	2	3	6	36
Energy Efficient Ethernet	TX and RX LPI, RMII	2	17	6	83
3.3-V AVD/CT AND 1.8-V VDDIO					
100BASE-TX	MII, Link-Up, No Traffic	22	36	10	209
	MII, Link-Up, 960-ns IPG (100% Utilization), 1514-byte Packets	22	36	12	213
	RMII, Link-Up, No Traffic	22	36	3	197
	RMII, Link-Up, 960-ns IPG (100% Utilization), 1514-byte Packets	22	36	4	199
	RGMII, Link-Up, No Traffic	22	36	5	200
	RGMII, Link-Up, 960-ns IPG (100% Utilization), 1514-byte Packets	22	36	5	200
10BASE-Te	MII, Link-Up, No Traffic	2	18	4	73
	MII, Link-Up, 960ns IPG (100% Utilization), 1514-byte Packets	49	18	4	228
	RMII, Link-Up, No Traffic	2	18	3	71
	RMII, Link-Up, 960-ns IPG (100% Utilization), 1514-byte Packets	49	18	3	227
	RGMII, Link-Up, No Traffic	2	18	4	73
	RGMII, Link-Up, 960-ns IPG (100% Utilization), 1514-byte Packets	49	18	4	228

Power Supply Characteristics (continued)

Table 145. Power Supply Characteristics(1) (continued)

PARAMETER	TEST CONDITIONS	MAGNETIC SUPPLY (mA)	AVD SUPPLY (mA)	VDDIO SUPPLY (mA)	TOTAL POWER (mW)
Passive Sleep	RMII, bits[15:12] = 0b0111 in register 0x0011	2	16	3	65
Active Sleep	RMII, bits[15:12] = 0b0110 in register 0x0011	2	16	3	65
IEEE Power Down	RMII, bits[11] = 1 in register 0x0000	2	4	3	25
Deep Power Down	RMII, bits[11] = 1 in register 0x0000 and bit[2] = 1 in register 0x0428	2	3	3	22
Energy Efficient Ethernet	TX and RX LPI, RMII	2	17	3	68

Power Supply Characteristics (continued)

Table 145. Power Supply Characteristics[1] (continued)

PARAMETER	TEST CONDITIONS	MAGNETIC SUPPLY (mA)	AVD SUPPLY (mA)	VDDIO SUPPLY (mA)	TOTAL POWER (mW)
1.8-V AVD/CT AND 3.3-V VDDIO					
100BASE-TX	MII, Link-Up, No Traffic	22	36	15	154
	MII, Link-Up, 960-ns IPG (100% Utilization), 1514-byte Packets	22	36	21	174
	RMII, Link-Up, No Traffic	22	36	6	124
	RMII, Link-Up, 960-ns IPG (100% Utilization), 1514-byte Packets	22	36	7	128
	RGMII, Link-Up, No Traffic	22	36	8	131
	RGMII, Link-Up, 960-ns IPG (100% Utilization), 1514-byte Packets	22	36	9	134
10BASE-Te	MII, Link-Up, No Traffic	1	17	7	56
	MII, Link-Up, 960-ns IPG (100% Utilization), 1514-byte Packets	49	17	7	142
	RMII, Link-Up, No Traffic	1	17	6	52
	RMII, Link-Up, 960-ns IPG (100% Utilization), 1514-byte Packets	49	17	6	139
	RGMII, Link-Up, No Traffic	1	17	7	56
	RGMII, Link-Up, 960-ns IPG (100% Utilization), 1514-byte Packets	49	17	7	142
Passive Sleep	RMII, bits[15:12] = 0b0111 in register 0x0011	1	16	6	50
Active Sleep	RMII, bits[15:12] = 0b0110 in register 0x0011	1	16	6	50
IEEE Power Down	RMII, bits[11] = 1 in register 0x0000	1	4	6	29
Deep Power Down	RMII, bits[11] = 1 in register 0x0000 and bit[2] = 1 in register 0x0428	1	3	6	27
Energy Efficient Ethernet	TX and RX LPI, RMII	1	17	6	52

Power Supply Characteristics (continued)

Table 145. Power Supply Characteristics(1) (continued)

PARAMETER	TEST CONDITIONS	MAGNETIC SUPPLY (mA)	AVD SUPPLY (mA)	VDDIO SUPPLY (mA)	TOTAL POWER (mW)
1.8-V AVD/CT AND 1.8-V VDDIO					
100BASE-TX	MII, Link-Up, No Traffic	22	36	10	122
	MII, Link-Up, 960-ns IPG (100% Utilization), 1514-byte Packets	22	36	12	126
	RMII, Link-Up, No Traffic	22	36	3	110
	RMII, Link-Up, 960-ns IPG (100% Utilization), 1514-byte Packets	22	36	4	112
	RGMII, Link-Up, No Traffic	22	36	5	113
	RGMII, Link-Up, 960-ns IPG (100% Utilization), 1514-byte Packets	22	36	5	113
10BASE-Te	MII, Link-Up, No Traffic	1	17	4	40
	MII, Link-Up, 960-ns IPG (100% Utilization), 1514-byte Packets	49	17	4	126
	RMII, Link-Up, No Traffic	1	17	3	38
	RMII, Link-Up, 960-ns IPG (100% Utilization), 1514-byte Packets	49	17	3	124
	RGMII, Link-Up, No Traffic	1	17	4	40
	RGMII, Link-Up, 960-ns IPG (100% Utilization), 1514-byte Packets	49	17	4	126
Passive Sleep	RMII, bits[15:12] = 0b0111 in register 0x0011	1	16	3	36
Active Sleep	RMII, bits[15:12] = 0b0110 in register 0x0011	1	16	3	36
IEEE Power Down	RMII, bits[11] = 1 in register 0x0000	1	4	3	14
Deep Power Down	RMII, bits[11] = 1 in register 0x0000 and bit[2] = 1 in register 0x0428	1	3	3	13
Energy Efficient Ethernet	TX and RX LPI, RMII	1	17	3	38

11 Layout

11.1 Layout Guidelines

11.1.1 Signal Traces

PCB traces are lossy and long traces can degrade signal quality. Traces should be kept short as possible. Unless mentioned otherwise, all signal traces should be 50-Ω single-ended impedance. Differential traces should be 50-Ω single-ended and 100-Ω differential. Take care to ensure impedance is controlled throughout. Impedance discontinuities will cause reflections leading to emissions and signal integrity issues. Stubs should be avoided on all signal traces, especially differential signal pairs.

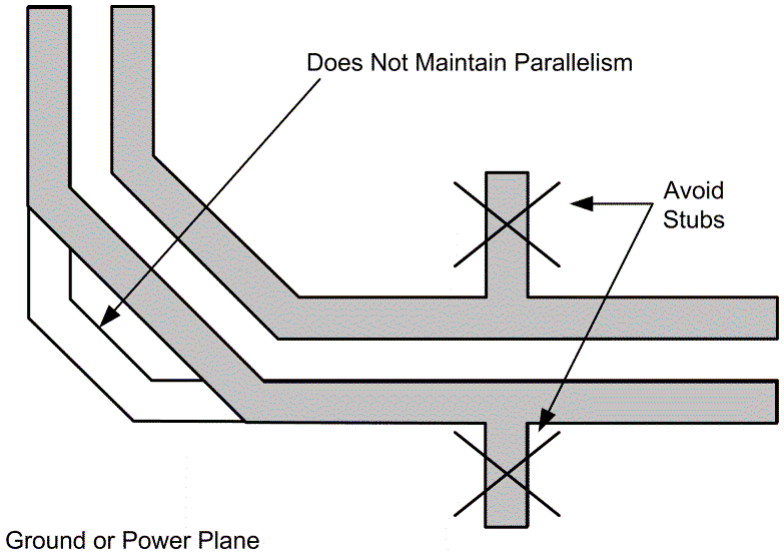


Figure 37. Differential Signal Traces

Within the differential pairs, trace lengths should be run parallel to each other and matched in length. Matched lengths minimize delay differences, avoiding an increase in common mode noise and emissions. Length matching is also important for MAC interface connections. All transmit signal traces should be length matched to each other and all receive signal traces should be length matched to each other.

Ideally, there should be no crossover or vias on signal path traces. Vias present impedance discontinuities and should be minimized when possible. Route trace pairs on the same layer. Signals on different layers should not cross each other without at least one return path plane between them. Differential pairs should always have a constant coupling distance between them. For convenience and efficiency, TI recommends routing critical signals first (that is, MDI differential pairs, reference clock, and MAC IF traces).

Layout Guidelines (continued)

11.1.2 Return Path

A general best practice is to have a solid return path beneath all signal traces. This return path can be a continuous ground or DC power plane. Reducing the width of the return path can potentially affect the impedance of the signal trace. This effect is more prominent when the width of the return path is comparable to the width of the signal trace. Breaks in return path between the signal traces should be avoided at all cost. A signal crossing a split plane may cause unpredictable return path currents and could impact signal quality and result in emissions issues.

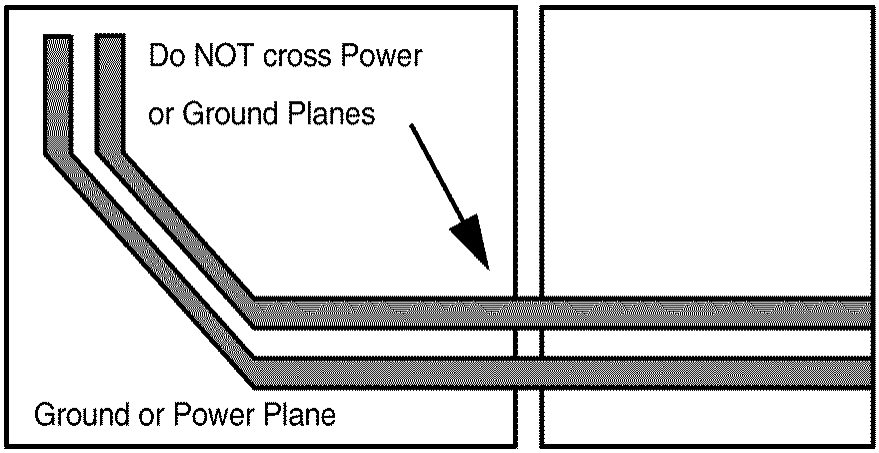


Figure 38. Differential Signal Pair and Plane Crossing

Layout Guidelines (continued)

11.1.3 Transformer Layout

There must be no metal layer running beneath the transformer. Transformers can inject noise into metal beneath them, which can affect the performance of the system. Because the DP83822 is a current mode line driver design, the center tap pin on the device side of the transformer must be tied to the analog supply rail (AVD). De-coupling capacitors must be placed near the center tap pin of the transformer as shown in Figure 33.

11.1.3.1 Transformer Recommendations

The following magnetics have been tested with the DP83822 using the DP83822EVM.

Table 146. Recommended Transformers

MANUFACTURER	PART NUMBER
Pulse Electronics	HX1198FNL
	HX1188NL
	HX1188FNL
	H2019NL
	H1102NL
Abracon	ALAN101
Bel Fuse	S5585999J1F
Sumida	CLP0612
Wurth Electronics	7490120110
	733330
	7490100111a

Table 147. Transformer Electrical Specifications

PARAMETER	TEST CONDITIONS	TYP	UNIT
Turn Ratio	±2%	1:1	-
Insertion Loss	1 - 100 MHz	–1	dB
Return Loss	1 - 30 MHz	–16	dB
	30 - 60 MHz	–12	dB
	60 - 80 MHz	–10	dB
Differential to Common Rejection Ratio	1 - 50 MHz	–30	dB
	50 - 150 MHz	–20	dB
Crosstalk	30 MHz	–35	dB
	60 MHz	–30	dB
Isolation	HPOT	1500	Vrms

11.1.4 Metal Pour

All metal pours that are not signals or power must be tied to ground. There must be no floating metal in the system, and there must be no metal between differential traces.

11.1.5 PCB Layer Stacking

To meet signal integrity and performance requirements, a minimum four-layer PCB is recommended. However, a six-layer PCB should be used when possible.

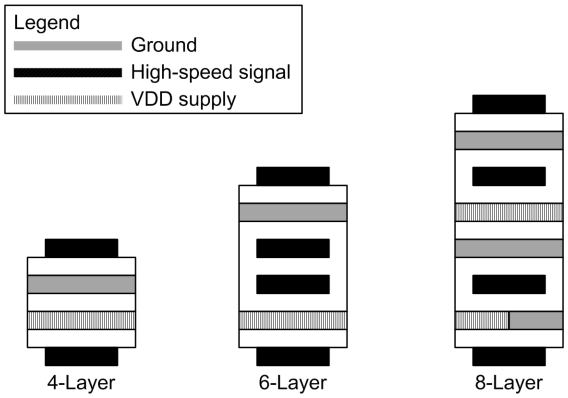


Figure 39. Recommended Layer Stack-Up

11.2 Layout Example

See the DP83822EVM for more information regarding layout.

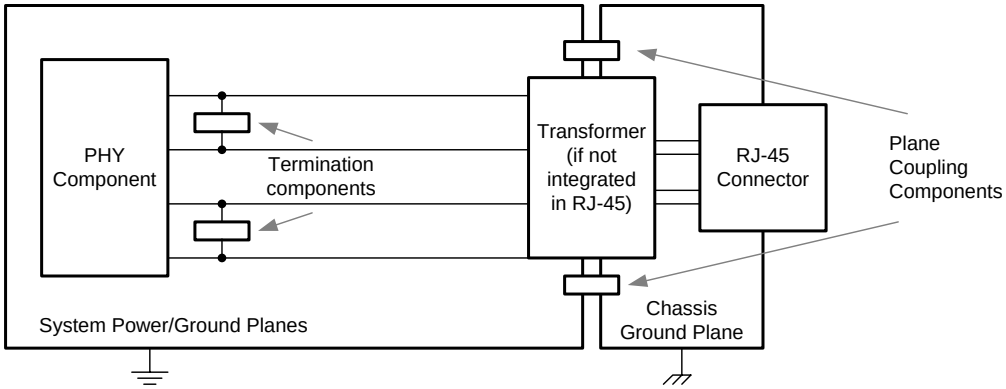


Figure 40. Layout Example

12 Device and Documentation Support

12.1 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

Table 148. Related Links

PARTS	PRODUCT FOLDER	ORDER NOW	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
DP83822HF	Click here	Click here	Click here	Click here	Click here
DP83822IF	Click here	Click here	Click here	Click here	Click here
DP83822H	Click here	Click here	Click here	Click here	Click here
DP83822I	Click here	Click here	Click here	Click here	Click here

12.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

12.3 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

12.4 Trademarks

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

12.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

12.6 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
DP83822HFRHBR	ACTIVE	VQFN	RHB	32	3000	Green (RoHS & no Sb/Br)	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	822HF	Samples
DP83822HFRHBT	ACTIVE	VQFN	RHB	32	250	Green (RoHS & no Sb/Br)	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	822HF	Samples
DP83822HRHBR	ACTIVE	VQFN	RHB	32	3000	Green (RoHS & no Sb/Br)	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	822H	Samples
DP83822HRHBT	ACTIVE	VQFN	RHB	32	250	Green (RoHS & no Sb/Br)	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	822H	Samples
DP83822IFRHBR	ACTIVE	VQFN	RHB	32	3000	Green (RoHS & no Sb/Br)	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	822IF	Samples
DP83822IFRHBT	ACTIVE	VQFN	RHB	32	250	Green (RoHS & no Sb/Br)	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	822IF	Samples
DP83822IRHBR	ACTIVE	VQFN	RHB	32	3000	Green (RoHS & no Sb/Br)	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	822I	Samples
DP83822IRHBT	ACTIVE	VQFN	RHB	32	250	Green (RoHS & no Sb/Br)	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	822I	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

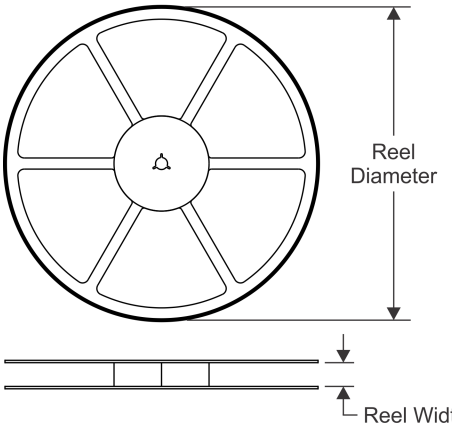
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

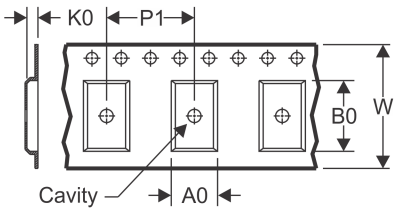
(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

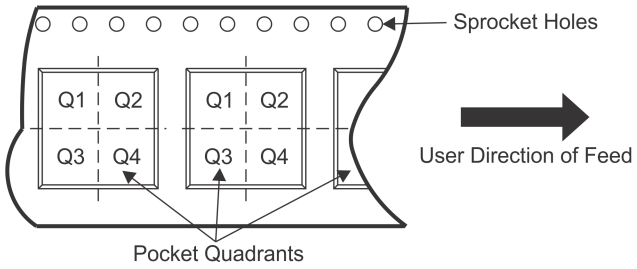


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

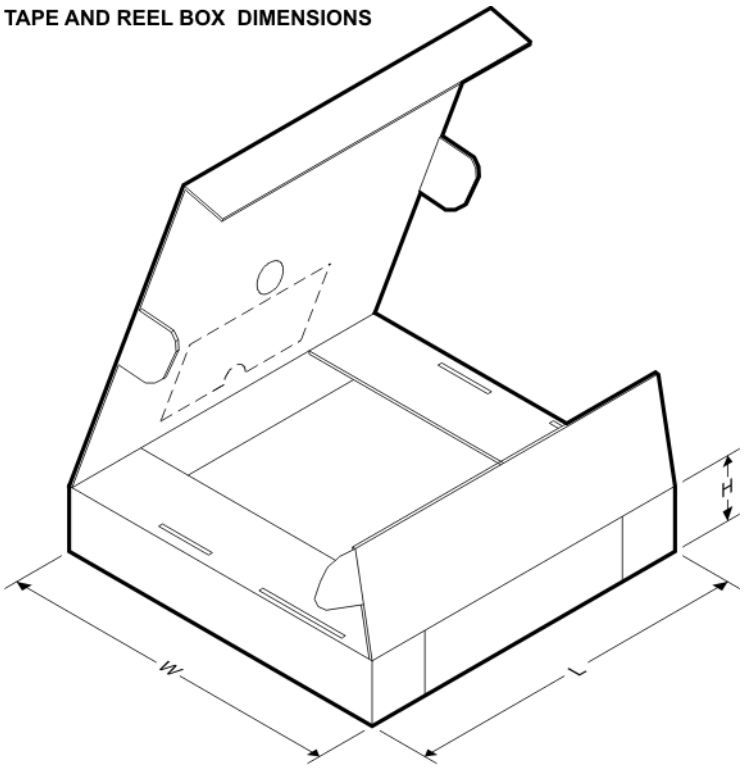
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
DP83822HFRHBR	VQFN	RHB	32	3000	330.0	12.4	5.3	5.3	1.1	8.0	12.0	Q1
DP83822HFRHBT	VQFN	RHB	32	250	178.0	12.4	5.3	5.3	1.1	8.0	12.0	Q1
DP83822HRHBR	VQFN	RHB	32	3000	330.0	12.4	5.3	5.3	1.1	8.0	12.0	Q1
DP83822HRHBT	VQFN	RHB	32	250	178.0	12.4	5.3	5.3	1.1	8.0	12.0	Q1
DP83822IFRHBR	VQFN	RHB	32	3000	330.0	12.4	5.3	5.3	1.1	8.0	12.0	Q1
DP83822IFRHBT	VQFN	RHB	32	250	178.0	12.4	5.3	5.3	1.1	8.0	12.0	Q1
DP83822IRHBR	VQFN	RHB	32	3000	330.0	12.4	5.3	5.3	1.1	8.0	12.0	Q1
DP83822IRHBT	VQFN	RHB	32	250	178.0	12.4	5.3	5.3	1.1	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
DP83822HFRHBR	VQFN	RHB	32	3000	367.0	367.0	35.0
DP83822HFRHBT	VQFN	RHB	32	250	210.0	185.0	35.0
DP83822HRHBR	VQFN	RHB	32	3000	367.0	367.0	35.0
DP83822HRHBT	VQFN	RHB	32	250	213.0	191.0	55.0
DP83822IFRHBR	VQFN	RHB	32	3000	367.0	367.0	35.0
DP83822IFRHBT	VQFN	RHB	32	250	213.0	191.0	55.0
DP83822IRHBR	VQFN	RHB	32	3000	367.0	367.0	35.0
DP83822IRHBT	VQFN	RHB	32	250	213.0	191.0	55.0

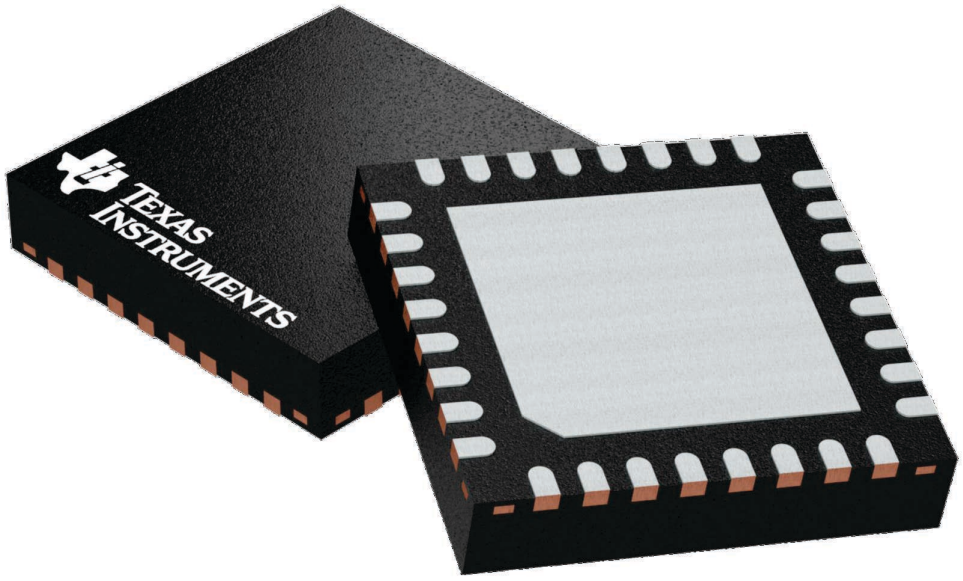
GENERIC PACKAGE VIEW

RHB 32

VQFN - 1 mm max height

5 x 5, 0.5 mm pitch

PLASTIC QUAD FLATPACK - NO LEAD



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

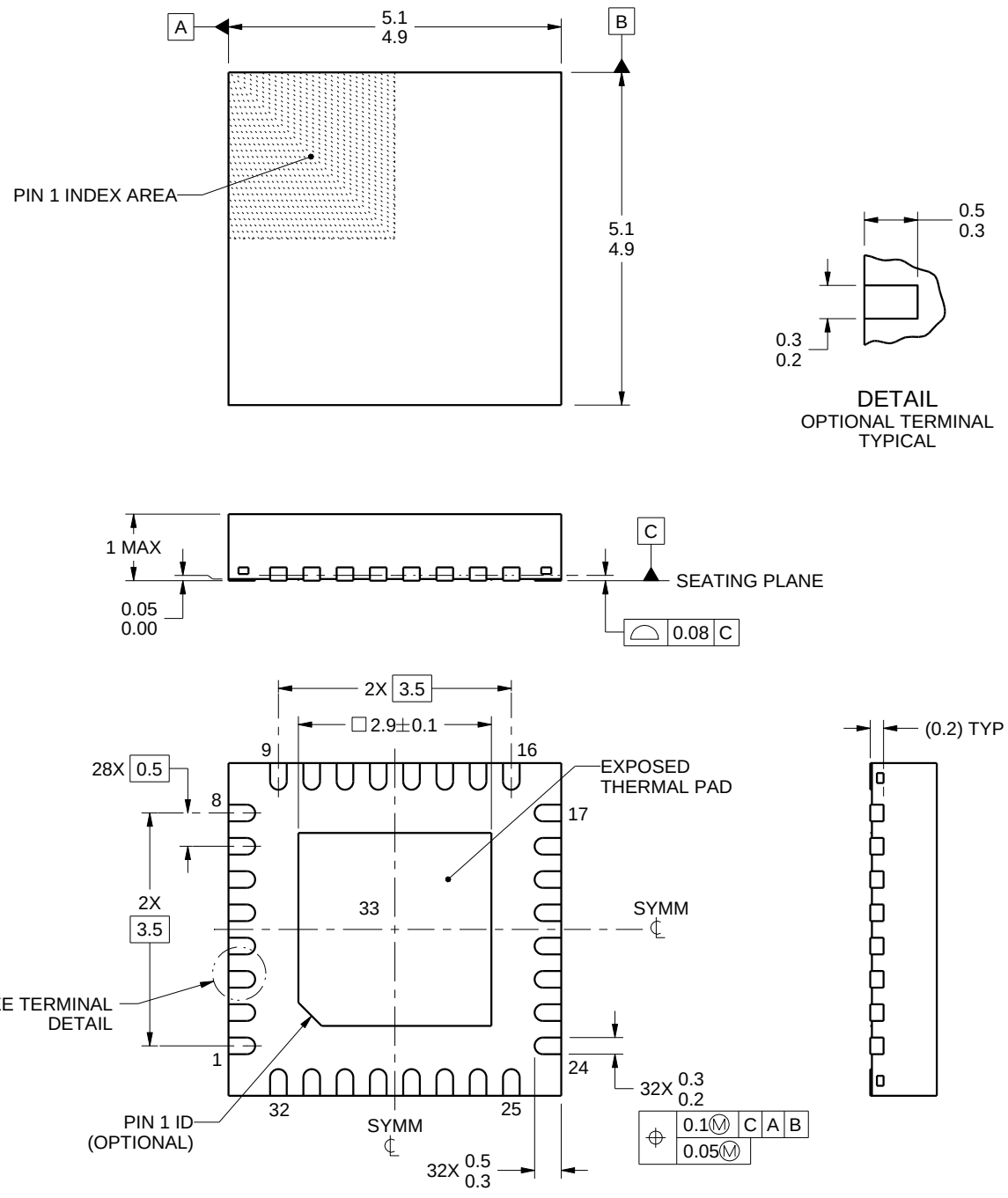
4224745/A

PACKAGE OUTLINE

RHB0032B

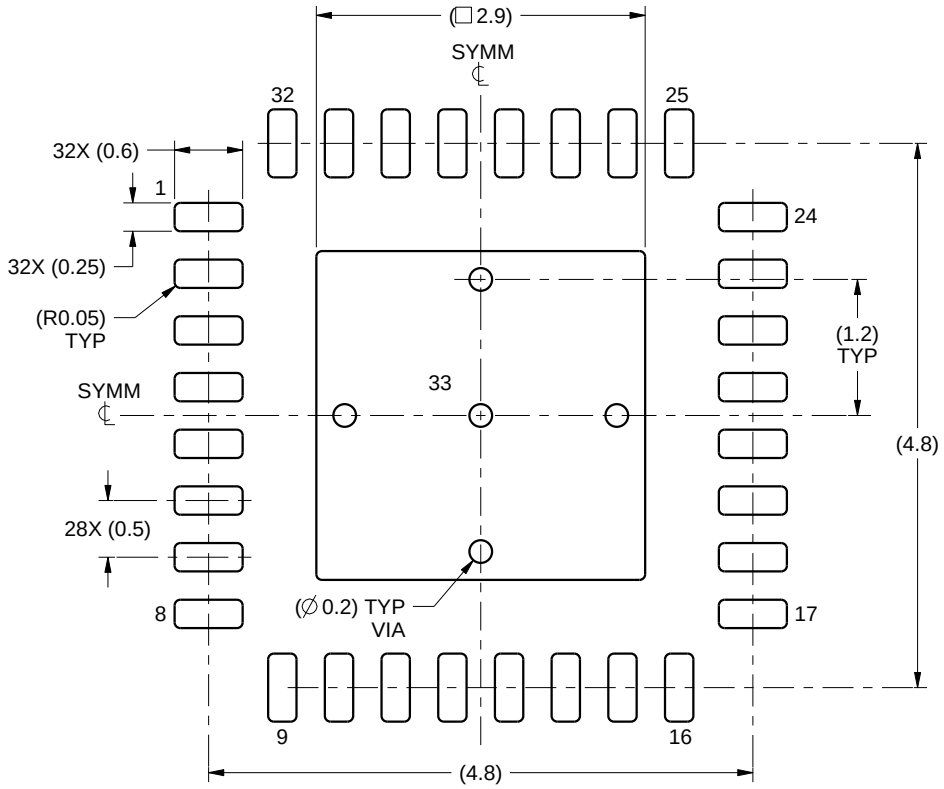
VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



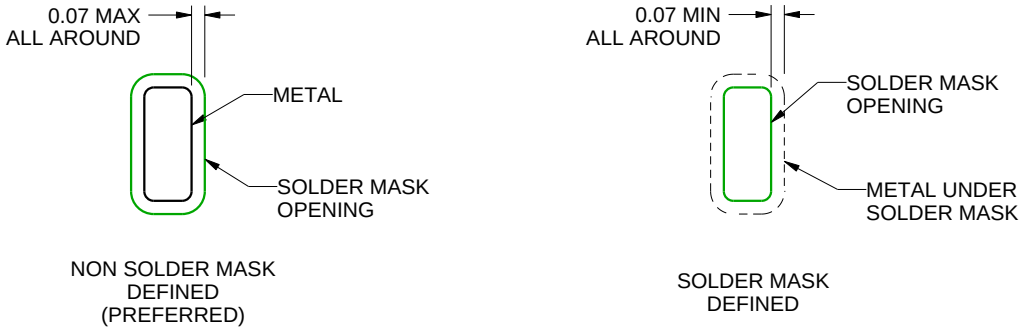
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE

SCALE:15X

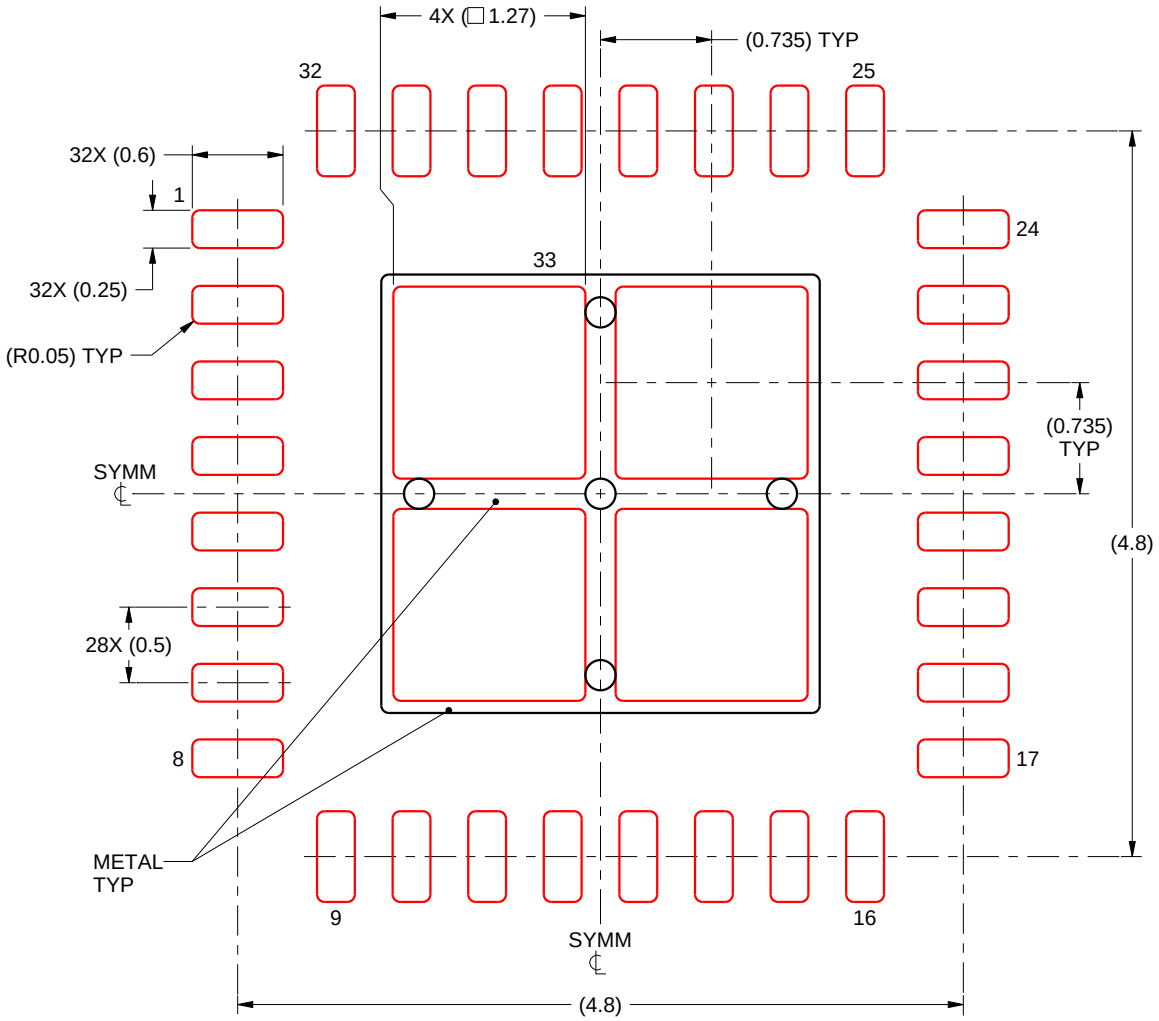


SOLDER MASK DETAILS

4223216/A 08/2016

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 33
76.7% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:20X

4223216/A 08/2016

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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