Buck Converter Design Project

EE365 - Power Electronics

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- Goal of project:
  - Design a Buck converter with the following specifications.
- Specification:
  - $32\ V \leqq V_{in} \leqq 48\ V$.
  - $V_{out} = 24\ V$.
  - $f_{switch} = 50\ kHz$.
  - $P_{Nominal} = 50\ W$.
  - $I_{L,\ peak\ ripple} = 10\% \cdot I_L$
  - $V_{out,\ peak\ ripple} = 1\% \cdot V_{out}$

1.Buck Converter Specifications

- I/O Voltage transfer function:

  Vout/ Vin = D (range: 0.5 - 0.75)

  $$\Delta I_L = \frac{V_{out}}{L_{min}}(1 - D)T_s$$

  $L_{min} = L_{selected}$ = 1.2 mH (D = 0.5)

- $$C_{min} = \frac{\Delta I_L \; T_s}{8 \Delta V_{out}}$$ = 2.167 μF,

  $C_{selected}$ = 2.2 μF

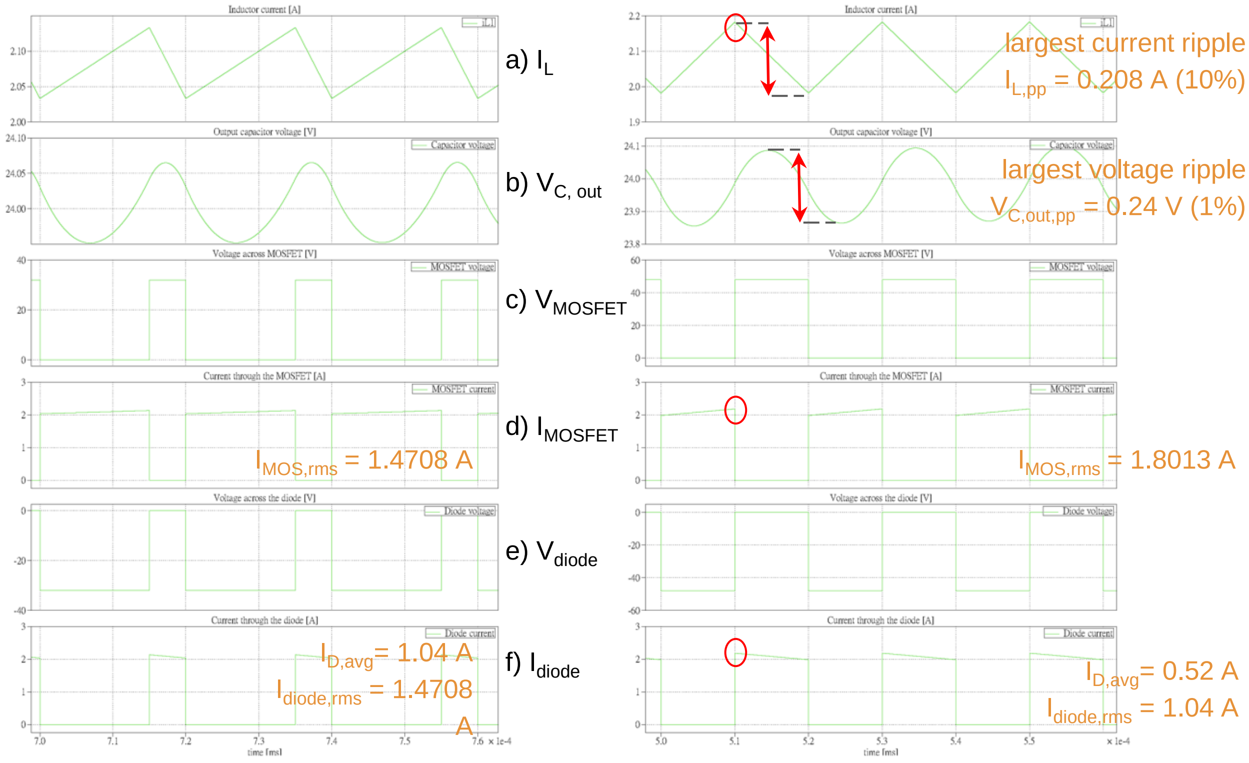
2.Semiconductor Components

- $$I_{L,Max} = I_L + \frac{\Delta I_{L,pp}}{2}$$

  = $I_{MOSFET,max}$ = $I_{diode,max}$ = 2.184 A

- $V_{MOSFET,max}$ = $V_{diode,max}$ = 48 V
- MOSFET model 4: ZXMN10A11K
- Diode model 1: B3100-13-F

PLECS verification through simulations



V_{in} = 48 V with D = 0.75

V_{in} = 32 V with D = 0.5

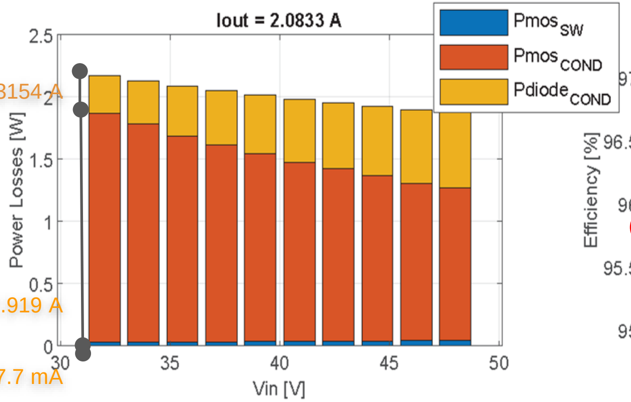
3.Buck Converter Power Losses

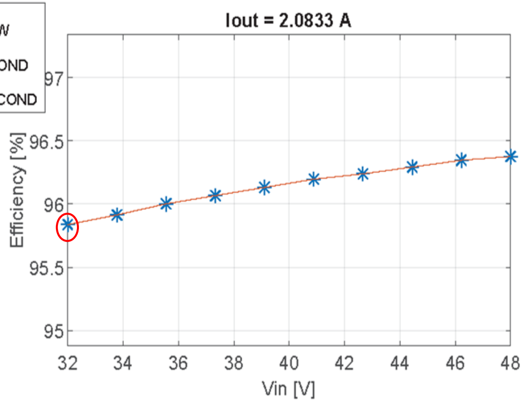
- Choice of the operating point: **V_{in} = 32 V, P_{out} = 50 W**.
- $P_{Cond,MOS} = R_{DS,on} \cdot I_{D,rms}^2 = 0.6 \times 1.82^2$
- $P_{Cond,Diode} = U_{D0} \cdot I_{D,avg} + R_D \cdot I_{D,rms}^2 = 0.2 \times 0.525 + 0.2 \times 1.05^2$
- $P_{on,MOS} = E_{on,MOS} \cdot f_{sw}$
  - $E_{on,MOS} \cong V_{in} \cdot I_L \cdot (t_{ri}+t_{fu})/2$
- $P_{off,MOS} = E_{off,MOS} \cdot f_{sw}$
  - $E_{off,MOS} \cong V_{in} \cdot I_{d,off} \cdot (t_{ru}+t_{fi})/2$ with $I_{d,off} = I_{L,max} = 2.184$ A
- MATLAB losses tool verification

$P_{cond,Diode}$ = 0.3154 A

$P_{cond,MOS}$ = 1.919 A

$P_{sw,MOS}$ = 27.7 mA





Property	Value	Unit
L	1.2	mH
C	2.2	µF
$P_{cond,MOSFET}$	1.99	W
$P_{on,MOSFET}$	7.6	mW
$P_{off,MOSFET}$	14.9	mW
$P_{cond,DIODE}$	0.33	W
P_{total}	2.3425	W
Efficiency	95.31	%
MOSFET model	4	
DIODE model	1	

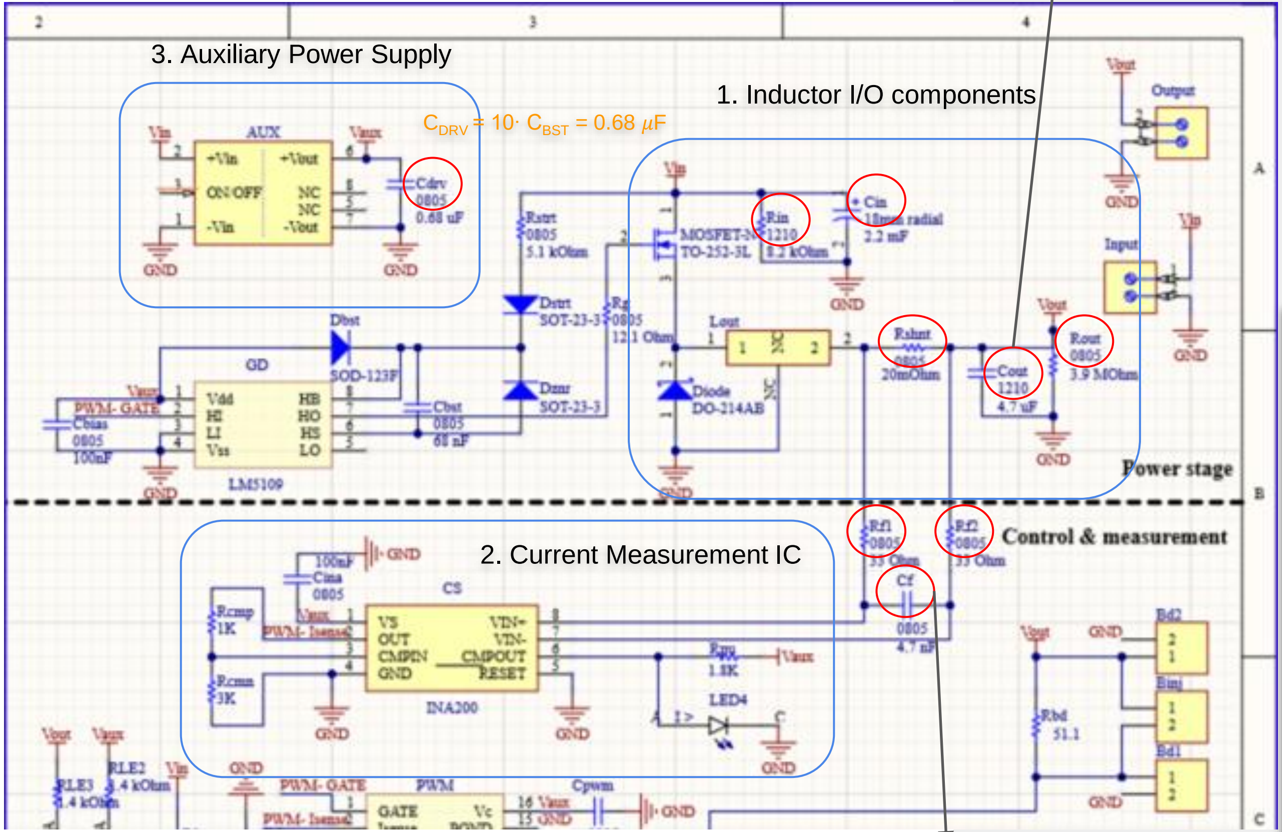
$P_{sw,MOS}$ = 22.5 mA

$$P_{ttl} = P_{cond,M} + P_{con,D} + P_{on,M} + P_{off,M}$$
$$\eta = \frac{P_{out} - P_{ttl}}{P_{in}}.$$

- Heatsink selection for diode and MOSFET

12V, 2W
(Paux,min ≅ 0.245 W)

Verify the theoretical ESR ($\Delta V_{C,out,ripple}$ / $\Delta I_{L,\ ripple}$) with the value from data sheet of C_{out} model

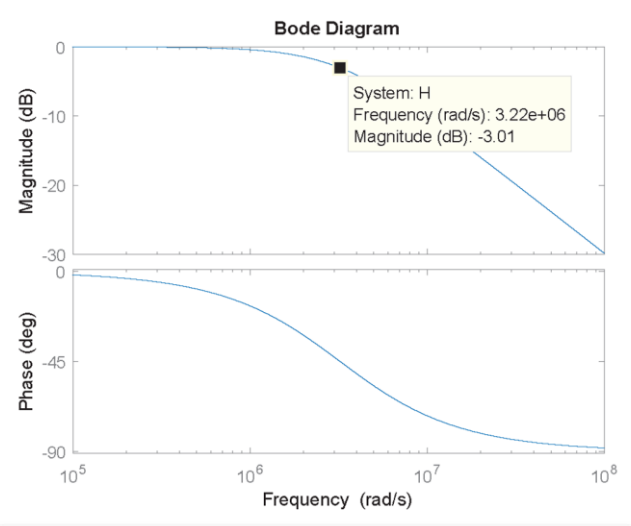


1. Select R_{in}, C_{in}, R_{out}, C_{out}

   Power dissipations: P_{ESR}, $P_{R,in}$, $P_{R,out}$

2. Select R_{shunt}, R_f, C_f

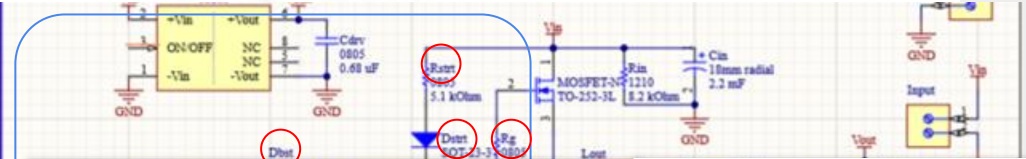
   Power dissipation: P_{shunt}

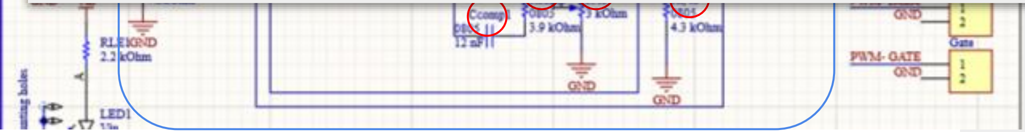


Current Measurement Filtering

Current measurement filtering: R_f & C_f for the desired cutoff frequency ($f_c = 1/(4\pi RC) = 500$ kHz)

5. Half Bridge Gate Driver

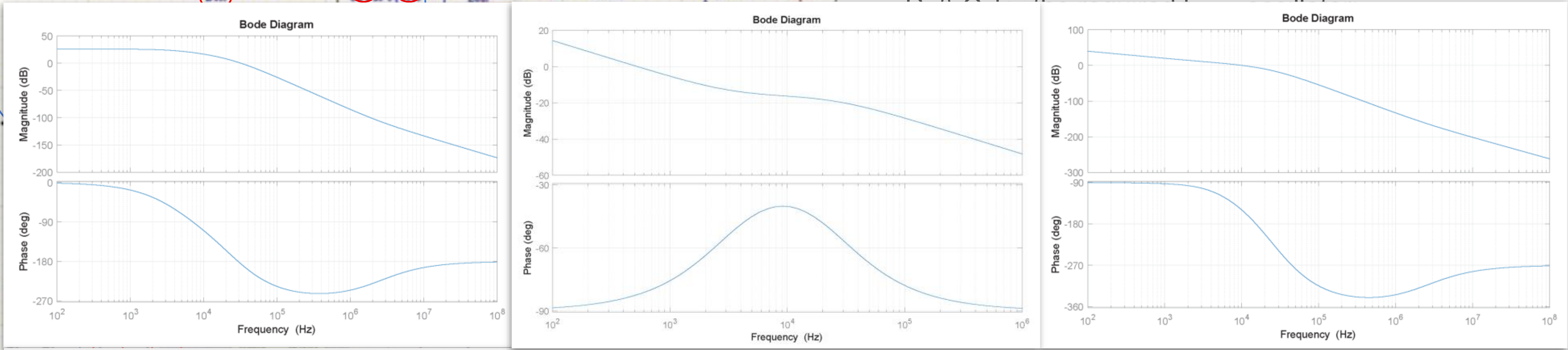




4. PWM Controller IC

4. $C_{soft\ start}$ for 10 ms start-up time ($t_{ss} = 9x10^4 \cdot C_{ss}$);

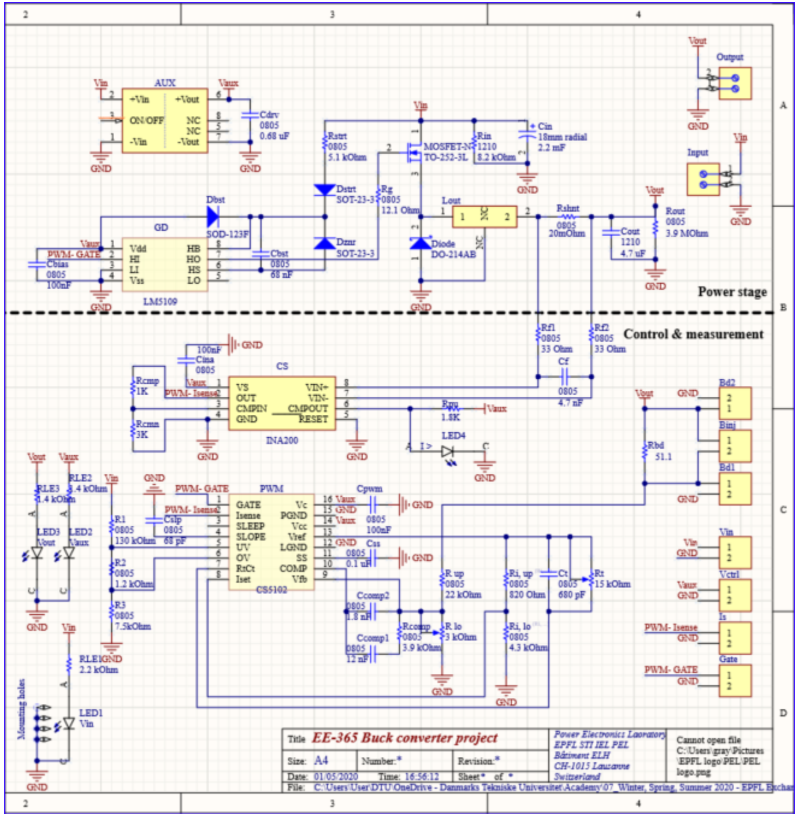
R_1, R_2, R_3 for under-and-over-voltage protection;



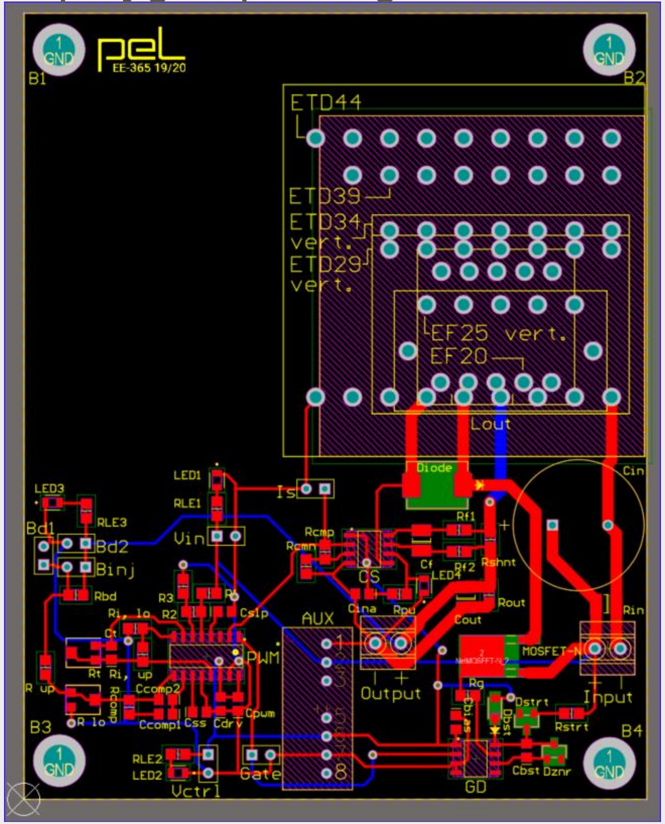
Transfer functions:
Left: Control-to-Output; Center: Compensator; Right: Final Control-to-Output with Compensator

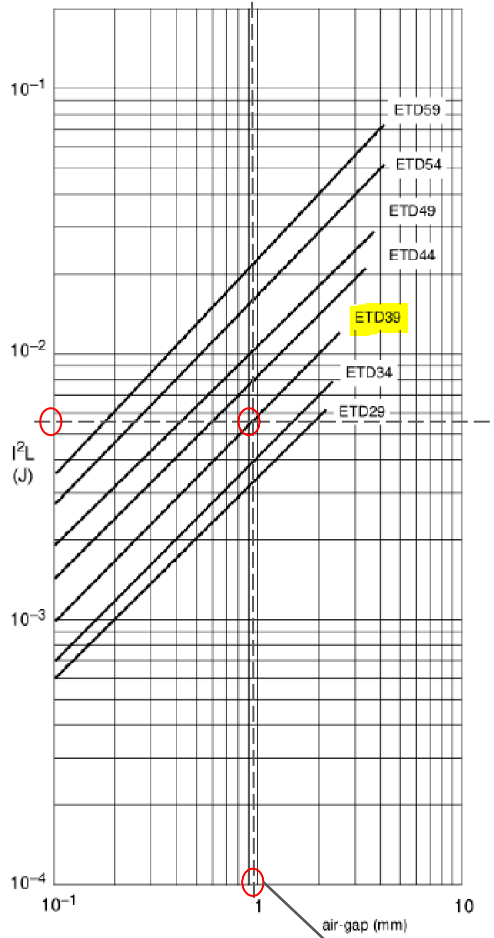
Bootstrap, start-up & zener diodes

❑ PCB schematic



❑ PCB layout overview with polygon pourings shelved





I^2L chart

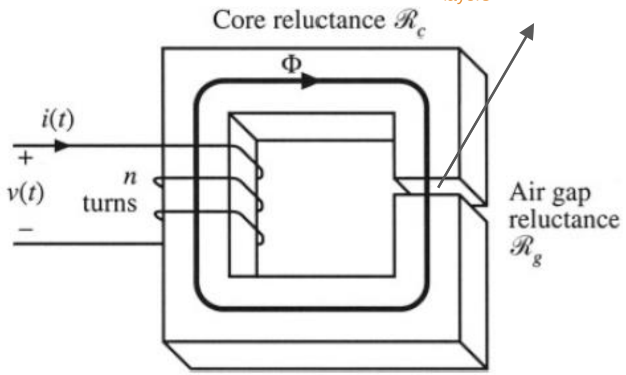
$l_{g,estimate}$= 0.95 mm

1. Inductor specification & Design constraints

- $B_{max} = 0.3$ T
- $K_u = 0.5$
- $R_{L,max}$= 0.22Ω (2% P_{out})
- $J_W = 2\ A/mm^2$

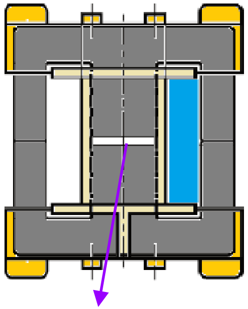
2. Preselection of inductor cores

Air gap length l_g
Kapton tap layers
N_{layers}



Inductor Geometry

Inductor Core model: ETD39/20/13



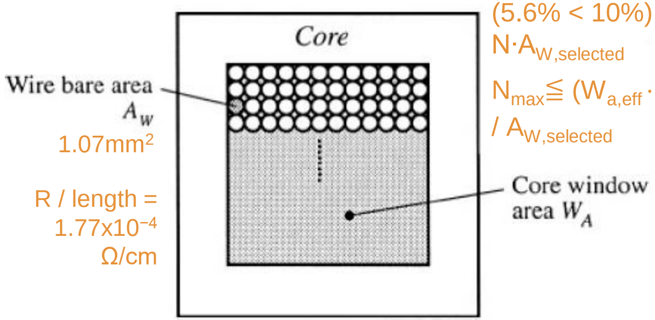
Core c-s area A_c

$A_{p,core} = W_{A,eff} \cdot A_c$
$\geqq A_{p,min} = (L \cdot I_{L,pk} \cdot I_{L,rms}) / (B_{max} \cdot J_w \cdot K_u)$

3. Magnetic wire selection & number of turns calculation

conductor area (5.6% < 10%)
$N \cdot A_{W,selected}$

$N_{max} \leqq (W_{a,eff} \cdot K_u) / A_{W,selected}$



1.07mm²

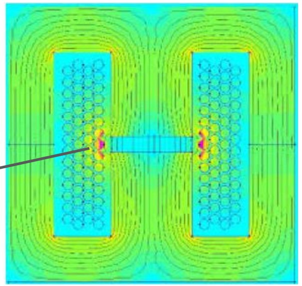
R / length = 1.77×10^{-4} Ω/cm

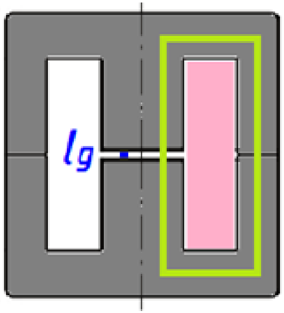
Core Window Area Utilization

4. Calculation of air gap length, fringing flux factor & adjustment of $N_{selected}$ with F_{fringe}

G = 25.7mm

$F_{fringe} = 1.28$





Fringing flux induced copper losses

$l_g = (\mu_0 \cdot N^2_{selected} \cdot A_C) / L - MPL / \mu_r$

$= 0.75$ mm

$l_{g,estimate} = 0.95$ mm

$N_{layers} = l_g / \text{thickness} \cdot ½ = 5.8$

thus count 6 layers.

$$N_{new\ selected} = \sqrt{\left(l_g + \frac{MPL}{\mu_r}\right)\frac{L/F_{fringe}}{\mu_0 \cdot A_C}}$$

$= 68.92$

5. Verification of the design constraints

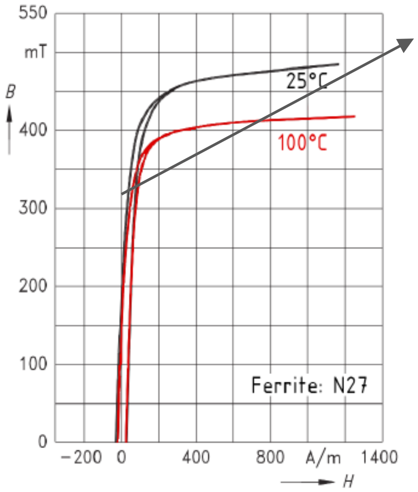
$R_L = N_{new} \cdot MLT \cdot \frac{R}{length}$ = 83 mΩ, while $R_{L,max}$ = 220 mΩ

$P_{Cu,dc} = 0.38$ W = 0.76% P_{out}

$B_{ac} = 14.4$ mT

$B_{pk} = 302.5$ mT

$K_u = 0.43$ with N_{new}



$B_{pk} < B_{sat}$

Saturation flux density of ferrite N27

- Compute the overall efficiency of your Buck converter for the nominal output power.
  - $\eta_{Buck,best} = 94.4\%$

    with $V_{in} = 48$ V, $P_{loss,R1,min} = 1.8$ W
  - $\eta_{Buck,worst} = 93.8\%$

    with $V_{in} = 32$ V, $P_{loss,R1,max} = 2.17$ W

Summary table for the Buck Converter Design

Electrical specification		
Nominal inductance	L_{nom}	1.2 mH
Effective current	$I_{L,rms}$	2.14 A
Current ripple	$\Delta I_{L,pk-pk}$	2.08 A
Ripple frequency	f_{sw}	50 kHz
Core specification		
Core shape and size		ETD39/20/13
Coil former		B66364B1016T001
Core material		N27
Peak flux density	B_{pk}	302.5 mT
Air gap length	l_g	0.75 mm
Number of Kapton tape layers		6
Winding specification		
wire diameter	$\varnothing$	1.2 mm
number of turns	N	68
Losses and temperature rise		
Core losses	P_{core}	0.069 W
Winding losses	$P_{Cu,dc}$	0.38 W
Total inductor losses	$P_{L,loss}/P_{out}$	0.9 %
Temperature rise	ΔT	7.2 K

- Challenges/ Problems
  - Understanding how to find the good components on DigiKey
  - Understanding the relationship between the to ICs in Report 2 and finding the needed info in the datasheets and Application Notes.
- Learnings
  - Extract needed information from application notes and data sheets.
  - How to select a component from DigiKey.
  - How is Buck converter constituted from A to Z.
- Feedback for the design project
  - Include more theory related to the project in the lectures.

Thank you for your attention!