I^2C Communication - Physical Layer

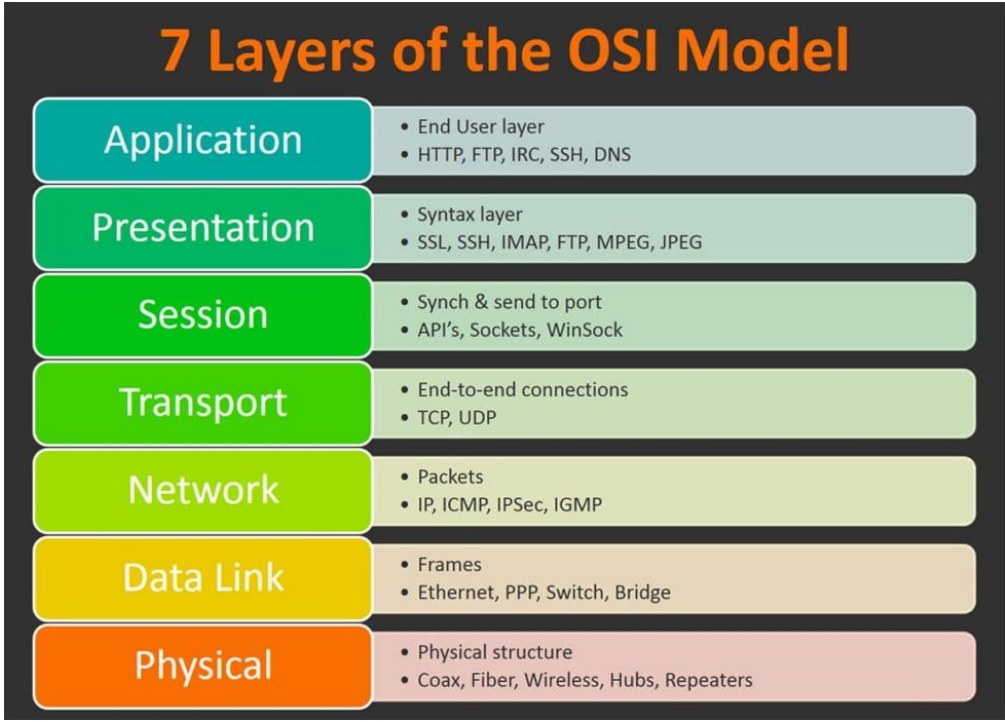
Nathan Gardner - Technical Presentation

I^2C basic overview

- Invented in 1982 by Philips Semiconductors (now NXC Semiconductors)
- Original I^2C was patented in 1981 but has since been expanded greatly and specified
- De Facto Standard for many years official specification in 1992
- NXC has stake in specification now, as well as many other companies
- Focus on Physical Layer of I^2C

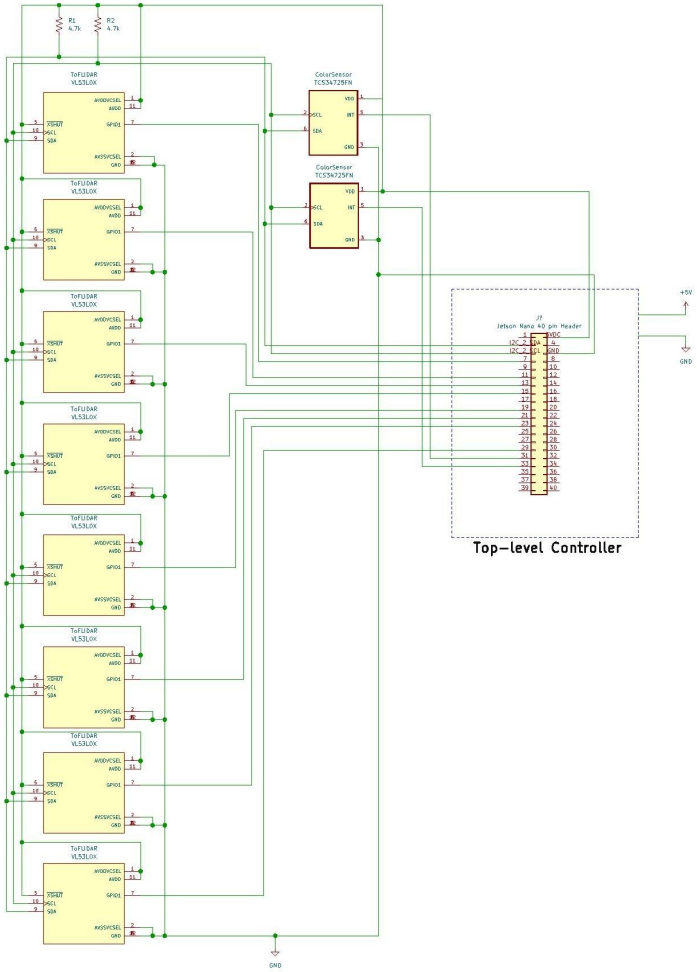
What is the Physical Layer?

- Physical structure of the connections and circuit typology
- I^2C Physical: bus topology, open drain bus, clock stretching, multi-master, clock and data arbitration



How is the SECON robot using it?

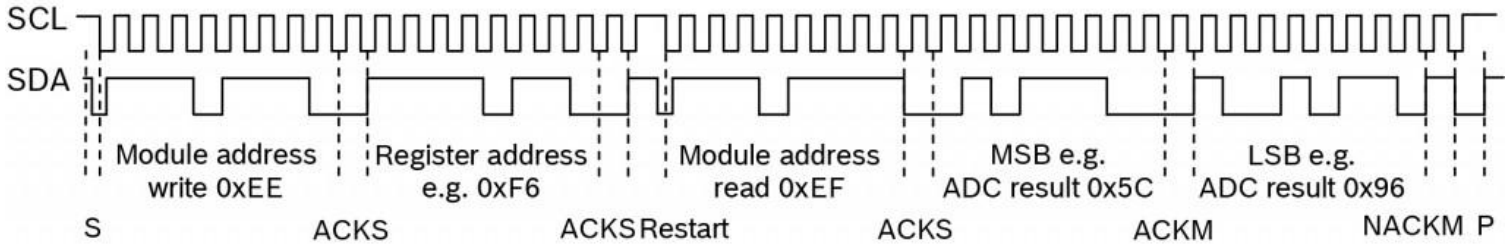
- Communication with sensors onboard robot
- Ten sensors in vision subsystem all connected via two wire communication to controller



Two line bus topology

Serial Clock (SCL) - Clock for data, rising edge sensitive

Serial Data (SDA) - Data line, where data electrical signals will be read from



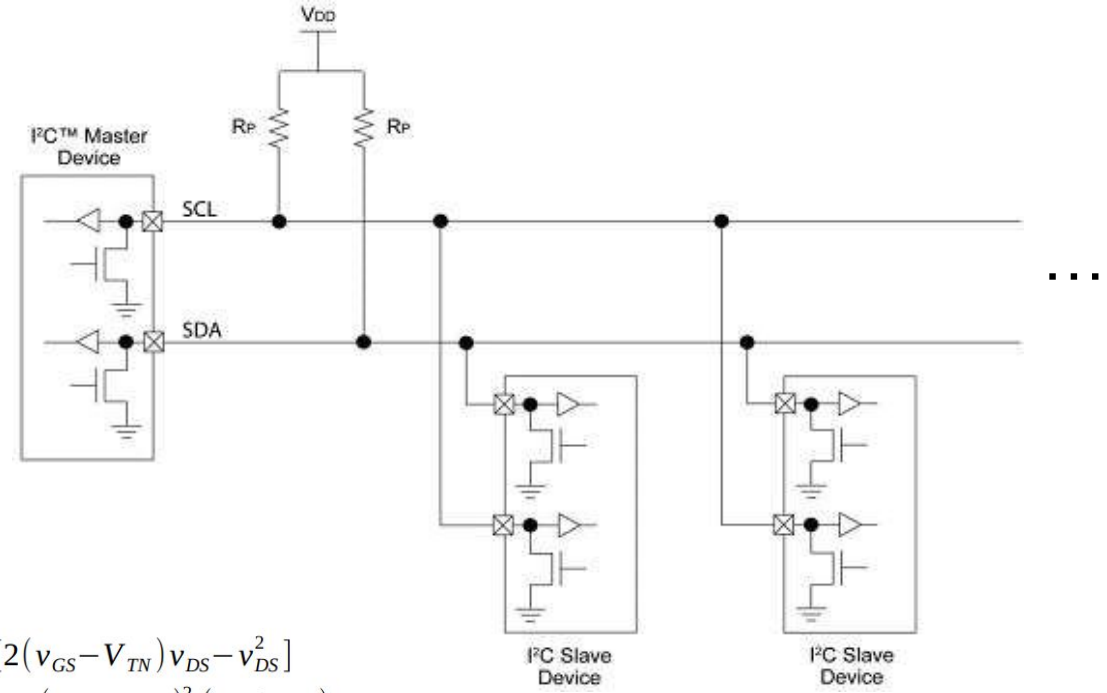
Note:

Can simply be thought of as a D flip-flop in this presentation

- D = SDA
- CLK = SCL

Circuit typology

- Open-drain (open-collector) configuration
- All signals are generated by pulling down SCL or SDA



MOSFETs (n-channel)

Cutoff: $v_{GS} < V_{TN}$, $i_D = 0$

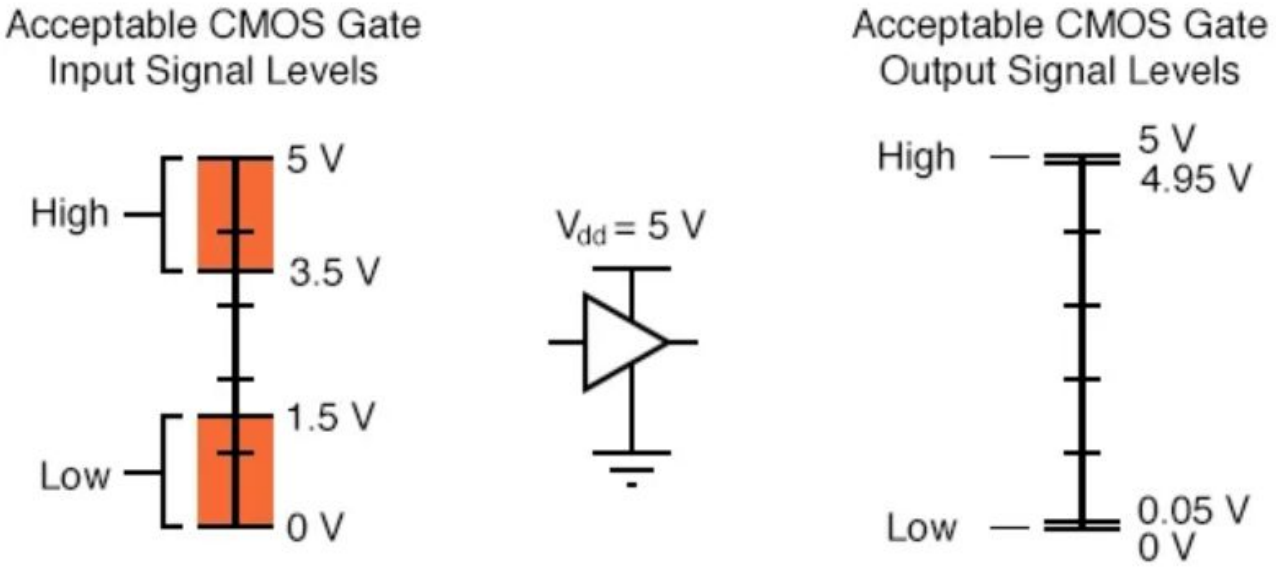
Triode: $v_{GS} > V_{TN}$ and $v_{DS} < v_{DS}(sat)$, $i_D = K_n\,[2(v_{GS}-V_{TN})v_{DS}-v_{DS}^2]$

Saturation: $v_{GS} > V_{TN}$ and $v_{DS} > v_{DS}(sat)$, $i_D = K_n\,(v_{GS}-V_{TN})^2\,(1+\lambda v_{DS})$

where $v_{DS}(sat) = v_{GS} - V_{TN}$

and $K_n = \frac{k'_n}{2}\frac{W}{L}$ (note: for simplified model assume $\lambda = 0$)

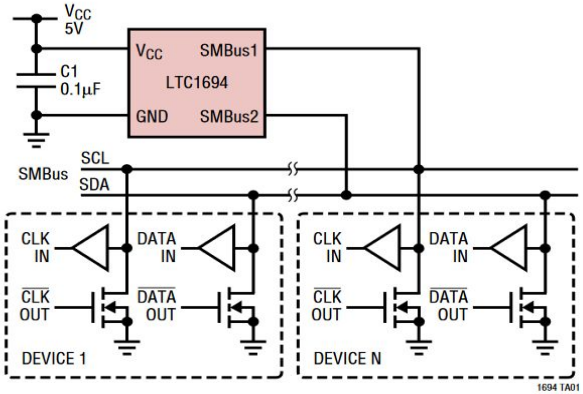
CMOS gate input levels

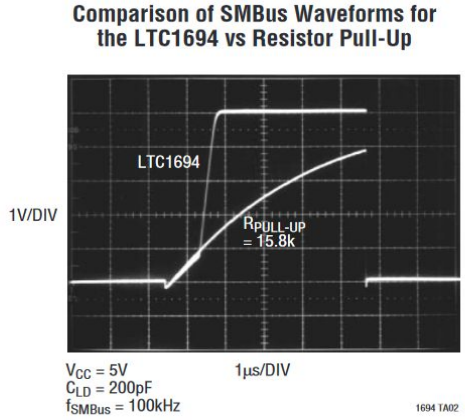


Parasitic capacitance

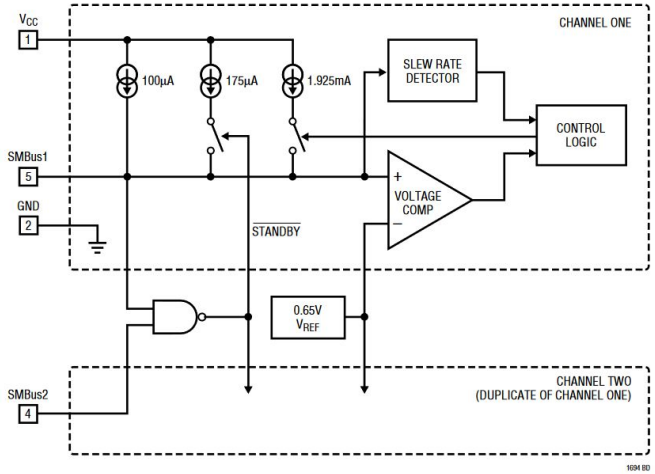
- Limited by total bus capacitance of 400 pF in slower speed implementations
- Longer runs and shielded wire increases capacitance on the bus
- Main reason for limited number of peripheral devices, limited wire length
- RC circuit created, $\tau = RC$
- Active pull-ups and current sources added

TYPICAL APPLICATION





BLOCK DIAGRAM

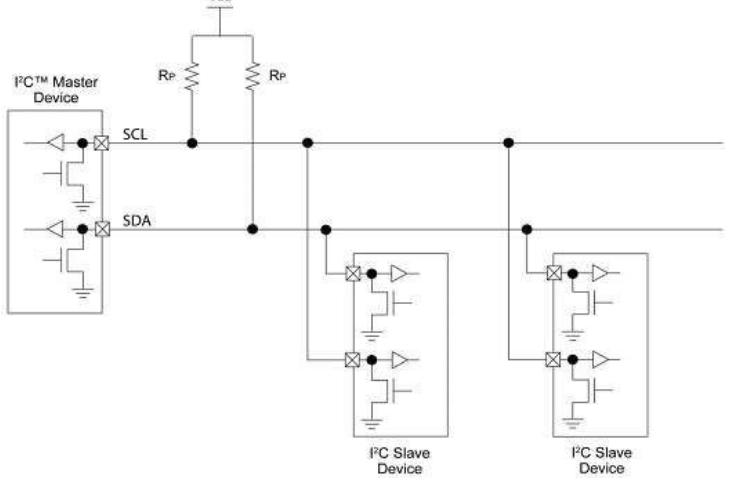


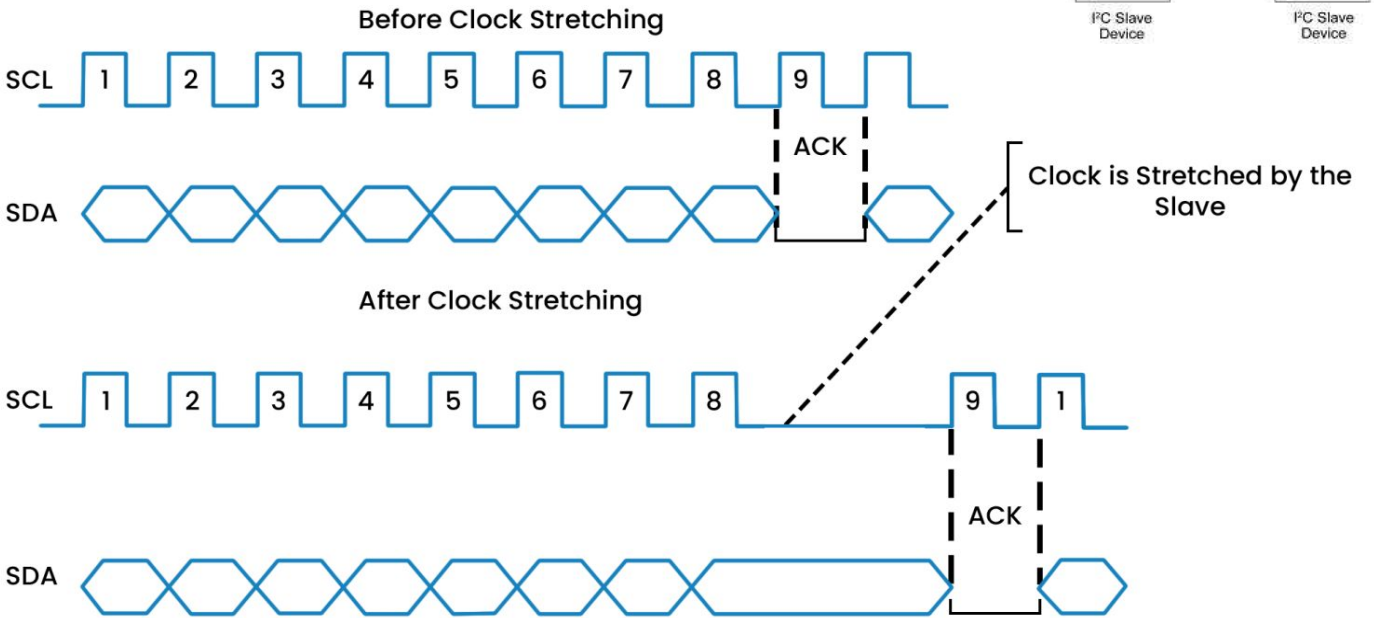
Rise time of an I^2C line is derived using equation 7.

$$t_r = (V_{IH(MIN)} - V_{IL(MAX)}) \bullet C_{BUS}/I_{PULL\text{-}UP(B)} \qquad (7)$$

*from LTC1694 datasheet

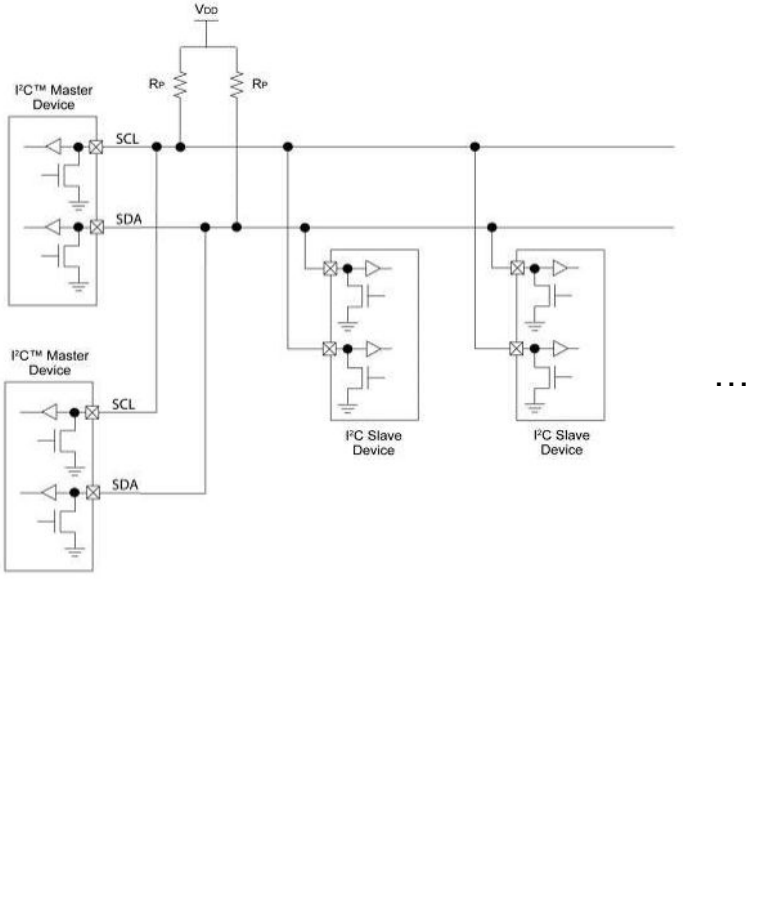
Clock stretching





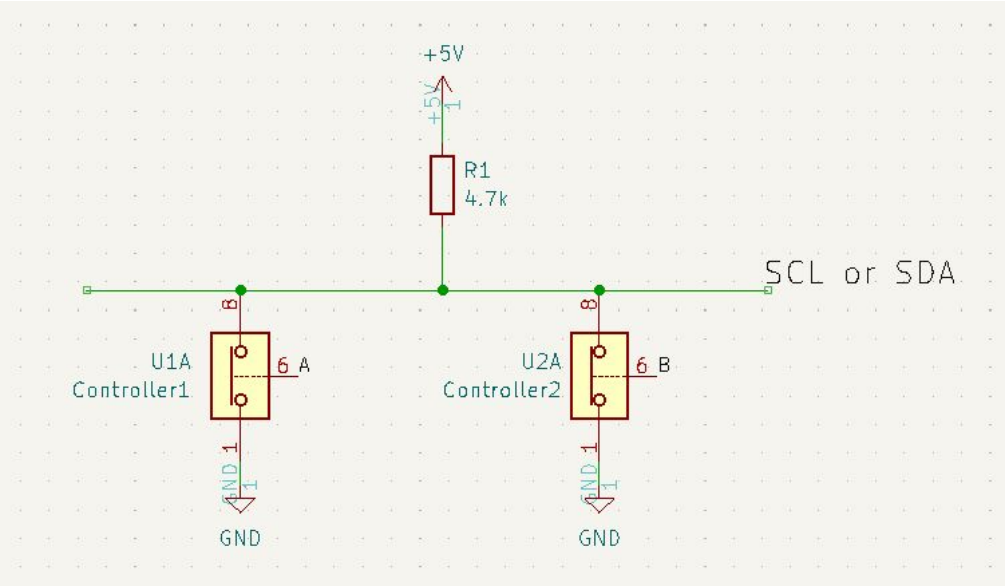
Multiple master controllers

- Multiple master devices are allowed in I^2C protocol
- Controllers can write/ read any of the target controllers
- This created some other issues, solved by arbitration



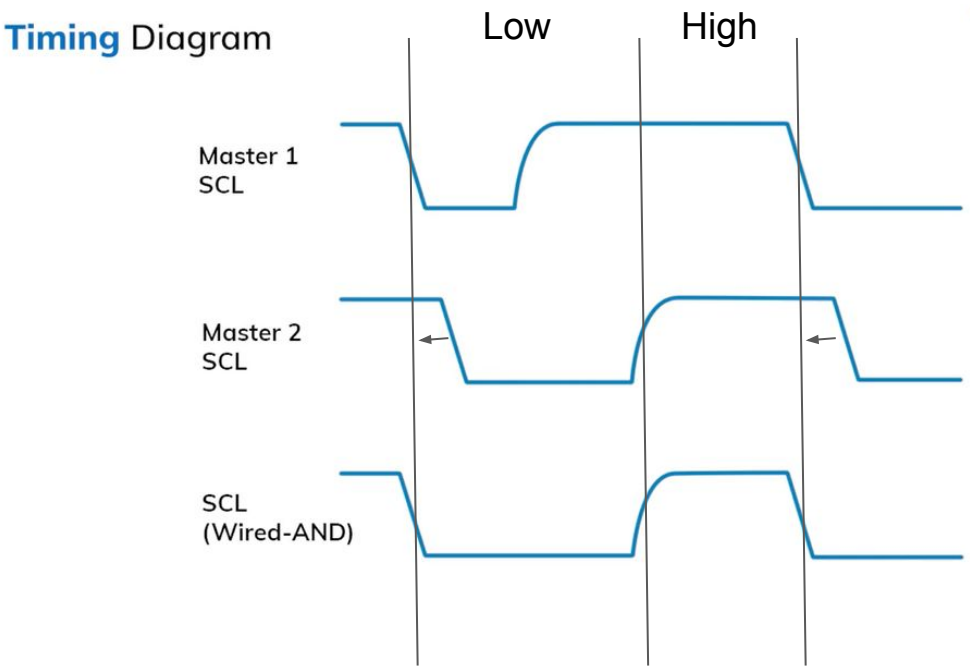
Wired-AND

A	B	Output
0	0	0
0	1	0
1	0	0
1	1	1



SCL Arbitration

- Two master clocks
- Wired-AND ensure SCL allows for
  - The longest low signal
  - The shortest high signal
- Master 2 clock will actually phase shift compared to the expected

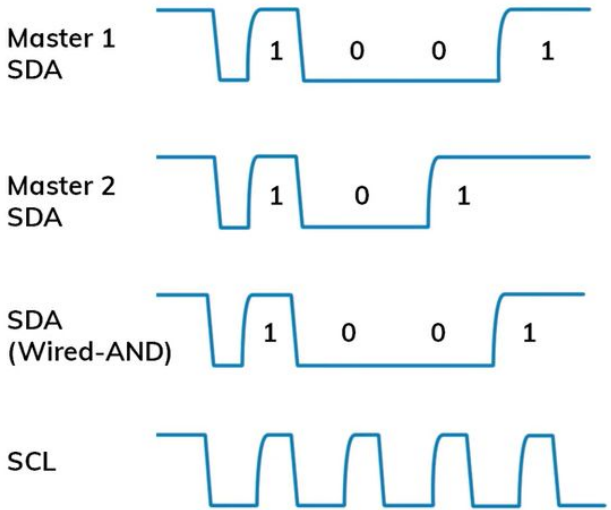


SDA Arbitration

- Arbitrates SDA with two masters are writing to the bus

A	B	Output
0	0	0
0	1	0
1	0	0
1	1	1

Timing Diagram



Thank you

Questions?

Sources

Buffer information:
https://www.allaboutcircuits.com/textbook/digital/chpt-3/logic-signal-voltage-levels/

LTC1694 Datasheet: https://docs.rs-online.com/eecb/0900766b810ed93f.pdf

I^2C Information and diagrams: https://prodigytechno.com/