Pomona College

Computer Science

# Fall 2024: CSCI 181RT

## Real-Time Systems in the Real World

### Lecture 20

Tuesday, November 5, 2024
Edmunds Hall 105
2:45 PM - 4:00 PM

Professor Jennifer DesCombes

Pomona College

# Agenda

- Go Backs
- Discussion on Code Framework
- User Input UART Assignment Review
- Hardware Features and Capabilities - OS Related
- Lab #9 Review
- Look Ahead
- Assignment
- Action Items

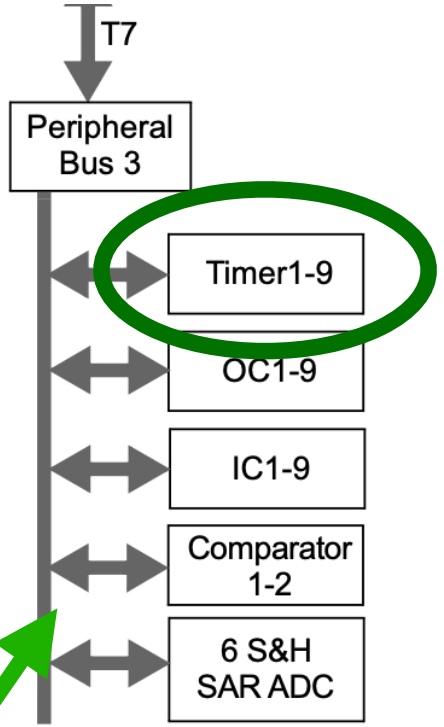
# Go Backs

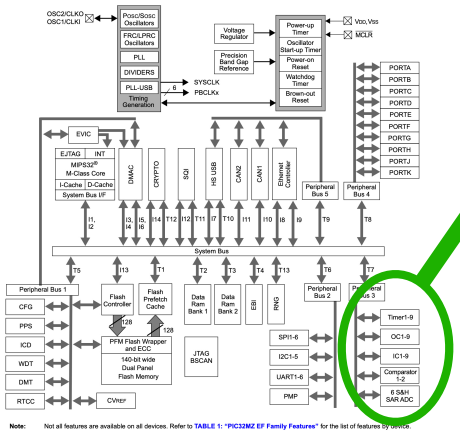
- General?
- Action Item Status
  - AI240910-2: Find recommended book on computer architecture.
  - AI240924-1: At what point as a development team grows does it make sense to have dedicated software and integration testers?
  - AI241024-1: Provide documentation on how to disable compiler optimization.

# Hardware Features and Capabilities - OS Related

- Timer 1 - Only One of This Type Per Package
- Timer 2 to 9 - Multiples of This Type Per Package
  - Can be Used at 16-bit Timers
  - Can be Joined as Pairs for 32-bit Timers

    2 & 3, 4 & 5, 6 & 7, 8 & 9 - Mix and Match



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# Hardware Features and Capabilities - OS Related

- Timer 1 - Only One of This Type Per Package

## 13.0 TIMER1

**Note:** This data sheet summarizes the features of the PIC32MZ EF family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **Section 14. "Timers"** (DS60001105) in the *"PIC32 Family Reference Manual"*, which is available from the Microchip web site (www.microchip.com/PIC32).

PIC32MZ EF devices feature one synchronous/asynchronous 16-bit timer that can operate as a free-running interval timer for various timing applications and counting external events. This timer can also be used with the Low-Power Secondary Oscillator (SOSC) for real-time clock applications.

The following modes are supported by Timer1:

- Synchronous Internal Timer
- Synchronous Internal Gated Timer
- Synchronous External Timer
- Asynchronous External Timer

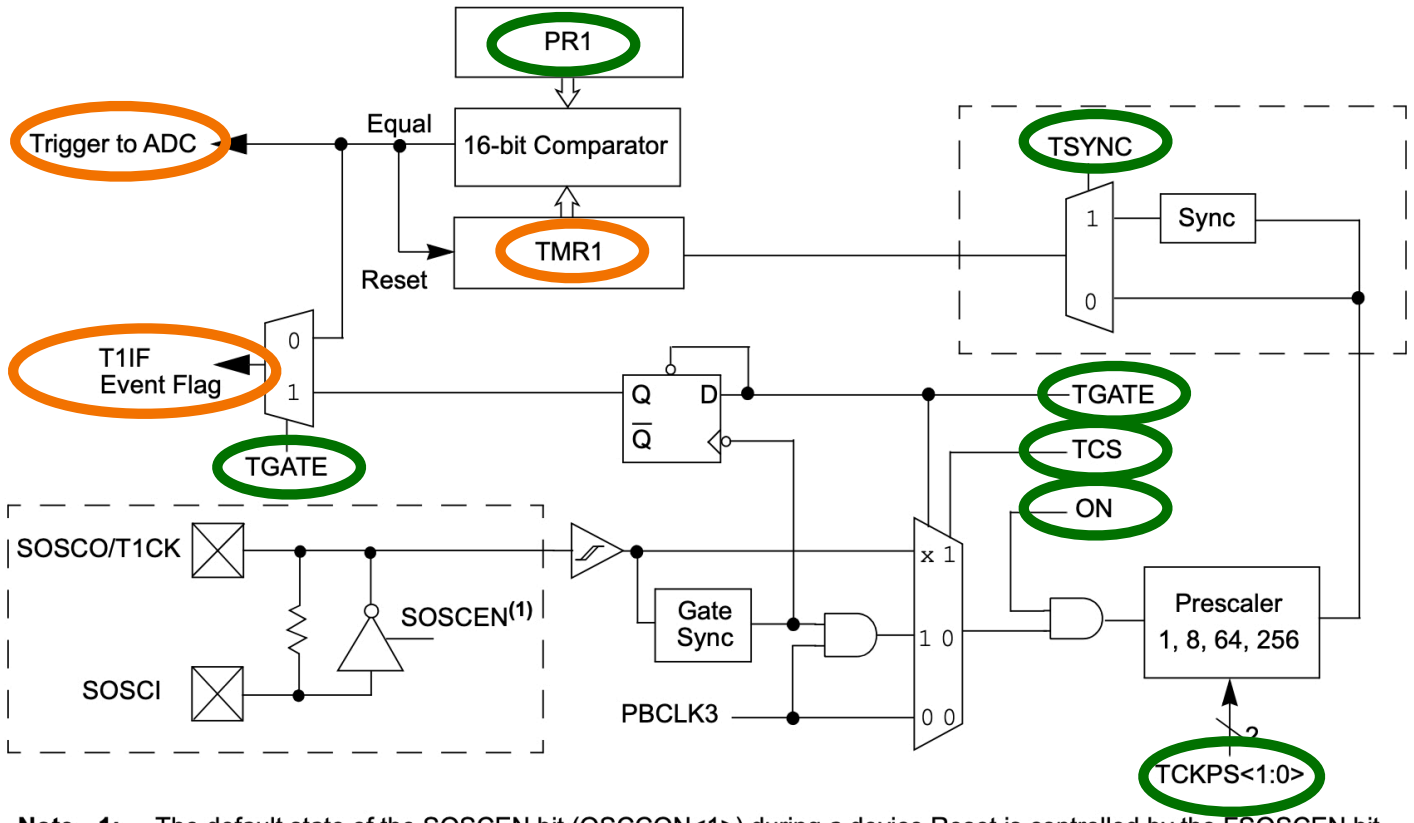
## 13.1 Additional Supported Features

- Selectable clock prescaler
- Timer operation during Sleep and Idle modes
- Fast bit manipulation using CLR, SET and INV registers
- Asynchronous mode can be used with the SOSC to function as a real-time clock
- ADC event trigger

# Hardware Features and Capabilities - OS Related

- Timer 1
- **Green** = Config.
- **Orange** = Control Out (status or Interrupt

**FIGURE 13-1: TIMER1 BLOCK DIAGRAM**




**Note 1:** The default state of the SOSCEN bit (OSCCON<1>) during a device Reset is controlled by the FSOSCEN bit in Configuration Word, DEVCFG1.

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# Hardware Features and Capabilities - OS Related

- Timer 1 - Register List
- Configuration Options Should Match **Green** from Block Diagram
- Block Diagrams May be Simplified - Always Check Register Map

### 13.2 Timer1 Control Register

**TABLE 13-1: TIMER1 REGISTER MAP**

| Virtual Address (BF84_#) | Register Name(1) | Bit Range | Bits | | | | | | | | | | | | | | | All Resets |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | 31/15 | 30/14 | 29/13 | 28/12 | 27/11 | 26/10 | 25/9 | 24/8 | 23/7 | 22/6 | 21/5 | 20/4 | 19/3 | 18/2 | 17/1 | 16/0 | |
| 0000 | T1CON | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | ON | — | SIDL | TWDIS | TWIP | — | — | — | TGATE | — | TCKPS<1:0> | | — | TSYNC | TCS | — | 0000 |
| 0010 | TMR1 | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | TMR1<15:0> | | | | | | | | | | | | | | | | 0000 |
| 0020 | PR1 | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | PR1<15:0> | | | | | | | | | | | | | | | | FFFF |

**Legend:** x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

**Note 1:** All registers in this table have corresponding CLR, SET and INV registers at their virtual addresses, plus offsets of 0x4, 0x8 and 0xC, respectively. See **Section 12.3 "CLR, SET, and INV Registers"** for more information.

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# Hardware Features and Capabilities - OS Related

- Timer 1 - Register List
- Configuration Options Should Match **Green** from Block Diagram
- Block Diagrams May be Simplified - Always Check Register Map

### 13.2 Timer1 Control Register

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|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | 31/15 | 30/14 | 29/13 | 28/12 | 27/11 | 26/10 | 25/9 | 24/8 | 23/7 | 22/6 | 21/5 | 20/4 | 19/3 | 18/2 | 17/1 | 16/0 | |
| 0000 | T1CON | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | ON | — | SIDL | TWDIS | TWIP | — | — | — | TGATE | — | TCKPS<1:0> | | — | TSYNC | TCS | — | 0000 |
| 0010 | TMR1 | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | TMR1<15:0> | | | | | | | | | | | | | | | | 0000 |
| 0020 | PR1 | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | PR1<15:0> | | | | | | | | | | | | | | | | FFFF |

**Legend:** x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

**Note 1:** All registers in this table have corresponding CLR, SET and INV registers at their virtual addresses, plus offsets of 0x4, 0x8 and 0xC, respectively. See **Section 12.3 "CLR, SET, and INV Registers"** for more information.

bit 12 **TWDIS:** Asynchronous Timer Write Disable bit
1 = Writes to TMR1 are ignored until pending write operation completes
0 = Back-to-back writes are enabled (Legacy Asynchronous Timer functionality)

bit 11 **TWIP:** Asynchronous Timer Write in Progress bit
In Asynchronous Timer mode:
1 = Asynchronous write to TMR1 register in progress
0 = Asynchronous write to TMR1 register complete
In Synchronous Timer mode:
This bit is read as '0'.

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# Hardware Features and Capabilities - OS Related

- Timer 2 to 9 - Multiples of This Type Per Package

## 14.0 TIMER2/3, TIMER4/5, TIMER6/7, AND TIMER8/9

| | |
|---|---|
| **Note:** | This data sheet summarizes the features of the PIC32MZ EF family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **Section 14. "Timers"** (DS60001105) of the *"PIC32 Family Reference Manual"*, which is available from the Microchip web site (www.microchip.com/PIC32). |

The PIC32MZ EF family of devices features eight synchronous 16-bit timers (default) that can operate as a free-running interval timer for various timing applications and counting external events.

The following modes are supported:

- Synchronous internal 16-bit timer
- Synchronous internal 16-bit gated timer
- Synchronous external 16-bit timer

Four 32-bit synchronous timers are available by combining Timer2 with Timer3, Timer4 with Timer5, Timer6 with Timer7, and Timer8 with Timer9.

The 32-bit timers can operate in one of three modes:

- Synchronous internal 32-bit timer
- Synchronous internal 32-bit gated timer
- Synchronous external 32-bit timer

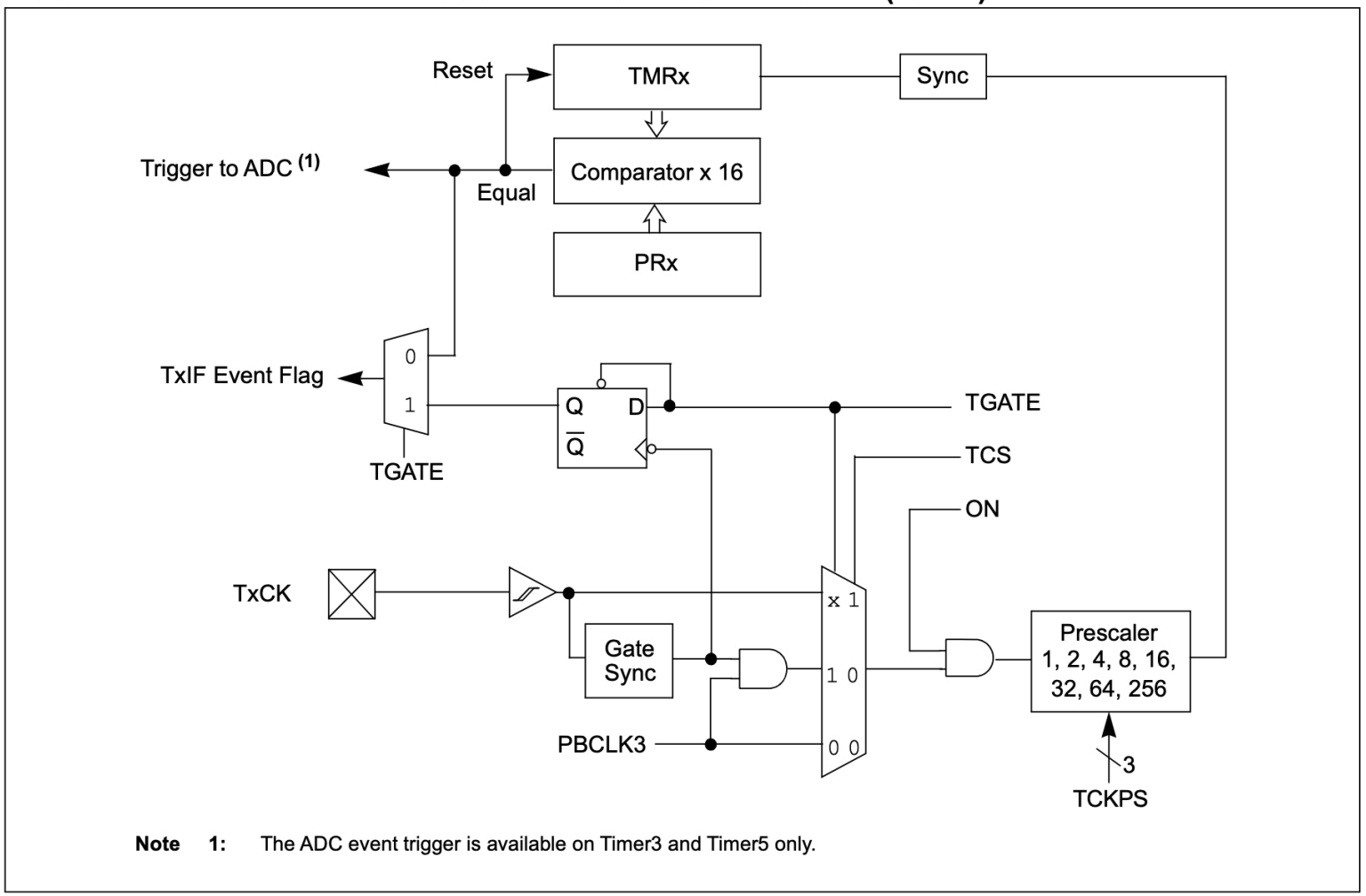
### 14.1 Additional Supported Features

- Selectable clock prescaler
- Timers operational during CPU idle
- Time base for Input Capture and Output Compare modules (Timer2 through Timer7 only)
- ADC event trigger (Timer3 and Timer5 only)
- Fast bit manipulation using CLR, SET, and INV registers

# Hardware Features and Capabilities - OS Related

- Timer 1
- 16-bit Block Diagram

**FIGURE 14-1: TIMER2 THROUGH TIMER9 BLOCK DIAGRAM (16-BIT)**

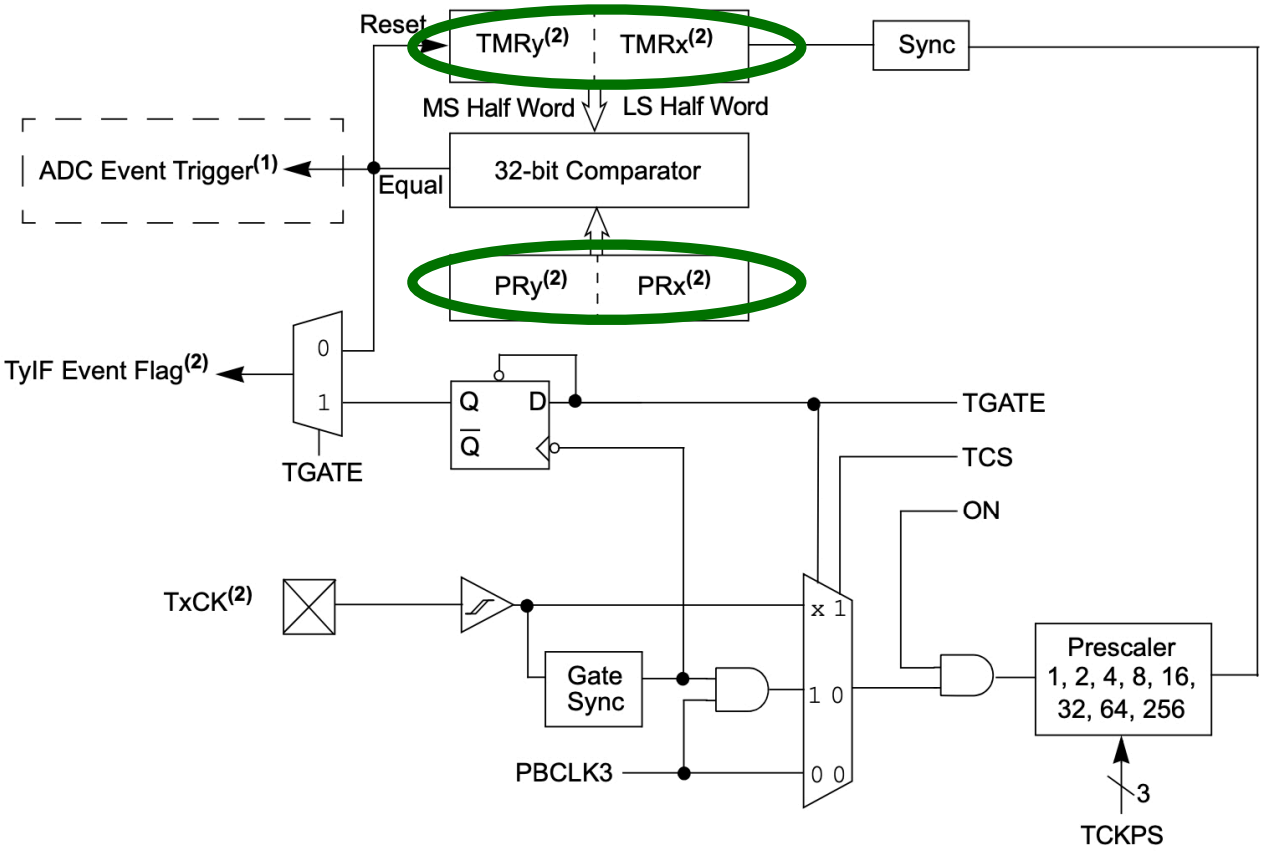



**Note 1:** The ADC event trigger is available on Timer3 and Timer5 only.

# Hardware Features and Capabilities - OS Related

- Timer 1
- 32-bit Block Diagram
- **Green** = Combined Registers from Timer n & (n+1)

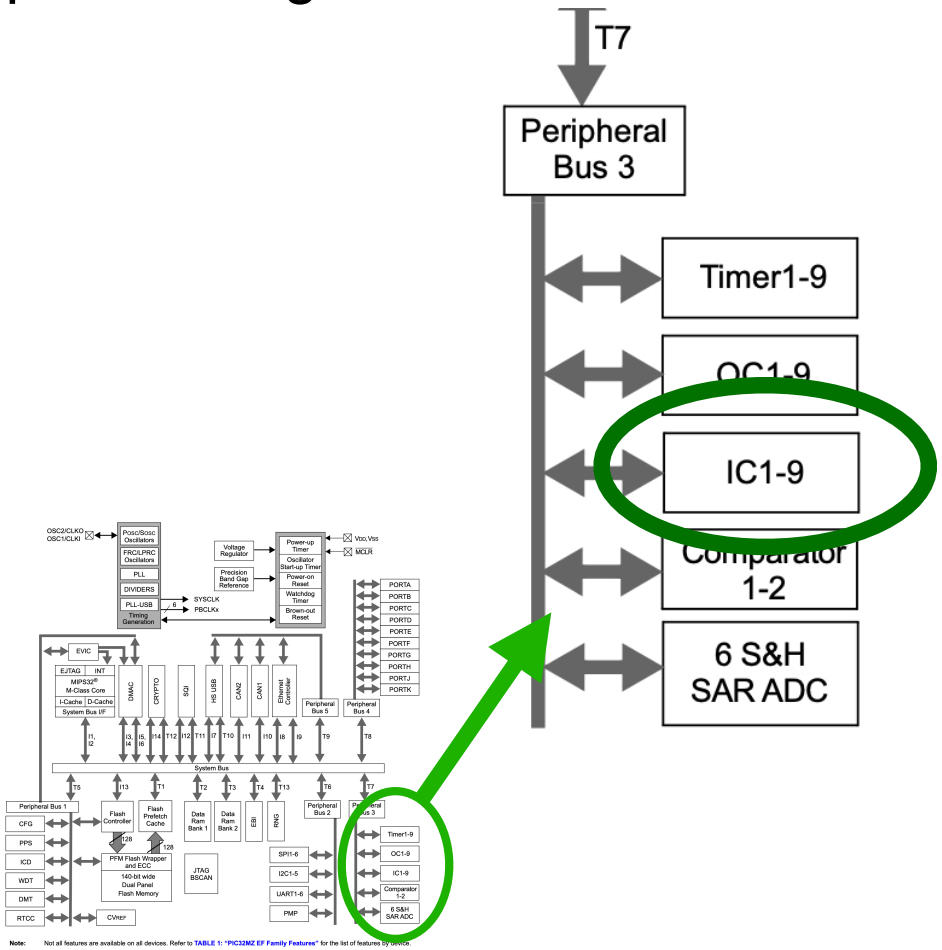
**FIGURE 14-2: TIMER2/3, TIMER4/5, TIMER6/7, AND TIMER8/9 BLOCK DIAGRAM (32-BIT)**




**Note 1:** ADC event trigger is available only on the Timer2/3 and TImer4/5 pairs.
**2:** In this diagram, 'x' represents Timer2, 4, 6, or 8, and 'y' represents Timer3, 5, 7, or 9.

# Hardware Features and Capabilities - OS Related

- Input Compare - Up to 9 Circuits per Package



# Hardware Features and Capabilities - OS Related

- Input Compare - Up to 9 Circuits per Package

## 17.0 INPUT CAPTURE

| | |
|---|---|
| **Note:** | This data sheet summarizes the features of the PIC32MZ EF family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **Section 15. "Input Capture"** (DS60001122) of the *"PIC32 Family Reference Manual"*, which is available from the Microchip web site (www.microchip.com/PIC32). |

The Input Capture module is useful in applications requiring frequency (period) and pulse measurement.

The Input Capture module captures the 16-bit or 32-bit value of the selected Time Base registers when an event occurs at the ICx pin.

Capture events are caused by the following:

- Capture timer value on every edge (rising and falling), specified edge first
- Prescaler capture event modes:
  - Capture timer value on every 4th rising edge of input at ICx pin
  - Capture timer value on every 16th rising edge of input at ICx pin

Each input capture channel can select between one of six 16-bit timers for the time base, or two of six 16-bit timers together to form a 32-bit timer. The selected timer can use either an internal or external clock.

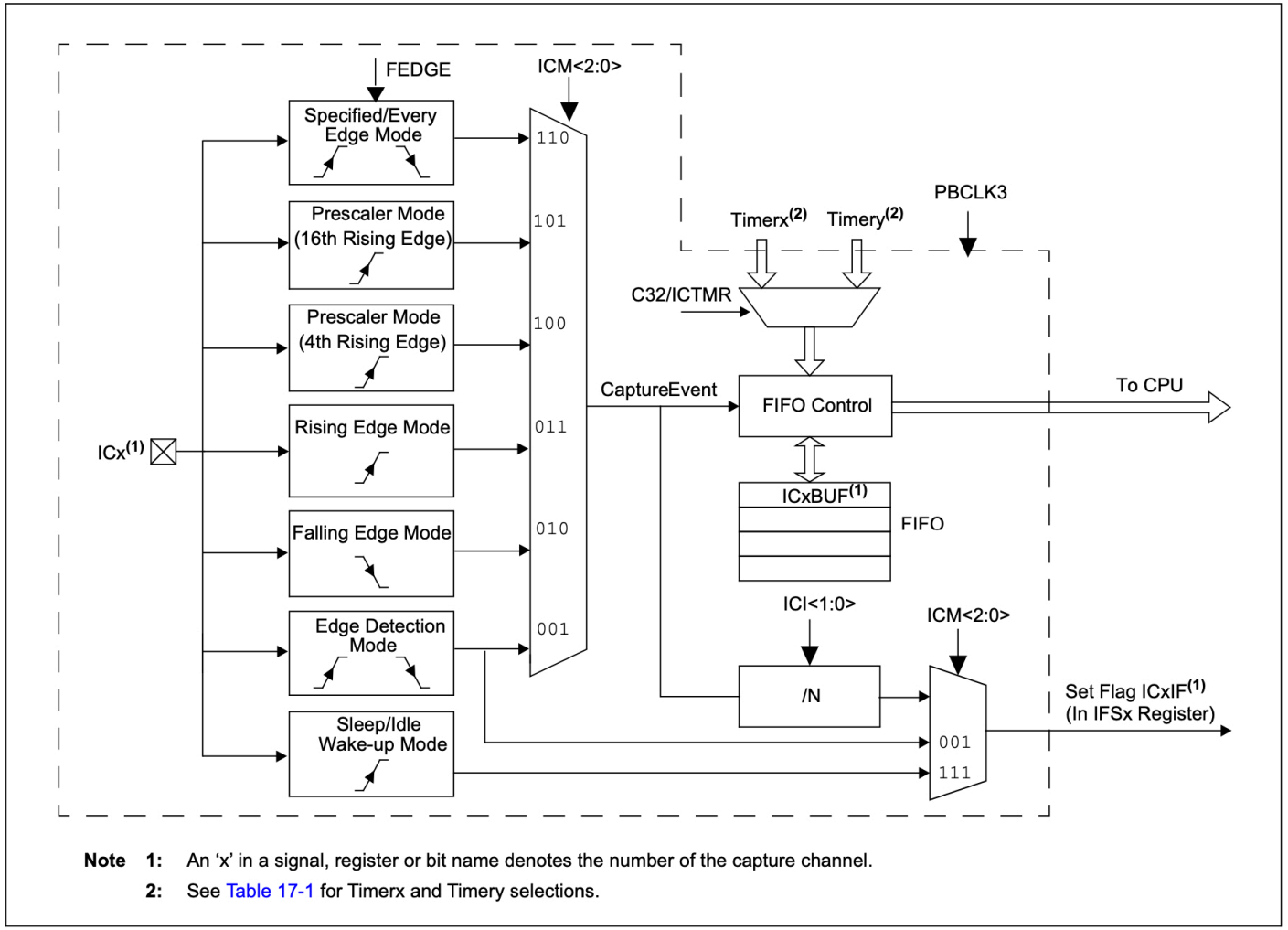
Other operational features include:

- Device wake-up from capture pin during Sleep and Idle modes
- Interrupt on input capture event
- 4-word FIFO buffer for capture values; Interrupt optionally generated after 1, 2, 3, or 4 buffer locations are filled
- Input capture can also be used to provide additional sources of external interrupts

# Hardware Features and Capabilities - OS Related

- Input Compare

**FIGURE 17-1: INPUT CAPTURE BLOCK DIAGRAM**




**Note 1:** An 'x' in a signal, register or bit name denotes the number of the capture channel.

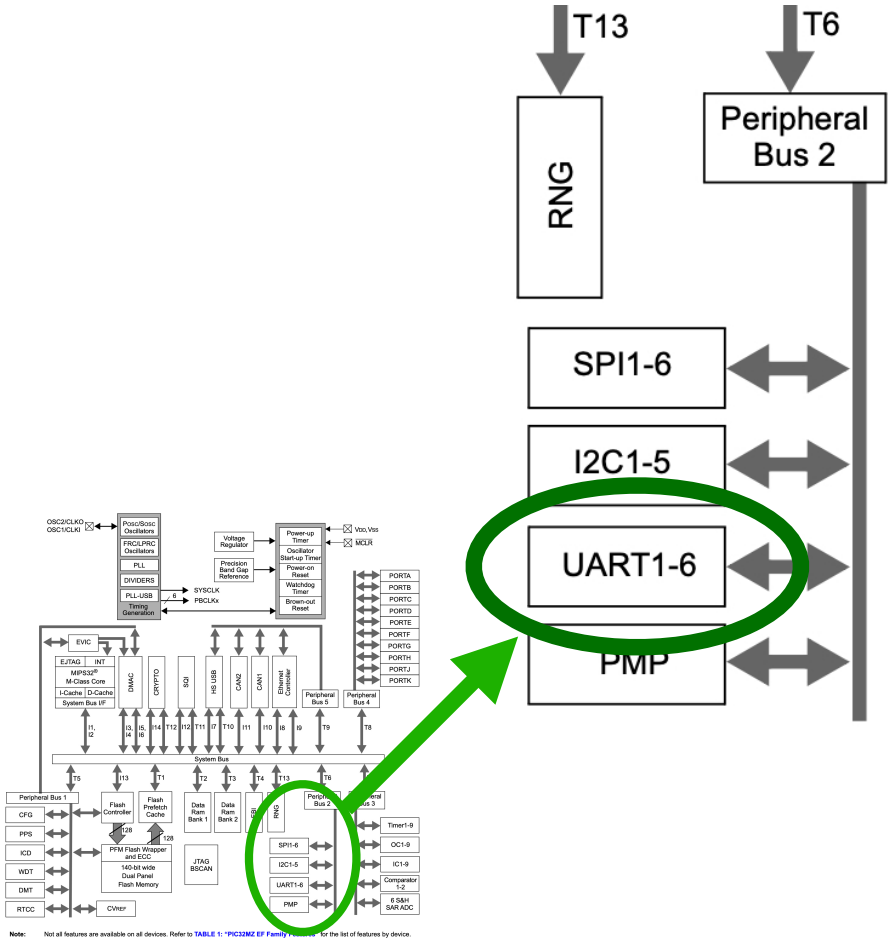
**2:** See Table 17-1 for Timerx and Timery selections.

# Hardware Features and Capabilities - OS Related

- Input Compare
  - More Information as Part of Additional Assignment

# Hardware Features and Capabilities - OS Related

- Serials Port - UART - Up to 6 Circuits per Package



# Hardware Features and Capabilities - OS Related

- Serials Port - UART - Up to 6 Circuits per Package

## 22.0 UNIVERSAL ASYNCHRONOUS RECEIVER TRANSMITTER (UART)

**Note:** This data sheet summarizes the features of the PIC32MZ EF family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **Section 21. "Universal Asynchronous Receiver Transmitter (UART)"** (DS60001107) in the *"PIC32 Family Reference Manual"*, which is available from the Microchip web site (www.microchip.com/PIC32).

The UART module is one of the serial I/O modules available in the PIC32MZ EF family of devices. The UART is a full-duplex, asynchronous communication channel that communicates with peripheral devices and personal computers through protocols, such as RS-232, RS-485, LIN, and IrDA®. The module also supports the hardware flow control option, with UxCTS and UxRTS pins, and also includes an IrDA encoder and decoder.

The primary features of the UART module are:

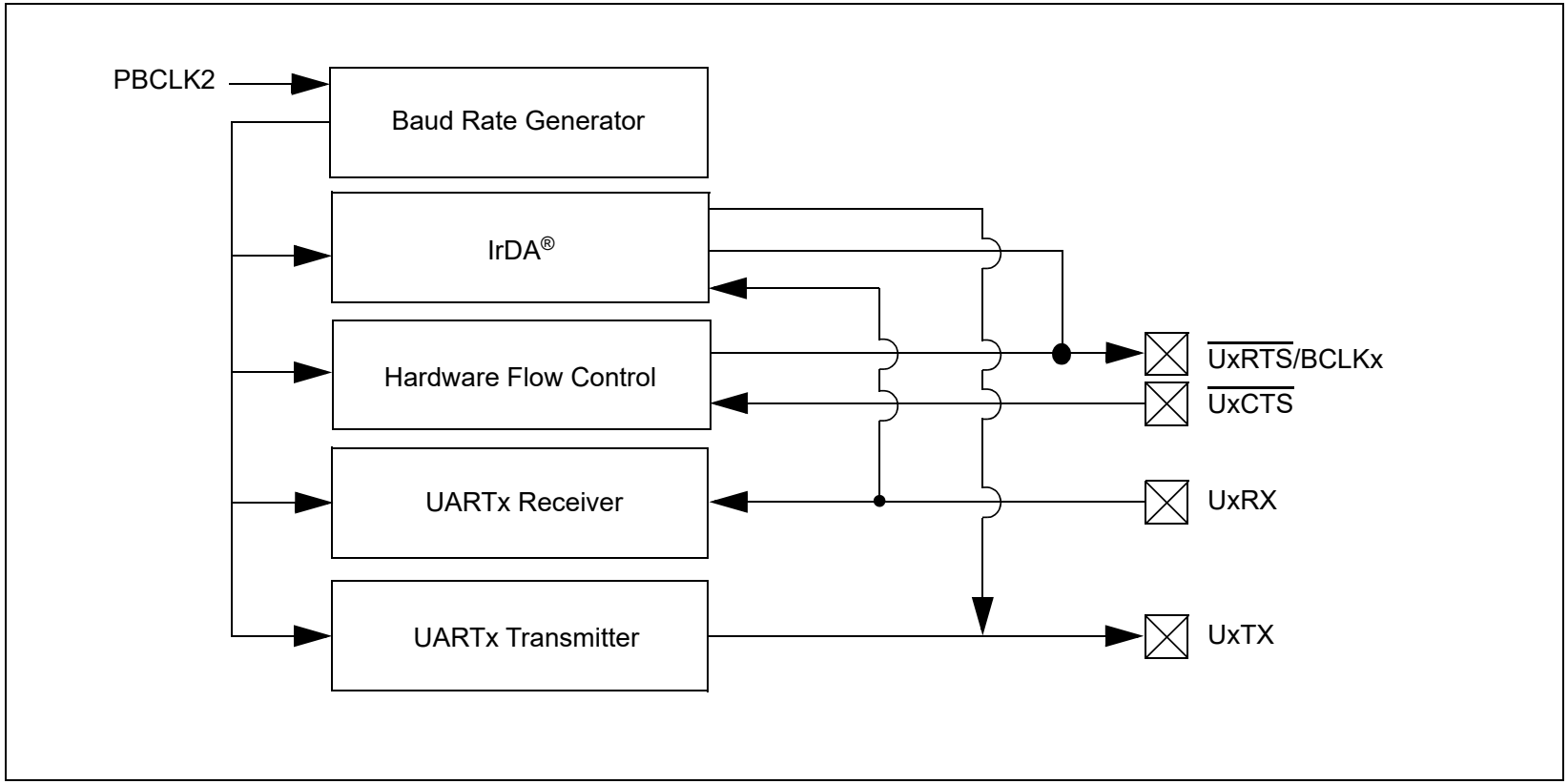
- Full-duplex, 8-bit or 9-bit data transmission
- Even, Odd or No Parity options (for 8-bit data)
- One or two Stop bits
- Hardware auto-baud feature
- Hardware flow control option
- Fully integrated Baud Rate Generator (BRG) with 16-bit prescaler
- Baud rates ranging from 76 bps to 25 Mbps at 100 MHz (PBCLK2)
- 8-level deep First-In-First-Out (FIFO) transmit data buffer
- 8-level deep FIFO receive data buffer
- Parity, framing and buffer overrun error detection
- Support for interrupt-only on address detect (9th bit = 1)
- Separate transmit and receive interrupts
- Loopback mode for diagnostic support
- LIN Protocol support
- IrDA encoder and decoder with 16x baud clock output for external IrDA encoder/decoder support

Figure 22-1 illustrates a simplified block diagram of the UART module.

# Hardware Features and Capabilities - OS Related

- UART

**FIGURE 22-1: UART SIMPLIFIED BLOCK DIAGRAM**



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# Hardware Features and Capabilities - OS Related

- UART Registers - Page 1

### 22.1 UART Control Registers

**TABLE 22-1: UART1 THROUGH UART6 REGISTER MAP**

| Virtual Address (BF82_#) | Register Name | Bit Range | Bits | | | | | | | | | | | | | | | | All Resets |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | 31/15 | 30/14 | 29/13 | 28/12 | 27/11 | 26/10 | 25/9 | 24/8 | 23/7 | 22/6 | 21/5 | 20/4 | 19/3 | 18/2 | 17/1 | 16/0 | |
| 2000 | U1MODE(1) | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | ON | — | SIDL | IREN | RTSMD | — | UEN<1:0> | | WAKE | LPBACK | ABAUD | RXINV | BRGH | PDSEL<1:0> | | STSEL | 0000 |
| 2010 | U1STA(1) | 31:16 | — | — | — | — | — | — | — | ADM_EN | ADDR<7:0> | | | | | | | | 0000 |
| | | 15:0 | UTXISEL<1:0> | | UTXINV | URXEN | UTXBRK | UTXEN | UTXBF | TRMT | URXISEL<1:0> | | ADDEN | RIDLE | PERR | FERR | OERR | URXDA | 0110 |
| 2020 | U1TXREG | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | — | — | — | — | — | — | — | TX8 | Transmit Register | | | | | | | | 0000 |
| 2030 | U1RXREG | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | — | — | — | — | — | — | — | RX8 | Receive Register | | | | | | | | 0000 |
| 2040 | U1BRG(1) | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | Baud Rate Generator Prescaler | | | | | | | | | | | | | | | | 0000 |
| 2200 | U2MODE(1) | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | ON | — | SIDL | IREN | RTSMD | — | UEN<1:0> | | WAKE | LPBACK | ABAUD | RXINV | BRGH | PDSEL<1:0> | | STSEL | 0000 |
| 2210 | U2STA(1) | 31:16 | — | — | — | — | — | — | — | ADM_EN | ADDR<7:0> | | | | | | | | 0000 |
| | | 15:0 | UTXISEL<1:0> | | UTXINV | URXEN | UTXBRK | UTXEN | UTXBF | TRMT | URXISEL<1:0> | | ADDEN | RIDLE | PERR | FERR | OERR | URXDA | 0110 |
| 2220 | U2TXREG | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | — | — | — | — | — | — | — | TX8 | Transmit Register | | | | | | | | 0000 |
| 2230 | U2RXREG | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | — | — | — | — | — | — | — | RX8 | Receive Register | | | | | | | | 0000 |
| 2240 | U2BRG(1) | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | Baud Rate Generator Prescaler | | | | | | | | | | | | | | | | 0000 |
| 2400 | U3MODE(1) | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | ON | — | SIDL | IREN | RTSMD | — | UEN<1:0> | | WAKE | LPBACK | ABAUD | RXINV | BRGH | PDSEL<1:0> | | STSEL | 0000 |
| 2410 | U3STA(1) | 31:16 | — | — | — | — | — | — | — | ADM_EN | ADDR<7:0> | | | | | | | | 0000 |
| | | 15:0 | UTXISEL<1:0> | | UTXINV | URXEN | UTXBRK | UTXEN | UTXBF | TRMT | URXISEL<1:0> | | ADDEN | RIDLE | PERR | FERR | OERR | URXDA | 0110 |
| 2420 | U3TXREG | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | — | — | — | — | — | — | — | TX8 | Transmit Register | | | | | | | | 0000 |
| 2430 | U3RXREG | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | — | — | — | — | — | — | — | RX8 | Receive Register | | | | | | | | 0000 |
| 2440 | U3BRG(1) | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | Baud Rate Generator Prescaler | | | | | | | | | | | | | | | | 0000 |

**Legend:** x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

**Note 1:** This register has corresponding CLR, SET and INV registers at its virtual address, plus an offset of 0x4, 0x8 and 0xC, respectively. See **Section 12.3 "CLR, SET, and INV Registers"** for more information.

# Hardware Features and Capabilities - OS Related

- UART Registers - Page 2

**TABLE 22-1: UART1 THROUGH UART6 REGISTER MAP (CONTINUED)**

| Virtual Address (BF82_#) | Register Name | Bit Range | Bits | | | | | | | | | | | | | | | | All Resets |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | 31/15 | 30/14 | 29/13 | 28/12 | 27/11 | 26/10 | 25/9 | 24/8 | 23/7 | 22/6 | 21/5 | 20/4 | 19/3 | 18/2 | 17/1 | 16/0 | |
| 2600 | U4MODE(1) | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | ON | — | SIDL | IREN | RTSMD | — | UEN<1:0> | | WAKE | LPBACK | ABAUD | RXINV | BRGH | PDSEL<1:0> | | STSEL | 0000 |
| 2610 | U4STA(1) | 31:16 | — | — | — | — | — | — | — | ADM_EN | ADDR<7:0> | | | | | | | | 0000 |
| | | 15:0 | UTXISEL<1:0> | | UTXINV | URXEN | UTXBRK | UTXEN | UTXBF | TRMT | URXISEL<1:0> | | ADDEN | RIDLE | PERR | FERR | OERR | URXDA | 0110 |
| 2620 | U4TXREG | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | — | — | — | — | — | — | — | TX8 | Transmit Register | | | | | | | | 0000 |
| 2630 | U4RXREG | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | — | — | — | — | — | — | — | RX8 | Receive Register | | | | | | | | 0000 |
| 2640 | U4BRG(1) | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | Baud Rate Generator Prescaler | | | | | | | | | | | | | | | | 0000 |
| 2800 | U5MODE(1) | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | ON | — | SIDL | IREN | RTSMD | — | UEN<1:0> | | WAKE | LPBACK | ABAUD | RXINV | BRGH | PDSEL<1:0> | | STSEL | 0000 |
| 2810 | U5STA(1) | 31:16 | — | — | — | — | — | — | — | ADM_EN | ADDR<7:0> | | | | | | | | 0000 |
| | | 15:0 | UTXISEL<1:0> | | UTXINV | URXEN | UTXBRK | UTXEN | UTXBF | TRMT | URXISEL<1:0> | | ADDEN | RIDLE | PERR | FERR | OERR | URXDA | 0110 |
| 2820 | U5TXREG | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | — | — | — | — | — | — | — | TX8 | Transmit Register | | | | | | | | 0000 |
| 2830 | U5RXREG | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | — | — | — | — | — | — | — | RX8 | Receive Register | | | | | | | | 0000 |
| 2840 | U5BRG(1) | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | Baud Rate Generator Prescaler | | | | | | | | | | | | | | | | 0000 |
| 2A00 | U6MODE(1) | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | ON | — | SIDL | IREN | RTSMD | — | UEN<1:0> | | WAKE | LPBACK | ABAUD | RXINV | BRGH | PDSEL<1:0> | | STSEL | 0000 |
| 2A10 | U6STA(1) | 31:16 | — | — | — | — | — | — | — | ADM_EN | ADDR<7:0> | | | | | | | | 0000 |
| | | 15:0 | UTXISEL<1:0> | | UTXINV | URXEN | UTXBRK | UTXEN | UTXBF | TRMT | URXISEL<1:0> | | ADDEN | RIDLE | PERR | FERR | OERR | URXDA | 0110 |
| 2A20 | U6TXREG | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | — | — | — | — | — | — | — | TX8 | Transmit Register | | | | | | | | 0000 |
| 2A30 | U6RXREG | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | — | — | — | — | — | — | — | RX8 | Receive Register | | | | | | | | 0000 |
| 2A40 | U6BRG(1) | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | Baud Rate Generator Prescaler | | | | | | | | | | | | | | | | 0000 |

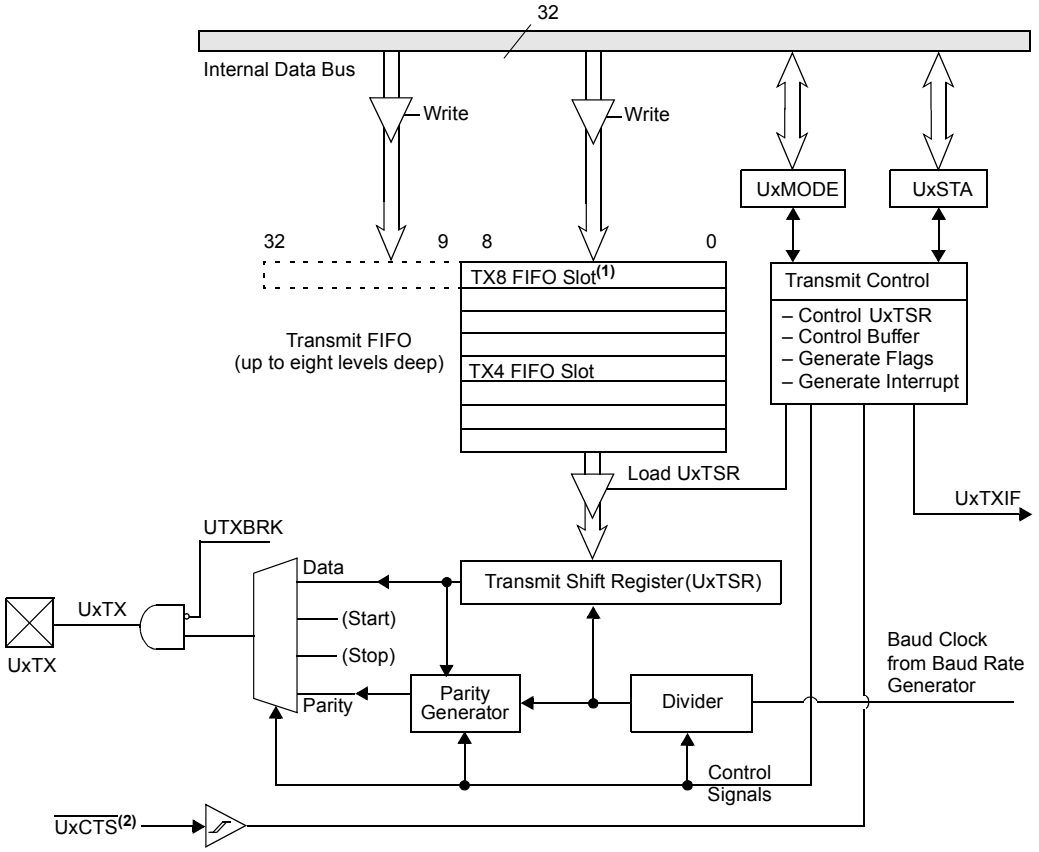
**Legend:** x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

**Note 1:** This register has corresponding CLR, SET and INV registers at its virtual address, plus an offset of 0x4, 0x8 and 0xC, respectively. See **Section 12.3 "CLR, SET, and INV Registers"** for more information.

# Hardware Features and Capabilities - OS Related

- UART - Detailed Tx Block Diagram from Family Reference Guide

**Figure 21-3: UART Transmitter Block Diagram**




**Note 1:** Refer to the **"UART"** chapter in the specific device data sheet for availability of the 8-level-deep FIFO.

**2:** Refer to the **"Pin Tables"** section in the specific device data sheet for availability of the $\overline{\text{UxCTS}}$ pin.

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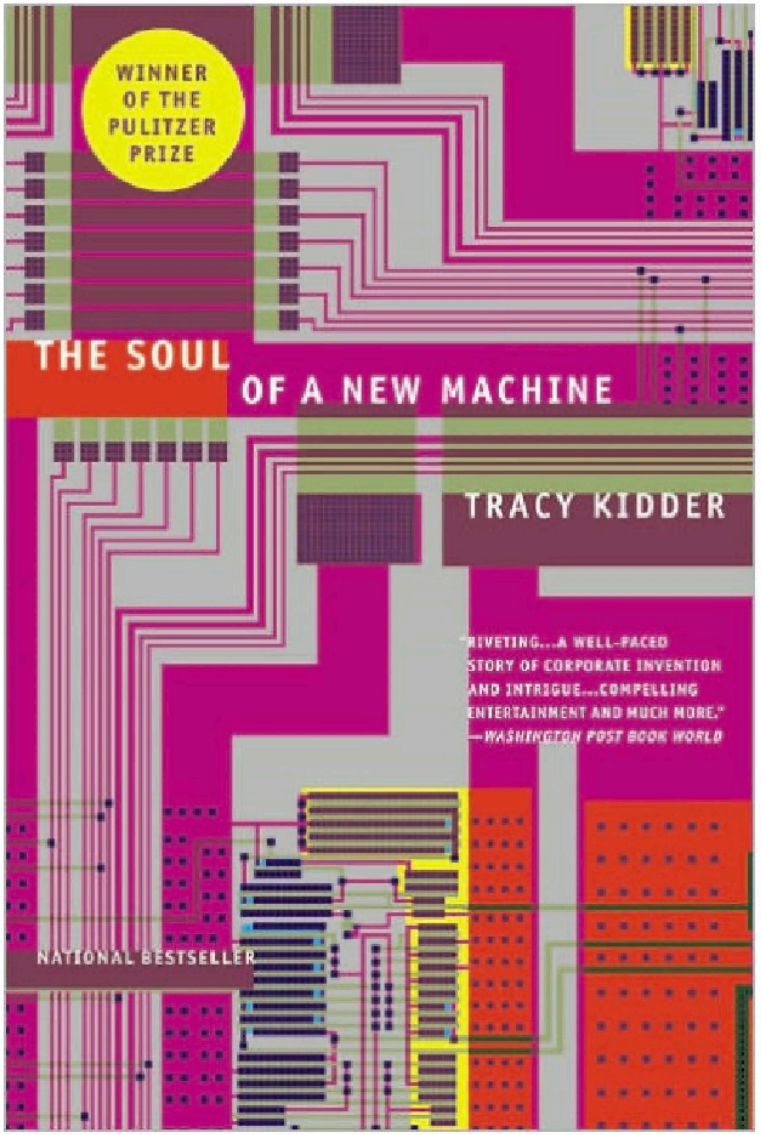
# Look Ahead

- Discussion on Reading
- Review of Lab 10
- Fielders Choice

# Assignment - Readings

- The Soul Of A New Machine
  - One Week Assignment
  - Chapters 5 and 6: Midnight Programmer, Flying Upside Down
  - Send Me Discussion Topics by 10:00 AM on Tuesday, November 12, 2024.



# Assignment - Hardware Documentation

- Chip Documentation - Chapter 17 - Input Compare
- Functional Modes
- Register Operations
- Download Full Documentation
  - More Information?
  - Better Presentation - Easier to Understand?

# Assignment - Hardware Documentation

- Chip Documentation - Chapter 21 - UART
- Review Block Diagrams
- Look for Interrupt Options

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# Action Items and Discussion

| AI#: | Owner | Slide # | Document | Action |
|---|---|---|---|---|
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