Computer Science

Fall 2024: CSCI 181RT Real-Time Systems in the Real World

Lecture 4

Thursday, September 5, 2024 Edmunds Hall 105 2:45 PM - 4:00 PM

Professor Jennifer DesCombes



Agenda

- Go Backs
- Discussion on Reading
- Discussion on Lab
- Computer Memory Utilization
- Initial Investigation of Interrupts
- Assignment
- Look Ahead
- Action Items



Go Backs

- General?
- Lab Start Time Clarification
 - Lab starts nominally at 1:15, promptly at 1:20
- Action Item Status
 - Al240903-1: Send out emails concerning types of preferred tea brands to those who indicated a beverage preference of tea. - OK to Close?



Discussion on Reading

- K & R
 - General Questions?
- Journal Article Software Requirements Analysis for Real-Time Process-Control Systems
 - Complexity?

A. Essential Value Assumptions

The existence of an input at the black-box boundary does not in itself require a value assumption. For example, a hard-wired hardware interrupt has no value, but it may still trigger an output. In other words, the existence of I helps trigger O, but v(I) is not referred to further in the definition of v(O) or v(O). When v(I) is used in the definition of v(O) appropriate assumptions on the acceptable characteristics of v(I) must be specified, e.g., range of acceptable values, set of acceptable values, parity of acceptable values, etc.

Criterion 6.5: A value assumption is required for every input I where v(I) is used to define the value or the time for some output O.

B. Essential Timing Assumptions

Timing problems are one of the common causes of runtime failures in process-control systems, and timing is often inadequately specified. The need for and importance of specifying timing assumptions in the software requirements stems from the basic nature and importance of timing in process-control systems as described previously. Several different timing assumptions are essential in the requirements specification of triggers: ranges, capacity, and load.

1) Time Ranges: While the specification of the value of an event is usual but optional, a timing specification is always required. The mere existence of an observable event (with no timing specification) in and of itself is never sufficient—at the least, inputs must be required to arrive after program startup or handled as described in Section V-A. For systems described using a state machine specification, this basic timing assumption



Discussion on Lab

- Associates Code Samples Distributed
 - Review Prior to Next Weeks Lab
- Likes? Dislikes?
- Update on Evaluation Boards



Computer Memory Utilization

- For This Discussion, Treat Memory as Contiguous & Real
 - Top, Bottom, Upside Down?
 - Program Space (if loaded from storage)
 - Memory Mapped IO
 - Constants
 - Global Variables
 - Heap (dynamic allocation)
 - Stack (dynamic use)



Source: CU Boulder - CSCI 3753 Operating Systems

Stack Behavior

max address

- Run-time memory image
- Essentially code, data, stack, and heap
- Code and data loaded from executable file
- Stack grows downward, heap grows upward

Run-time memory User stack Unallocated Heap Read/write .data, .bss Read-only .init, .text, .rodata

address 0



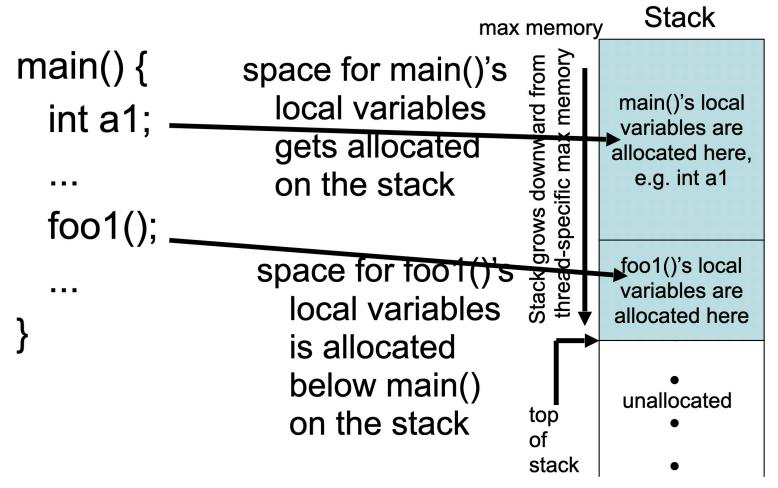
Computer Memory Utilization - Tools

- Stack
 - Push, Pop (Pull)
 - Frame Creation
 - Save Prior Frame Pointer (dedicated variable, register, other)
 - Allocate Space on the Stack
 - Stack Overflow
- Heap
 - Allocate, Deallocate
 - Fragmentation
 - Leaks



Source: CU Boulder - CSCI 3753 Operating Systems

Relating the Code to the Stack





Source: CU Boulder - CSCI 3753 Operating Systems

Entering a Function

Stack max memory foo1(int v1, v2) { main()'s local Pc → local var's main's variables are frame allocated here, assembly code: e.g. int a1 foo1 first saves the old frame pointer by pushing it onto the arg 2 stack: pushl %ebp arg 1 return address foo1 resets frame saved fr ptr %ebp ptr to new base %ebp (current stack ptr): local var's movl %esp, %ebp %esp foo1's foo1 saves any callee CPU registers frame on stack (not shown) foo1 allocates local variables by decrementing stack ptr



Initial Investigation of Interrupts

- Complexity Next Level Up from Simple Polling
- Respond to Internal or External Events
 - Internal Timers, Fault Conditions
 - External Logic Inputs, Ports, Input Compare, Input Count
- How Do I Stop?
- How Do I Start?
- Hardware and Toolset Awareness



Assignment - Readings

Lecture Reading

Stacks and Frames Demystified

CU Boulder CSCI 3753 Operating Systems, Spring 2005, Prof. Rick Han

(.pdf provided)

Assignment: Send a Discussion Topic/Question from the CU Presentation to Prof DesCombes by Tuesday 10:00 AM

K&R - Page 83 - ??

Chapter 4: Functions and Program Structure

Chapter 5: Pointers and Arrays

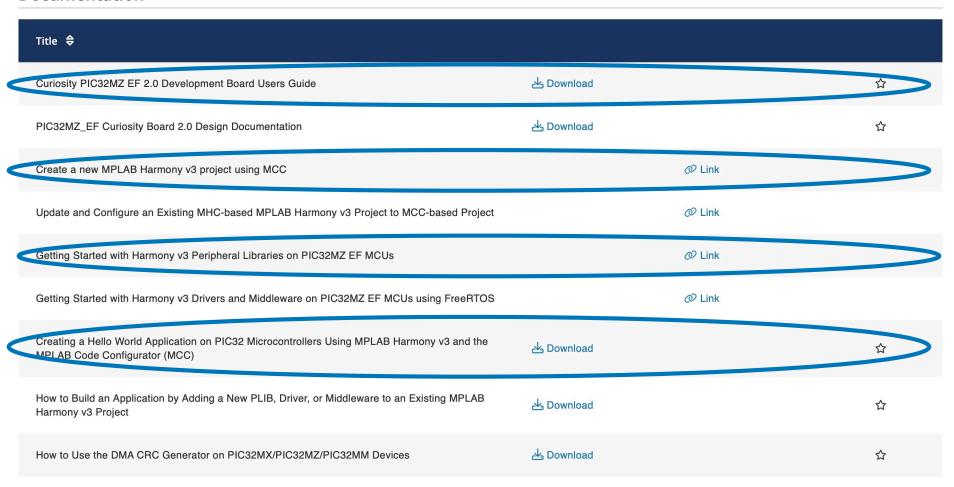
Chapter 6: Structures

- Lab Reading
 - Review Associates' Lab 1 Programs



Assignment - Lab Preparation

Documentation





Assignment - Lab Preparation

Research Microchip Development Tools - Begin Install if Want

MPLAB Harmony 3

Embedded Software Development Framework for 32-bit Microcontrollers and Microprocessors

https://www.microchip.com/en-us/tools-resources/configure/mplab-harmony



Look Ahead

- Discuss Readings
- More on Interrupt Based Real-time Systems



Action Items and Discussion

Al#:	Owner	Slide #	Document	Action