



Computer Science

Fall 2024: CSCI 181RT Real-Time Systems in the Real World

Lecture 19

Thursday, October 31, 2024
Edmunds Hall 105
2:45 PM - 4:00 PM

Professor Jennifer DesCombes

Agenda

- Happy Halloween!



Agenda (the less fun one)

- Go Backs
- Discussion on Code Framework
- User Input UART Assignment Review
- Lab #9 Review
- Hardware Features and Capabilities - OS Related
- Look Ahead
- Assignment
- Action Items

Go Backs

- General?
- Action Item Status
 - AI240910-2: Find recommended book on computer architecture.
 - AI240924-1: At what point as a development team grows does it make sense to have dedicated software and integration testers?
 - AI241024-1: Provide documentation on how to disable compiler optimization.

Discussion on Code Framework

- Overall?
- IO Initialization?
- Project/Hardware Unique Headers
- main?
- Functional Division of Code/Processing
- Use of Module Operator

User Input UART Assignment Review

- Which Option Selected - Smart Task or Smart Interrupt
- Issues?

User Input UART Assignment Review

- Faster User Input

```
sem_t uartRxBufHasData;  
char arrayToReceieve[256];  
void trapUARTReadBuf ( *char );
```

Interrupt will occur when a byte has been received.

```
int myRet;  
trapUARTReadBuf( &arrayToReceive );  
myRet = sem_wait( &uartRxBufHasData );
```

Perform a Software ‘Trap’ to Execute Code In Supervisor/ Interrupt State

Wait for the Rx portion of the UART to receive all data in message.

User Input UART Assignment Review

- User Input
- Determine End of String using '\r'

Software Trap

'trapUARTReadBuf'

```
sem_t uartTxNotBusy;
char arrayToSend[256];
int trapCharCount;
char *trapCharArray;

void trapUARTReadBuf ( *char arrayToReceive )
{
    trapCharArray = arrayToReceive;
    trapCharCount = 0;
}
```

Rx Complete Interrupt

```
ReadUART( trapCharArray[ trapCharCount ] );
if ( trapCharArray[ trapCharCount ] != '\r' )
{
    trapCharCount += 1;
    asm(RINT);
}
else
{
    int myRet;
    myRet = sem_post( &uartRxBufHasData );
    goto( RESCHEDULE );
}
```



User Input UART Assignment Review

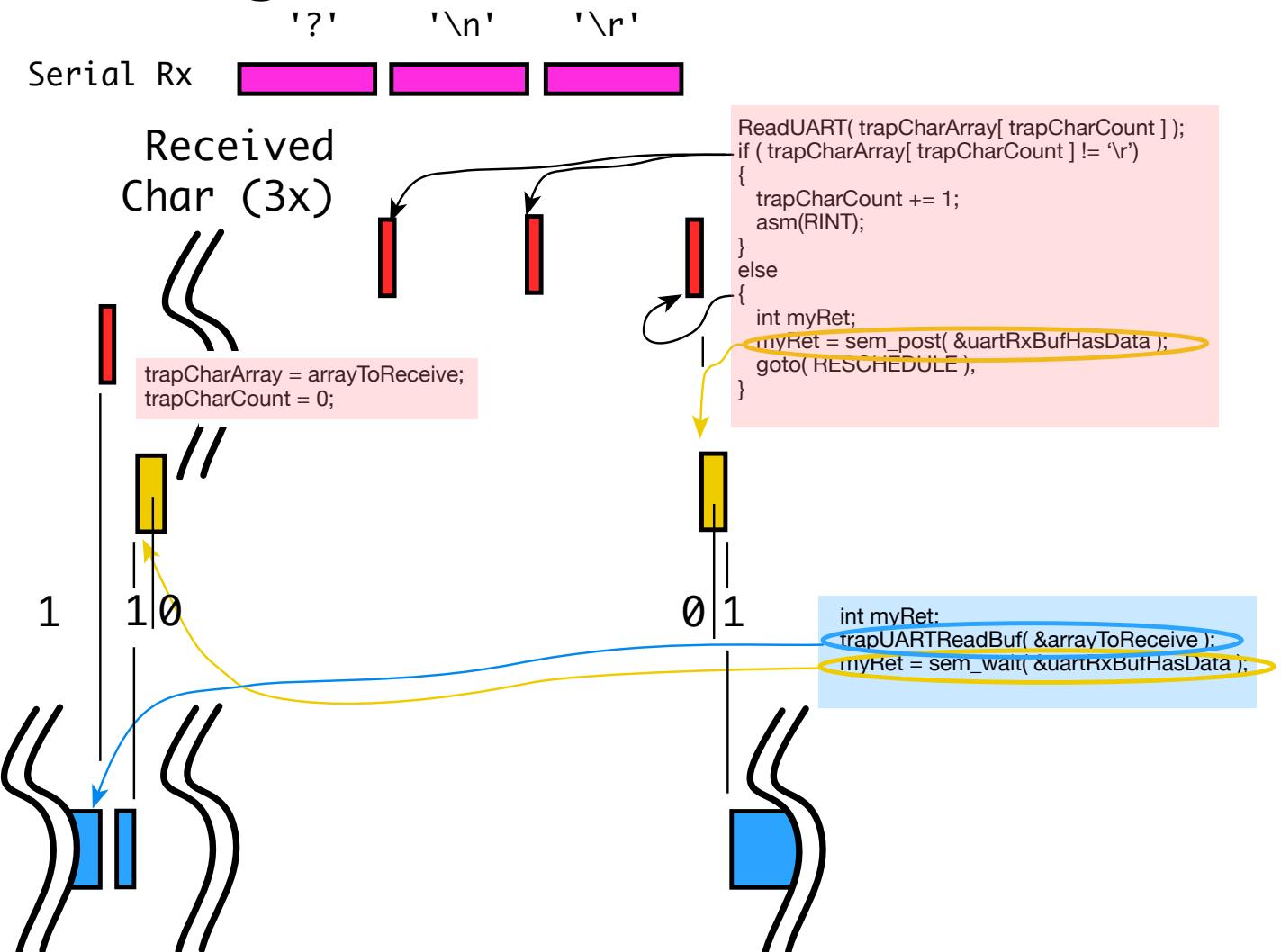
- User Input (Faster)

UART Interrupts
Software Traps

Kernel/OS

uartTxNotBusy
Value

User IO Task



Lab #9 Review

- Goals for Lab (from Lab 7 & 8)
 - Read Digital Input (GPIO1, Connector 501-Pin 5, Processor RK4)
 - Drive LED to Match Digital Input
- Sampling Rate and Data Input Rate (from Lab 7 & 8)
 - Use Function Generator to Experiment

Interrupts and OS Support

- OS Hardware Interrupts - Time and Timers ✓
- Peripheral Hardware Interrupts
 - Input Compare (IC) ✓
 - Serial Port (UART, USART) ✓



Hardware Features and Capabilities - OS Related

Microchip PIC32MZ Embedded Connectivity with Floating Point Unit (EF) Family



MICROCHIP

32-bit MCUs (up to 2 MB Live-Update Flash and 512 KB SRAM) with FPU, Audio and Graphics Interfaces, HS USB, Ethernet, and Advanced Analog

Memory Interfaces

- 50 MHz External Bus Interface (EBI)
- 50 MHz Serial Quad Interface (SQI)

Audio and Graphics Interfaces

- Graphics interfaces: EBI or PMP
- Audio data communication: I²S, LJ, and RJ
- Audio control interfaces: SPI and I²C
- Audio host clock: Fractional clock frequencies with USB synchronization

High-Speed (HS) Communication Interfaces (with Dedicated DMA)

- USB 2.0 Hi-Speed On-The-Go (OTG) controller
- 10/100 Mbps Ethernet MAC with MII and RMII interface

Security Features

- Crypto Engine with RNG for data encryption/decryption and authentication (AES, 3DES, SHA, MD5, and HMAC)
- Advanced memory protection:
 - Peripheral and memory region access control

Direct Memory Access (DMA)

- Eight channels with automatic data size detection
- Programmable Cyclic Redundancy Check (CRC)

Input/Output

- 5V-tolerant pins with up to 32 mA source/sink
- Selectable open drain, pull-ups, pull-downs, and slew rate controls
- External interrupts on all I/O pins
- PPS to enable function remap

Advanced Analog Features

- 12-bit ADC module:
 - 18 Msps with up to six Sample and Hold (S&H) circuits (five dedicated and one shared)
 - Up to 48 analog inputs
 - Can operate during Sleep and Idle modes
 - Multiple trigger sources
 - Six Digital Comparators and six Digital Filters
- Two comparators with 32 programmable voltage references
- Temperature sensor with ±2°C accuracy

Communication Interfaces

- Two CAN modules (with dedicated DMA channels):
 - 2.0B Active with DeviceNet™ addressing support
- Six UART modules (25 Mbps):
 - Supports up to LIN 2.1 and IrDA® protocols
- Six 4-wire SPI modules (up to 50 MHz)
- SQI configurable as an additional SPI module (50 MHz)
- Five I²C modules (up to 1 Mbaud) with SMBus support
- Parallel Host Port (PMP)
- Peripheral Pin Select (PPS) to enable function remap

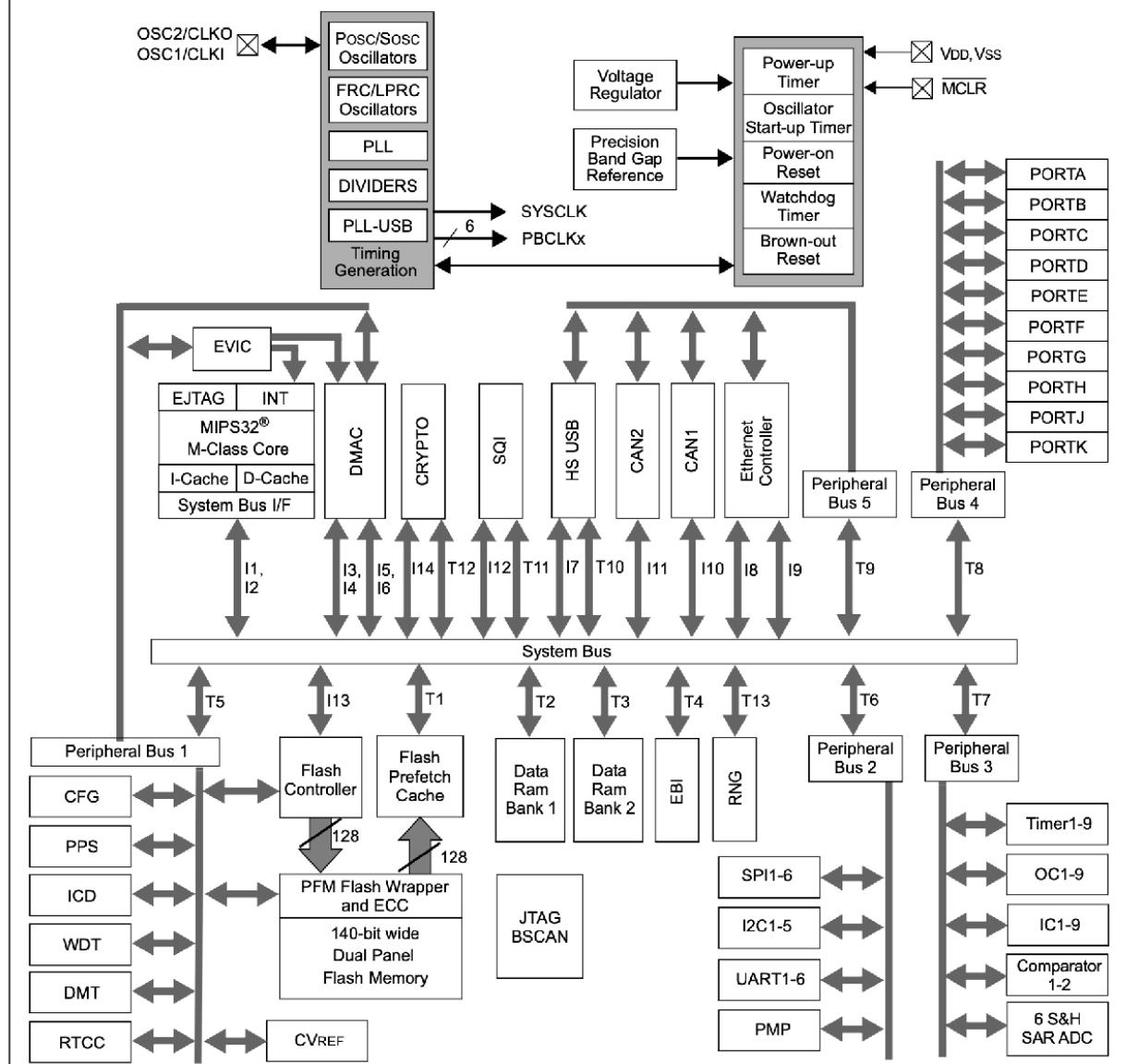
Timers/Output Compare/Input Capture

- Nine 16-bit or up to four 32-bit timers/counters
- Nine Output Compare (OC) modules
- Nine Input Capture (IC) modules
- Real-Time Clock and Calendar (RTCC) module



Hardware Features and Capabilities - OS Related

FIGURE 1-1: PIC32MZ EF FAMILY BLOCK DIAGRAM



Note: Not all features are available on all devices. Refer to [TABLE 1: "PIC32MZ EF Family Features"](#) for the list of features by device.

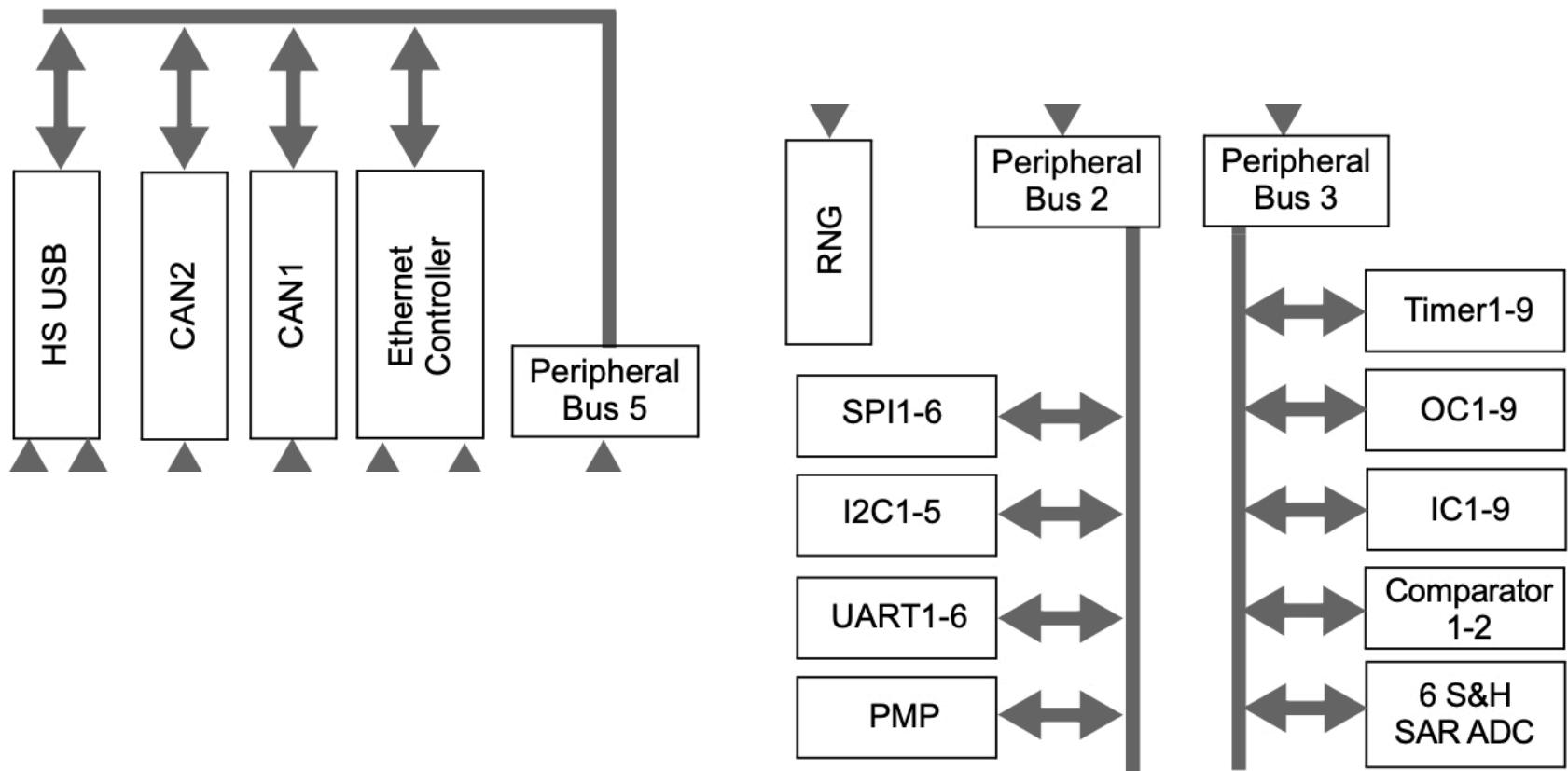
Hardware Features and Capabilities - OS Related

Communication Interfaces

- Two CAN modules (with dedicated DMA channels):
 - 2.0B Active with DeviceNet™ addressing support
- Six UART modules (25 Mbps):
 - Supports up to LIN 2.1 and IrDA® protocols
- Six 4-wire SPI modules (up to 50 MHz)
- SQI configurable as an additional SPI module (50 MHz)
- Five I²C modules (up to 1 Mbaud) with SMBus support
- Parallel Host Port (PMP)
- Peripheral Pin Select (PPS) to enable function remap

Hardware Features and Capabilities - OS Related

- Communications Devices



Hardware Features and Capabilities - OS Related

- More Pins, More Copies of Each Hardware Feature
- Each Package Is Different, Often From Same Die

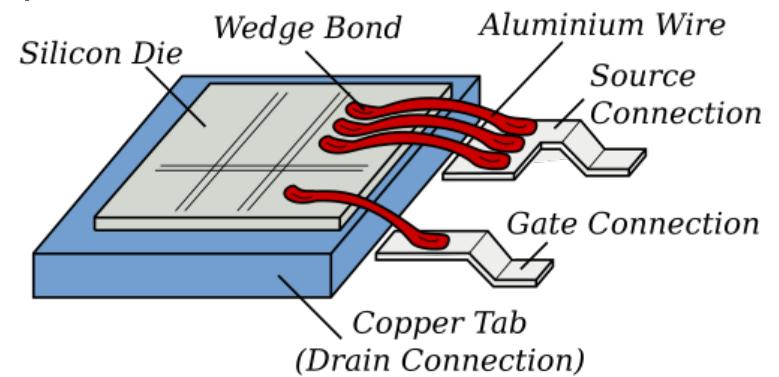
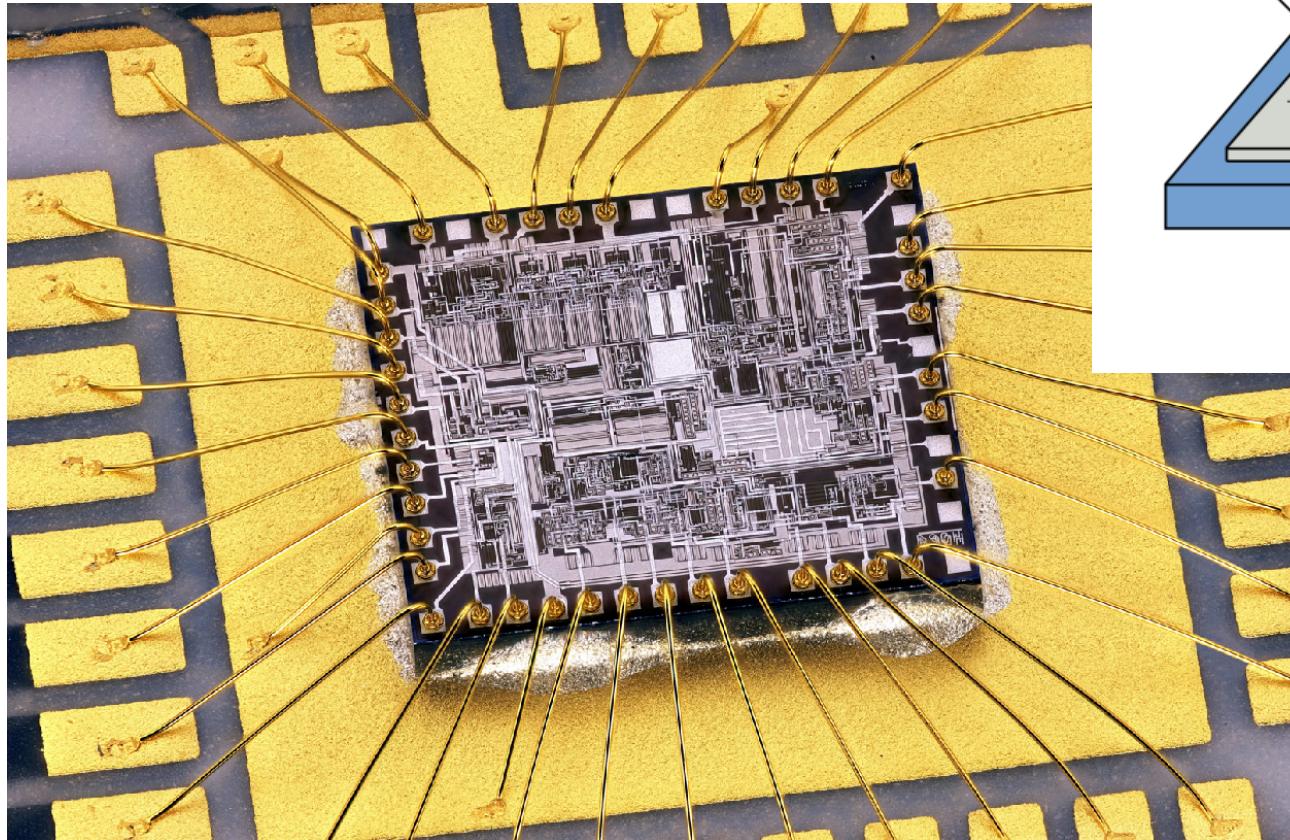
TABLE 1: PIC32MZ EF FAMILY FEATURES

Device	Program Memory (kB)	Data Memory (kB)	Pins	Packages	Boot Flash Memory (kB)	Remappable Peripherals					Crypto	RNG	DMA Channels (Programmable/Dedicated)	ADC (Channels)	Analog Comparators	USB 2.0 HS OTG	I ² C	PMP	EBI	SQI	RTCC	Ethernet	I/O Pins	JTAG	Trace	
						Remappable Pins	Timers/Capture/Compare ⁽¹⁾	UART	SPI/I ² S	External Interrupts ⁽²⁾																
PIC32MZ0512EFE064	512	128	64	TQFP, QFN	160	34	9/9/9	6	4	5	0	N	Y	8/12	24	2	Y	4	Y	N	Y	Y	46	Y	Y	
PIC32MZ0512EFF064											2	N	Y	8/16												
PIC32MZ0512EFK064											2	Y	Y	8/18												
PIC32MZ1024EFE064											0	N	Y	8/12												
PIC32MZ1024EFF064											2	N	Y	8/16												
PIC32MZ1024EFK064											2	Y	Y	8/18												
PIC32MZ0512EFE100											0	N	Y	8/12	40	2	Y	5	Y	Y	Y	Y	Y	78	Y	Y
PIC32MZ0512EFF100											2	N	Y	8/16												
PIC32MZ0512EFK100											2	Y	Y	8/18												
PIC32MZ1024EFE100											0	N	Y	8/12												
PIC32MZ1024EFF100											2	N	Y	8/16												
PIC32MZ1024EFK100											2	Y	Y	8/18												
PIC32MZ1024EFE064											0	N	Y	8/12												
PIC32MZ1024EFF064											2	N	Y	8/16												
PIC32MZ1024EFK064											2	Y	Y	8/18												



Hardware Features and Capabilities - OS Related

- Wire Bonding of Die to Carrier (package)



Hardware Features and Capabilities - OS Related

- More Pins, More Copies of Each Hardware Feature

TABLE 1: PIC32MZ EF FAMILY FEATURES

Device	Program Memory (KB)	Data Memory (KB)	Pins	Packages	Boot Flash Memory (KB)	Remappable Peripherals					
						Remappable Pins	Timers/ Capture/ Compare ⁽¹⁾	UART	SPI/I ² S	External Interrupts ⁽²⁾	CAN 2.0B
PIC32MZ0512EFE064	512	128	64	TQFP, QFN	160	34	9/9/9	6	4	5	0
PIC32MZ0512EFF064											2
PIC32MZ0512EFK064											2
PIC32MZ1024EFE064											0
PIC32MZ1024EFF064											2
PIC32MZ1024EFK064											2
PIC32MZ0512EFE100	512	128	100	TQFP, TFBGA	160	51	9/9/9	6	6	5	0
PIC32MZ0512EFF100											2
PIC32MZ0512EFK100											2
PIC32MZ1024EFE100											0
PIC32MZ1024EFF100											2
PIC32MZ1024EFK100											2

Hardware Features and Capabilities - OS Related

- More Pins, More Copies of Each Hardware Feature

TABLE 1: PIC32MZ EF FAMILY FEATURE

Device	Program Memory (KB)	Data Memory (KB)	Pins	Packages	Boot Flash Memory (KB)	ADC (Channels)	Analog Comparators	USB 2.0 HS OTG	I ² C	PMP	EBI	SQI	RTCC	Ethernet	IO Pins
PIC32MZ0512EFE064	512	128	64	TQFP, QFN	160	24	2	Y	4	Y	N	Y	Y	Y	46
PIC32MZ0512EFF064															
PIC32MZ0512EFK064	1024	256	100	TQFP, TFBGA	160	40	2	Y	5	Y	Y	Y	Y	Y	78
PIC32MZ1024EFE064															
PIC32MZ1024EFF064															
PIC32MZ1024EFK064															
PIC32MZ0512EFE100	512	128	100	TQFP, TFBGA	160	40	2	Y	5	Y	Y	Y	Y	Y	78
PIC32MZ0512EFF100															
PIC32MZ0512EFK100															
PIC32MZ1024EFE100															
PIC32MZ1024EFF100															
PIC32MZ1024EFK100															

Hardware Features and Capabilities - OS Related

- Timer 1 - Only One of This Type Per Package

13.0 TIMER1

Note: This data sheet summarizes the features of the PIC32MZ EF family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **Section 14. “Timers”** (DS60001105) in the *“PIC32 Family Reference Manual”*, which is available from the Microchip web site (www.microchip.com/PIC32).

PIC32MZ EF devices feature one synchronous/asynchronous 16-bit timer that can operate as a free-running interval timer for various timing applications and counting external events. This timer can also be used with the Low-Power Secondary Oscillator (Sosc) for real-time clock applications.

The following modes are supported by Timer1:

- Synchronous Internal Timer
- Synchronous Internal Gated Timer
- Synchronous External Timer
- Asynchronous External Timer

13.1 Additional Supported Features

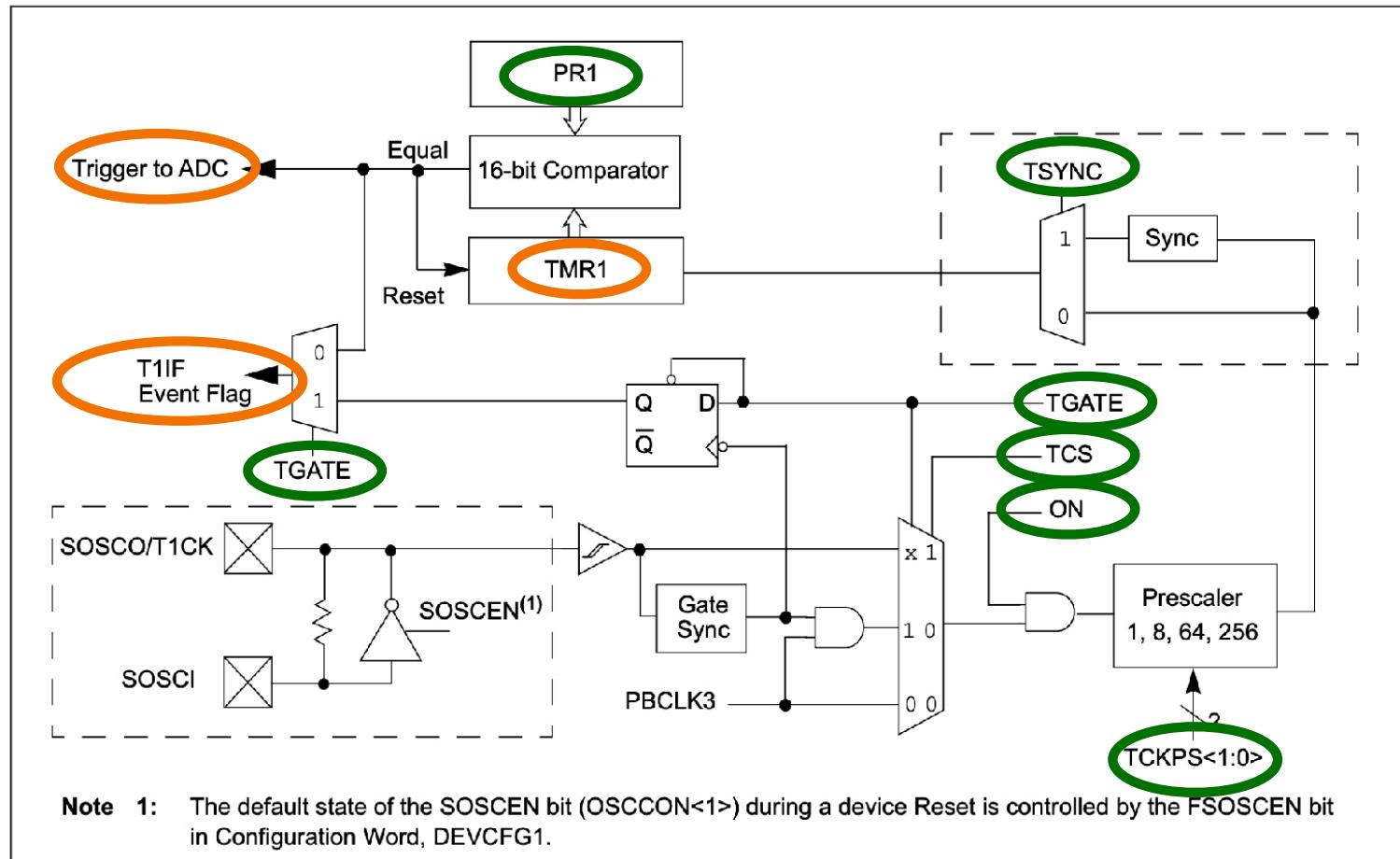
- Selectable clock prescaler
- Timer operation during Sleep and Idle modes
- Fast bit manipulation using CLR, SET and INV registers
- Asynchronous mode can be used with the Sosc to function as a real-time clock
- ADC event trigger



Hardware Features and Capabilities - OS Related

- Timer 1
- **Green** = Config.
- **Orange** = Control Out (status or Interrupt)

FIGURE 13-1: TIMER1 BLOCK DIAGRAM



Hardware Features and Capabilities - OS Related

- Timer 1 - Register List
- Configuration Options Should Match **Green** from Block Diagram
- Block Diagrams May be Simplified - Always Check Register Map

13.2 Timer1 Control Register

TABLE 13-1: TIMER1 REGISTER MAP

Virtual Address (BF84_#)	Register Name()	Bit Range	Bits															
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0
0000	T1CON	31:16	—	—	—			—	—	—	—	—	—	—	—	—	—	0000
		15:0	ON	—	—	SIDL	TWDIS	TWIP	—	—	—	TGATE	—	TCKPS<1:0>	—	TSYNC	TCS	—
0010	TMR1	31:16	—	—	—			—	—	—	—	—	—	—	—	—	—	0000
		15:0																0000
0020	PR1	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0																FFFF

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: All registers in this table have corresponding CLR, SET and INV registers at their virtual addresses, plus offsets of 0x4, 0x8 and 0xC, respectively. See [Section 12.3 "CLR, SET, and INV Registers"](#) for more information.

Hardware Features and Capabilities - OS Related

- Timer 1 - Register List
- Configuration Options Should Match **Green** from Block Diagram
- Block Diagrams May be Simplified - Always Check Register Map

13.2 Timer1 Control Register

TABLE 13-1: TIMER1 REGISTER MAP

Virtual Address (BF84_#)	Register Name{} Bit Range	Bits																All Resets
		31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
0000	T1CON	31:16	—	—	—	SIDL	TWDIS	TWIP	—	—	—	—	—	—	—	—	—	0000
		15:0	ON	—	—		—	—	—	TGATE	—	TCKPS<1:0>	—	TSYNC	TCS	—	—	0000
0010	TMR1	31:16	—	—	—	TMR1<15:0>	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0																0000
0020	PR1	31:16	—	—	—	PR1<15:0>	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0																FFFF

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: All registers in this table have corresponding CLR, SET and INV registers at their virtual addresses, plus offsets of 0x4, 0x8 and 0xC, respectively. See [Section 12.3 "CLR, SET, and INV Registers"](#) for more information.

bit 12	TWDIS: Asynchronous Timer Write Disable bit 1 = Writes to TMR1 are ignored until pending write operation completes 0 = Back-to-back writes are enabled (Legacy Asynchronous Timer functionality)	bit 11	TWIP: Asynchronous Timer Write in Progress bit <u>In Asynchronous Timer mode:</u> 1 = Asynchronous write to TMR1 register in progress 0 = Asynchronous write to TMR1 register complete <u>In Synchronous Timer mode:</u> This bit is read as '0'.
--------	---	--------	---

Hardware Features and Capabilities - OS Related

- Timer 2 to 7 - Multiples of This Type Per Package

14.0 TIMER2/3, TIMER4/5, TIMER6/7, AND TIMER8/9

Note: This data sheet summarizes the features of the PIC32MZ EF family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **Section 14. “Timers”** (DS60001105) of the “*PIC32 Family Reference Manual*”, which is available from the Microchip web site (www.microchip.com/PIC32).

The PIC32MZ EF family of devices features eight synchronous 16-bit timers (default) that can operate as a free-running interval timer for various timing applications and counting external events.

The following modes are supported:

- Synchronous internal 16-bit timer
- Synchronous internal 16-bit gated timer
- Synchronous external 16-bit timer

Four 32-bit synchronous timers are available by combining Timer2 with Timer3, Timer4 with Timer5, Timer6 with Timer7, and Timer8 with Timer9.

The 32-bit timers can operate in one of three modes:

- Synchronous internal 32-bit timer
- Synchronous internal 32-bit gated timer
- Synchronous external 32-bit timer

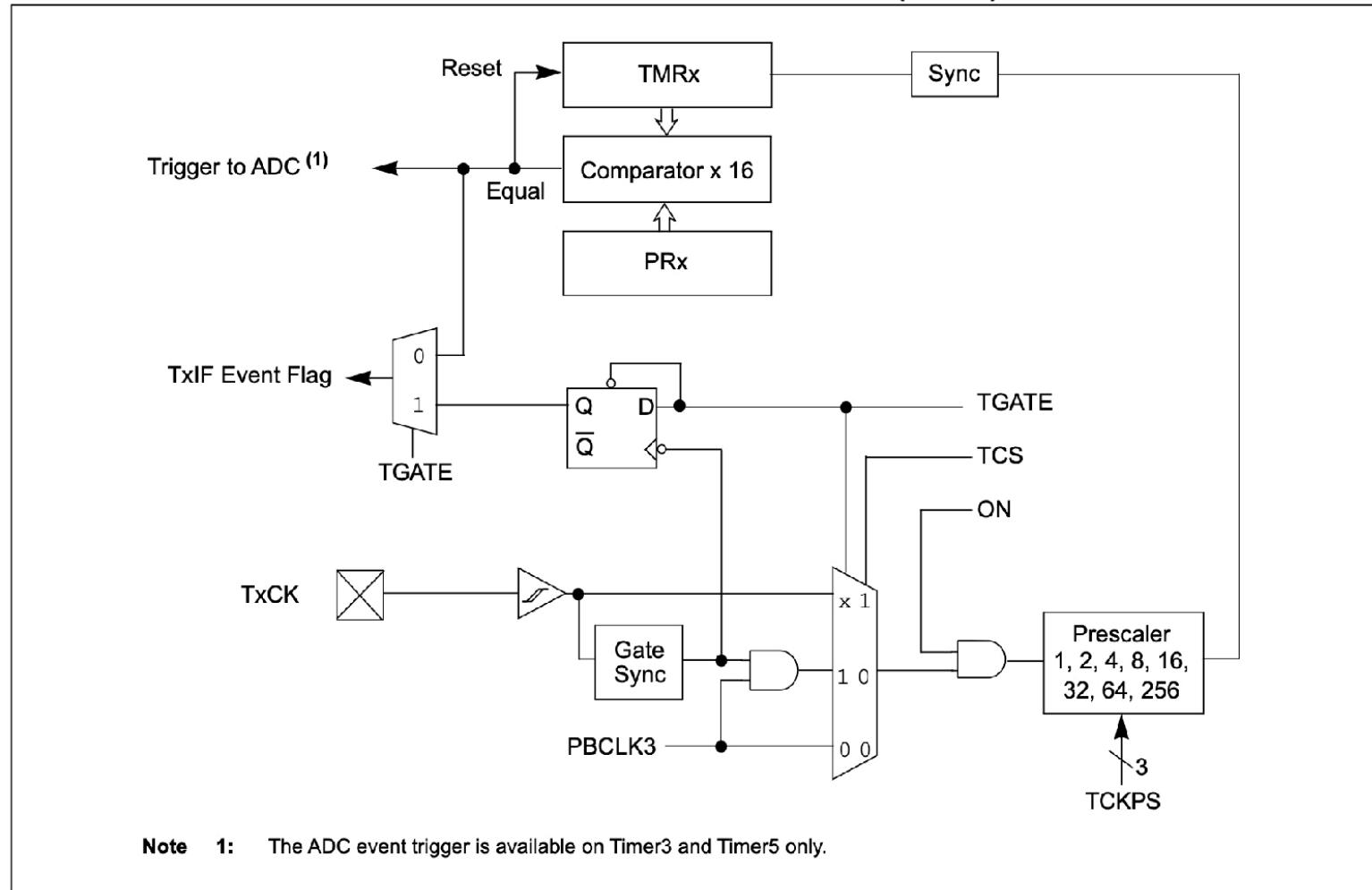
14.1 Additional Supported Features

- Selectable clock prescaler
- Timers operational during CPU idle
- Time base for Input Capture and Output Compare modules (Timer2 through Timer7 only)
- ADC event trigger (Timer3 and Timer5 only)
- Fast bit manipulation using CLR, SET, and INV registers

Hardware Features and Capabilities - OS Related

- Timer 1
- 16-bit Block Diagram

FIGURE 14-1: TIMER2 THROUGH TIMER9 BLOCK DIAGRAM (16-BIT)

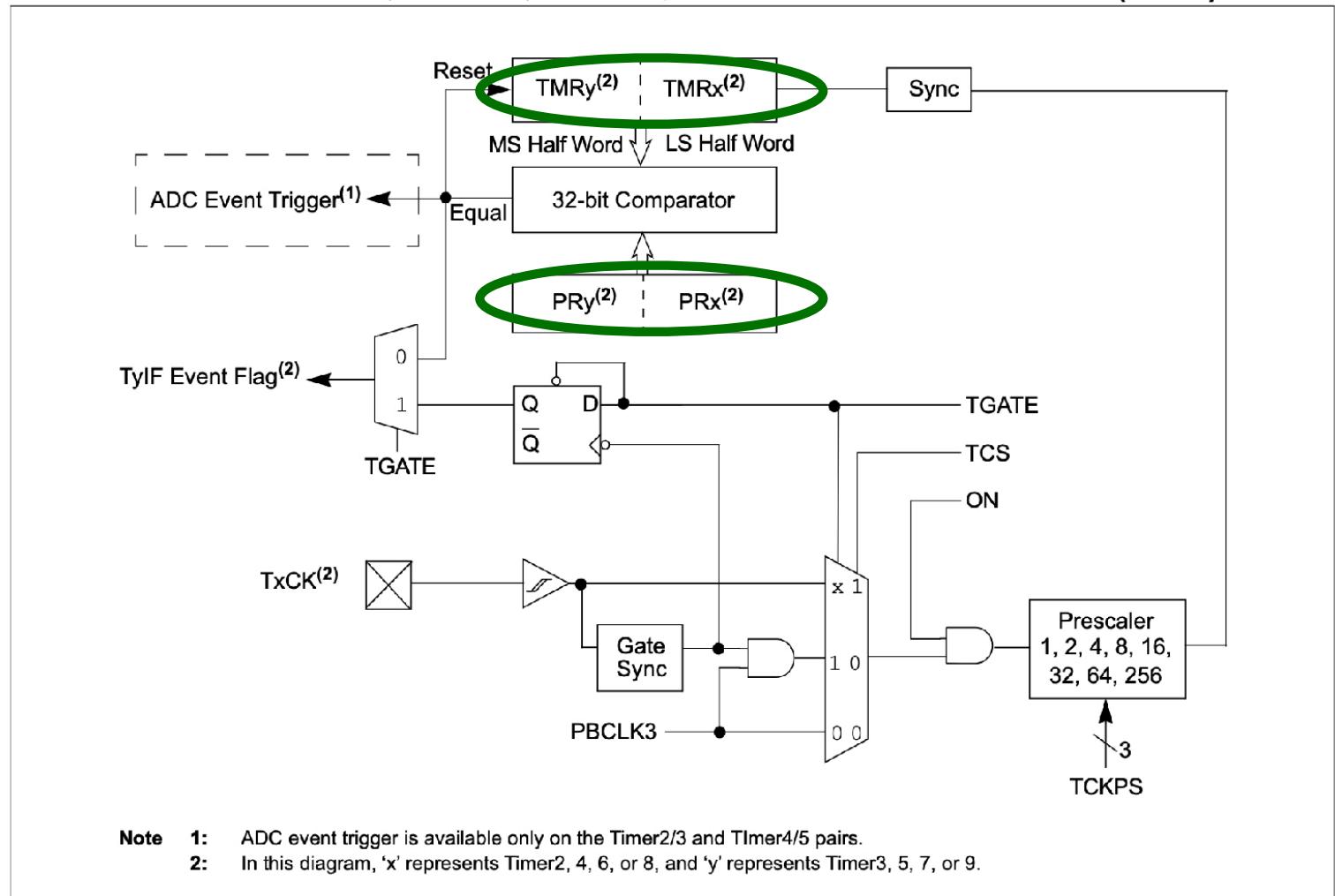




Hardware Features and Capabilities - OS Related

- Timer 1
- 32-bit Block Diagram
- **Green** = Combined Registers from Timer n & (n+1)

FIGURE 14-2: TIMER2/3, TIMER4/5, TIMER6/7, AND TIMER8/9 BLOCK DIAGRAM (32-BIT)



Hardware Features and Capabilities - OS Related

- Input Compare - Up to 10 Circuits per Package

17.0 INPUT CAPTURE

Note: This data sheet summarizes the features of the PIC32MZ EF family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **Section 15. “Input Capture”** (DS60001122) of the “*PIC32 Family Reference Manual*”, which is available from the Microchip web site (www.microchip.com/PIC32).

The Input Capture module is useful in applications requiring frequency (period) and pulse measurement.

The Input Capture module captures the 16-bit or 32-bit value of the selected Time Base registers when an event occurs at the ICx pin.

Capture events are caused by the following:

- Capture timer value on every edge (rising and falling), specified edge first

- Prescaler capture event modes:
 - Capture timer value on every 4th rising edge of input at ICx pin
 - Capture timer value on every 16th rising edge of input at ICx pin

Each input capture channel can select between one of six 16-bit timers for the time base, or two of six 16-bit timers together to form a 32-bit timer. The selected timer can use either an internal or external clock.

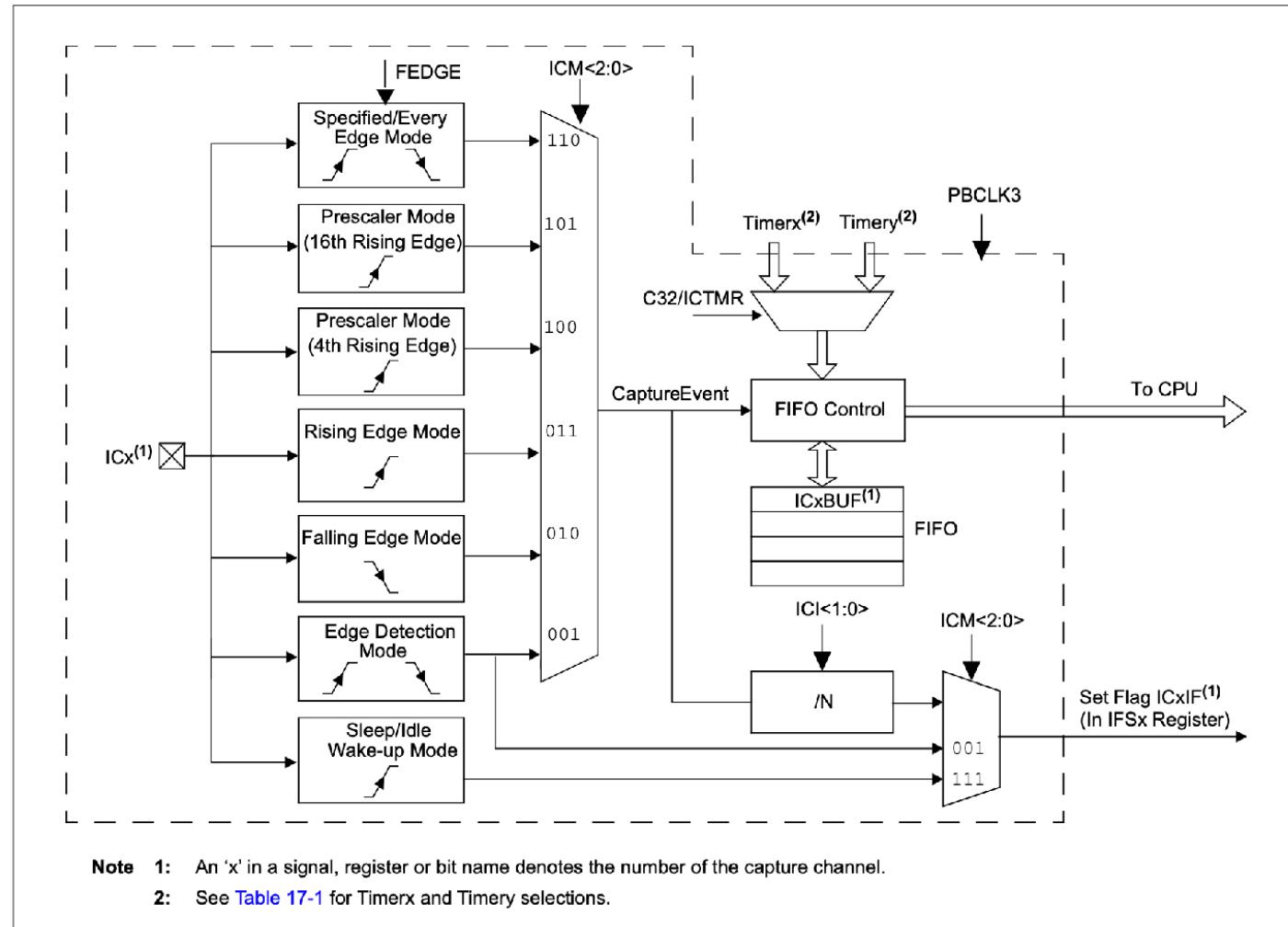
Other operational features include:

- Device wake-up from capture pin during Sleep and Idle modes
- Interrupt on input capture event
- 4-word FIFO buffer for capture values; Interrupt optionally generated after 1, 2, 3, or 4 buffer locations are filled
- Input capture can also be used to provide additional sources of external interrupts

Hardware Features and Capabilities - OS Related

- Input Compare

FIGURE 17-1: INPUT CAPTURE BLOCK DIAGRAM

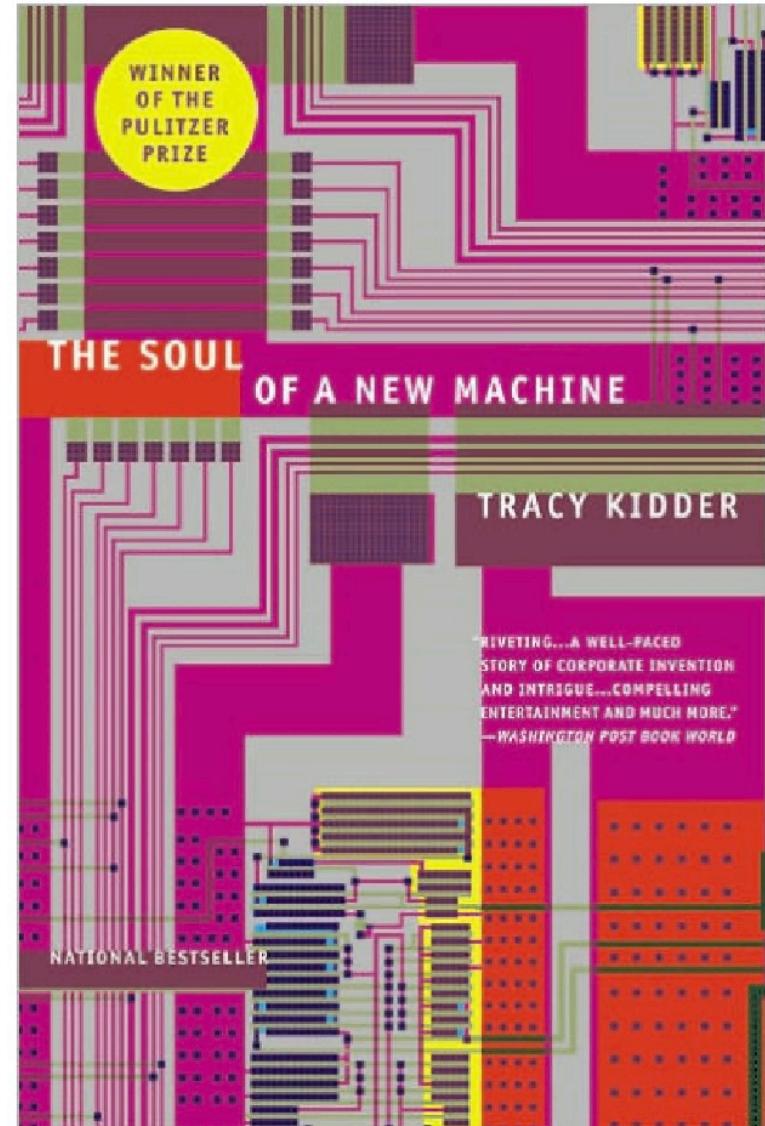


Look Ahead

- Discussion on Reading
- More Hardware Features and Capabilities - OS Related
- Preview of Lab 10

Assignment - Readings

- The Soul Of A New Machine
 - Prologue, Chapter 3 and 4: Building A Team, Wallach's Golden Moment.
 - Send Me Discussion Topics by 10:00 AM on Election Day, Tuesday, November 5, 2024.



Assignment - Hardware Documentation

- Chip Documentation - Chapter 17 - Input Compare
- Functional Modes
- Register Operations
- Download Full Documentation
 - More Information?
 - Better Presentation - Easier to Understand?

Action Items and Discussion

AI#:	Owner	Slide #	Document	Action