



Computer Science

Fall 2024: CSCI 181RT Real-Time Systems in the Real World

Lecture 24

Tuesday, November 19, 2024
Edmunds Hall 105
2:45 PM - 4:00 PM

Professor Jennifer DesCombes

Agenda

- Go Backs
- Discussion on Reading
- Discussion on Additional Assignments
- Field Programmable Gate Array (FPGA)
- FPGA Project Example
- Lab #12 Preview
- Look Ahead
- Assignment
- Action Items

Go Backs

- General?
- Action Item Status
 - AI240910-2: Find recommended book on computer architecture.
 - AI240924-1: At what point as a development team grows does it make sense to have dedicated software and integration testers?
 - AI241024-1: Provide documentation on how to disable compiler optimization.
 - AI241107-1: Generate drawing showing location of Task Test Points on evaluation board.

Discussion on Readings

- The Soul Of A New Machine
 - Chapters 8 & 9: The Wonderful Micromachines, A Workshop

Discussion on Additional Assignments

- Grace-Bluegrass Basic Logic Gates.pdf
- Xilinx_CPLD_Architecture.pdf
- Many_types_of_FPGAs.pdf
- University of Wisconsin programmable-logic.pdf
- CERN Introduction to FPGA Design.pdf

FPGA - Contents and Capabilities - S3E

- RAM - Discrete and Block
- Multipliers
- Multiple Clock Options
- Extended IO Capability

- Abundant, flexible logic resources
 - Densities up to 33,192 logic cells, including optional shift register or distributed RAM support
 - Efficient wide multiplexers, wide logic
 - Fast look-ahead carry logic
 - Enhanced 18 x 18 multipliers with optional pipeline
 - IEEE 1149.1/1532 JTAG programming/debug port
- Hierarchical SelectRAM™ memory architecture
 - Up to 648 Kbits of fast block RAM
 - Up to 231 Kbits of efficient distributed RAM
- Up to eight Digital Clock Managers (DCMs)
 - Clock skew elimination (delay locked loop)
 - Frequency synthesis, multiplication, division
 - High-resolution phase shifting
 - Wide frequency range (5 MHz to over 300 MHz)
- Eight global clocks plus eight additional clocks per each half of device, plus abundant low-skew routing



DS312-1 (v3.4) November 9, 2006

Spartan-3E FPGA Family: Introduction and Ordering Information

Product Specification

FPGA - Contents and Capabilities - S3E

- RAM - Discrete and Block
- Multipliers
- Multiple Clock Options
- Extended IO Capability

Table 1: Summary of Spartan-3E FPGA Attributes

Device	System Gates	Equivalent Logic Cells	CLB Array (One CLB = Four Slices)				Distributed RAM bits ⁽¹⁾	Block RAM bits ⁽¹⁾	Dedicated Multipliers	DCMs	Maximum User I/O	Maximum Differential I/O Pairs
			Rows	Columns	Total CLBs	Total Slices						
XC3S100E	100K	2,160	22	16	240	960	15K	72K	4	2	108	40
XC3S250E	250K	5,508	34	26	612	2,448	38K	216K	12	4	172	68
XC3S500E	500K	10,476	46	34	1,164	4,656	73K	360K	20	4	232	92
XC3S1200E	1200K	19,512	60	46	2,168	8,672	136K	504K	28	8	304	124
XC3S1600E	1600K	33,192	76	58	3,688	14,752	231K	648K	36	8	376	156

Notes:

1. By convention, one Kb is equivalent to 1,024 bits.



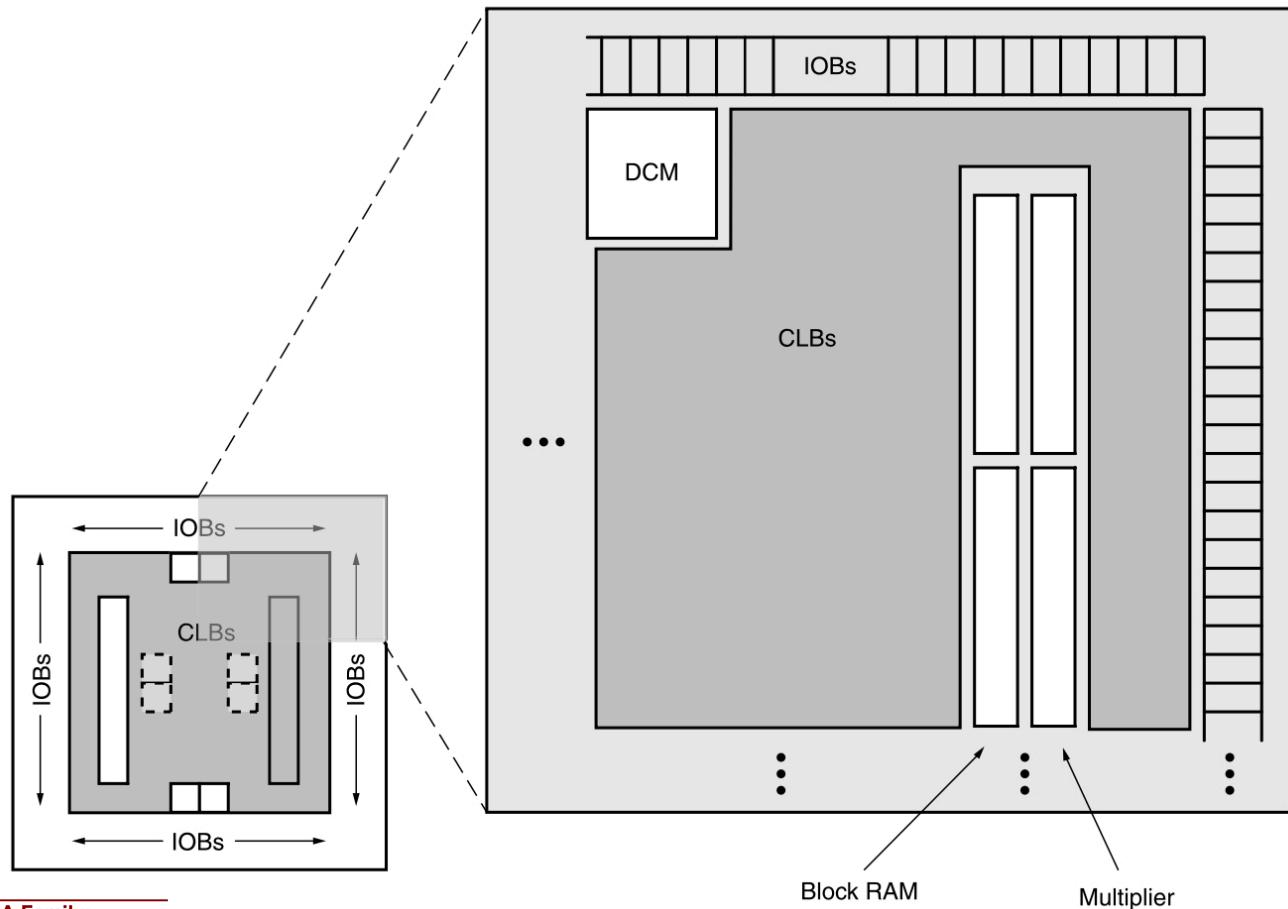
DS312-1 (v3.4) November 9, 2006

Spartan-3E FPGA Family: Introduction and Ordering Information

Product Specification

FPGA - Contents and Capabilities - S3E

- RAM - Discrete and Block
- Multipliers
- Multiple Clock Options
- Extended IO Capability



DS312-1 (v3.4) November 9, 2006

**Spartan-3E FPGA Family:
Introduction and Ordering
Information**

Product Specification



FPGA - Contents and Capabilities - S3E

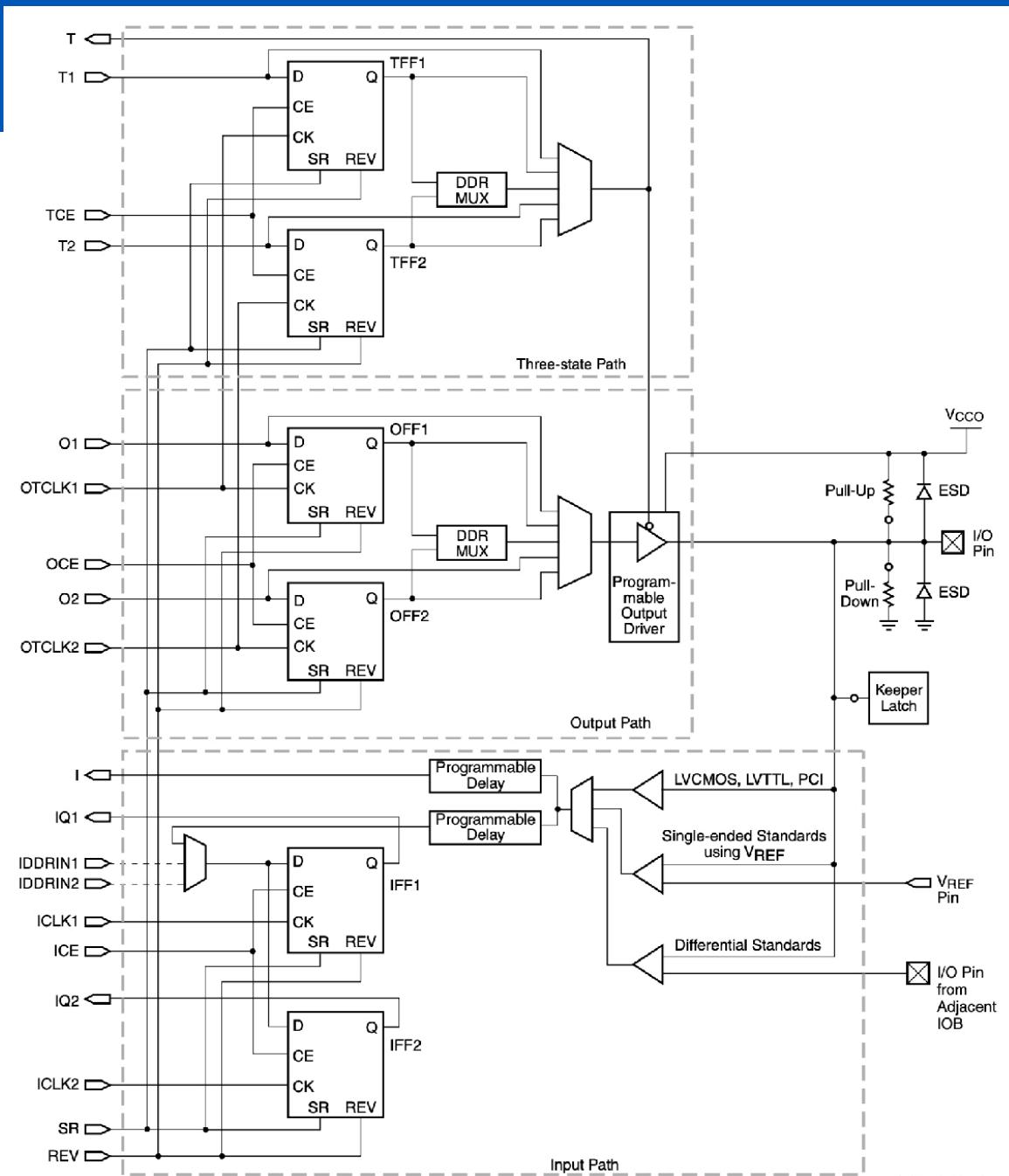
- RAM - Discrete and Block
- Multipliers
- Multiple Clock Options
- Extended IO Capability



DS312-1 (v3.4) November 9, 2006

Spartan-3E FPGA Family:
Introduction and Ordering
Information

Product Specification



FPGA - Contents and Capabilities - S6

- PCIe and High Speed Interfaces
- PCI (Parallel)
- DSP Blocks
- Memory Controllers
 - Integrated Endpoint block for PCI Express designs (LXT)
 - Low-cost PCI® technology support compatible with the 33 MHz, 32- and 64-bit specification.
 - Efficient DSP48A1 slices
 - High-performance arithmetic and signal processing
 - Fast 18 x 18 multiplier and 48-bit accumulator
 - Pipelining and cascading capability
 - Pre-adder to assist filter applications

- Integrated Memory Controller blocks
 - DDR, DDR2, DDR3, and LPDDR support
 - Data rates up to 800 Mb/s (12.8 Gb/s peak bandwidth)
 - Multi-port bus structure with independent FIFO to reduce design timing issues
- Abundant logic resources with increased logic capacity
 - Optional shift register or distributed RAM support
 - Efficient 6-input LUTs improve performance and minimize power
 - LUT with dual flip-flops for pipeline centric applications
- Block RAM with a wide range of granularity
 - Fast block RAM with byte write enable
 - 18 Kb blocks that can be optionally programmed as two independent 9 Kb block RAMs
- Clock Management Tile (CMT) for enhanced performance
 - Low noise, flexible clocking
 - Digital Clock Managers (DCMs) eliminate clock skew and duty cycle distortion
 - Phase-Locked Loops (PLLs) for low-jitter clocking
 - Frequency synthesis with simultaneous multiplication, division, and phase shifting
 - Sixteen low-skew global clock networks



FPGA - Contents and Capabilities - S6

- PCIe and High Speed Interfaces
- PCI (Parallel)
- DSP Blocks
- Memory Controllers



Spartan-6 Family Overview

DS160 (v2.0) October 25, 2011

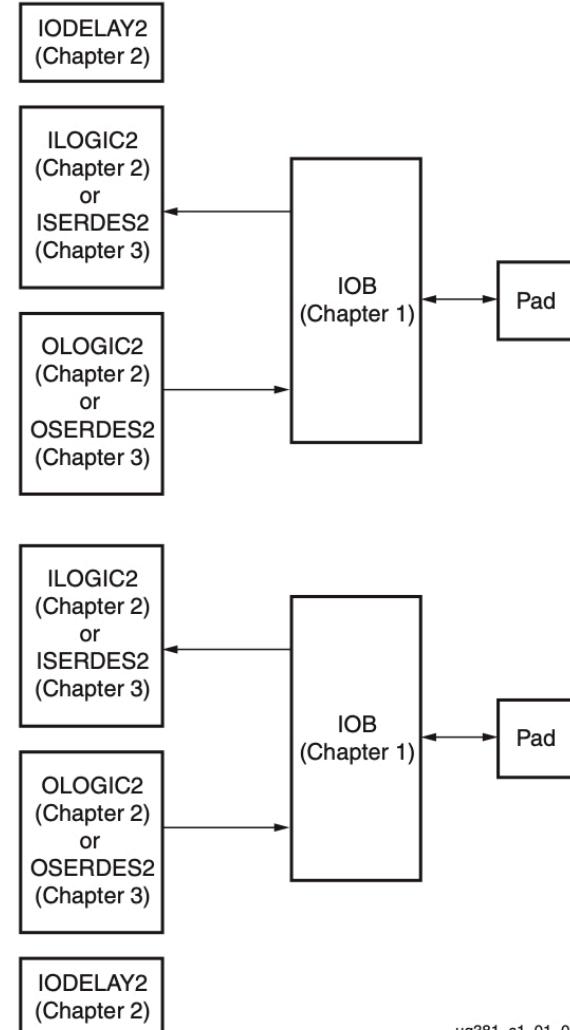
Product Specification

Table 1: Spartan-6 FPGA Feature Summary by Device

Device	Logic Cells ⁽¹⁾	Configurable Logic Blocks (CLBs)			DSP48A1 Slices ⁽³⁾	Block RAM Blocks		CMTs ⁽⁵⁾	Memory Controller Blocks (Max) ⁽⁶⁾	Endpoint Blocks for PCI Express	Maximum GTP Transceivers	Total I/O Banks	Max User I/O
		Slices ⁽²⁾	Flip-Flops	Max Distributed RAM (Kb)		18 Kb ⁽⁴⁾	Max (Kb)						
XC6SLX4	3,840	600	4,800	75	8	12	216	2	0	0	0	4	132
XC6SLX9	9,152	1,430	11,440	90	16	32	576	2	2	0	0	4	200
XC6SLX16	14,579	2,278	18,224	136	32	32	576	2	2	0	0	4	232
XC6SLX25	24,051	3,758	30,064	229	38	52	936	2	2	0	0	4	266
XC6SLX45	43,661	6,822	54,576	401	58	116	2,088	4	2	0	0	4	358
XC6SLX75	74,637	11,662	93,296	692	132	172	3,096	6	4	0	0	6	408
XC6SLX100	101,261	15,822	126,576	976	180	268	4,824	6	4	0	0	6	480
XC6SLX150	147,443	23,038	184,304	1,355	180	268	4,824	6	4	0	0	6	576

FPGA - Contents and Capabilities - S6

- PCIe and High Speed Interfaces
- PCI (Parallel)
- DSP Blocks
- Memory Controllers

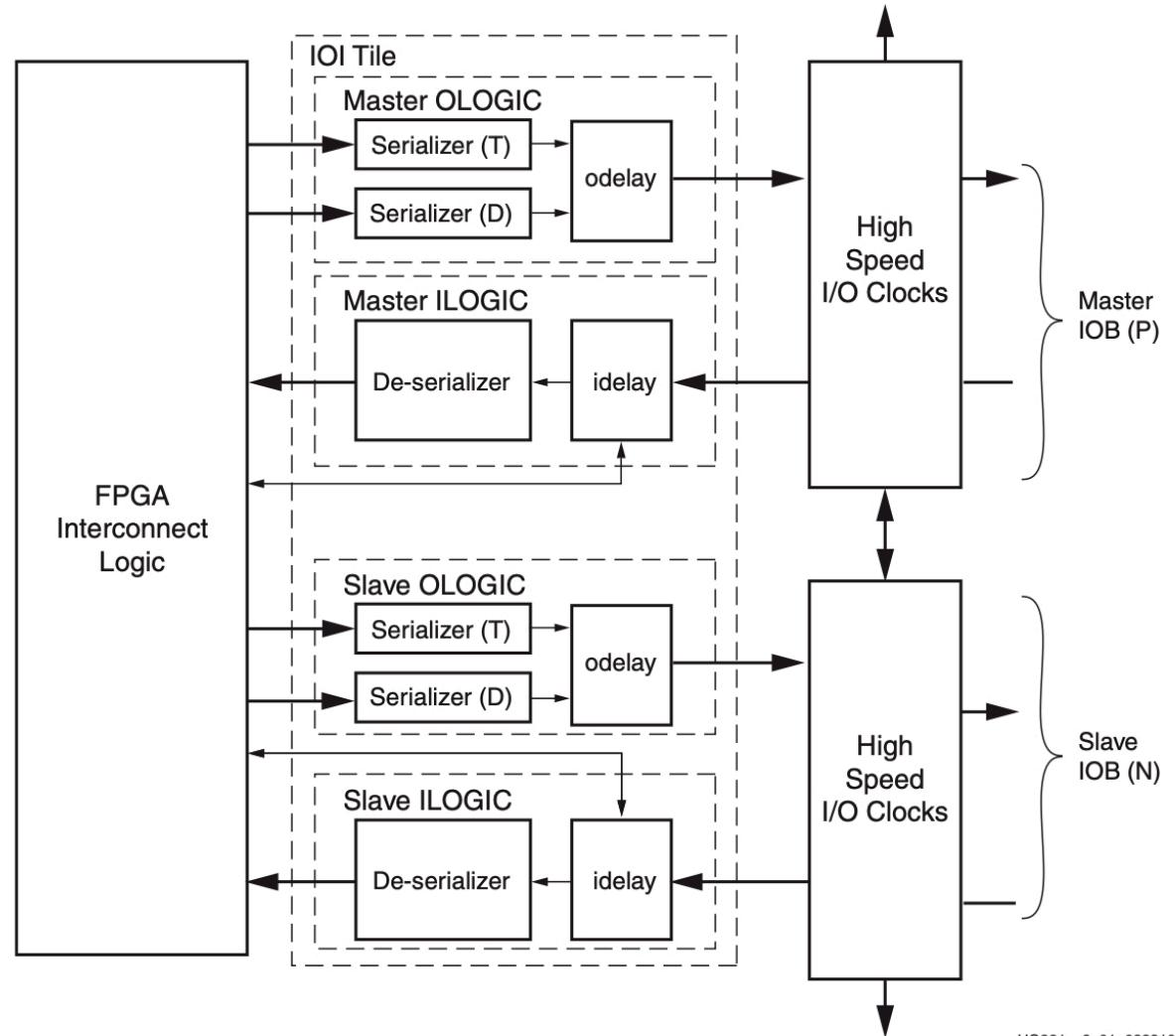


ug381_c1_01_041709

Figure 1-1: Spartan-6 FPGA I/O Tile

FPGA - Contents and Capabilities - S6

- PCIe and High Speed Interfaces
- PCI (Parallel)
- DSP Blocks
- Memory Controllers



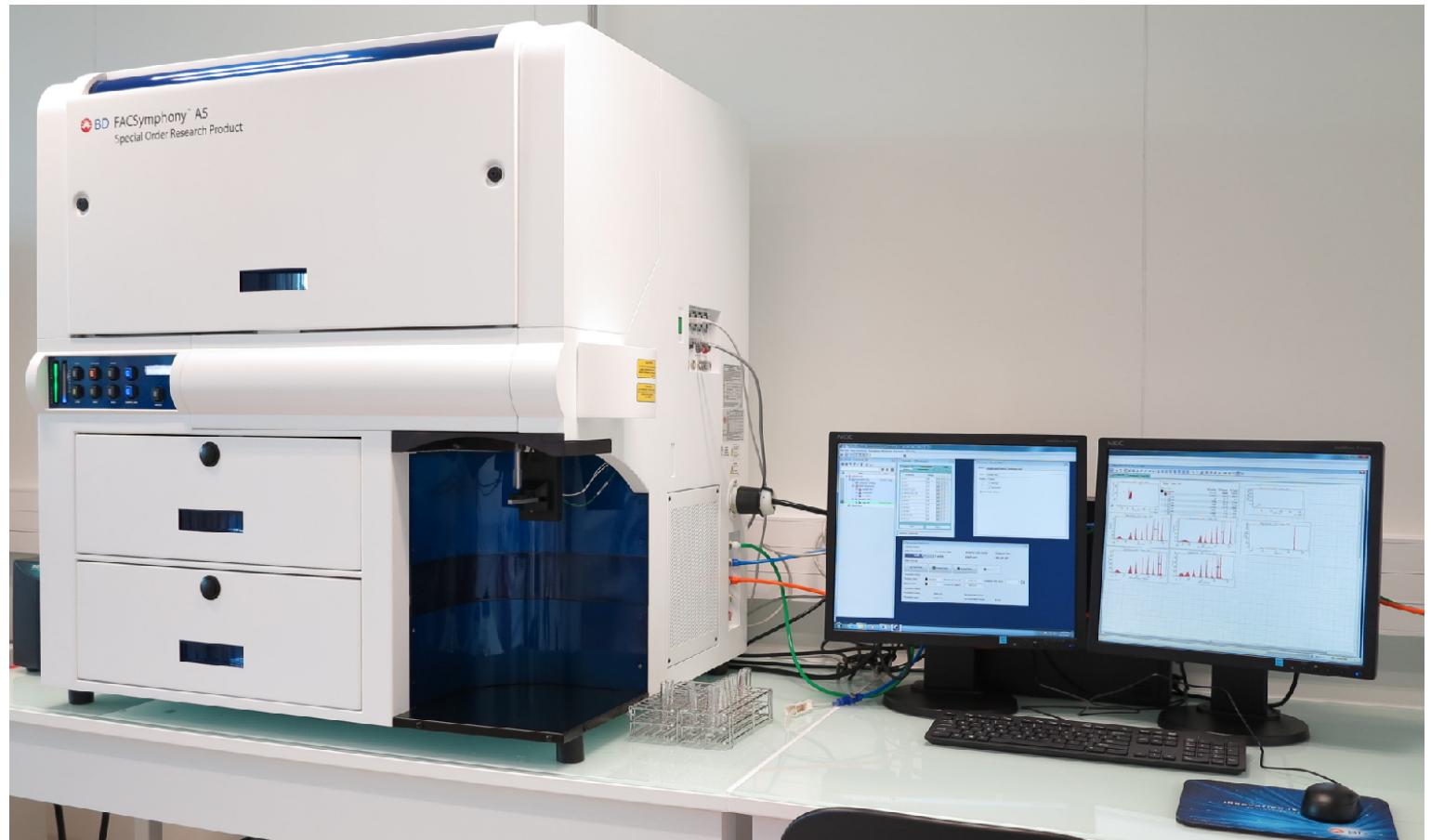
UG381_c2_01_022310

FPGA - Contents and Capabilities - Current Generation

- 10X to 1000X Capability of Spartan 6
- More Dedicated Interfaces and Protocols
- Higher Speed
- Integrated Processors
- Integrated Processors and Video Processors
- Very Complex Components and Support Circuitry

Real Time Systems?

- This?



FPGA - Case Study - X60 Cell Sorter

- 2016 Project
- Derived from 2014 Project

**X60 / Sorter System
Preliminary Design Review**

**Prepared for
BD Biosciences**

**April 28, 2016
General Micro Systems**

GMS CONFIDENTIAL
X60/Sorter PDR
28 April 2016



**X60 Sorter
Preliminary Design Review
*Sort Processing***

**Prepared for
BD Biosciences**

**April 28, 2016
General Micro Systems**

GMS CONFIDENTIAL
X60/Sorter PDR
28 April 2016



FPGA - Case Study - X60 Cell Sorter

- Agenda Builds Story
- Difficult Topics at End of Presentation

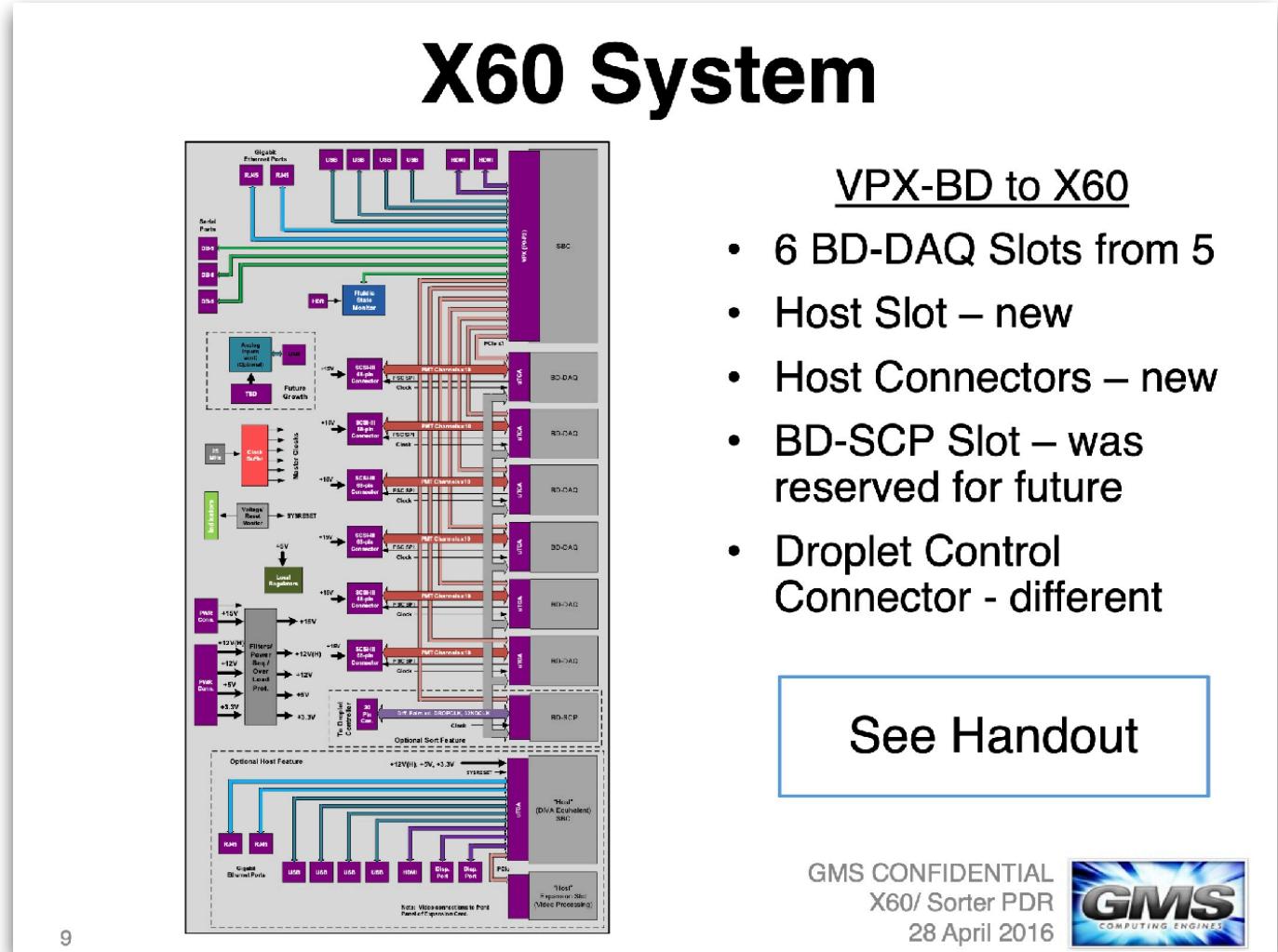
BD X60 / Sorter PDR Topics

- Customer Requirements Overview
- Enhancements Overview
- Performance Analysis Update
- X60 System Overview
- Specifications Overview – Three documents
- Programmatic – Deliverables, Schedule, Risks
- Design Details Discussion
- Action Items and Approval



FPGA - Case Study - X60 Cell Sorter

- Hardware Block Diagram
- “Handout” Contained Enlarged Image



VPX-BD to X60

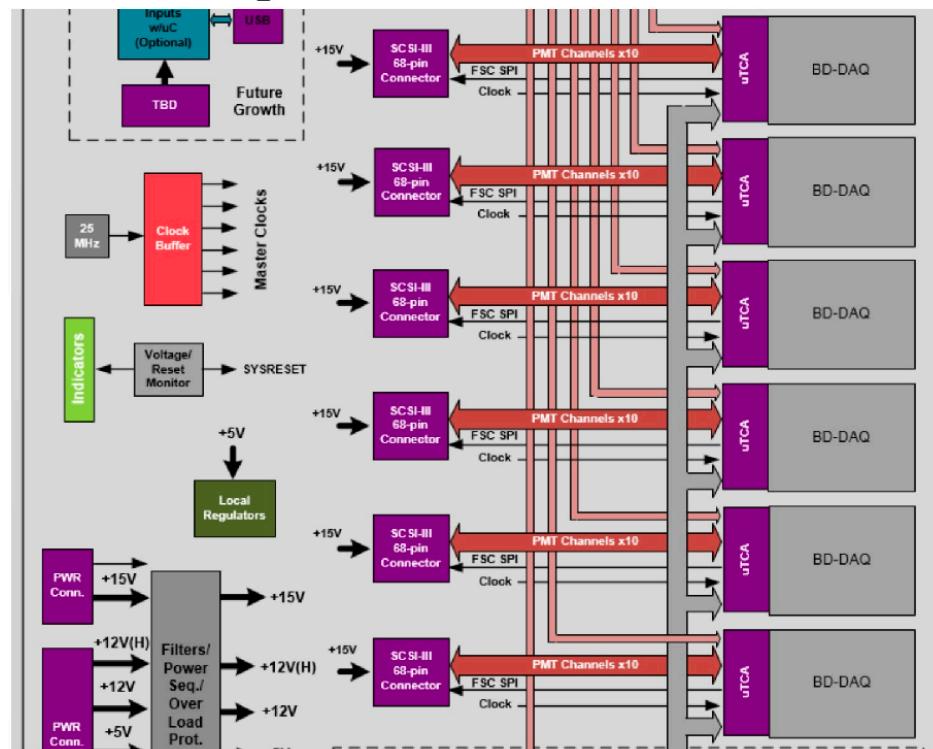
- 6 BD-DAQ Slots from 5
- Host Slot – new
- Host Connectors – new
- BD-SCP Slot – was reserved for future
- Droplet Control Connector - different

See Handout

FPGA - Case Study - X60 Cell Sorter

- Zoom In Hardware Block Diagram
- Discussion of What is the Same (DAQ Cards)

X60 System – BD-DAQ



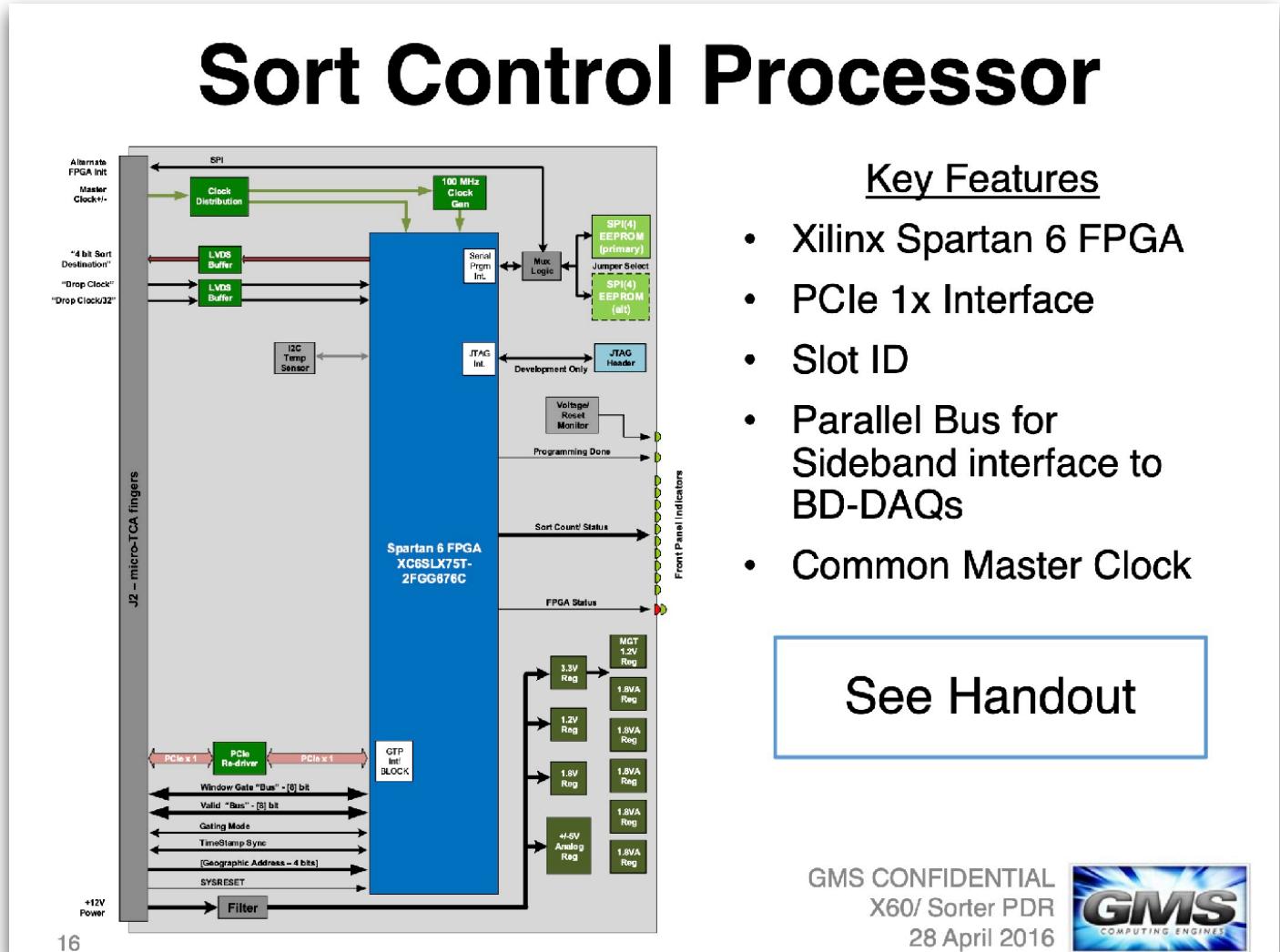
GMS CONFIDENTIAL
X60/ Sorter PDR
28 April 2016





FPGA - Case Study - X60 Cell Sorter

- SCP Hardware Block Diagram
- “Handout” Contained Enlarged Image



FPGA - Case Study - X60 Cell Sorter

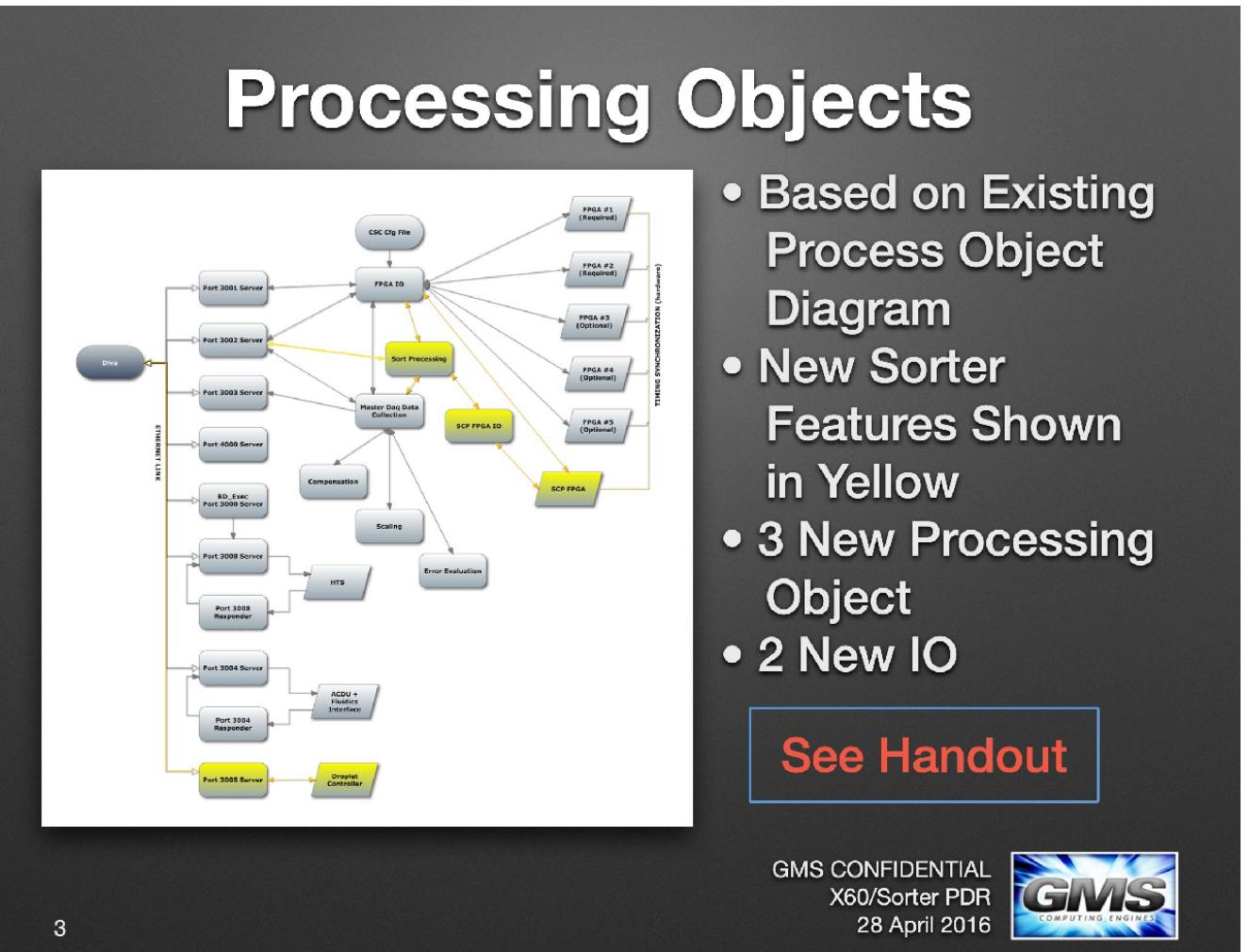
- Agenda Builds Story
- Difficult Topics at End of Presentation

VPX Sorter System Design, Software and Firmware

- Processing Objects
- Data Flow
- SCP Functions
- Processing Sequence and Timing
- Real Time Operating System
- CPU Core Allocation and Timing
- Performance and Margin Analysis

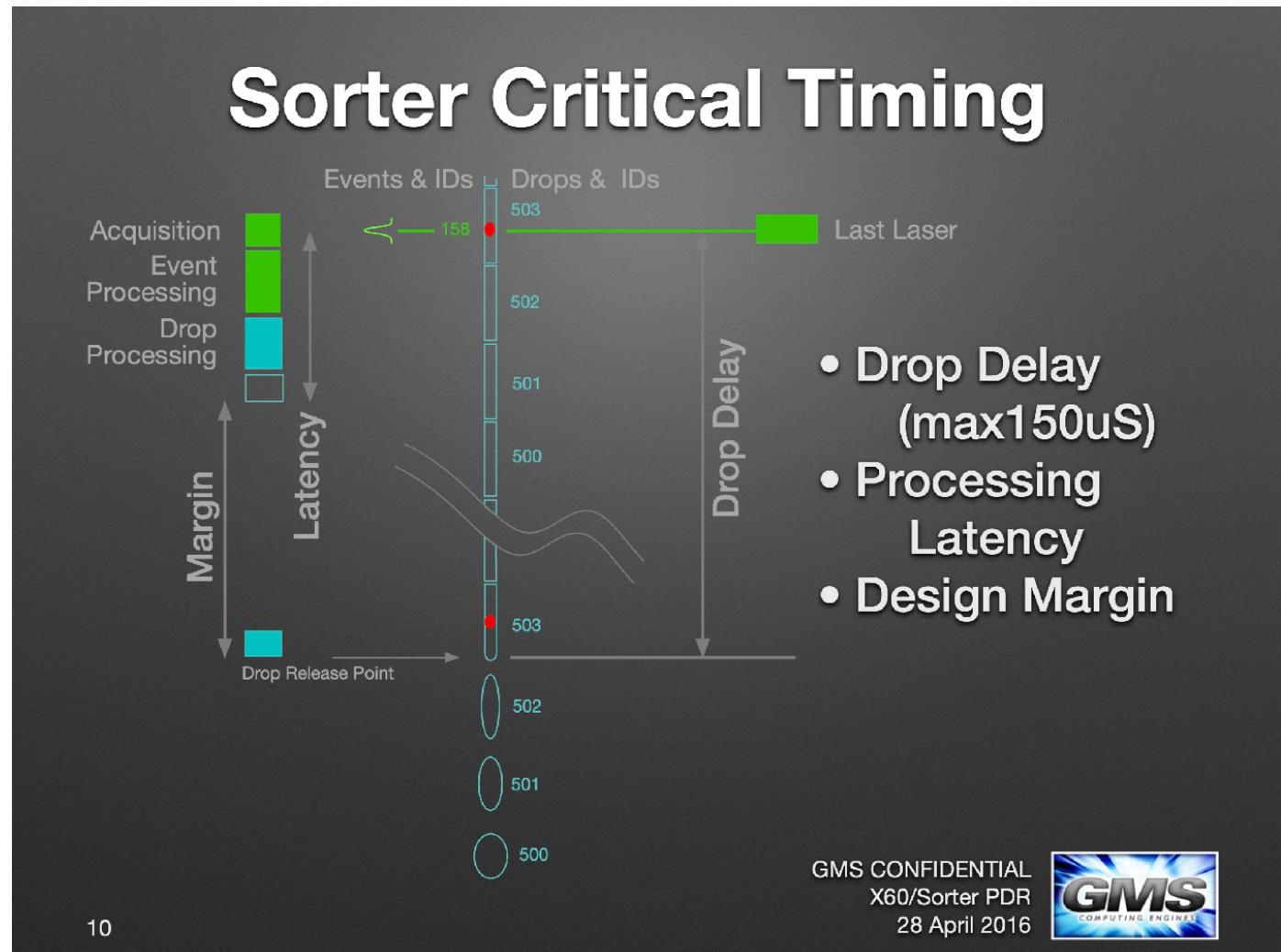
FPGA - Case Study - X60 Cell Sorter

- Not Much Changed
- Expresses Low Risk (even if not)



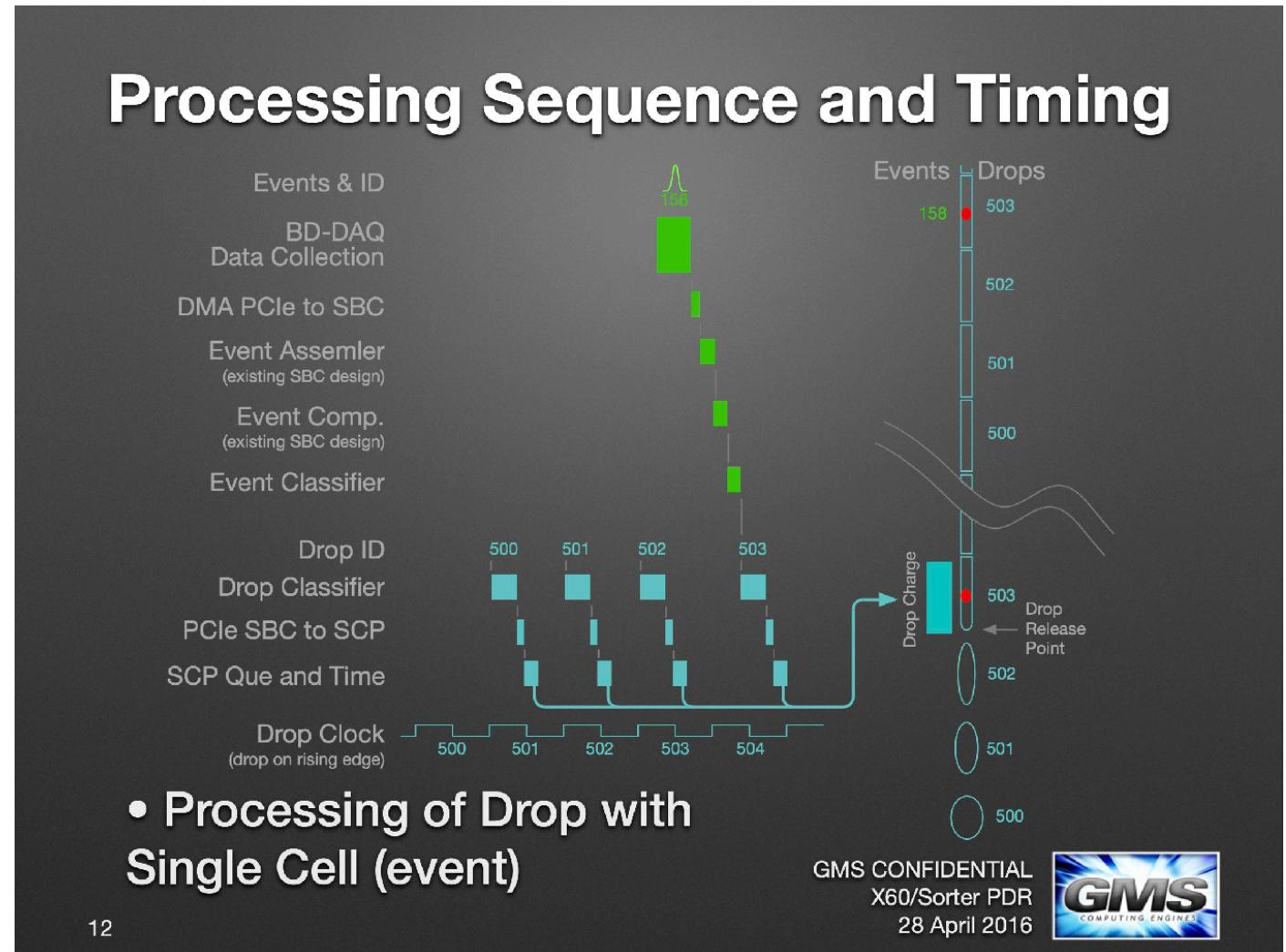
FPGA - Case Study - X60 Cell Sorter

- Start of Process Discussion
- For More Information, Search ‘Cell Cytometer’ or ‘Flow Cytometer’



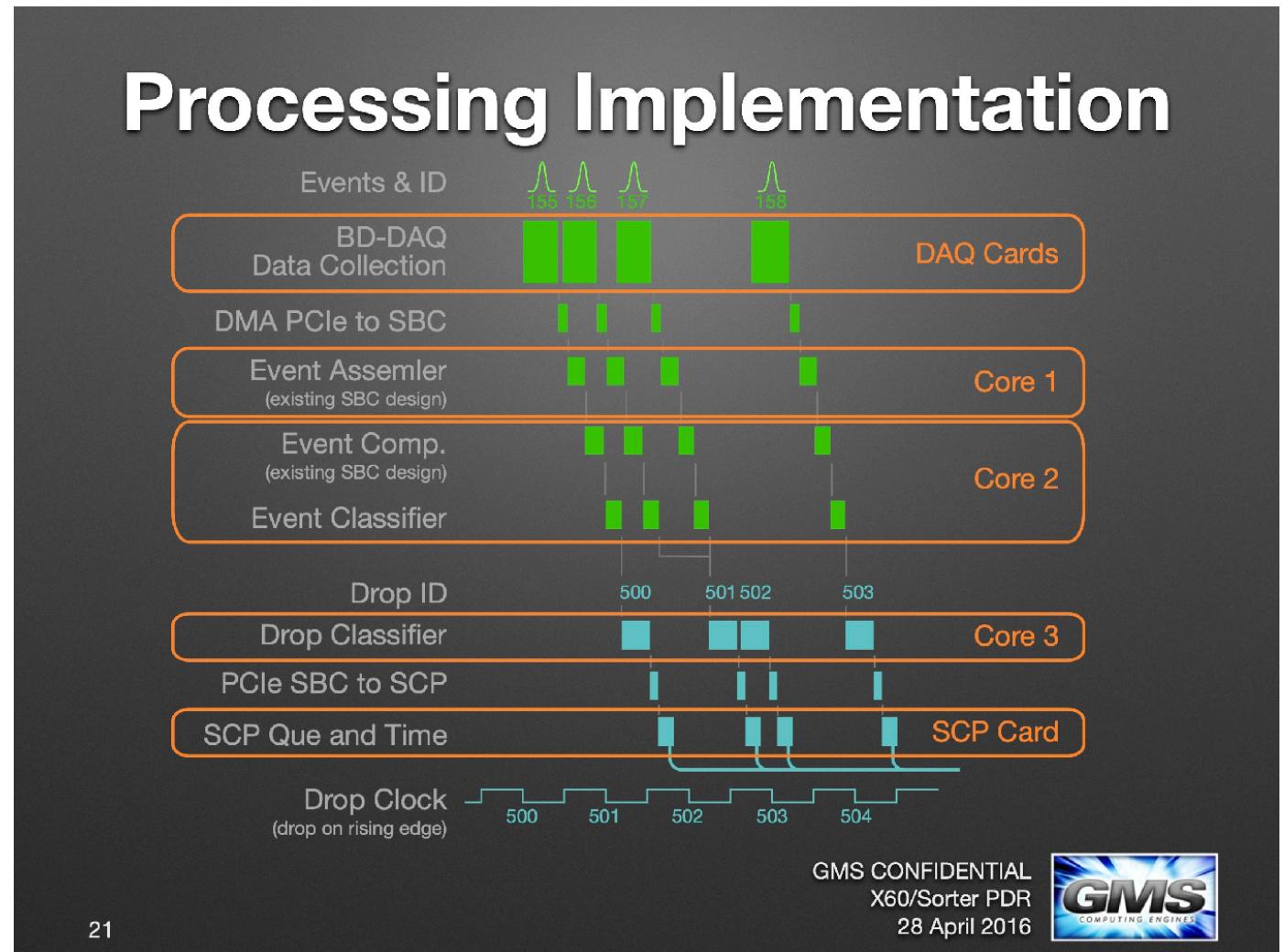
FPGA - Case Study - X60 Cell Sorter

- Introduction of Real Time Sequence and Discrete Processing
- Transitional Drawing to Correlate Hardware to Software Timing



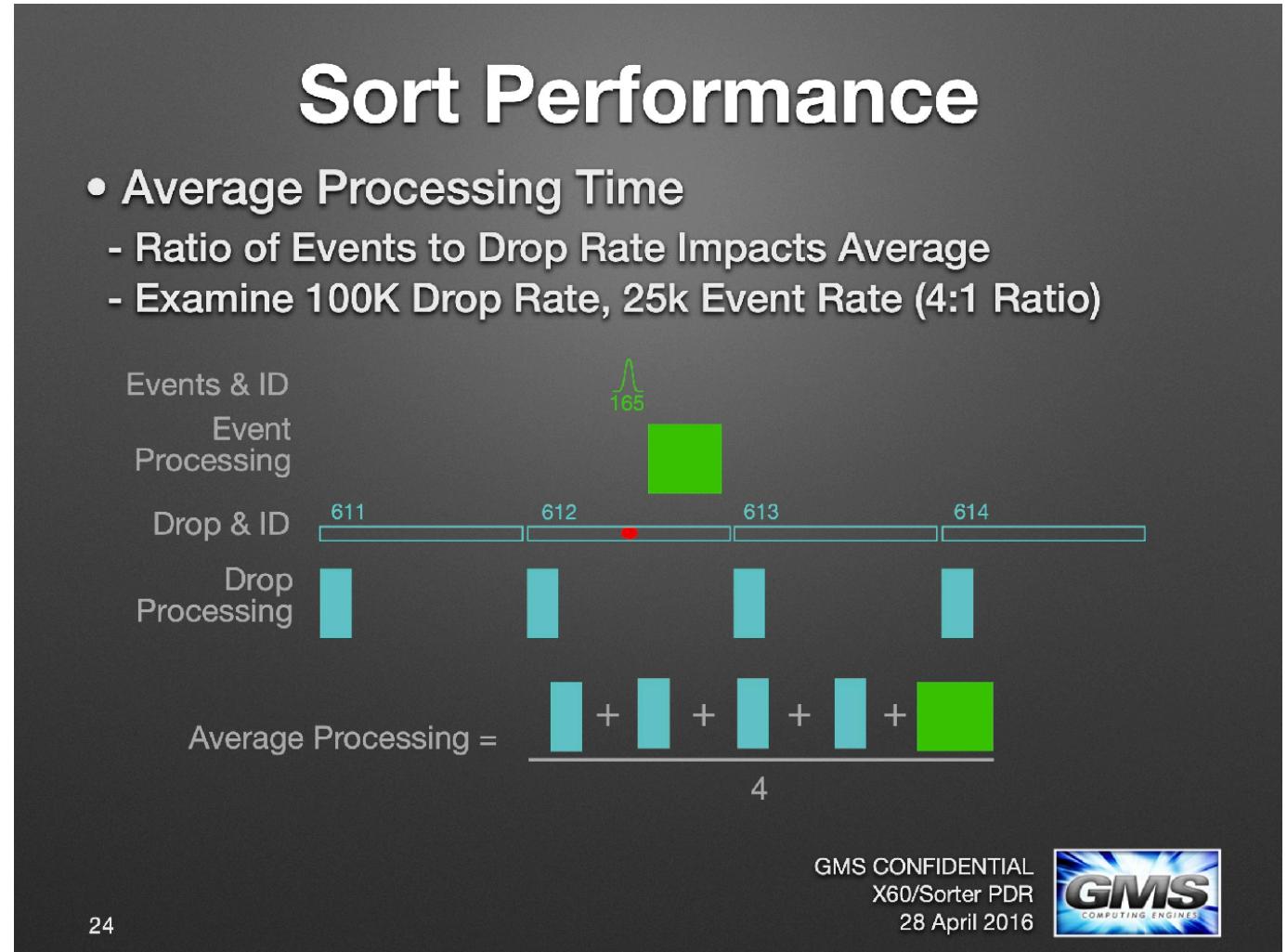
FPGA - Case Study - X60 Cell Sorter

- Introduction of Tasks and Hardware / Core Assignments



FPGA - Case Study - X60 Cell Sorter

- Timeline Analysis - Average
- Typically There are Few Cells Compared to Drops
- Other Charts Show Latency and Worst Case Loading



Lab 12 Preview

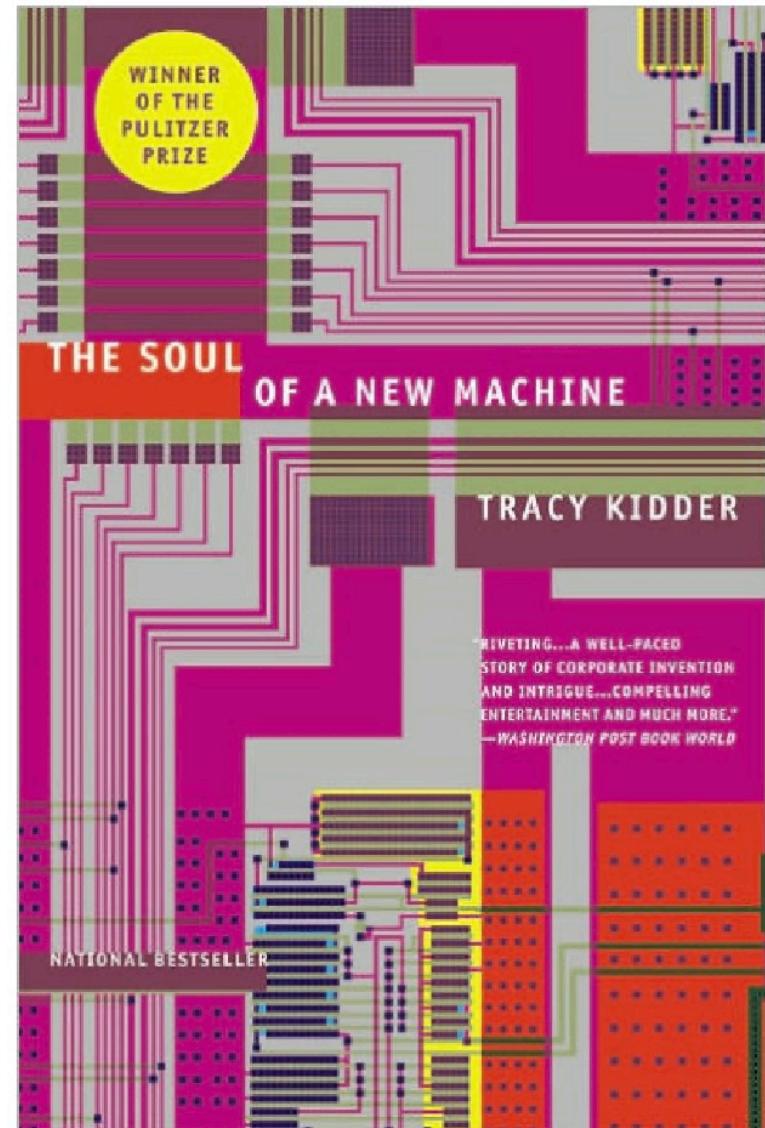
- Use Newest Version of Template with RTOS ✓
 - Improved Partitioning with Functional & Data Privacy ✓
- Incorporate Hardware Input Capture Function
 - Configuration of Input Capture
 - Creation of Interrupt Handler

Look Ahead

- Discussion on Reading
- Discussion on Presentations
- Review of Lab 12
- Fielder's Choice

Assignment - Readings

- The Soul Of A New Machine
 - Chapters 10: The Case of the Missing NAND Gate
 - Send Me Discussion Topics by 10:00 AM on Thursday, November 21, 2024.



Assignment - Additional

- BD-X60-Sorter-PDR-Hardware.pdf
- BD-X60-Sorter-PDR-Software.pdf

Action Items and Discussion

AI#:	Owner	Slide #	Document	Action