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Computer Science

Spring 2025: CSCI 181RT

Real-Time Systems in the Real World

Lecture 6

Thursday, February 6, 2025
Edmunds Hall 105
2:45 PM - 4:00 PM

Professor Jennifer DesCombes

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Agenda

- Go Backs
- Discussion on Reading
- Discussion on Lab
- Quick Review of Interrupts
- More on Interrupts
- Assignment
- Look Ahead
- Action Items

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Go Backs

- General?
- Action Item Status
  - No chart error related action items this time!
  - AI250204-1: malloc vs calloc - OK to Close?

Discussion on Reading

- K & R
  - General Questions on Structures?
  - Passing Structures via Pointers
- Microcode
- PIC32MZ Embedded Connectivity

Discussion on Lab

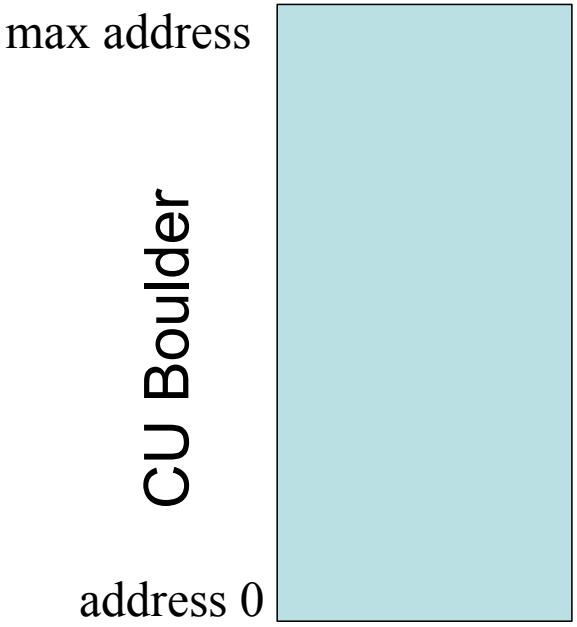
- Oops! Not this time.

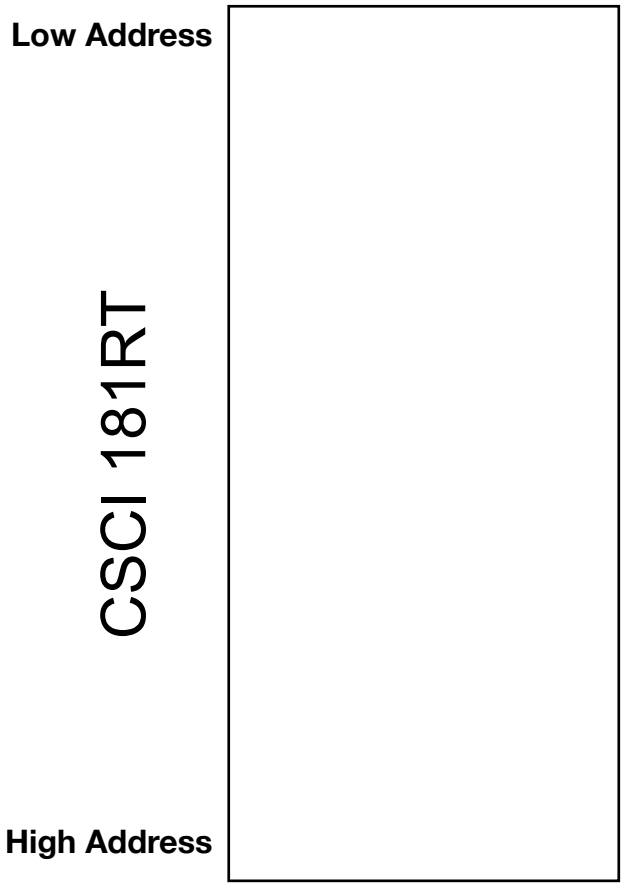
Initial Investigation of Interrupts - Review

- Complexity - Next Level Up from Simple Polling
- Respond to Internal or External Events
  - Internal - Timers, Fault Conditions
  - External - Logic Inputs, Ports, Input Compare, Input Count
- How Do I Stop?
- How Do I Start?
- Hardware and Toolset Awareness

Memory Organization - Another Oops!

- CU Boulder - Low Memory at Bottom
- 181RT - Low Memory at Top
- Incorrect Preference Stated in Prior Lecture





More on Interrupts

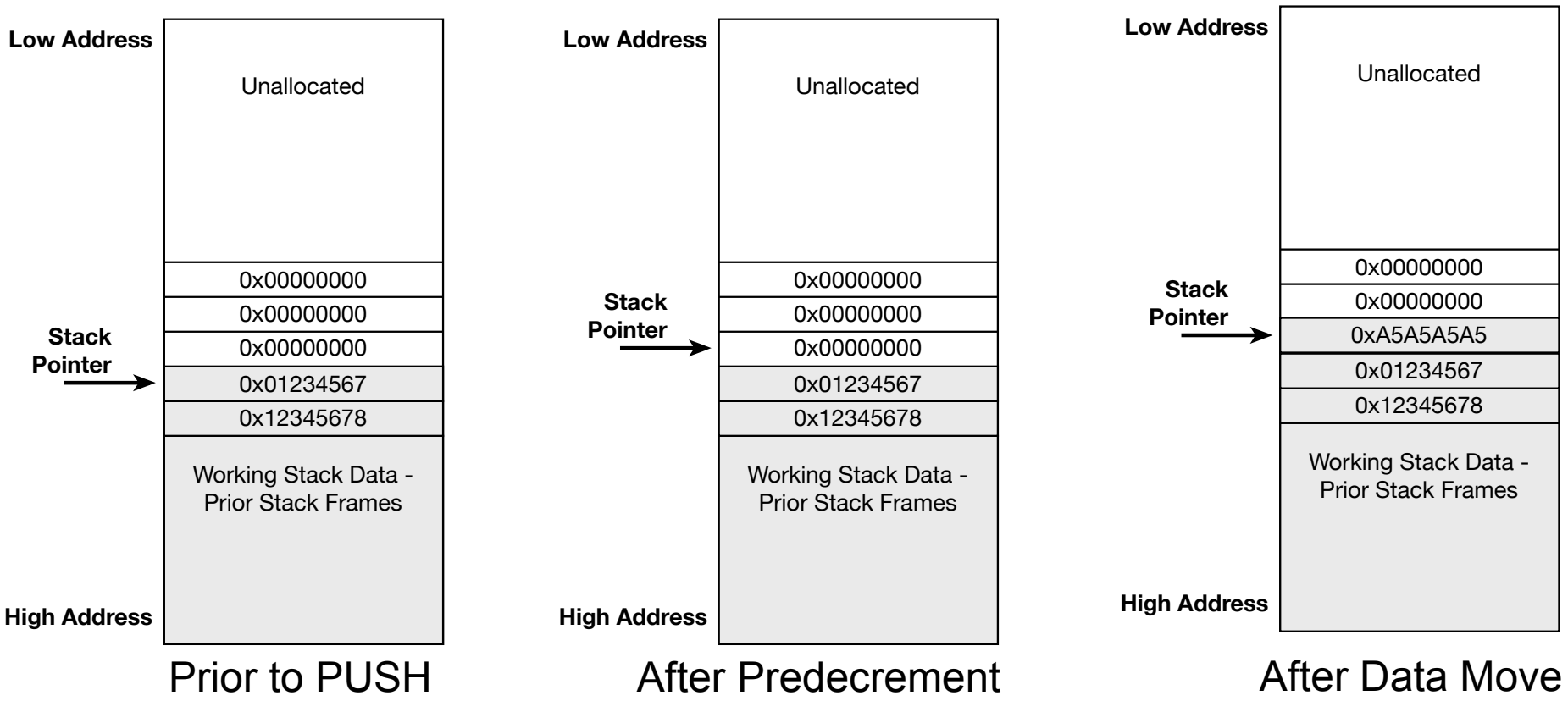
- Terms
- Single Interrupt Stack
- Multiple Nested Interrupts
- Nested Stack Frames
  - User Space
  - Supervisor Space
- So What?

Interrupts - Terms and Definitions

- User Space, User Mode, Others…
- Supervisor Space, Supervisor Mode, Others…
- PUSH - Predecrement and Move Data onto Stack
- POP - Move Data off of Stack and Postincrement
- Other Implementations:
  - POP uses Postincrement
  - PUSH uses Predecrement

Interrupts - PUSH

- PUSH - Predecrement and Move Data onto Stack
- PUSH (SP, 0xA5A5A5A5);



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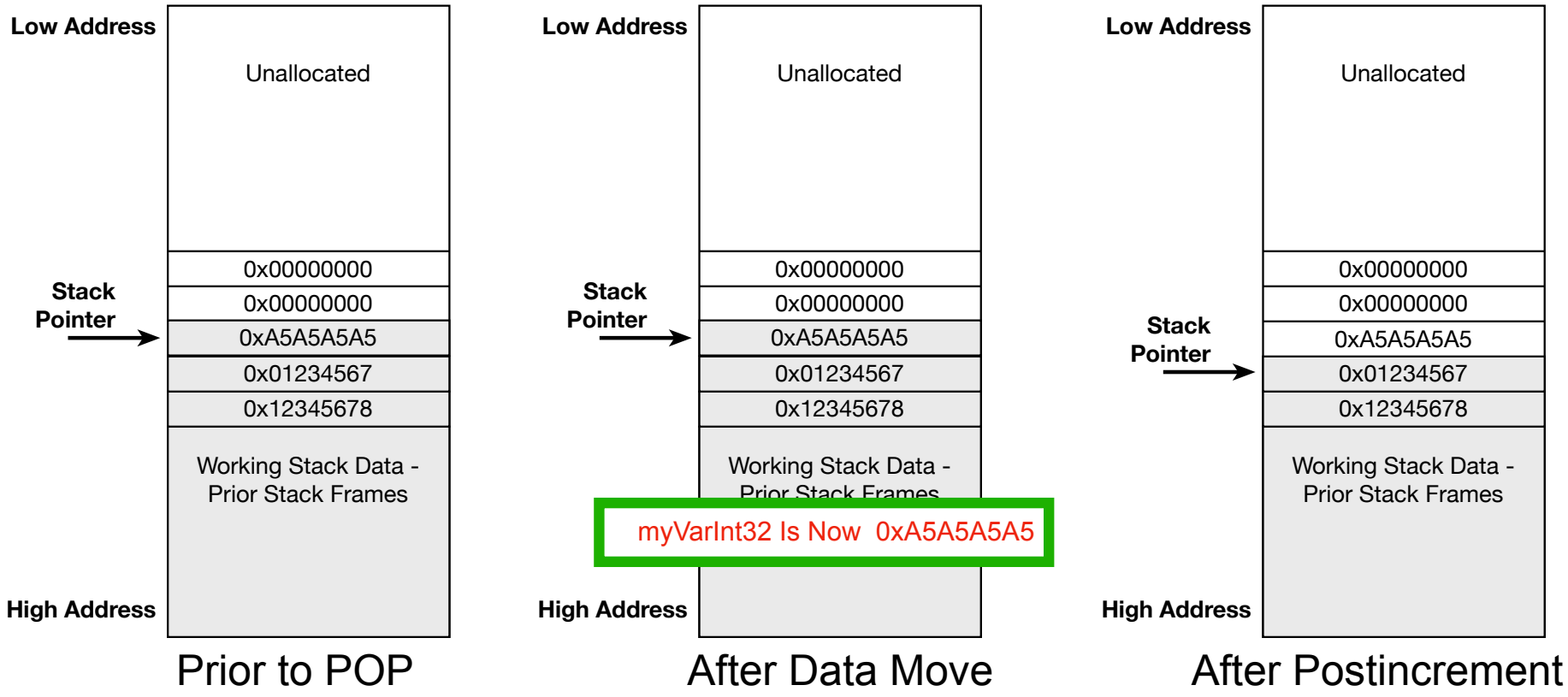
Interrupts - POP

- POP - Move Data off of Stack and Postincrement
- POP (SP, myVarInt32);



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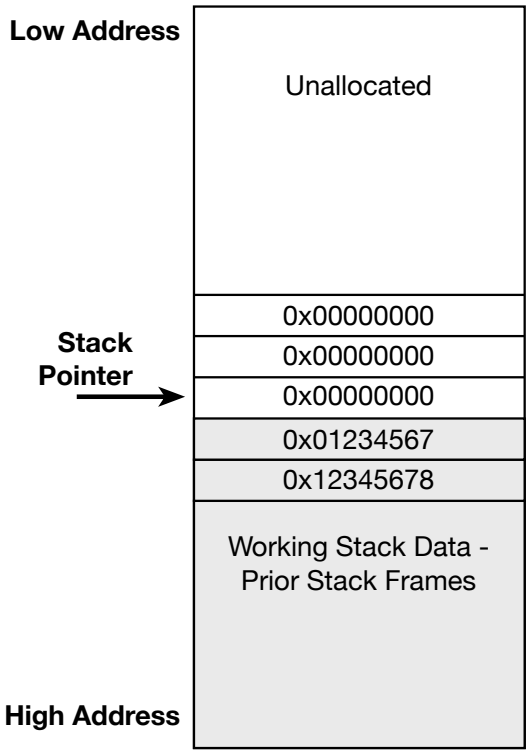
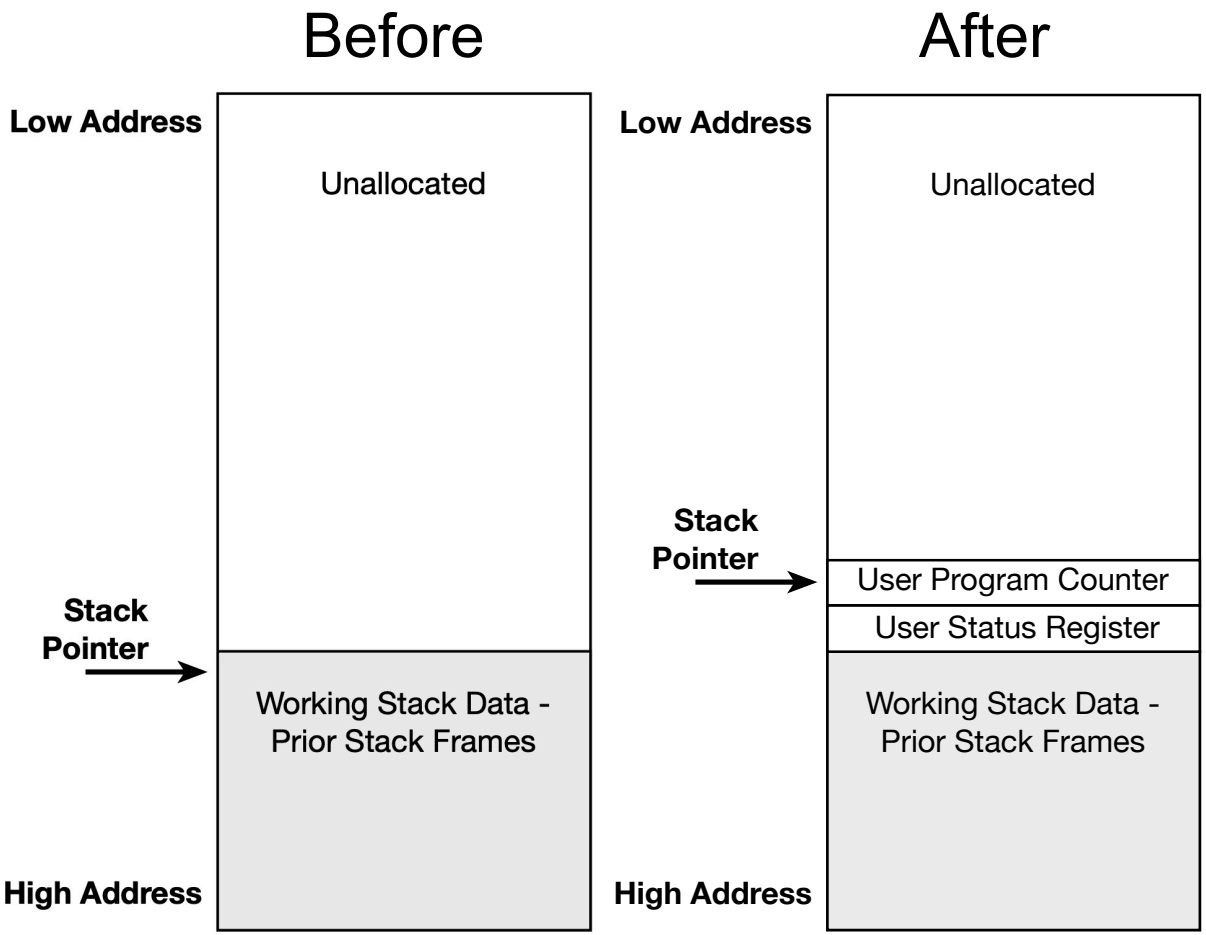
Interrupts - Alternate Stack Configurations

- Stack Pointer Is Maintained at Next Available Location
- PUSH uses Postincrement, POP uses Predecrement



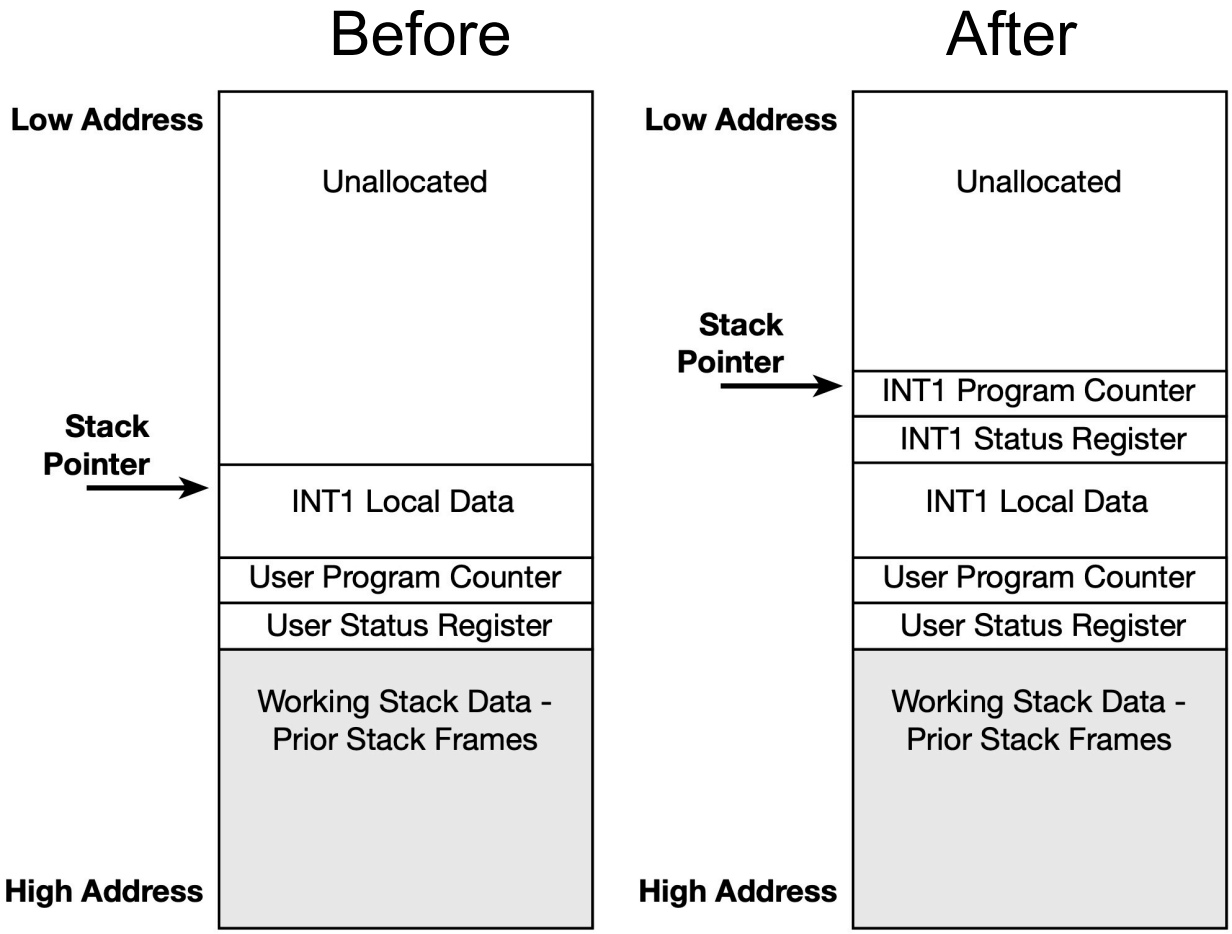
Interrupts - Single Interrupt Stack Frame

- PUSH SR
- PUSH Program Counter
- User Mode Code is Now Interrupted by INT1, Which is Now Running
- INT1 Local Data Routine Data Can Be Placed On Stack



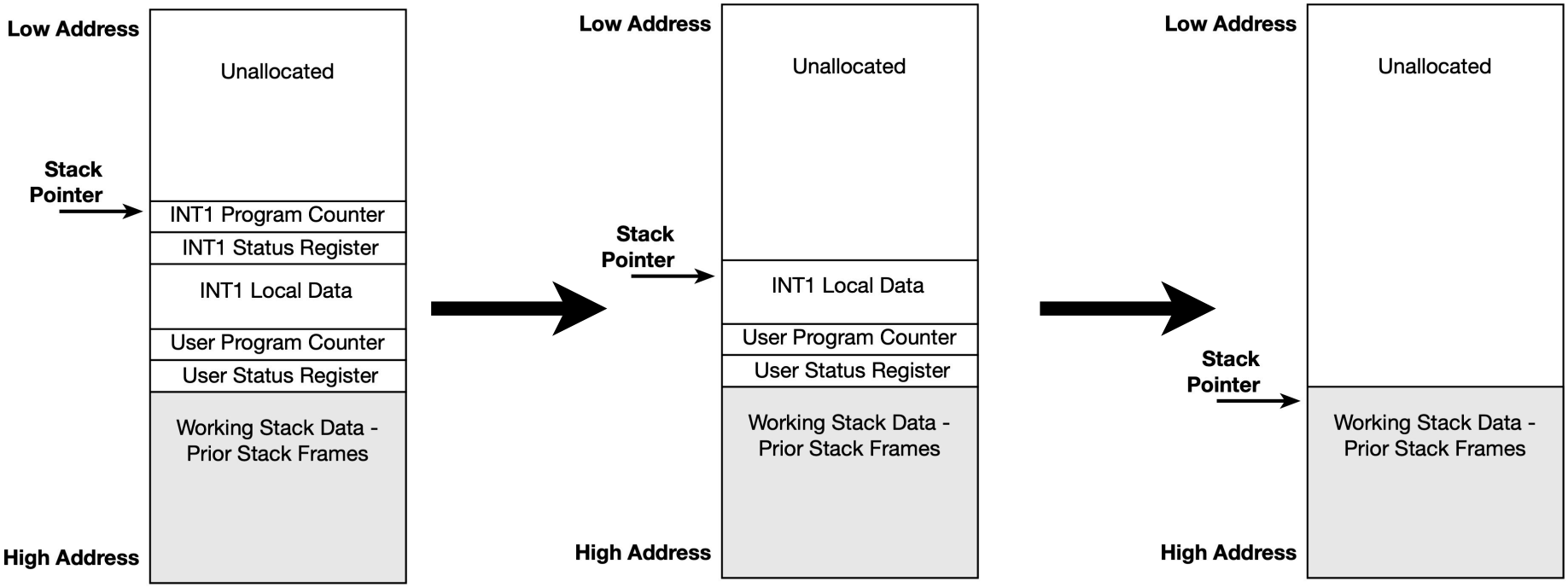
Interrupts - Multiple Nested Stack Frames

- PUSH INT1 SR
- PUSH INT1 Program Counter
- Note INT1 Local Data Storage Space on Stack
- INT1 is Now Interrupted by INT2, Which is Now Running



Interrupts - Unwinding and Returning (RINT)

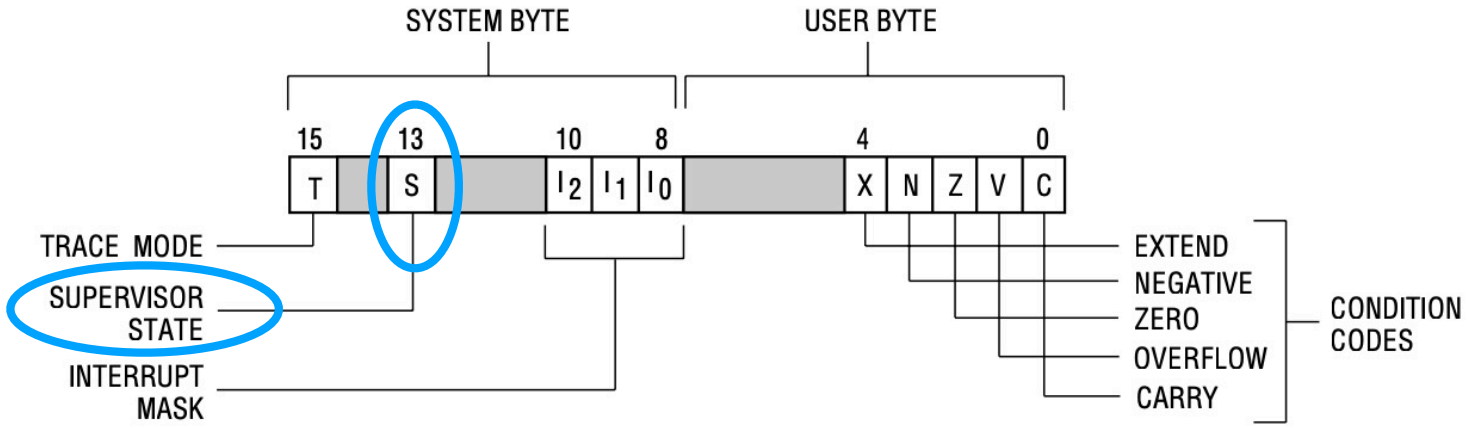
- Use POP to Restore PC and SR
- Compiler Knows How Much Local Data to Purge
- Determine User Mode, from SR, to End Interrupt Processing



Interrupts - Use of SR to Detect User Mode

2.1.3 Status Register

The status register (SR),contains the interrupt mask (eight levels available) and the following condition codes: overflow (V), zero (Z), negative (N), carry (C), and extend (X). Additional status bits indicate that the processor is in the trace (T) mode and/or in the supervisor (S) state (see Figure 2-4). Bits 5, 6, 7, 11, 12, and 14 are undefined and reserved for future expansion



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Interrupts - Variations In Stack Processing

- Various Systems Will Implement Different Techniques
- Single Stack, Supervisor Mode Stack, Multiple Stacks
- Takeaway - They Are All Using The Same Concept

Single Stack Pointer

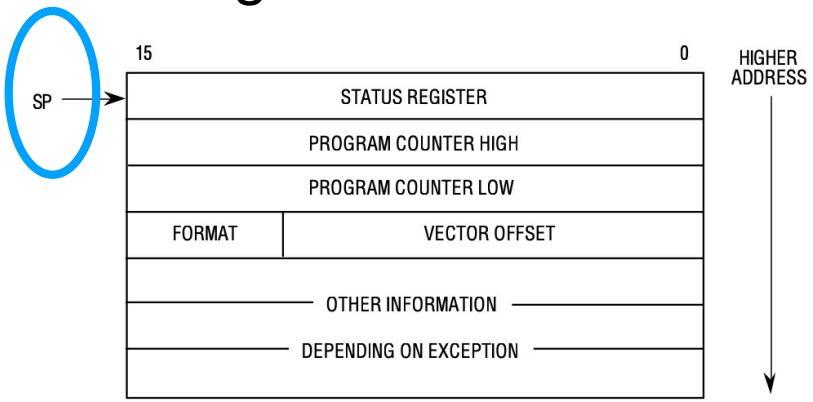

Figure 6-6. MC68010 Stack Frame

Supervisor Stack Pointer

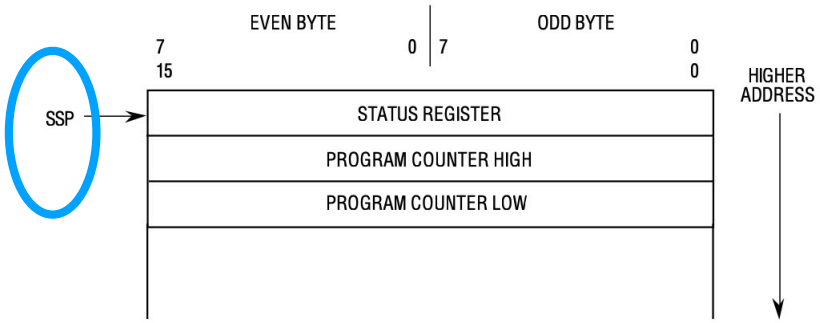

Figure 6-5. Group 1 and 2 Exception Stack Frame (MC68000, MC68HC000, MC68HC001, MC68EC000, and MC68008)

Interrupts - So What?

- Interrupts Interrupt, Process, and End
- Users Code is Interrupted, and Then Resumes
- Determining Transition from Supervisor to User is Critical
  - Interrupts Denote State Changes - Something Happened
  - Is the Proper Task Now Running?
  - Is that Important?

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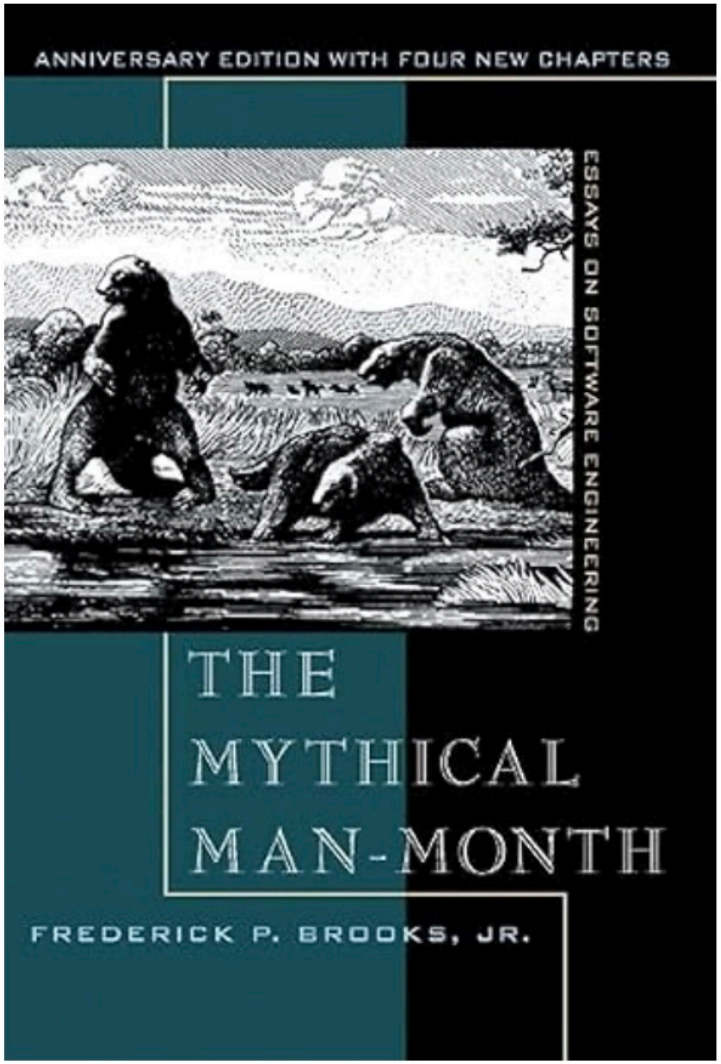
Assignment - Readings

- K&R - Page Confusion??
- K&R - Page 151-241
- Chapter 7: Input and Output
- Scan Chapter 8 & Appendix A

- The Mythical Man-Month
  - All Introductions and Forwards
  - Chapter 1: The Tar Pit



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Look Ahead

- Discussion on Reading
- Initial Discussions of Task Design
- Lab 2 Preview

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Action Items and Discussion

AI#:	Owner	Slide #	Document	Action