CPSC 2610
Lab Assignment 6
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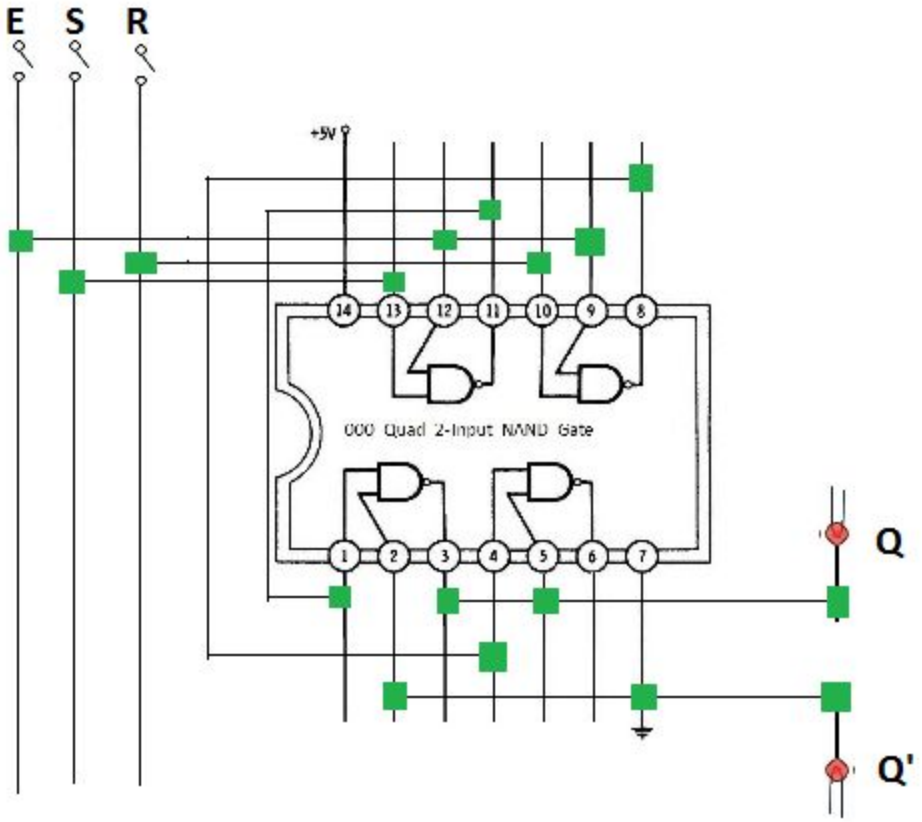
1.

a.

E	S	R	Q	Q+
0	X	X	0	0
0	X	X	1	1
1	0	0	0	0
1	0	0	1	1
1	0	1	0	0
1	0	1	1	0
1	1	0	0	1
1	1	0	1	1
1	1	1	Undetermined	Undetermined

b.

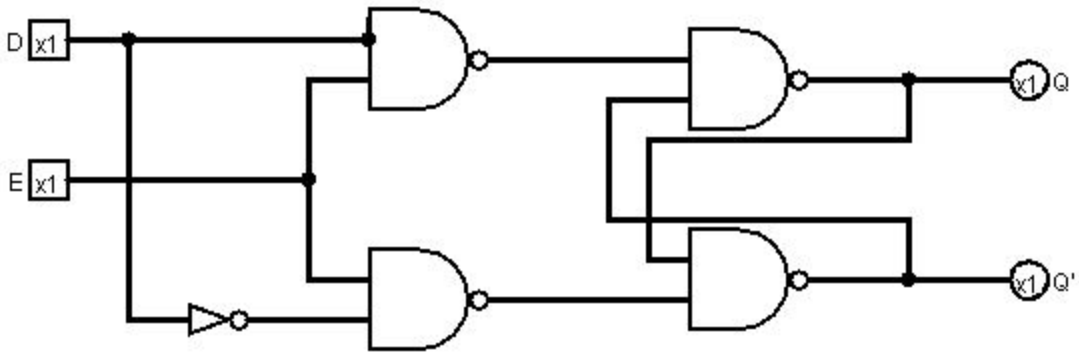


c.

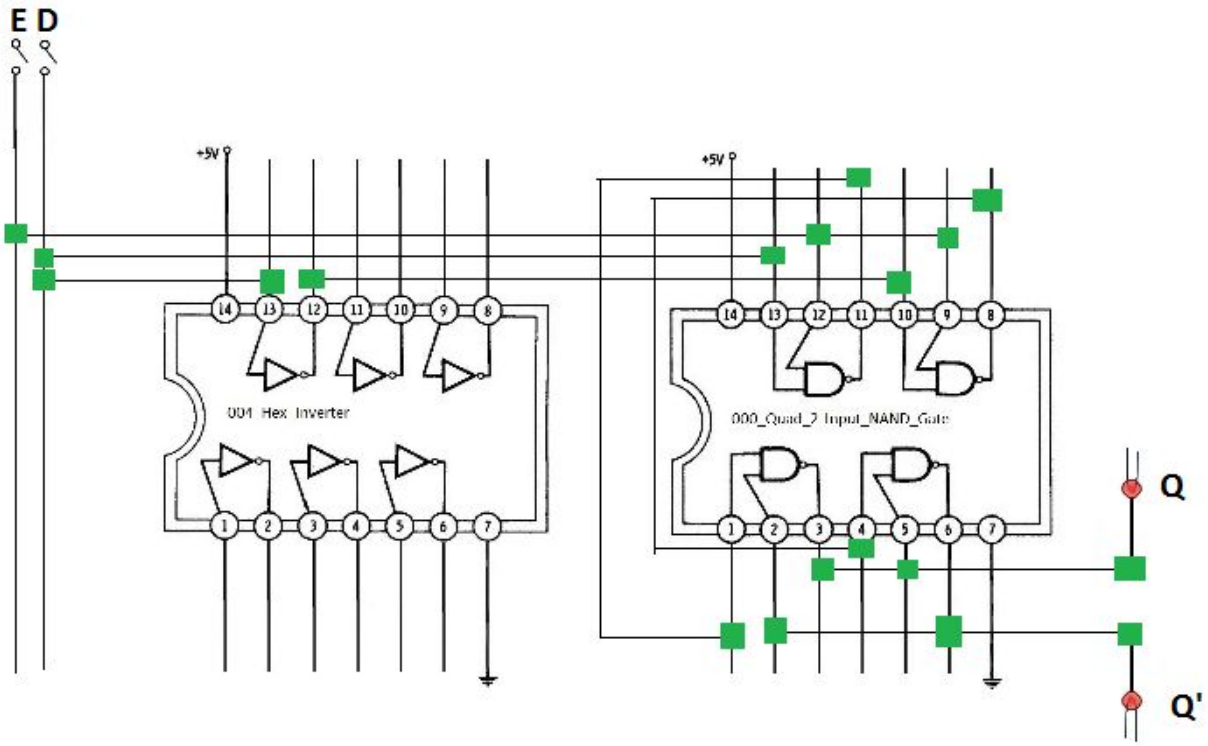
E	S	R	Q	Q+	Actual Behavior	Explanation
0 0 1 1 1 1 1 1 1	X X 0 0 0 0 1 1 1	X X 0 0 1 1 0 0 1	0 1 0 1 0 1 0 1 Undetermined	0 1 0 1 0 0 1 1 Undetermined	0 1 0 1 0 0 1 1 Undetermined	E is 0 so Q stays the same E is 1 and no inputs so Q stays the same

2.

a.



b.



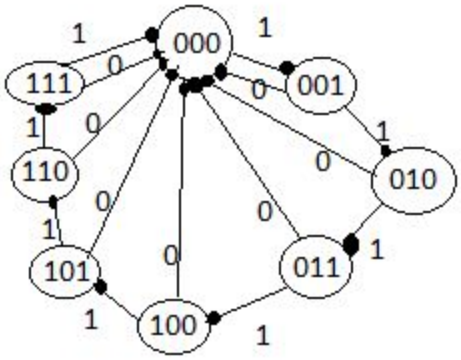
c. With the D-latch, input Enable acts as reset, and D act as both reset and set. When Enable is On, Q is set to 0, and when

3.

a.

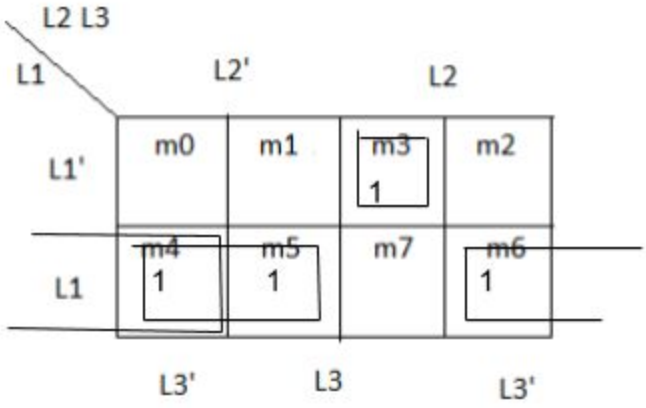
L1	L2	L3	R	L1+	L2+	L3+
X	X	X	0	0	0	0
0	0	0	1	0	0	1
0	0	1	1	0	1	0
0	1	0	1	0	1	1
0	1	1	1	1	0	0
1	0	0	1	1	0	1
1	0	1	1	1	1	0
1	1	0	1	1	1	1
1	1	1	1	0	0	0

b.



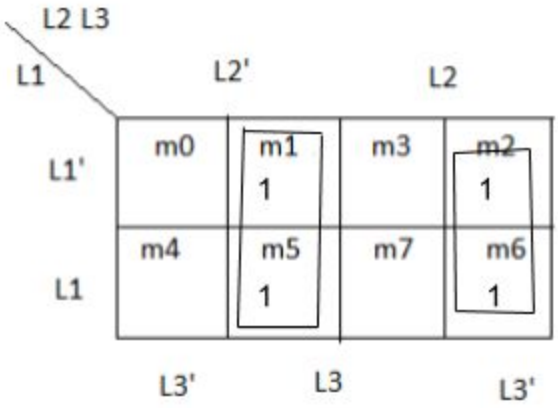
c.

L1+ = Σm(3, 4, 5, 6)



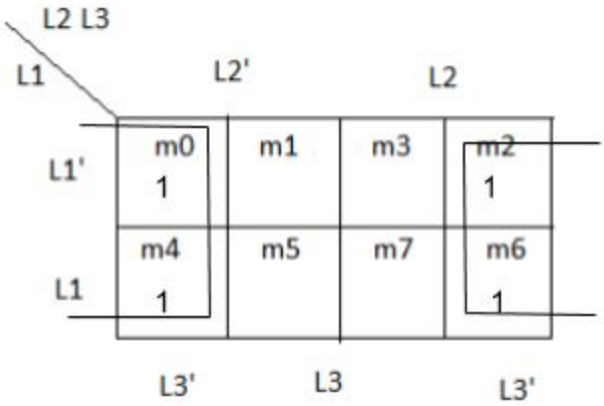
L1+ = L1.L2’ + L1.L3’ + L1’.L2.L3

L2+ = Σm(1, 2, 5, 6)



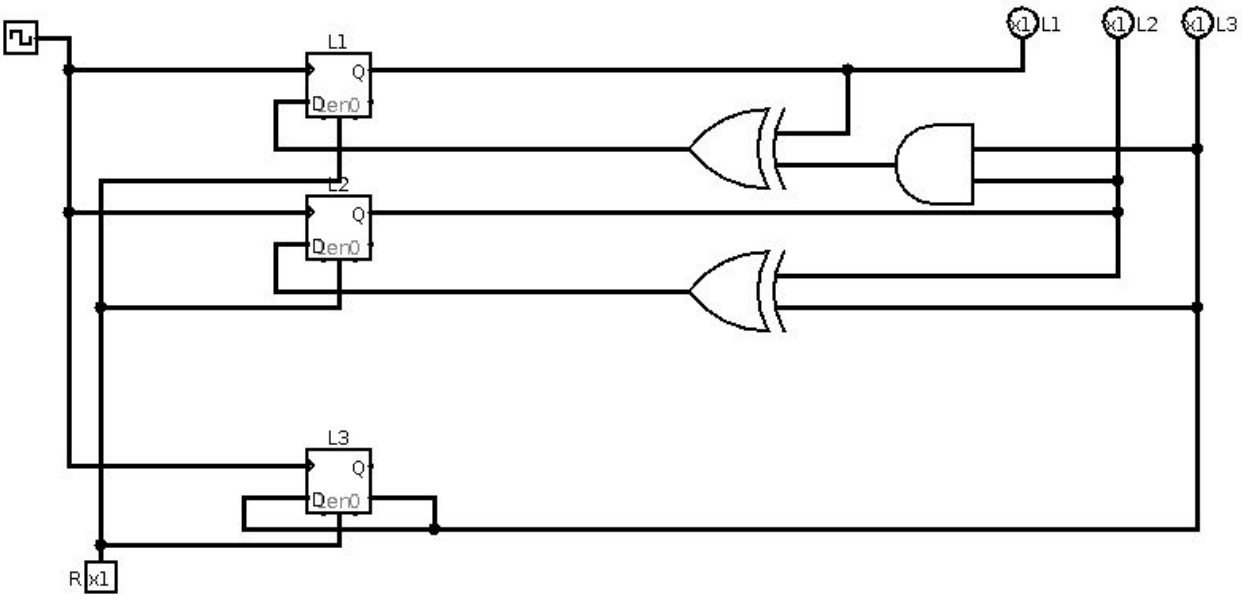
L2+ = L2’.L3 + L2.L3’

L3+ = Σm(0, 2, 4, 6)

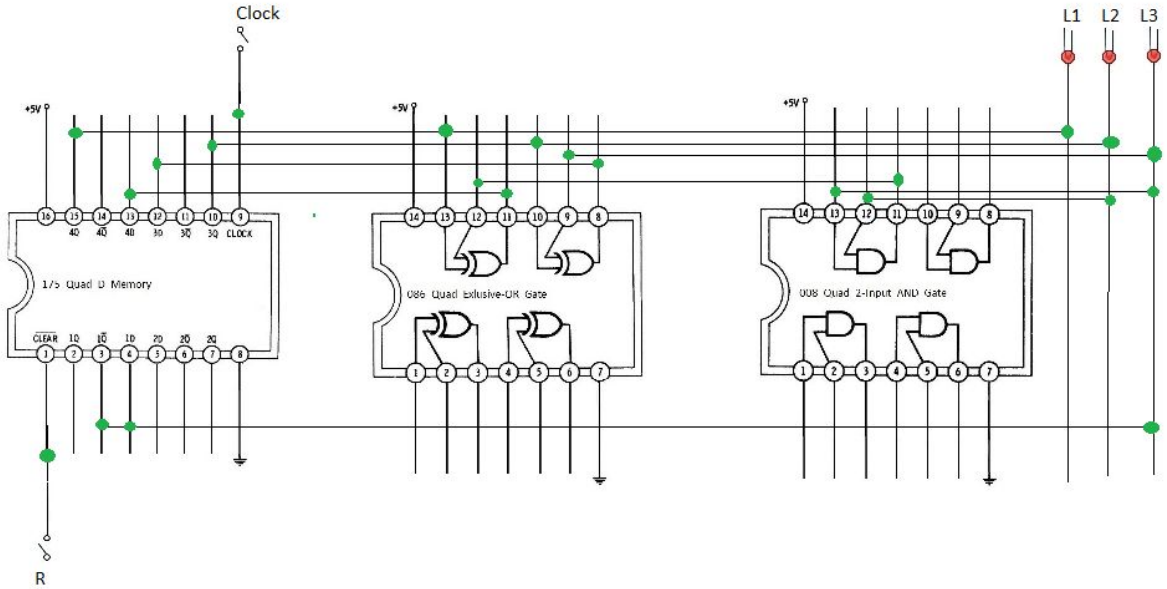


L3+ = L3’

d.

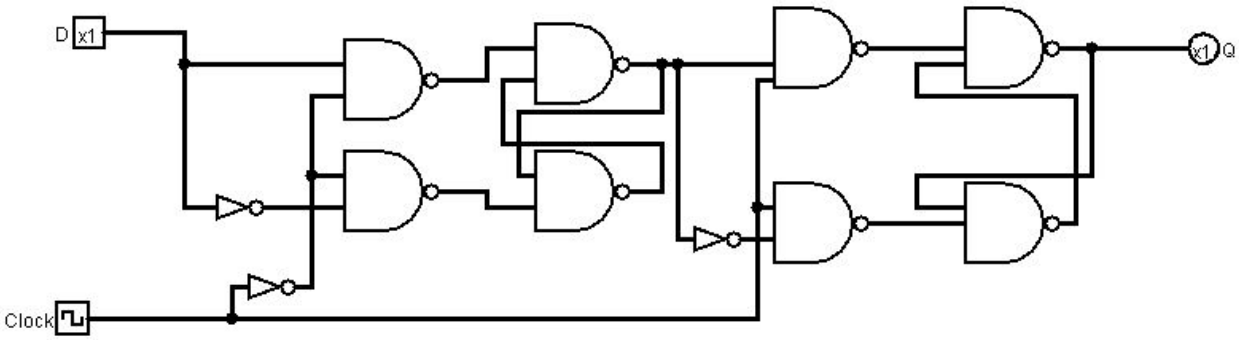

L1
Q
Den0
L2
Q
Den0
L3
Q
Den0
R
x1
x1 L1
x1 L2
x1 L3

e.

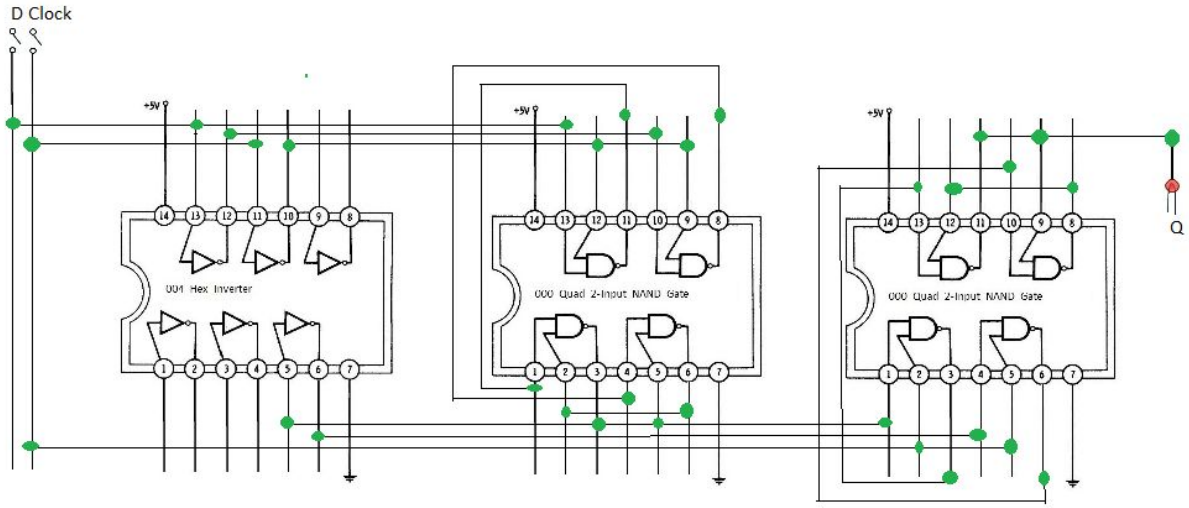

Clock
L1
L2
L3
+5V
175 Quad D Memory
CLEAR
CLOCK
086 Quad Exlusive-OR Gate
008 Quad 2-Input AND Gate
R

4.

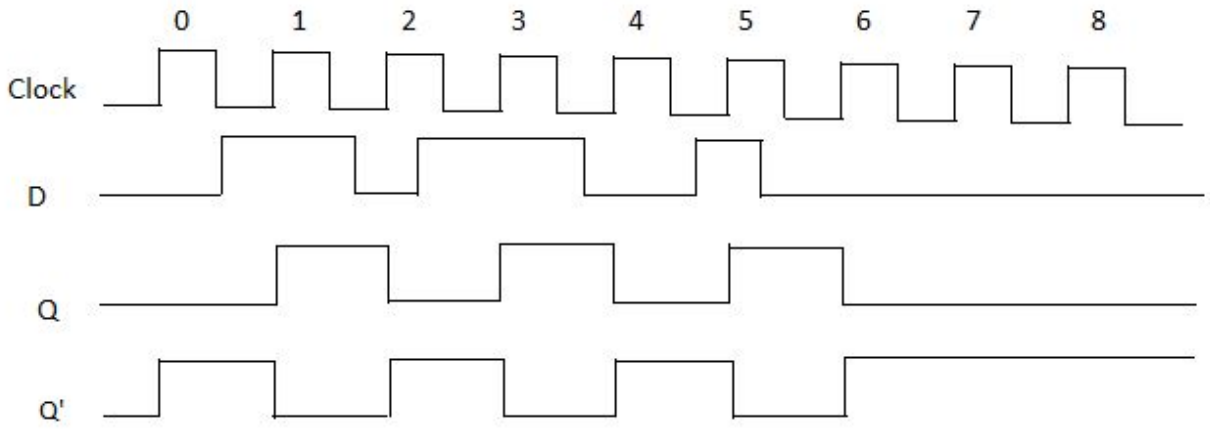
a.



b.



c.



d. Basically, when D is high, then Q is high, and Q' is low. The change in Q and Q' always occurs at the next positive edge (when the clock goes from low to high) of the clock sequence.

- At the beginning, Q’ would change to high at positive edge clock 0 because D was low at that point. Q would stay the same as D
- D went from low to high at low point between clock 0 and 1, so Q would go from low to high at the next positive edge, which was the beginning of 1.
- When D went from high to low at the middle of clock 1 and 2, Q would change from high to low at the positive edge at clock 2. Q’ would also change from low to high at the same time as Q.
- The rest would follow the same principles