

# CprE 3810, Computer Organization and Assembly Level Programming

## Team Contract – Project Part 1

Project Teams Group: D\_05

Team Members: James Gaul

Andrew Eslick

*Discuss the following aspects of teamwork with your team – make sure to get input from each member. Write down your team's consensus for each of the bolded headings. Italicized text contains instructions and examples and should be deleted once you've read it. Please see the example contract for rough length expectations.*

**Course Goals:** *List and acknowledge the goals of your individual team members.*

*Examples may include:*

- *Get an A (or at least as high a score as possible) on this project.*
- *Have a processor that works as reliably as possible, to ensure a solid foundation for future project portions.*

### **Team Expectations:**

- **Conduct:** *What are the expectations for personal conduct of group members?*
  - *Work reliably, remain polite and civil*
- **Communication:** *What is the best mode of communication for the group? How often should communication occur? How fast should a response be expected?*
  - *Text Messages, we will respond within 24 hours, barring emergency situations*
- **Group conventions:** *Naming conventions? Compilation and simulation methodology? Testbench strategies? Do file usage? Version control strategies? Commenting standards?*
  - *s\_ in front of signals, i\_ for input, o\_ for output*
  - *compilation and simulation will be placed in separate .do files, with a .go file to link the two*
  - *Do files to ensure readable names and values*
  - *We will use GitHub for version control*
- **Meetings:** *Given the significant portion of the course that the lab covers, it is expected that your team will spend more time working on the labs than in your scheduled lab sections. How will your group expect to handle this? Please include at least two additional times outside of lab that your team can meet (preferably in-person). Examples of other issues to consider include:*
  - *We can meet on Mondays, Fridays, Weekends, and some evenings.*

- o In the evenings, online works better for James.
- **Peer Evaluation Criteria:** Please create a brief criteria for how effort and contribution are defined. Note that teams with **vastly** divergent scores may require a meeting with course instructor and result in different grades for different group members. Teams with reasonably equitable scores will receive the same grade.
  - o Design – design is easy to follow, structural for everything beyond basic components, avoids process statements unless absolutely necessary
  - o Tests – Tests are easy to read and understand, check components as comprehensively as possible, provide easily

**Role Responsibilities:** Complete the following planning table. Each lab part should be the responsibility of one team member. Also make sure that no one team member is the lead on both the design and test aspects of a single lab part. These guidelines aid in all students having a complete view of the lab. Plan for an anticipated deadline (read the lab manual and ask your TAs for assistance in setting up a good timeline). Note that the non-lead is encouraged to participate and support the lead wherever possible, increasing both the quality of the lab part and each team member's knowledge.

Lab Part	Estimated Time	Design		Test	
		Lead	Deadline	Lead	Deadline
High-level design	1 hr	Andrew	8/8/25	James	8/20/25
Test programs	4 hr	James	8/20/25	Andrew	8/27/25
Control logic	2 hr	James	8/15/25	<b>Andrew</b>	8/20/25
Fetch logic	3 hr	Andrew	8/15/25	James	8/20/25
Barrel shifter	2 hr	James	8/15/25	<b>Andrew</b>	8/20/25
ALU integration + Misc updates	2 hr	Andrew	8/15/25	James	8/20/25
High-level integration	4 hr	James	8/20/25	Andrew	8/25/25
Synthesis (human effort)	1.5 hr	Andrew	8/20/25	James	8/25/25

*Estimated Time is given as a **very rough** guide for even distribution of tasks assuming you've already read through the lab document and have the prerequisite knowledge. Depending on your group's skill and prerequisite knowledge, some tasks may take disproportionately long or short. For your future planning, track this – for future prelabs you will be asked to note why past tasks took longer than expected and how you might avoid such issues in the future.*

**Integrity of Work:** Do not delete the following. We agree that the work we provide to other team members and ultimately submit for a grade is a direct result of our own work as described in the course syllabus. Specifically, we will generate all VHDL code ourselves and not copy VHDL code from online sources, other groups, book companion material, or past student projects to which anyone outside of my team has contributed.

**Student Signature** James Gaul **Date** 8/1/25

**Student Signature** Andy Eslick **Date** 8/1/25