

Instruction	Opcode (Binary)	Funct3 (Binary)	ct7 or Imm (Bin:	ALUSrc	Mem_We	Jump
add	"0110011"	"000"	"0000000"	0	0	0
sub	"0110011"	"000"	"0100000"	0	0	0
xor	"0110011"	"100"	"0000000"	0	0	0
or	"0110011"	"110"	"0000000"	0	0	0
and	"0110011"	"110"	"0000000"	0	0	0
sll	"0110011"	"001"	"0000000"	0	0	0
srl	"0110011"	"101"	"0000000"	0	0	0
sra	"0110011"	"101"	"0100000"	0	0	0
slt	"0110011"	"010"	"0000000"	0	0	0
sltu	"0110011"	"011"	"0000000"	0	0	0
addi	"0010011"	"000"		1	0	0
xori	"0010011"	"100"		1	0	0
ori	"0010011"	"110"		1	0	0
andi	"0010011"	"110"		1	0	0
slli	"0010011"	"001"		1	0	0
srli	"0010011"	"101"		1	0	0
srai	"0010011"	"101"		1	0	0
slti	"0010011"	"010"		1	0	0
sltiu	"0010011"	"011"		1	0	0
lb	"0000011"	"000"		1	0	0
lh	"0000011"	"001"		1	0	0
lw	"0000011"	"010"		1	0	0
lbu	"0000011"	"100"		1	0	0
lhu	"0000011"	"101"		1	0	0
sb	"0100011"	"000"		1	1	0
sh	"0100011"	"001"		1	1	0
sw	"0100011"	"010"		1	1	0
beq	"1100011"	"000"		0	0	0
bne	"1100011"	"001"		0	0	0
blt	"1100011"	"100"		0	0	0
bge	"1100011"	"101"		0	0	0
bltu	"1100011"	"110"		0	0	0
bgeu	"1100011"	"110"		0	0	0
jal	"1101111"			1	0	1
jalr	"1100111"	"000"		1	0	1
lui	"0110111"			1	0	0
auipc	"0010111"			1	0	0
ecall	"1110011"	"000"		1	0	0
ebreak	"1110011"	"000"		1	0	0
Halt	"1110011"			1	0	0

Control Signals					
MemToReg	Reg_WE	Branch	HaltProg	PCOFFSET	ModuleSel
0	1	0	0	0	"00"
0	1	0	0	0	"00"
0	1	0	0	0	"01"
0	1	0	0	0	"01"
0	1	0	0	0	"01"
0	1	0	0	0	"10"
0	1	0	0	0	"10"
0	1	0	0	0	"10"
0	1	0	0	0	"11"
0	1	0	0	0	"11"
0	1	0	0	0	"00"
0	1	0	0	0	"01"
0	1	0	0	0	"01"
0	1	0	0	0	"01"
0	1	0	0	0	"10"
0	1	0	0	0	"10"
0	1	0	0	0	"10"
0	1	0	0	0	"11"
0	1	0	0	0	"11"
1	1	0	0	0	"00"
1	1	0	0	0	"00"
1	1	0	0	0	"00"
1	1	0	0	0	"00"
1	1	0	0	0	"00"
0	0	0	0	0	"00"
0	0	0	0	0	"00"
0	0	0	0	0	"00"
0	0	1	0	0	x
0	0	1	0	0	x
0	0	1	0	0	x
0	0	1	0	0	x
0	0	1	0	0	x
0	0	1	0	0	x
0	1	0	0	0	"00"
0	1	0	0	1	"00"
0	1	0	0	0	"00"
0	1	0	0	0	"00"
0	0	0	0	0	x
0	0	0	0	0	x
0	0	0	1	0	x

