USB PD and other multi-fast charging protocol receiving chip CH224

Chinese
manual
version: 1G

http://wch.cn

1. summarize

CH224 single chip integrates USB PD and other fast charging protocols, supports PD3.0/2.0, BC1.2 and other boost fast charging protocols, automatically detects VCONN and simulates the E-Mark chip, supports up to 100W power, built-in PD communication module, high integration and streamlined peripherals. Integrated output voltage detection function, and provide over-temperature, over-voltage protection and other functions. Can be widely used in various electronic devices to expand the high power input such as wireless chargers, electric toothbrushes, rechargeable shavers, lithium battery power tools and other applications.

2. Functional Features

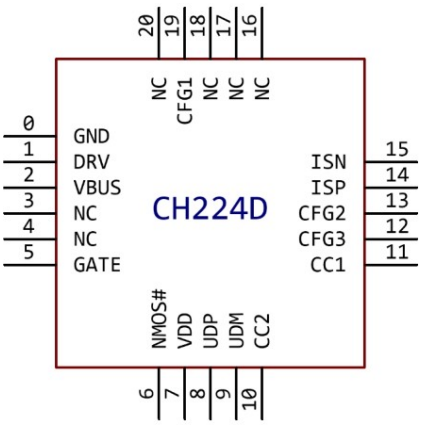
- Supports 4V to 22V input voltage
- Support PD3.0/2.0, BC1.2 and other fast charging protocols.
- Supports USB Type-C PD, supports forward and reverse plug detection and automatic switching
- Supports E-Mark emulation, auto-detection of VCONN, and PD requests for 100W of power
- The request voltage can be dynamically adjusted in a number of ways
- High single-chip integration, streamlined peripherals, low cost
- Built-in overvoltage protection module OVA, over-temperature protection module OTA

3. Applications

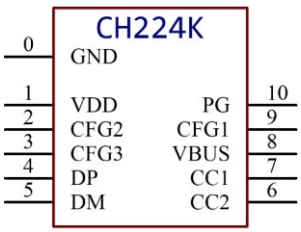
- wireless charger
- Laptop Charging Cable
- Lithium battery small appliances
- Lithium battery power tools
- Mobile Power

4. pinout

4.1. CH224 Package Pin Arrangement



QFN20-3*3



ESSOP-10

SOT23-6L

4.2. CH221K Pin Function Description

pin number	Pin Name	typology	Pin Description
1	VDD	power supply	Operating power input, external 1uF decoupling capacitor, series resistor to VBUS
2	GND	power supply	Operating power supply common ground
3	PG	open-drain output	Default Power Good indication, active low, customizable function
4,5	CC1, CC2	bi-directionality	Type-C CC Bus
6	CFG	analog input	Power Gear Configuration Input

4.3. CH224K Pin Function Description

pin number	Pin Name	typology	Pin Description
0	GND	power supply	Common Ground, Heat Sink
1	VDD	electric power source	Operating power input, external 1uF decoupling capacitor, series resistor to VBUS
4,5	DP, DM	bi-directionality	USB bus
6,7	CC1, CC2	bi-directionality	Type-C CC Bus
2,3,9	CFG1, CFG2. CFG3	analog input	Power Gear Configuration Input
8	VBUS	analog input	Voltage detection input, requires series resistor to external input VBUS
10	PG	open-drain output	Default Power Good indication, active low, customizable function

4.4. CH224D Pin Function Description

pin number CH224D	Pin Name	typology	Pin Description
0	GND	electric power source	Common Ground, Heat Sink
2	VBUS	electric power source	Operating power input
7	VDD	electric power source	Internal regulator output with external 1uF decoupling capacitor
8, 9	DP, DM	bi-directionality	USB bus
10, 11	CC1, CC2	bi-directionality	Type-C CC Bus
19, 13, 12	CFG1~3	importation	CFG1 is an analog input, CFG2, 3 are digital inputs with built-in pull-downs.
1	DRV	analog output	Weak drive output for driving configuration resistors
14, 15	ISP, ISN	differential input	For detecting operating current, customized function
5	GATE	high voltage output	For driving high-side power path NMOS, customized features
6	NMOS#	digital input	GATE pin drive NMOS enable, active low

5. Functional Description

5.1. summarize

CH224 is a protocol power receiving end IC that supports PD3.0/2.0, BC1.2 and other boost fast charging protocol inputs. It supports the request of voltage in the range of 4 to 22V and can dynamically configure the prioritized requested voltage slot in various ways.

CH221K only supports PD3.0/2.0 protocol.

CH224K/CH224D provides single resistor configuration mode and level configuration mode.CH221K provides single resistor configuration mode only.

5.2. CH224K/CH224D Voltage gear configuration

5.2.1 Single Resistor Configuration

Suitable for applications where different request voltages can be realized by modifying the resistor resistance value for the same PCB.

CFG1 to GND connection resistor, different resistance value corresponds to different voltage request gear. The CFG2 and CFG3 pins can be left open when using the single resistor configuration method. The resistor-requested voltage comparison table is as follows.

Resistance on CFG1	Requested Voltage
6.8K Ω	9V
24K Ω	12V
56K Ω	15V
NC	20V

5.2.2 Level Configuration

Suitable for applications where the MCU dynamically adjusts the requested voltage, or where the PCB trace has a fixed requested voltage.

CFG1, CFG2, and CFG3 are connected directly to the IO ports of the external MCU or directly to the VDD/GND pins of the CH224K/CH224D chips to configure the request voltage using the levels. The truth table is as follows.

CFG1	CFG2	CFG3	Requested Voltage
1	-	-	5V
0	0	0	9V
0	0	1	12V
0	1	1	15V
0	1	0	20V

When using the level configuration method, pay attention to the IO port voltage used and the default state.

The CFG2/CFG3 pin input voltage must not be higher than 3.7V for the CH224K and 5V for the CH224D.

If the MCU and other back-end circuits start up slowly, or the MCU pin has a specific default state, CFG1 may be in the floating state or IO configuration mode before startup, and then it is possible to request 20V. If the system can not withstand the 20V input, a configuration resistor should be added to the CFG1 pin to ensure that before the MCU starts up, CH224K/CH224D can be configured through the resistor and request the appropriate voltage. CH224K/CH224D can be configured with the resistor to request a suitable voltage before MCU startup.

5.3. CH221K Voltage Gear Configuration

CFG to VDD connection resistance, different resistance value corresponds to different voltage request gear. The resistance-requested voltage comparison table is as follows.

CFG to VDD resistance	Requested Voltage
10K Ω	5V
20K Ω	9V
47K Ω	12V
100K Ω	15V
200K Ω	20V

5.4. Analog E-Mark function

To use the analog E-Mark function to request greater than 20V or greater than 60W output, aType-C male connector must be used and a 1K Ω resistor must be connected to GND at pin CC2.(Please consult our technical support)

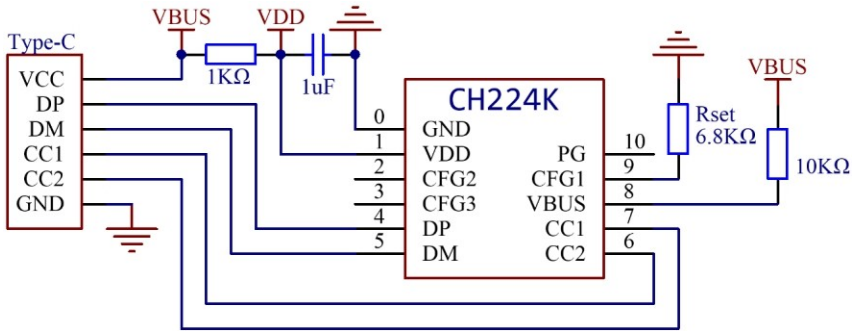
5.5. Use PD protocol only

If you do not need to use the A-port protocol (various protocols realized by DP and DM communication) you can select the CH221K model.

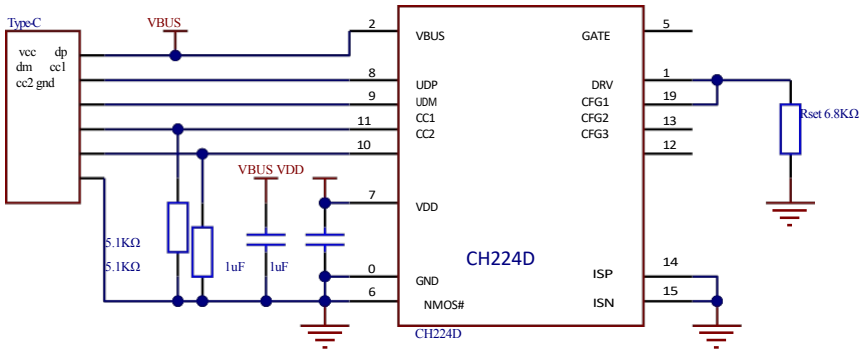
If you wish to block these protocols on the CH224K/CH224D, disconnect the DP/DM pins of the CH224K/CH224D from the DP/DM on the Type-C connector and short the DP and DM on the CH224K/CH224D side. for the CH224K this time, the VBUS pin can be NC.

6. reference schematic

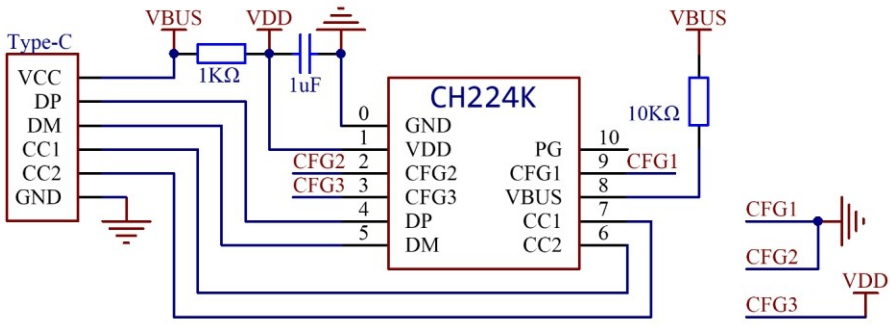
6.1. CH224K/CH224D using Type-C female, single resistor configurations 9/12/15/20V (resistor configuration 6.8K Ω for 9vshown)



Rset resistance	Requested Voltage
6.8K Ω	9V
24K Ω	12V
56K Ω	15V
NC	20V

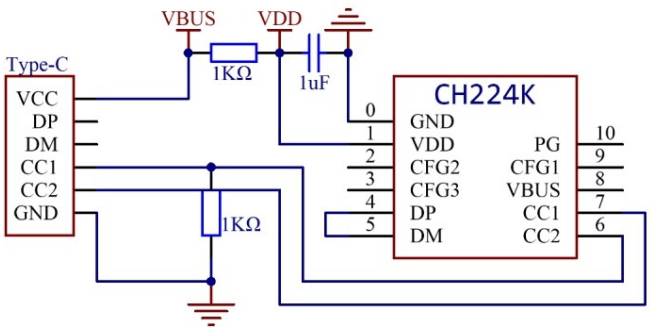


6.2. CH224K using Type-C female port, level configuration 5/9/12/15/20V (level mode configured as 12v in the figure)

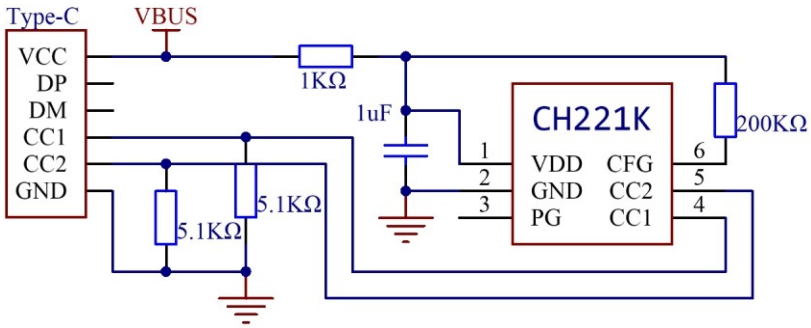


CFG1	CFG2	CFG3	requesting input voltage
1	-	-	5V
0	0	0	9V
0	0	1	12V
0	1	1	15V
0	1	0	20V

6.3. CH224K using Type-C male port, PD protocol and E-Mark analog only (resistor configuration NC at 20v in figure)



6.4. CH221K using Type-C female, single resistor configuration 20V



7. parameters

7.1. CH221K Chip Absolute Maximum

(Critical or exceeding the absolute maximum may result in improper operation or even damage to the chip)

name (of a thing)	Parameter description	minimum value	maximum values	unit (of measure)
TA	Ambient temperature during operation	-40	105	°C
TS	Ambient temperature during storage	-55	150	°C
VDD	Operating supply voltage (VDD pin to power, GND pin to ground)	-0.5	5.8	V
VODHV	Voltage on high voltage open-drain output pin PG	-0.5	13.5	V
VIOCC	Voltage on CC1,CC2 pins	-0.5	8	V
VIOUX	Voltage on CFG pin	-0.5	VDD+0.5	V
PD	Maximum power consumption of the whole chip (VDD voltage * current)		250	mW

7.2. CH224K Chip Absolute Maximum

(Critical or exceeding the absolute maximum may result in improper operation or even damage to the chip)

name (of a thing)	Parameter description	minimum value	maximum values	unit (of measure)
TA	Ambient temperature during operation	-40	90	°C
TS	Ambient temperature during storage	-55	105	°C
VDD	Operating supply voltage (VDD pin to power, GND pin to ground)	3.0	3.6	V
VIOHV	Voltage on pins supporting high voltage (CFG,VBUS)	-0.5	13.5	V
VIOCC	Voltage on CC1,CC2,CFG1 pins	-0.5	8	V
VIOUX	Voltage on DP, DM, CFG, CFG2, CFG3 pins	-0.5	VDD+0.5	V
VIOLV	Voltage on CFGHV pin		0.8	V
PD	Maximum power consumption of the whole chip (VDD voltage * current)		400	mW

7.3. CH224D Chip Absolute Maximum

(Critical or exceeding the absolute maximum may result in improper operation or even damage to the chip)

name (of a thing)	Parameter description	minimum value	maximum values	unit (of measure)
TA	Ambient temperature during operation	-40	100	°C
TS	Ambient temperature during storage	-55	125	°C
VDD	Operating supply voltage (VDD pin to power, GND pin to ground)	-0.5	6	V
VIOHV	Voltage on VBUS pin	-0.5	24	V
VIOCC	Voltage on CC1,CC2 pins	-0.5	20	V
VIOUX	DP,DM,CFG1,CFG2,CFG3,DRV,NMOS#,ISP,ISN Voltage on pins	-0.5	VDD+0.5	V
VIOHX	Voltage on GATE pin	-0.5	VIOHV+6.5	V
PD	Maximum power consumption of the whole chip (VDD voltage * current)		300	mW

7.4. CH221K Chip Electrical Parameters (Test Condition: TA=25°C)

name (of a thing)	Parameter description	minimum value	typical value	maximum values	unit (of measure)
VLDOK	CH221K Internal Power Regulator VDD Parallel Regulator	3.0	3.3	3.6	V
ILDO	Internal power regulator VDD Parallel absorption current capability	0		30	mA
VR	Voltage threshold for power-on reset of the power supply	2.2	2.4	2.6	V

7.5. CH224K Chip Electrical Parameters (Test condition: TA=25°C)

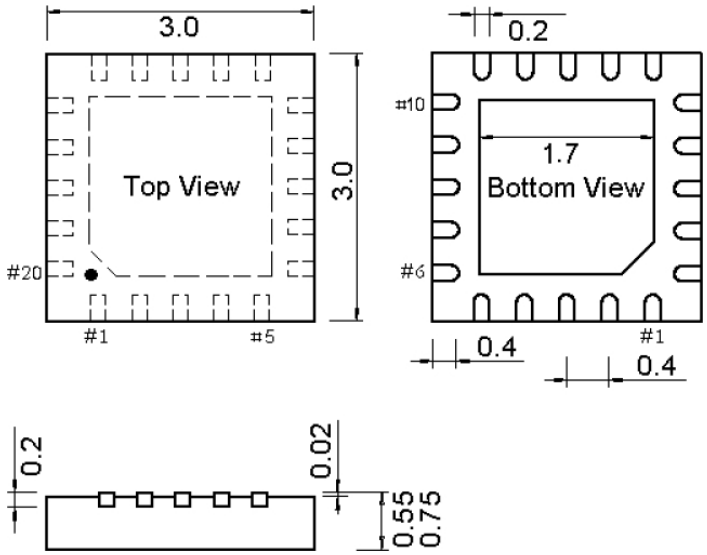
name (of a thing)	Parameter description	minimum value	typical value	maximum values	unit (of measure)
VLDOK	CH224K Internal Power Regulator VDD Parallel Regulator	3.24	3.3	3.36	V
ILDO	Internal power regulator VDD Parallel absorption current capability	0		30	mA
TOTA	Reference Threshold Temperature for OTA Over Temperature Protection Module	90	105	120	°C
VR	Voltage threshold for power-on reset of the power supply	2.2	2.4	2.6	V

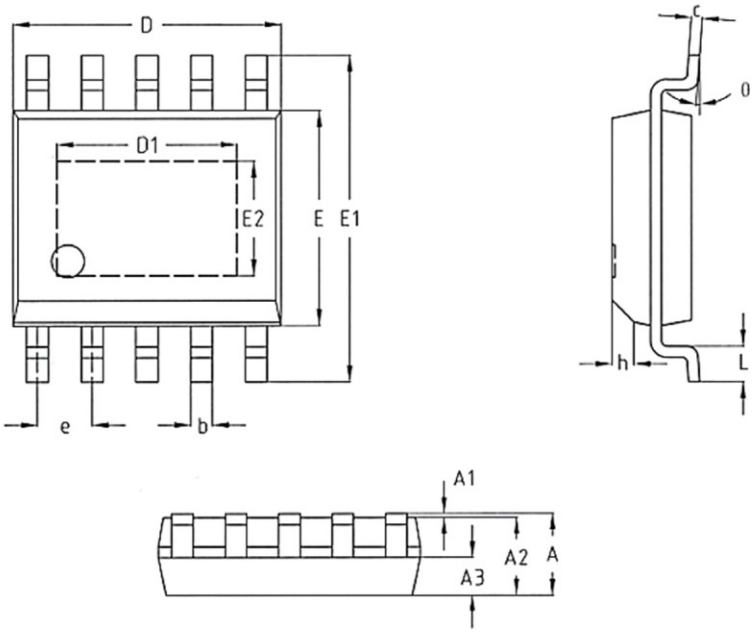
7.6. CH224D Chip Electrical Parameters (Test Condition: TA=25°C)

name (of a thing)	Parameter description	minimum value	typical value	maximum values	unit (of measure)
VLDO	Internal power regulator VDD output voltage	4.65	4.7	4.75	V
ILDO	Internal Power Regulator VDD External Load Capability			10	mA
VR	Voltage threshold for power-on reset of the power supply	2.2	2.4	2.6	V

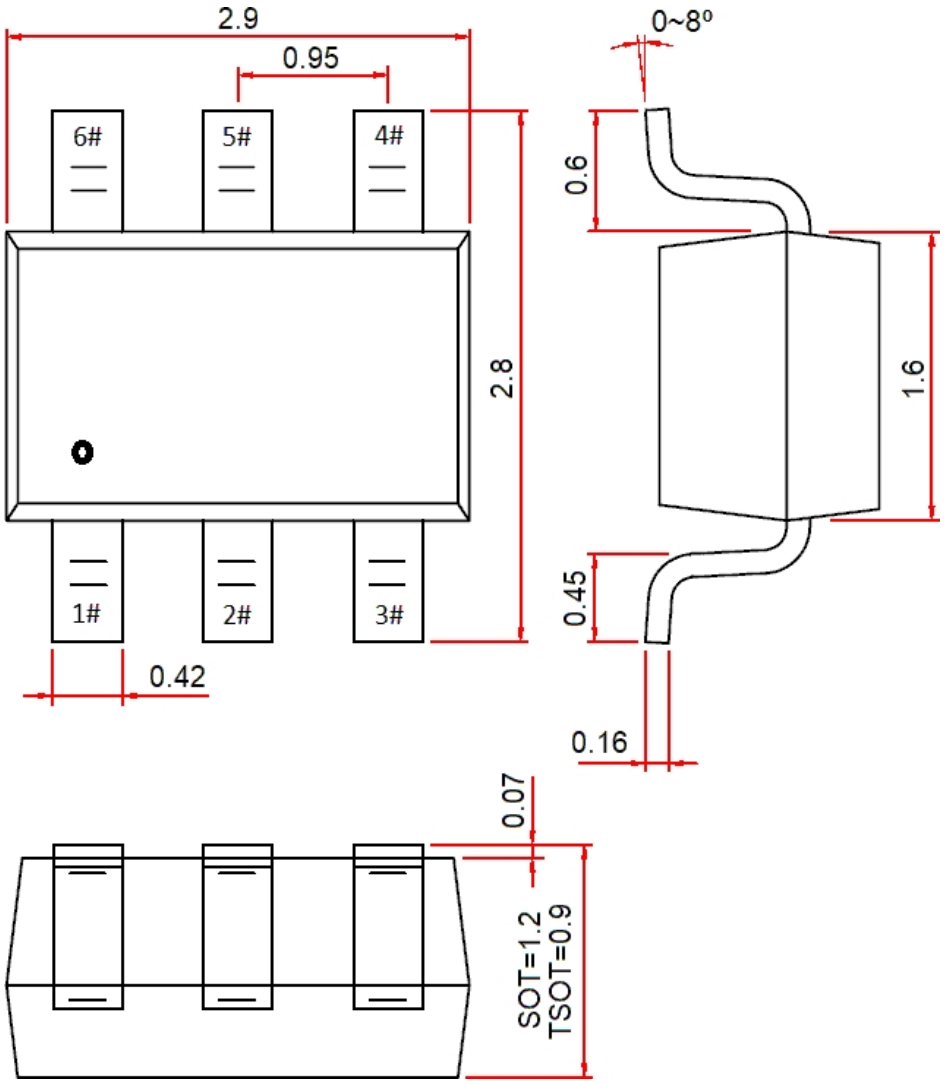
8. Package Information

Package form	Width of body molding		Pin Spacing		Package Description	Ordering Model
QFN20	3*3mm	118mil	0.40mm	15.7 mil	Square Flat Pinless Package	CH224D
ESSOP10	3.9mm	150 mil.	1.00mm	39 mil.	Narrow Pitch 10-Pin Chip with Backplane	CH224K
SOT23-6L	1.6mm	63 mil.	0.95mm	37 mil.	Small 6-Pin Chip	CH221K





符号	标称值
A	1.6
A2	1.45
D	4.9
D1	3.3
E	3.9
E1	6.0
E2	2.1
b	0.4
e	1.00BSC
c	0.2



Note: The units labeled in the encapsulation infographic are mm (millimeters).