	Reg Dst	Bra-nch	Mem Read	Mem ToReg	ALUop (2)	Mem Write	ALU src	Reg Write	Operation (4)
addi	0	0	0	0	00	0	1	1	0010
sw	X	0	0	X	00	1	1	0	0010
beq	X	1	0	X	01	0	0	0	0110