



```
** Generated for: hspiceD
** Generated on: Apr  8 13:42:48 2020
** Design library name: my
** Design cell name: inv_test
** Design view name: schematic
.GLOBAL vdd!

.TRAN 1e-12 200e-12 START=0.0

.TEMP 25.0
.OPTION
+   ARTIST=2
+   INGOLD=2
+   PARHIER=LOCAL
+   PSF=2
.INCLUDE "/home/ocf/peiyi/FreePDK45/ncsu_basekit/models/hspice/hspice_nom.include"

** Library name: my
** Cell name: inv
** View name: schematic
.subckt inv in out
m0 out in vdd! vdd! PMOS_VTL L=50e-9 W=180e-9 AD=18.9e-15 AS=18.9e-15 PD=390e-9 PS=390e-9
m1 out in 0 0 NMOS_VTL L=50e-9 W=90e-9 AD=9.45e-15 AS=9.45e-15 PD=300e-9 PS=300e-9 M=1
.ends inv
** End of subcircuit definition.

** Library name: my
** Cell name: inv_test
** View name: schematic
xi0 vin vout inv
v0 vdd! 0 DC=1.1
v1 vin 0 PULSE 0 1.1 0 10e-12 10e-12 40e-12 100e-12
c0 vout 0 1e-15
.END
```