Lecture Topics

CPSC330, Spring 2020

Under construction. Please do not use downloaded version, instead, use the links to get the latest version each time.

Lecture topics:

* Mar. 17:   
  *www1.chapman.edu/~zhao/CPSC330/slides/2.2minterm\_SOP\_\_2.3Boolean\_Axioms\_Theorem.ppt*
* Mar.18. Lab: *http://www1.chapman.edu/~zhao/CPSC330/Labs/SchematicInv\_CadenceSetup\_freePDK45.docx*
* Mar.19: Boolean theorem, simplify logic equation link as Mar.17
* Mar.24: Spring break
* Mar.27: Spring break
* Mar.31: Simplify logic equation using combination (AB+AB\_=A) expansion (C=C+CD, or C=CD+CD\_), DeMorgan’s Law
* Apr.2, Apr. 7, Apr.9: K map, how to simplify logic equation, quiz(Apr.9) : *www1.chapman.edu/~zhao/CPSC330/slides/2.4LogiToGate\_2.7KarnaughMap.ppt*
* Apr.8: lab
* Apr. 14: Quiz1 review, how to simplify equation using HW6 problem:

*www1.chapman.edu/~zhao/CPSC330/slides/2.8\_multiplexer\_decoder.pptx*

* Apr. 16: Quiz 2, Muliplexer
* Apr. 21: Ch.3 Latch, Flip flop

*www1.chapman.edu/~zhao/CPSC330/slides/Ch.3\_Latch\_Flip\_flop.pptx*

* Apr. 23:
  + Waveforms of Latch/Flip flop. Register, see the above link
  + *Finite State Machine: www1.chapman.edu/~zhao/CPSC330/slides/Ch.3\_finiteStateMachine.pptx*
* *Apr.28: Tue.Midterm*
* *Apr.29: Lab 8:NOR gate, NOR testing gate, input setup, simulation, waveform to verify function  
   www1.chapman.edu/~zhao/CPSC330/Labs/NOR\_Virtuoso\_Schmatic.docx  
   www1.chapman.edu/~zhao/CPSC330/Labs/NOR\_powerpoint.pptx*
* *Apr.30:*

*SystemVerilog: www1.chapman.edu/~zhao/CPSC330/slides/Ch4-SystemVerilog-DDCA-basic.pptx*

* *May 5:*
  + *Review FSM (Ch.3: 4.3), learn FSM Verilog example(Divide by 3, HDL example 4.30))*
  + *Vivado Simulation/synthesis tool tutorial:*

[*http://www1.chapman.edu/~zhao/CPSC330/Labs/Vivado2014-2Tutorial-SystemVerilog.doc*](http://www1.chapman.edu/~zhao/CPSC330/Labs/Vivado2014-2Tutorial-SystemVerilog.doc)

* *May 7: Verilog Compile, simulation of 3:8 decoder*

[*http://www1.chapman.edu/~zhao/CPSC330/Labs/Synthesis\_Basys3\_Vivado\_Decoder\_Tutorial.pdf*](http://www1.chapman.edu/~zhao/CPSC330/Labs/Synthesis_Basys3_Vivado_Decoder_Tutorial.pdf)

* *May 12. Synthesize, Implementation (using constraint file),bit generation of Verilog code*

*May 13, Wed. Basys3 board introduction;* ***Program the FPGA board****, a 3:8 decoder example*[*http://www1.chapman.edu/~zhao/CPSC330/Labs/Synthesis\_Basys3\_Vivado\_Decoder\_Tutorial.pdf*](http://www1.chapman.edu/~zhao/CPSC330/Labs/Synthesis_Basys3_Vivado_Decoder_Tutorial.pdf)

* *May 14 Course Evaluation;* ***Program the FPGA board****, counter using 7 segment display* www1.chapman.edu/~zhao/CPSC330/Labs/Seven\_segment\_wpi\_Counter\_Basys3TutorialVerilog.pdf

\*\*Note again:

Under construction. Please do not use downloaded version, instead, use the links to get the latest version each time.