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**1) Purpose of Lab 6:**

The purpose of Lab 6 was to simulate our test circuit. Simulation allows us to check the correctness of our circuit using software by applying input values to the circuit and checking the outputs they produce. This saves both time and money that would have gone into building the circuit using hardware.

**2) What we did for Lab 5:**

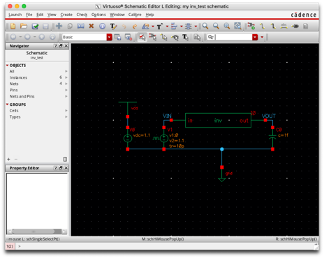
For Lab 5, we created a test inverter schematic that is built to test our previously built inverter schematic. The goal of the circuit is to make sure that the inverter produces the truth table in the figure below (NOT(A)).

**2.1) Inverter Truth Table:**

|  |  |
| --- | --- |
| A | A\_ |
| 0 | 1 |
| 1 | 0 |

**2.2) Inverter Test Circuit Schematic:**

The final design for our test circuit is shown below.



**2.3) Netlist:**

Next, we exported a SPICE Netlist to inv.sp to be used to simulate our test circuit outside of Virtuoso.

The contents of inv.sp are below:

\*\* Generated for: hspiceD

\*\* Generated on: Apr 8 13:42:48 2020

\*\* Design library name: my

\*\* Design cell name: inv\_test

\*\* Design view name: schematic

.GLOBAL vdd!

.TRAN 1e-12 200e-12 START=0.0

.TEMP 25.0

.OPTION

+ ARTIST=2

+ INGOLD=2

+ PARHIER=LOCAL

+ PSF=2

+ POST

.INCLUDE "/home/ocf/peiyi/FreePDK45/ncsu\_basekit/models/hspice/hspice\_nom.incle"

\*\* Library name: my

\*\* Cell name: inv

\*\* View name: schematic

.subckt inv in out

m0 out in vdd! vdd! PMOS\_VTL L=50e-9 W=180e-9 AD=18.9e-15 AS=18.9e-15 PD=390e-PS=390e-9 M=1

m1 out in 0 0 NMOS\_VTL L=50e-9 W=90e-9 AD=9.45e-15 AS=9.45e-15 PD=300e-9 PS=30-9 M=1

.ends inv

\*\* End of subcircuit definition.

\*\* Library name: my

\*\* Cell name: inv\_test

\*\* View name: schematic

xi0 vin vout inv

v0 vdd! 0 DC=1.1

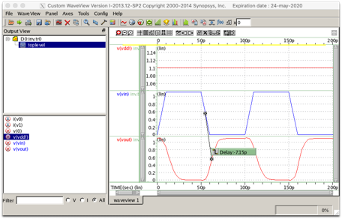
v1 vin 0 PULSE 0 1.1 0 10e-12 10e-12 40e-12 100e-12

c0 vout 0 1e-15

.END

**2.4) Waveform:**

Finally, we simulated our test inverter and produced the waveform diagram below:



This waveform simulation shows the constant voltage applied, “v(vdd!)” - at the top, in red, “voltage IN” - in the middle, in blue, and “voltage OUT” - at the bottom, in red. As the voltage IN increases from 0V to 1.1 V, the voltage OUT decreases from 1.1V to 0V.

**3) Delay Result:**

The delay result found for our circuit was -7.15p (picoseconds). This is the time between the voltage IN becoming small enough for the voltage OUT to become active. The switch point is about 0.5V. In Binary Logic this switch represents the timeframe between A going from 1 → 0 and A’ going from 0 → 1.