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**Introduction**

For this assignment, we designed a 2 input NAND circuit using virtuoso. We then compared the waveforms of the circuit using an NMOS width of 90 nm and 180 nm.

**Expected Truth Table**

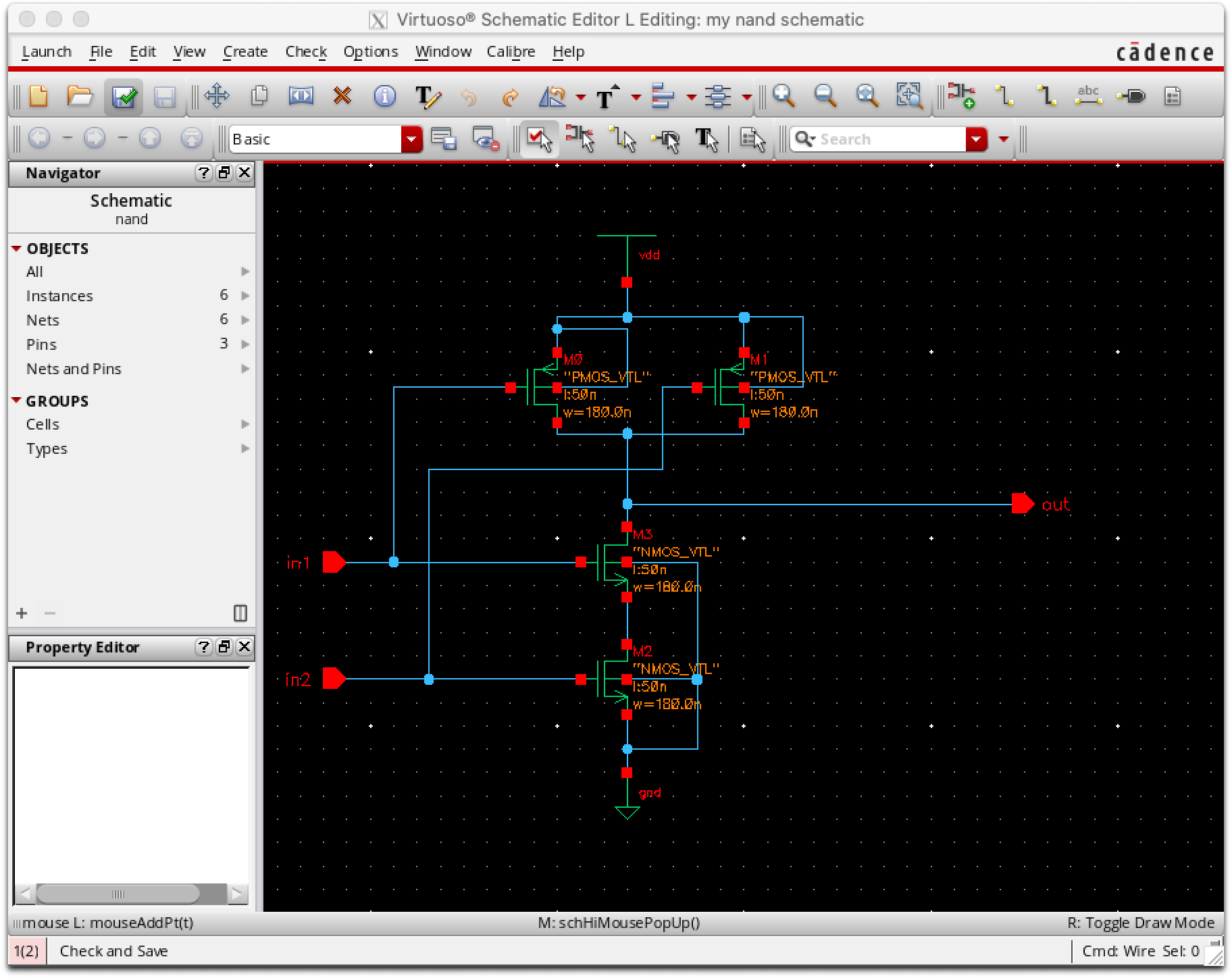
**NAND Truth Table**

|  |  |  |
| --- | --- | --- |
| **A** | **B** | **(AB)\_** |
| 0 | 0 | 1 |
| 0 | 1 | 1 |
| 1 | 0 | 1 |
| 1 | 1 | 0 |

**Procedure**

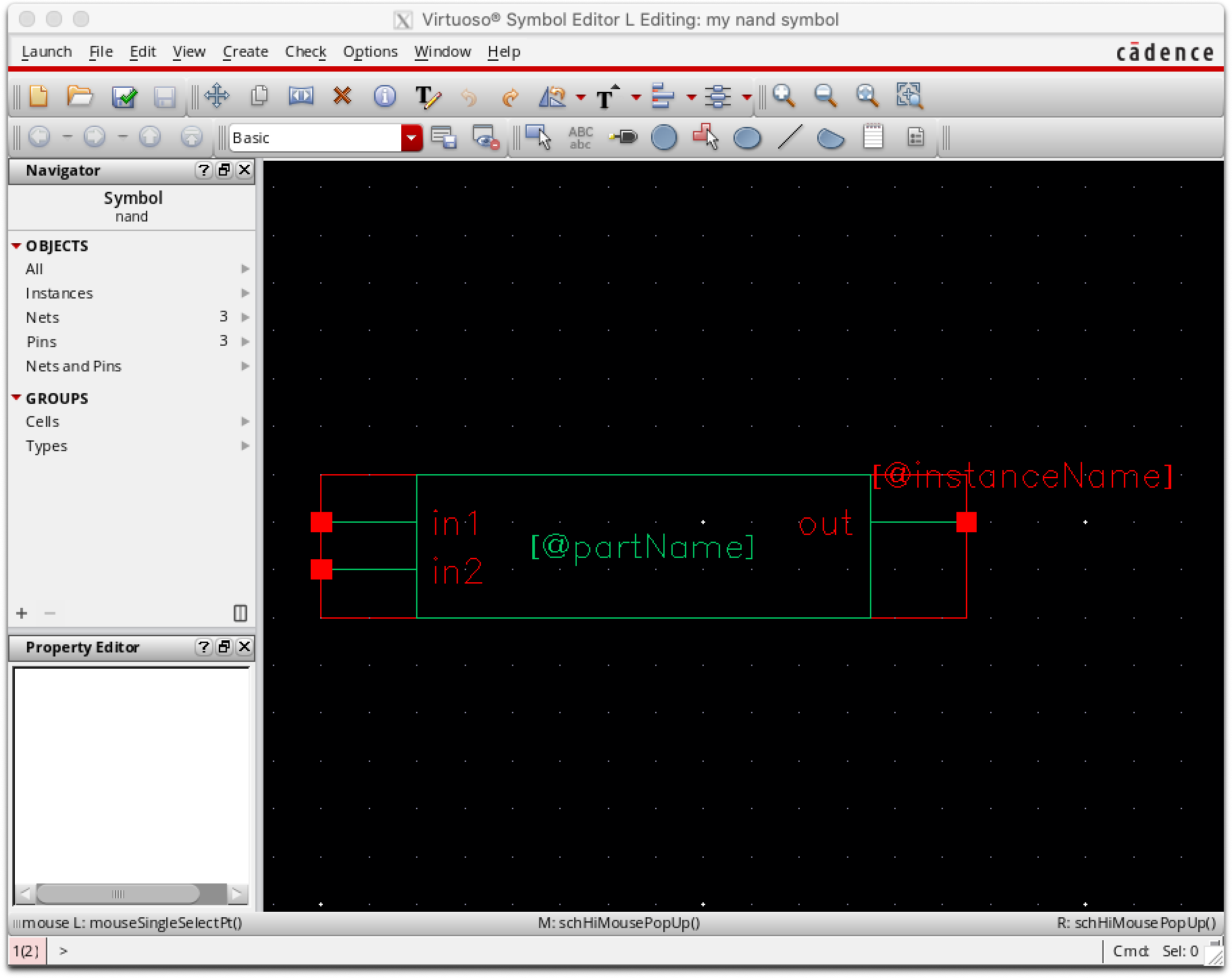
1. **Create NAND Schematic**

To create a 2-input NAND circuit, we connected two PMOS transistors in parallel and two NMOS transistors in series.



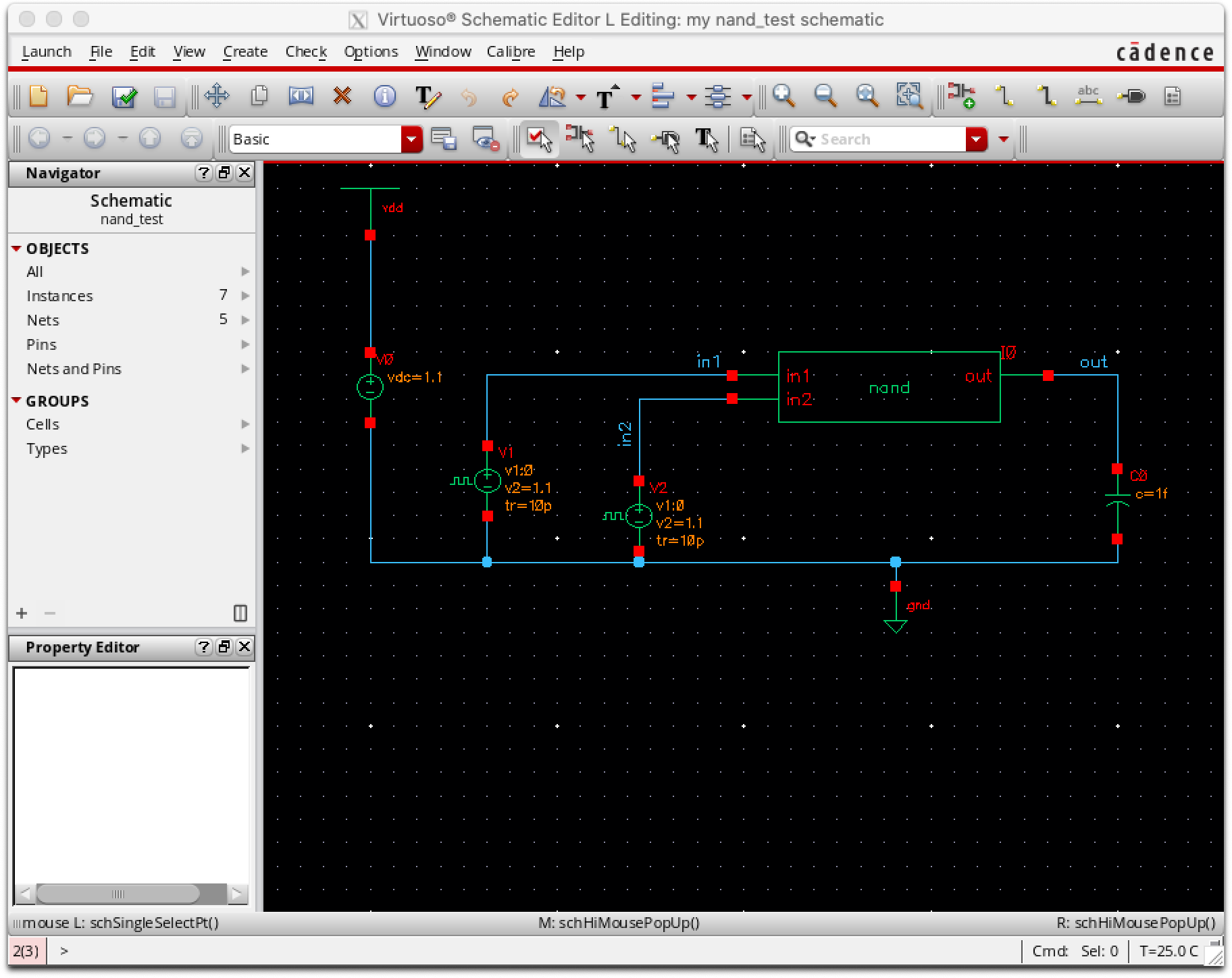
1. **Create NAND Symbol**

We then created a symbol for our circuit to use for testing as shown below.



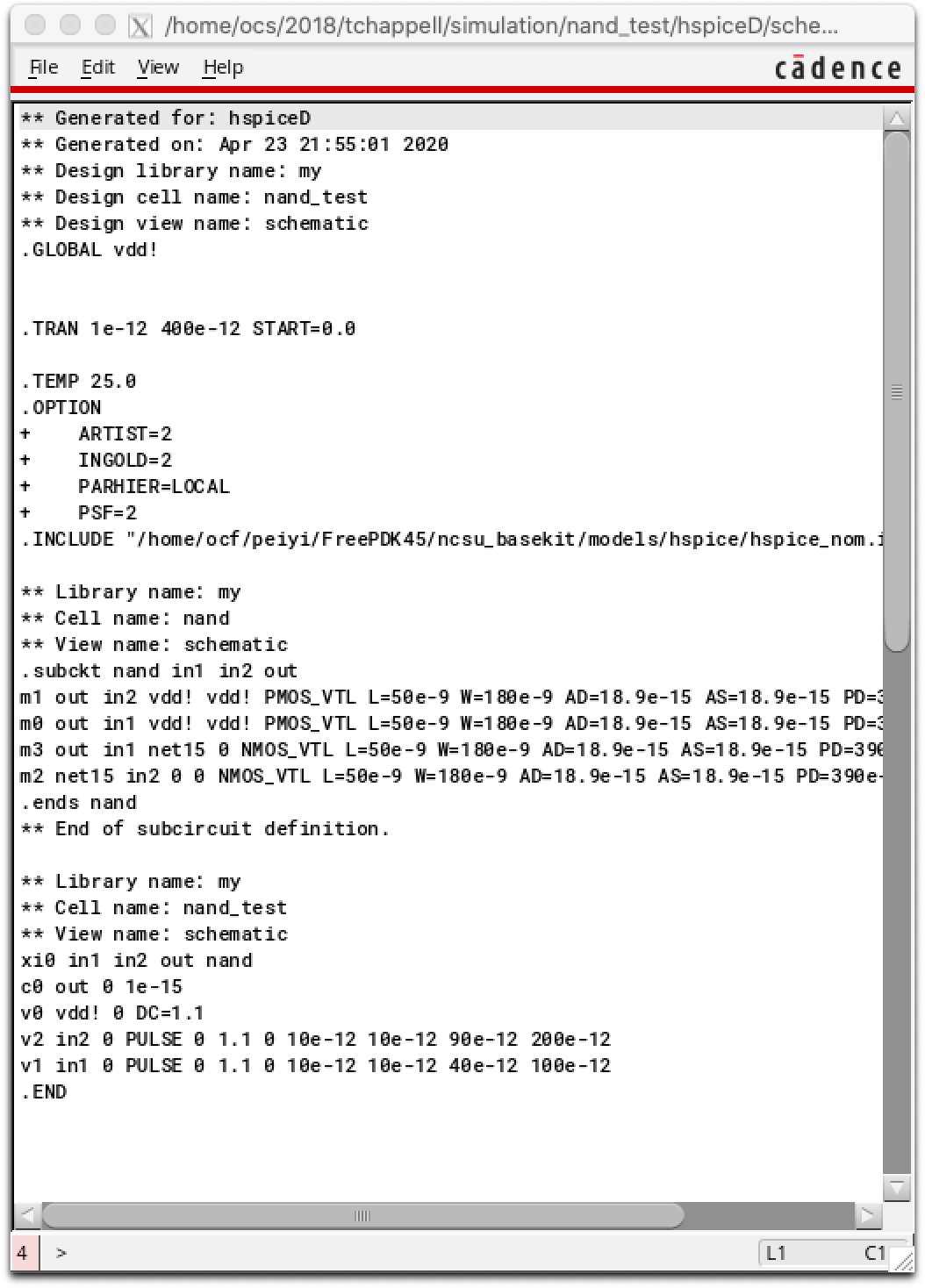
1. **Create NAND Test Circuit**

To test the NAND circuit, we used two pulses for the inputs. Input 1 has a pulse width of 40 ps and period of 100 ps. Input 2 has a pulse width of 90 ps and a period of 200 ps. This allows us to test all 4 possible input combinations.



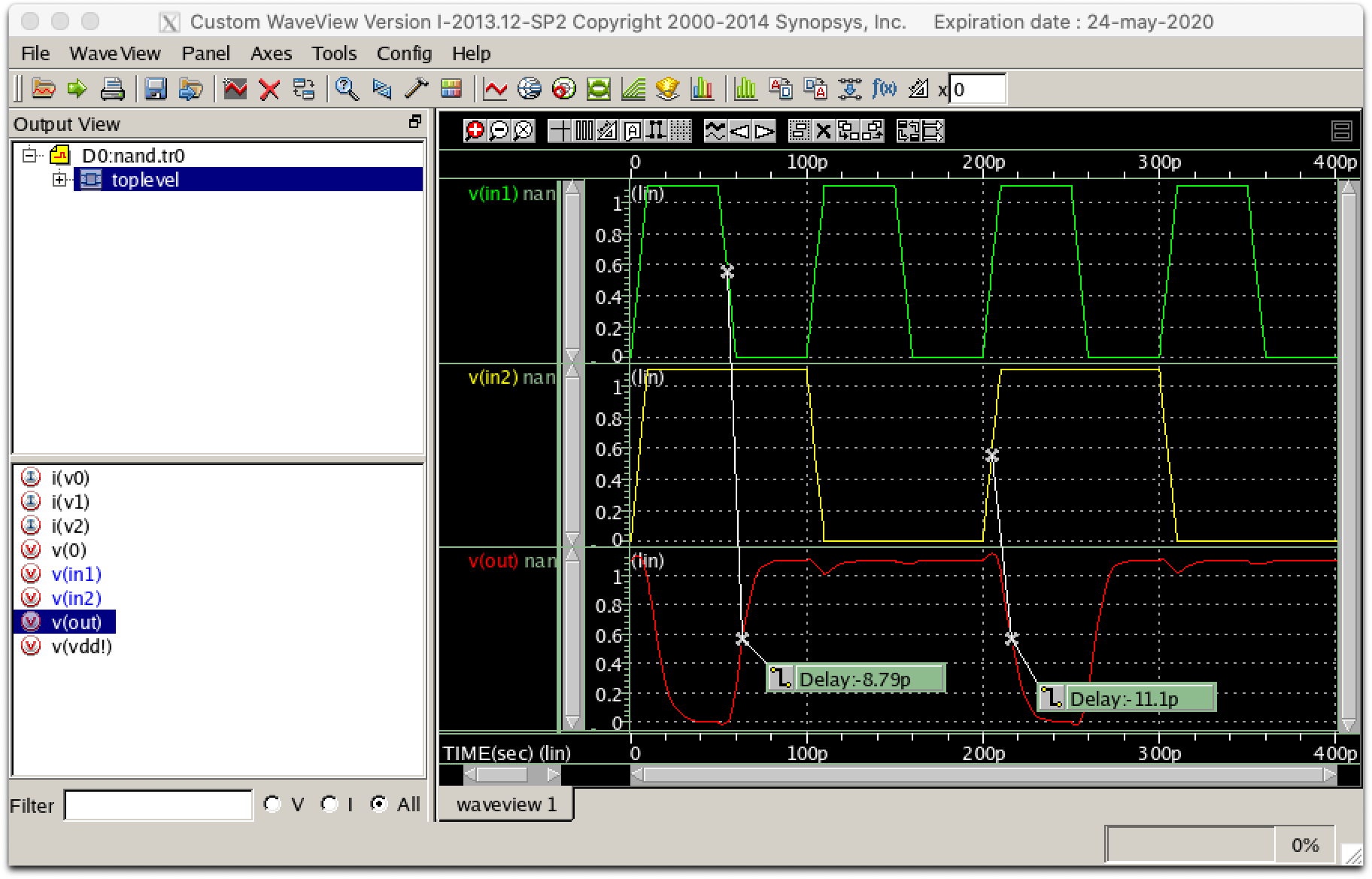
**4) Create Netlist and Run Hspice Software**

Next, we generated the netlist file, in ADE L, from the NAND circuit to be used to generate the waveforms and passed the netlist to hspice.



**5) Create Waveforms (NMOS 180 nm) in Custom WaveView**

We then generated the waveforms when NMOS width is 180 nm.



**6) Delay Times of NMOS (180 nm)**

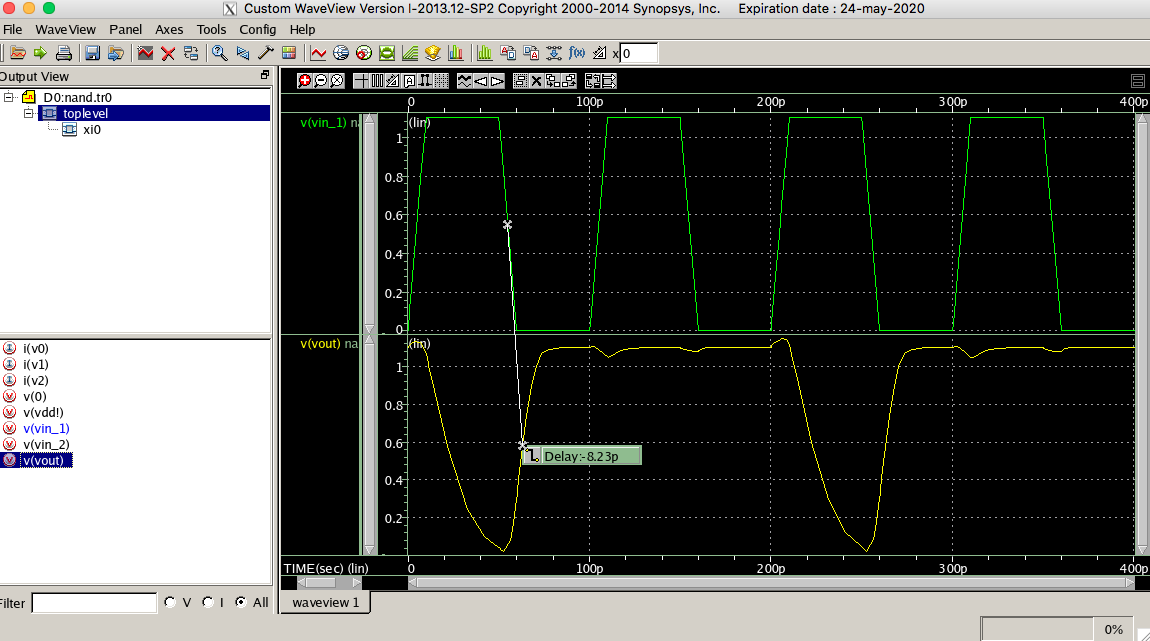
Using the “measurements” tool in Custom Waveview we observed that the circuit output was affecting the pulsed input of 0-1.1V. We observed that:

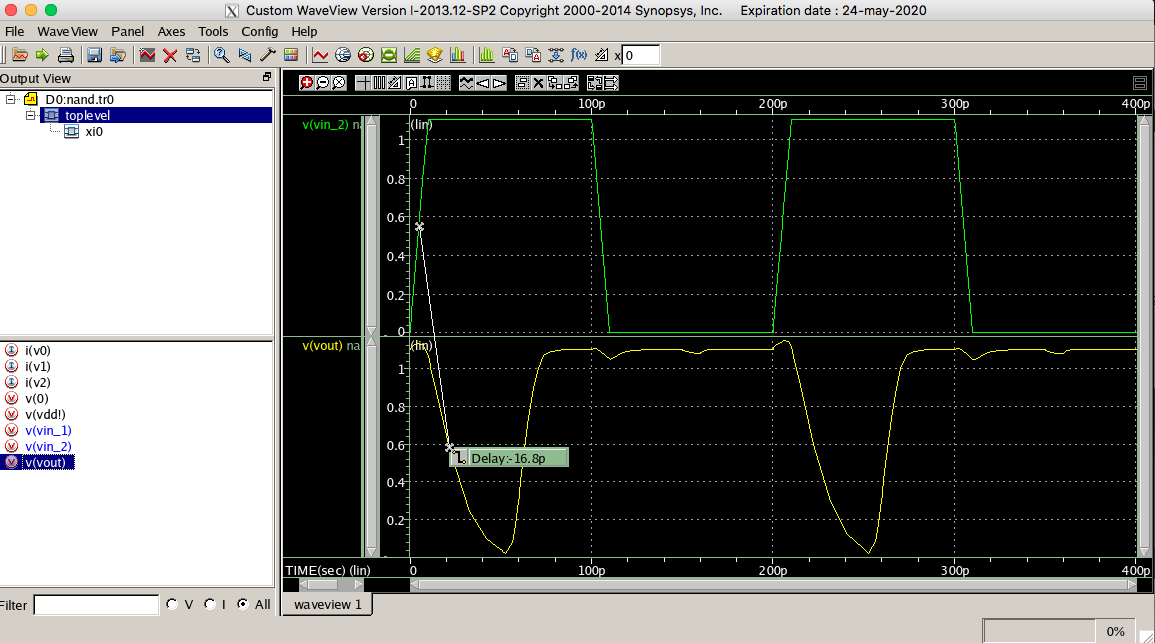
Output Rise Delay: -8.79 ps

Output Fall Delay: -11.1 ps

**7) Waveforms (NMOS 90 nm)**

Lastly, we repeated the procedure steps 1-6 using an NMOS width of 90nm.





**8 ) Delay Times of NMOS (90 nm)**

We observed that the values of the output delay differed from that of the NMOS with a width of 180nm as the following:

Output Rise Delay: -8.32 ps

Output Fall Delay: -16.8 ps

**Conclusion**

The reason the fall delay time is longer for when NMOS width is 90 nm is because the electrons need to move more distance to get to ground since the NMOS transistors are in series. Increasing the width allows for more electrons to flow quicker meaning NMOS with width of 180 nm will be faster.

The reason that the rise delay times are relatively the same between when NMOS width is 90 nm and 180 nm is because the PMOS width is the same (electrons need to move the same distance to get from power to output).

The result of decreasing the width of the delay could cause undesired effects in the state of the circuit and resultant truth table. The NMOS with the wider width is desired to maintain consistency in the electrical flow to give us the expected NAND table, shown below, as our resultant truth table.

**Resultant Truth Table**

**NAND Truth Table**

|  |  |  |
| --- | --- | --- |
| **A** | **B** | **(AB)\_** |
| 0 | 0 | 1 |
| 0 | 1 | 1 |
| 1 | 0 | 1 |
| 1 | 1 | 0 |