**Lab 8 NOR Design and Simulation**

**I. Purpose:**

Design a two input NOR gate. Simulate the NOR gate, check wave form, delay.

**II. Two input NOR schematic design**

*We have learned how to create inverter schematic and generate netlist describing the nodes connection in the circuit as well as describe transistor size (width). In this lab, you will design NOR schematic. The main steps to design NOR schematic are similar to the steps creating inverter:*

***1. Using Putty Xming:*** *www1.chapman.edu/~zhao/CPSC330/Labs/Putty-Xming-VPN.pptx  
 Create Working directory*

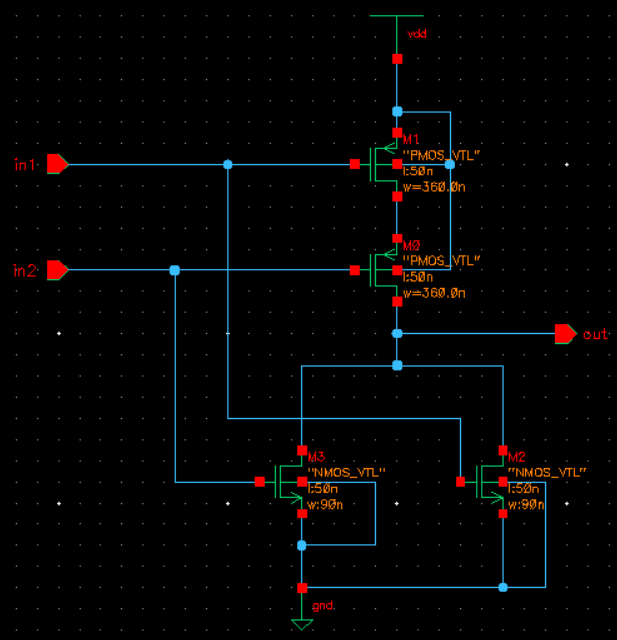
***2. NOR Schematic using Virtuoso: reference:*** *www1.chapman.edu/~zhao/CPSC330/Labs/SchematicInv\_CadenceSetup\_freePDK45.docx*

***2.a) Starting Virtuoso****: “virtuoso &”*

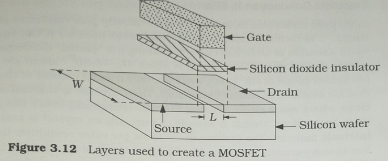
***2.b) Library Manager****: in “my” library,* ***create a new cell named “NOR”***

***2.c) Creating Schematic of NOR***

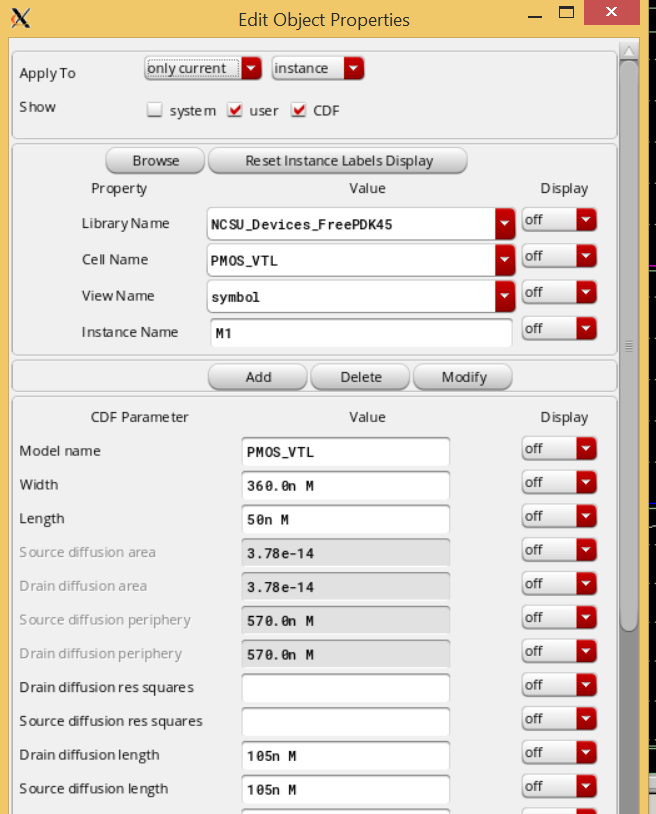
Notes: For inverter using 45nm technology, in lab4 we have used 180nm for PMOS and 90nm for NMOS Howerver, for NOR with 2 inputs, PMOS width will be 360nm, NMOS width will still be 90nm. The reason of using 360 nm for PMOS: 2 PMOS transistors in NOR are in series while NMOS transistors are in parallel. So charges in PMOS need to move through two channels of PMOS which means moving more distance in PMOS. To compensate for that, PMOS width needs to be larger such that the pull up path can reduce resistance and PMOS has more driving strength in order that PMOS and NMOS will have similar pull up and pull down time.



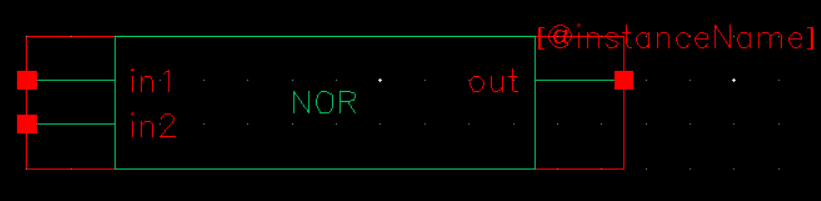
* This figure will help you to visualize the channel length L, transistor width:



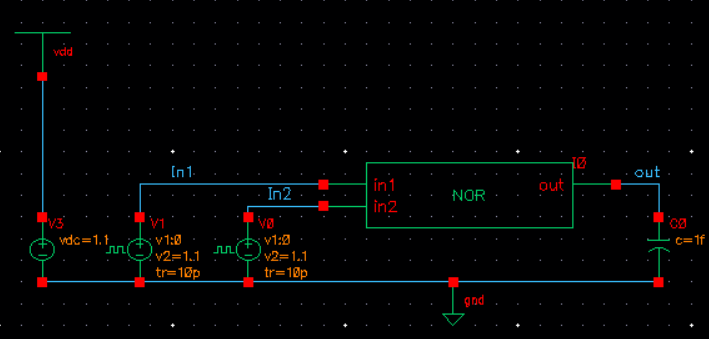
**How to change transistor width?**Click PMOS to select it, then press "Q" to bring out Property window. Change width there. You can reuse your test circuit. If you have closed your ADE L window, you need to do simulation steps in ADE L again; after that, create netlist, save input.ckt that pops out as nor.sp, then add POST, and run *hspice* command.



***2.d) Create symbol for NOR***

When the symbol appear, click [@partName] label in the middle, then press Q to bring out Property window, change the @partName to NOR.  


***3. NOR Test Circuit  
 3.a: Creating Test Circuit for NOR:*** *reference****:****www1.chapman.edu/~zhao/CPSC330/Labs/Simulation\_of\_Schematic.docx*

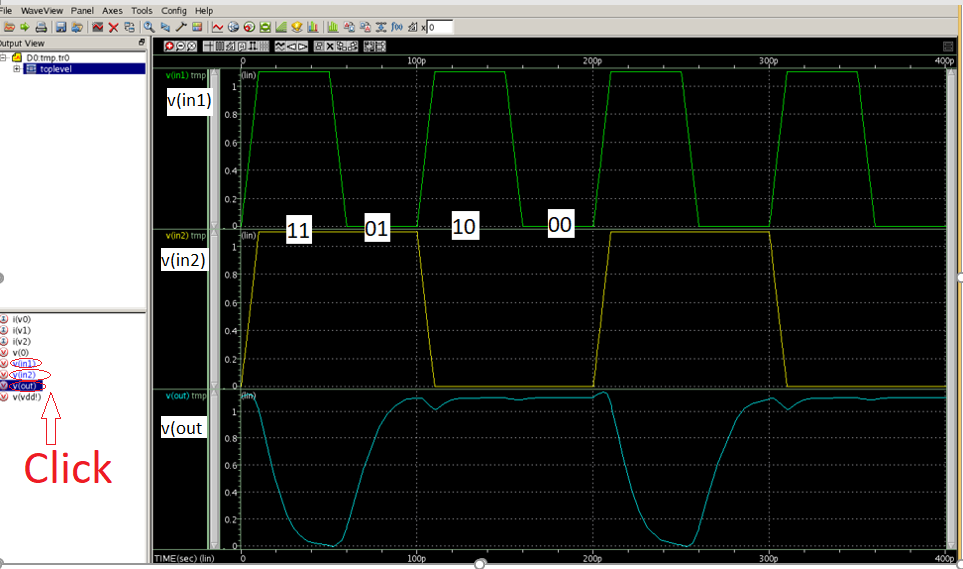
* **Create a test circuit based on the test circuit in inverter lab**. 
* Explanation of pulse input needed as “vpulse” in test circuit:
  + **Different from Inverter, NOR needs two inputs, which will have four cases in its truth table**

The following truth table shows the necessary states:   
VA VB NOR OUTPUT   
0 0 1

0 1 0

1 0 0

1 1 0

In order to cover the four cases: 00, 01, 10 and 11, you need to figure out how to create two pulses to cover the four cases in NOR truth table.   
Here is an example from previous NAND lab. It has pulse waveforms for Vin1, Vin2 that can cover the four cases: 00,01,10,11 in NAND, see the four small white boxes..   
In the example, the width and period of the second pulse will be doubled comparing with the first pulse. The start time of the two pulses could be different. In ADE L window. you may choose 400ps as “stop time”in Analysis/Choose.   
   


**Note*: in the above input waveforms of in1 and in2, the pulse width and period of in2(90p, 200p) are about two times of those of in1(40p,100p).*For your reference, the pulses calculation is listed here:**

Pulse width x 2 + Rise \_time + fall\_time = total length=period

In1: period 100, pulse width is 40, so 40x2+10+10=80+20=100

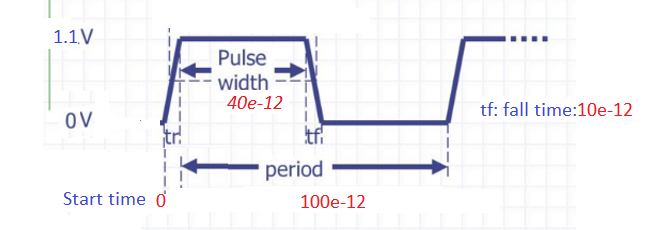
In2:period 200p, pulse width 90p , T\_rise=10p,T\_fall=10p, so 90X2+10+10=180+10+10=200

**Pulse code/parameter explanation:**

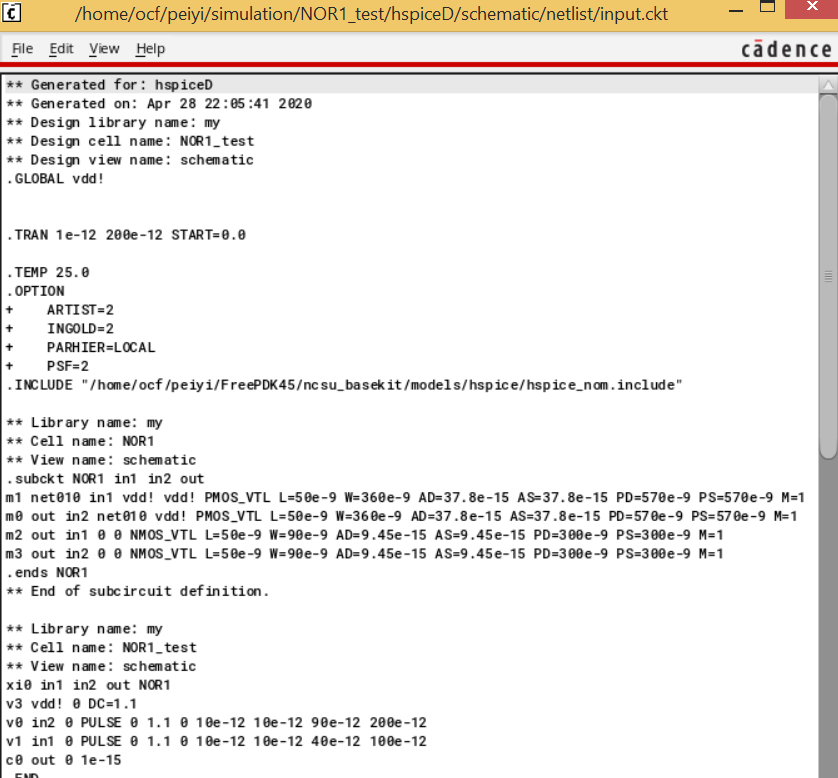
In netlist you will see something like the following code:

*v1 vin gnd PULSE 0 1.1 0 10e-12 10e-12 40e-12 100e-12*

|  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| *v1* | *vin* | *gnd* | *PULSE* | *0* | *1.1* | *0* | *10e-12* | *10e-12* | *40e-12* | *100e-12* |
| Voltage signa1 | label name in circuit |  |  | Initial voltage | Peak voltage | Start time, | rise time, | fall time | pulse width | period |

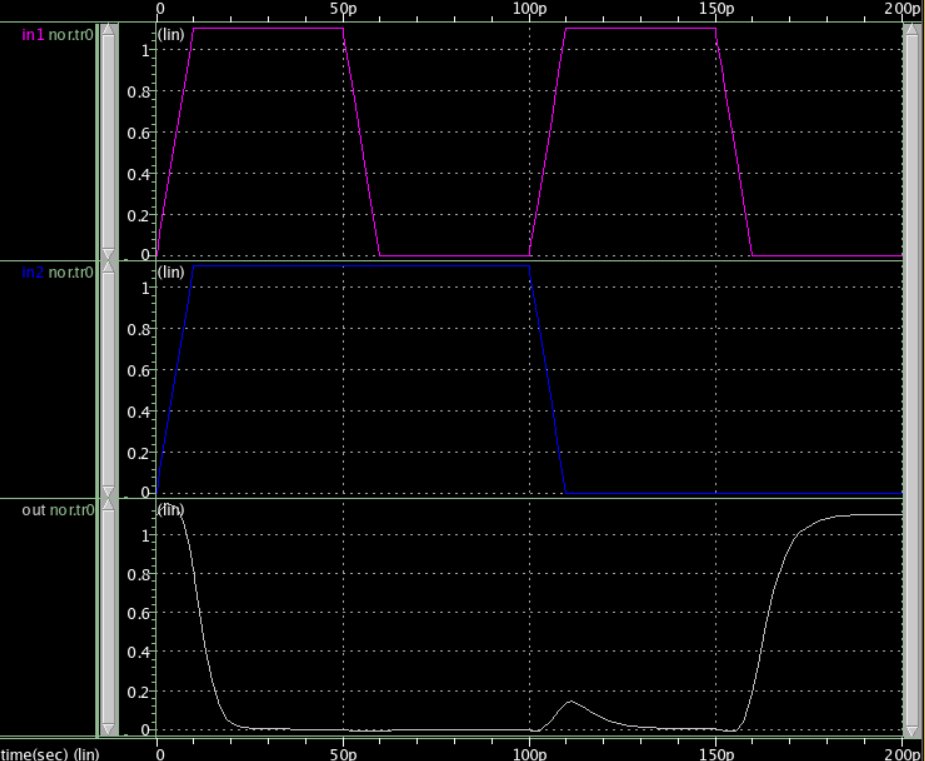


***4.*** ***Exporting SPICE Netlist in Virtuoso Analog Design Environment(ADE)****reference: www1.chapman.edu/~zhao/CPSC330/Labs/Simulation\_of\_Schematic.docx*You should follow all the steps in the above link. After the step of clicking Simulation→Netlist→Create to generate the SPICE netlist. You should see a new window showing the a file named input.ckt which is a netlist.

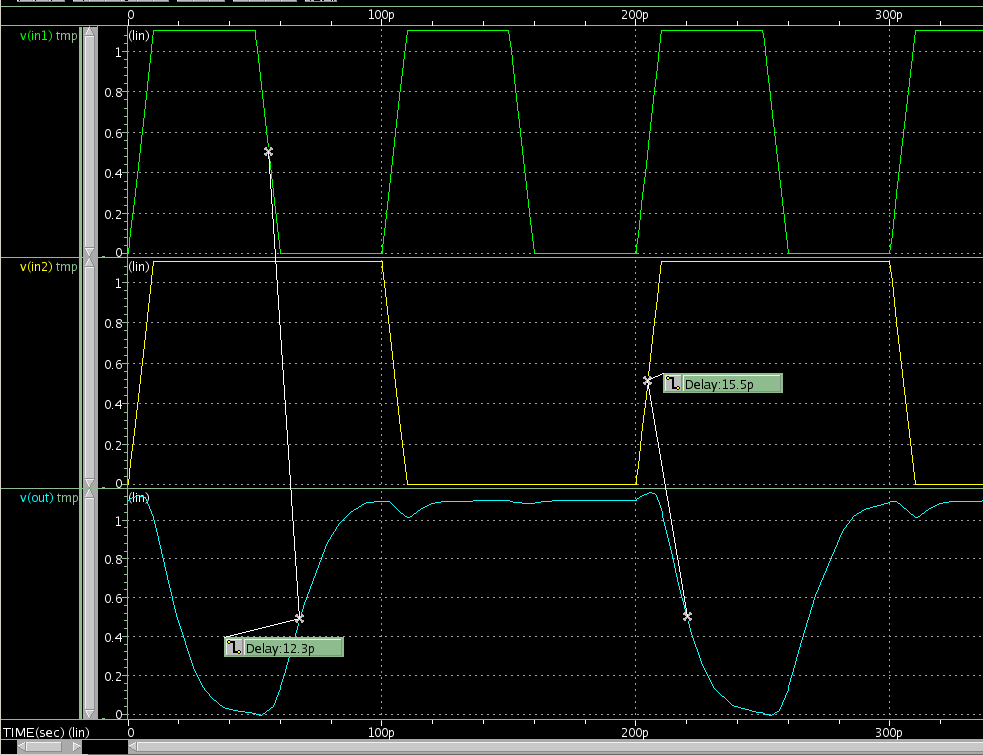
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Inside the above window, click File→Save As to save the input.ckt as 'nor.sp' in the directory 'simulation’.

***5. Waveform****: www1.chapman.edu/~zhao/CPSC330/Labs/Waveform-verification.docx,   
 Note:when opening the waveform, look for a file with extension “.tro “.*

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**How to measure the delay?** The following is copied from previous NAND lab.The fall time delay and rise time delay are showing as follows. You can drag the delay measuring points to 50% of the input and output values, respectively. Steps in delay measure is in previous lab about Waveform. You need to click **Tools→Measurement** to bring out the Measurement Tool window. Click Delay in that window:



Rise time delay where output changes  
 from 0 to 1

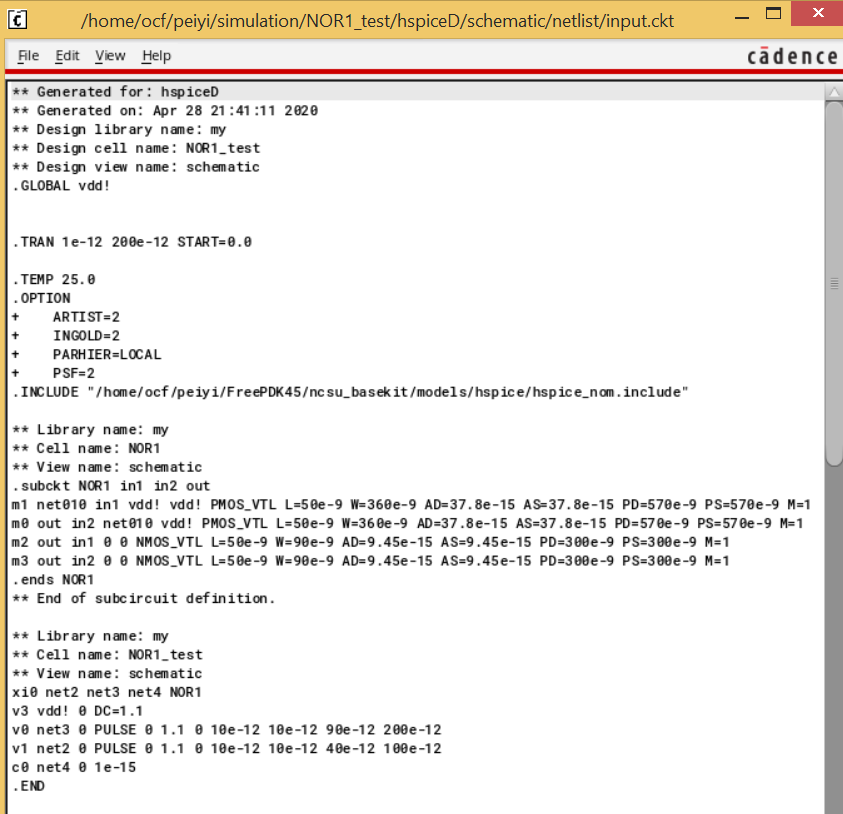
Fall time delay where output changes  
 from 1 to 0

***IV. Lab report:***

* *Check waveform and measure delays, record two delays (****output rise delay, output fall delay****) in a paper, you need to identify which input causes output to change and then measure the delay between the two signals. Note you can drag the delay line to get delay between different signals.*
* Change NMOS width to 180nm, record two delays.
* Compare the output rise delays between NMOS using 90 nm and 180 nm, then compare the output fall delay of NMOS using 90 nm and 180 nm, explain what you observe and why.
* Lab report requirement is here: **www1.chapman.edu/~zhao/CPSC330/Labs/report\_Lab.docx**

P.S.

1. input.ckt that is created after the step “Simulation/Netlist/Create” is copied here for your reference:

If you forget to label wires in test circuit, the input.ckt will name input node using net2, net3 three instead of In1, In2; and it will name output node net4:    
If you go back to add labels, then you click “Check and save” ; if you have not close ADE L window, you just go to “Simulation/Netlist/Create” to create a new input.ckt

2. There is a few schematic in the top part of the following link: <https://www.eda.ncsu.edu/wiki/Tutorial:Layout_Tutorial2>

3. *Hotkeys:*

* *Undo: press ‘u’; redo: press “shift + u”*
* *Select an object: press 'ESC' and then click it, the object will be highlighted*
* *Move an object: Select it first (see the above Select step), then drag it*
* *Delete an object: Select it first, then press Delete on keyboard*
* *Press “f”: full view of current circuit*
* *Edit the properties: press 'q' and then click the object*
* *Un-select an object: press 'ESC' and then click the background*
* *Create instances: press 'i'*
* *Create narrow wires: press 'w'*
* *Name wires: press 'l'*