// decoder.sv

`timescale 1ns / 1ps

//////////////////////////////////////////////////////////////////////////////////

// Company:

// Engineer:

//

// Create Date: 05/13/2020 07:39:47 PM

// Design Name:

// Module Name: decoder

// Project Name:

// Target Devices:

// Tool Versions:

// Description:

//

// Dependencies:

//

// Revision:

// Revision 0.01 - File Created

// Additional Comments:

//

//////////////////////////////////////////////////////////////////////////////////

module divideby3FSM (input logic clk,

input logic reset,

output logic q);

typedef enum logic [1:0] {S0, S1, S2} statetype;

statetype [1:0] state, nextstate;

// state register

always\_ff @ (posedge clk, posedge reset)

if (reset) state <= S0;

else state <= nextstate;

// next state logic

always\_comb

case (state)

S0: nextstate = S1;

S1: nextstate = S2;

S2: nextstate = S0;

default: nextstate = S0;

endcase

// output logic

assign q = (state == S0);

endmodule

###################################################################

// fsm\_tb.sv

`timescale 1ns / 1ps

//////////////////////////////////////////////////////////////////////////////////

// Company:

// Engineer:

//

// Create Date: 05/13/2020 07:43:13 PM

// Design Name:

// Module Name: fsm\_tb

// Project Name:

// Target Devices:

// Tool Versions:

// Description:

//

// Dependencies:

//

// Revision:

// Revision 0.01 - File Created

// Additional Comments:

//

//////////////////////////////////////////////////////////////////////////////////

module fsm\_tb(

);

logic clk;

logic reset;

logic q;

//input logic clk,

//input logic reset,

//output logic q

divideby3FSM divideby3FSM\_uut(.clk(clk), .reset(reset), .q(q));

initial

begin

reset <=1;#20;

reset <=0;

end

always

begin

clk = 1; #50;

clk = 0; #50;

end

endmodule

################################################

#decoder.xdc

# Switches

set\_property PACKAGE\_PIN V17 [get\_ports {sw[0]}]

set\_property IOSTANDARD LVCMOS33 [get\_ports {sw[0]}]

set\_property PACKAGE\_PIN V16 [get\_ports {sw[1]}]

set\_property IOSTANDARD LVCMOS33 [get\_ports {sw[1]}]

set\_property PACKAGE\_PIN W16 [get\_ports {sw[2]}]

set\_property IOSTANDARD LVCMOS33 [get\_ports {sw[2]}]

# LEDs

set\_property PACKAGE\_PIN U16 [get\_ports {led[0]}]

set\_property IOSTANDARD LVCMOS33 [get\_ports {led[0]}]

set\_property PACKAGE\_PIN E19 [get\_ports {led[1]}]

set\_property IOSTANDARD LVCMOS33 [get\_ports {led[1]}]

set\_property PACKAGE\_PIN U19 [get\_ports {led[2]}]

set\_property IOSTANDARD LVCMOS33 [get\_ports {led[2]}]

set\_property PACKAGE\_PIN V19 [get\_ports {led[3]}]

set\_property IOSTANDARD LVCMOS33 [get\_ports {led[3]}]

set\_property PACKAGE\_PIN W18 [get\_ports {led[4]}]

set\_property IOSTANDARD LVCMOS33 [get\_ports {led[4]}]

set\_property PACKAGE\_PIN U15 [get\_ports {led[5]}]

set\_property IOSTANDARD LVCMOS33 [get\_ports {led[5]}]

set\_property PACKAGE\_PIN U14 [get\_ports {led[6]}]

set\_property IOSTANDARD LVCMOS33 [get\_ports {led[6]}]

set\_property PACKAGE\_PIN V14 [get\_ports {led[7]}]

set\_property IOSTANDARD LVCMOS33 [get\_ports {led[7]}]