Lab 5: Inverter Simulation using HSPICE

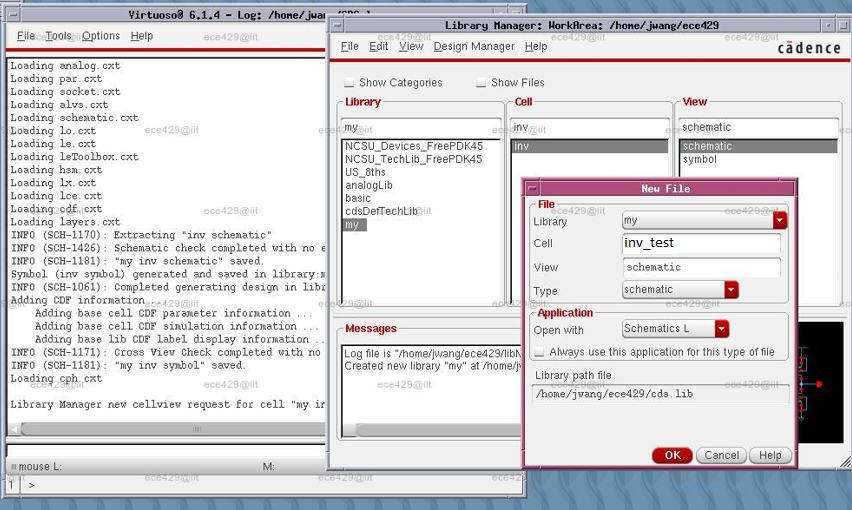
**Please check this tutorial frequently. Do not use your previously downloaded version since it might become an old version.**

**Warning: exit Cadence using File/Exit at Virtuoso 6.1.7-Log window to avoid lock of your account.**

In this lab we will create test circuit, and produce netlist in order for simulation of the circuit. Netlist is a text describing the node connection in the circuit and contains the transistor information (including transistor width) in the circuit in the lab. Simulation is a process of applying input values to the circuit and checking outputs for correctness. Millions of dollars will be saved by debugging in simulation instead of hardware.   
[**Inverter Simulation using HSPICE**](#Hspice)   
Steps:  
 a): [Creating Test Circuit](#TestCircuit)   
 b): [Exporting Hspice netlist](#ExportSPICE_NETLIST)

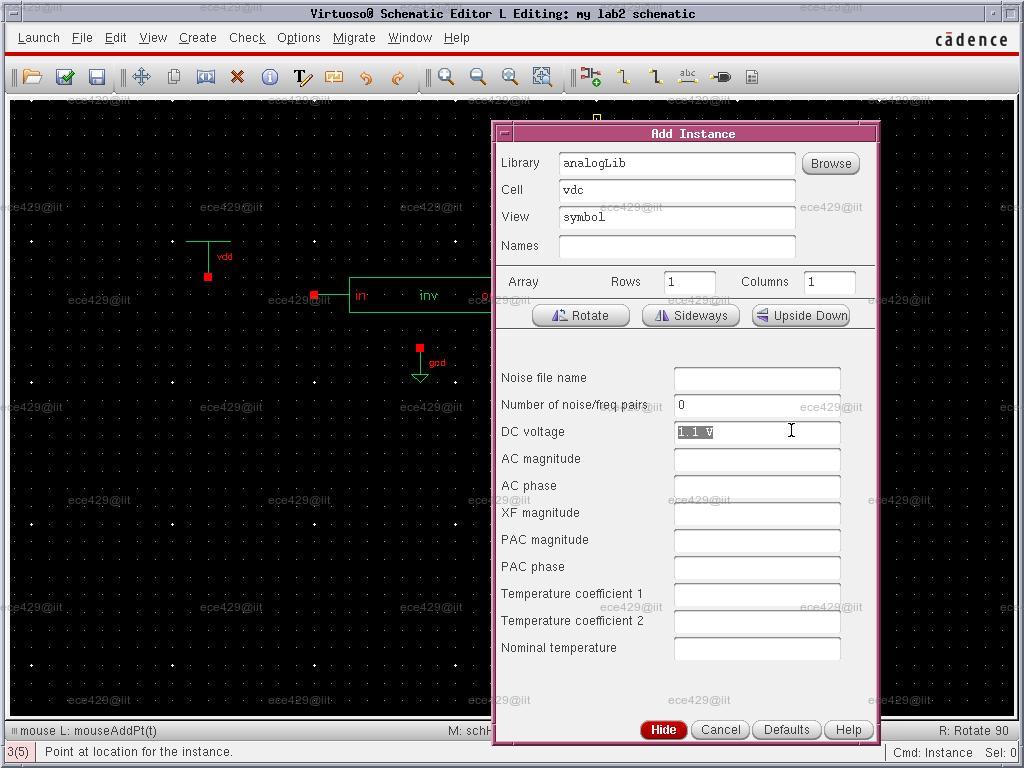
**a)** **Creating Testing Circuit**

We are now ready to draw a testing circuit to test our inverter schematic. For this purpose, while selecting ‘my’ from Library panel, using **File->New->Cell View,** create a cell called 'inv\_test' in the library 'my' and choose 'schematic' as its type

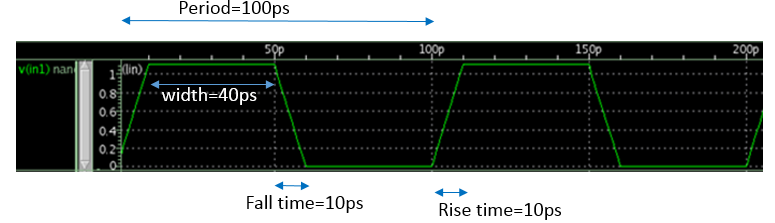


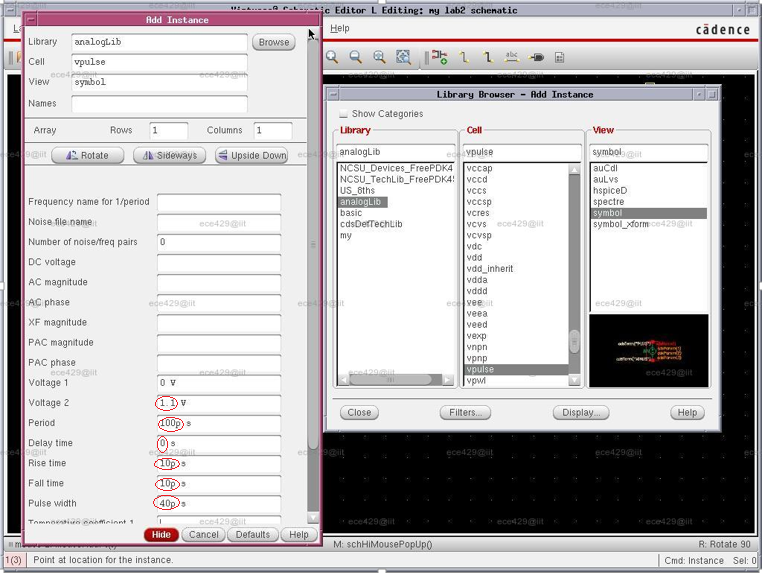
Similar to the inverter schematic, using **Create->Instance,** create an instance of our inverter from the 'symbol' view of the cell 'inv' in the library 'my' and place it. Moreover, using **Create->Instance,** introduce the global nets 'vdd' and 'gnd' from 'analogLib'.

To add excitations, using **Create->Instance,** first add an instance of 'vdc' from 'analogLib'. Modify its 'DC voltage' to 1.1 before placing it under 'vdd'.



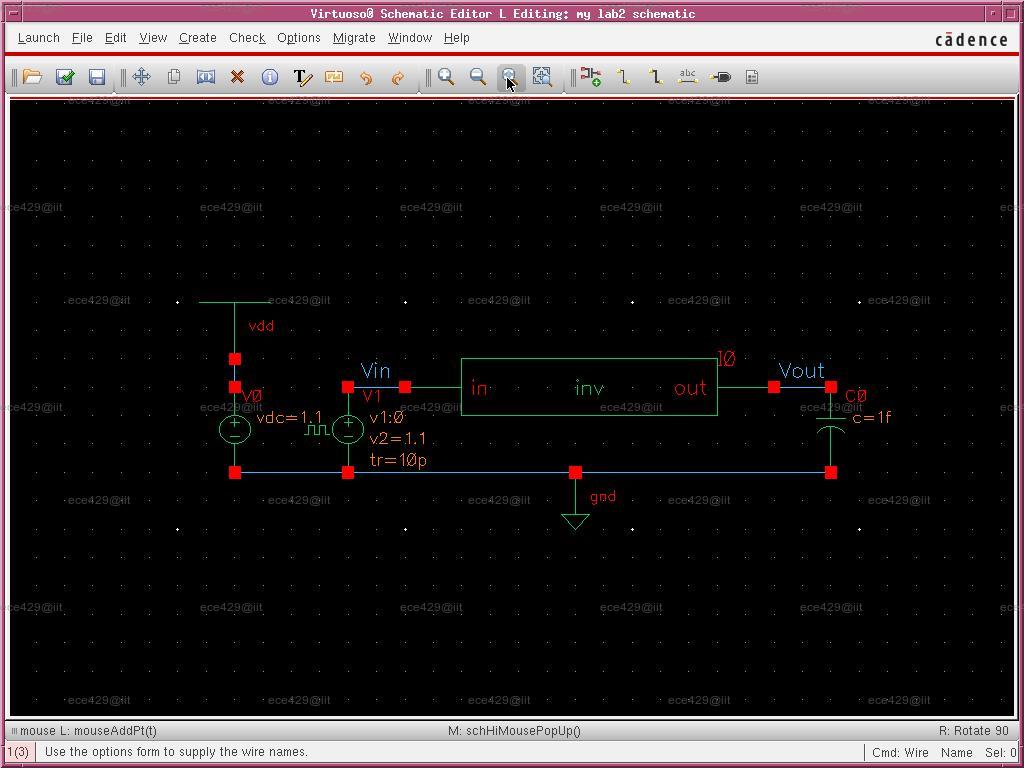
Next we need to provide an input to the circuit. We want to use the following pulse as input:

  
To create the above pulse, we add an instance of 'vpulse' from 'analogLib'. We need to add the following properties: 'Voltage 1'=0, 'Voltage 2'=1.1, 'Period'=100p, 'Delay time'=0, 'Rise time'=10p, 'Fall time'=10p, 'Pulse width'=40p. Note that you can change the properties of an instance after placing it by first selecting it and then clicking **Edit→Properties→Objects**.



*Note: only input those in red circle. Do not input “V” in voltage boxes and “s” in time boxes. They will be filled in automatically by the tool.*

Finally, add an instance of 'cap' from 'analogLib' with 'Capacitance'=1fF as the load of the inverter and wire the circuit as shown below. Note: it is not “1 f” or “1 pf”. Note: for a capacitor of “1f F” , first “f” is 10 to the power of -15; the second “F” is capacitor’s unit which stands for Faraday. Faraday was the scientist who contributed greatly to science.  
You may also want to use **Create→Wire Name** to name the input and the output wires of the inverter to 'Vin' and 'Vout' respectively, make sure that the wire name is attached to the wire .



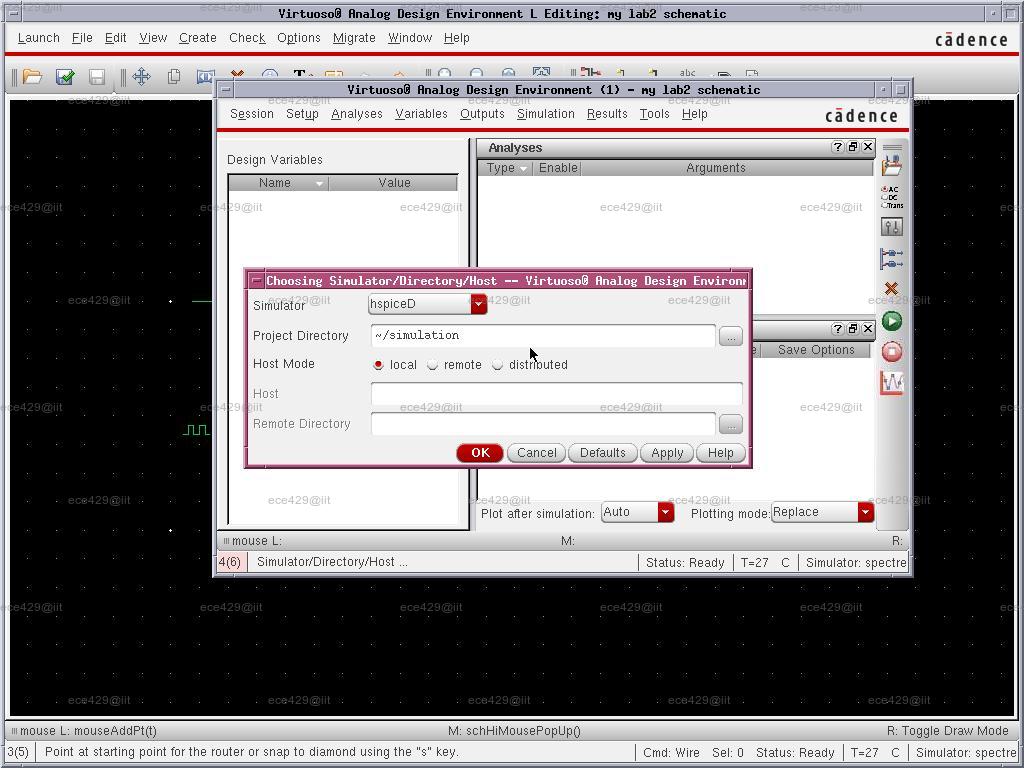
Click **File→Check and Save** to validate and store your design. There should be no error or warning.   
 [To to top](#Top)ease skip all of the following content at this moment.

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b)** **Exporting SPICE Netlist**

Although we can complete SPICE simulations within Virtuoso, we prefer to export a SPICE netlist from our schematic and to complete the simulations externally because the device parameters in SPICE netlists can be easily modified by any text editor.

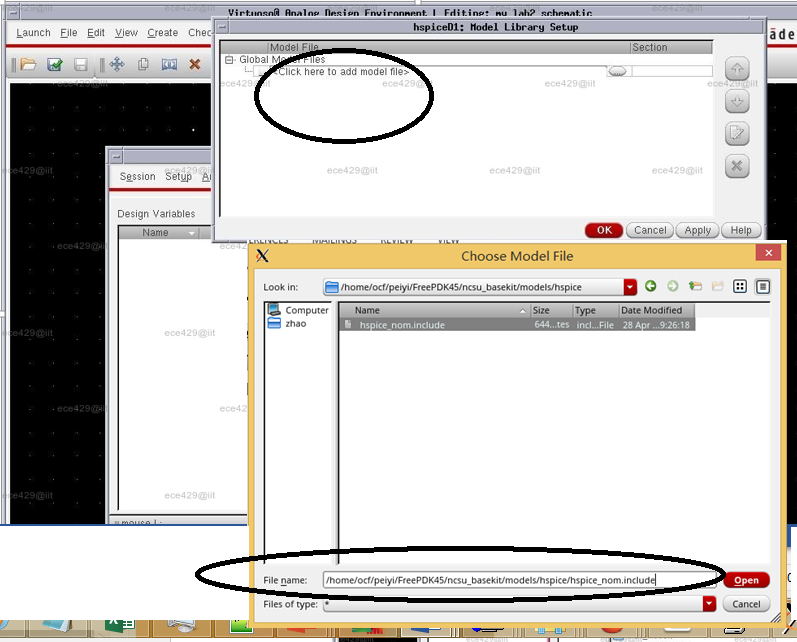
Inside Virtuoso Schematic Editor with the schematic open, click **Launch→ADE L** to bring out the Virtuoso Analog Design Environment(ADE) window.

Click **Setup→Simulator/Directory/Host** to bring out the Choosing Simulator/Directory/Host dialog box. Change 'Simulator' to 'hspiceD' and then click 'OK'.

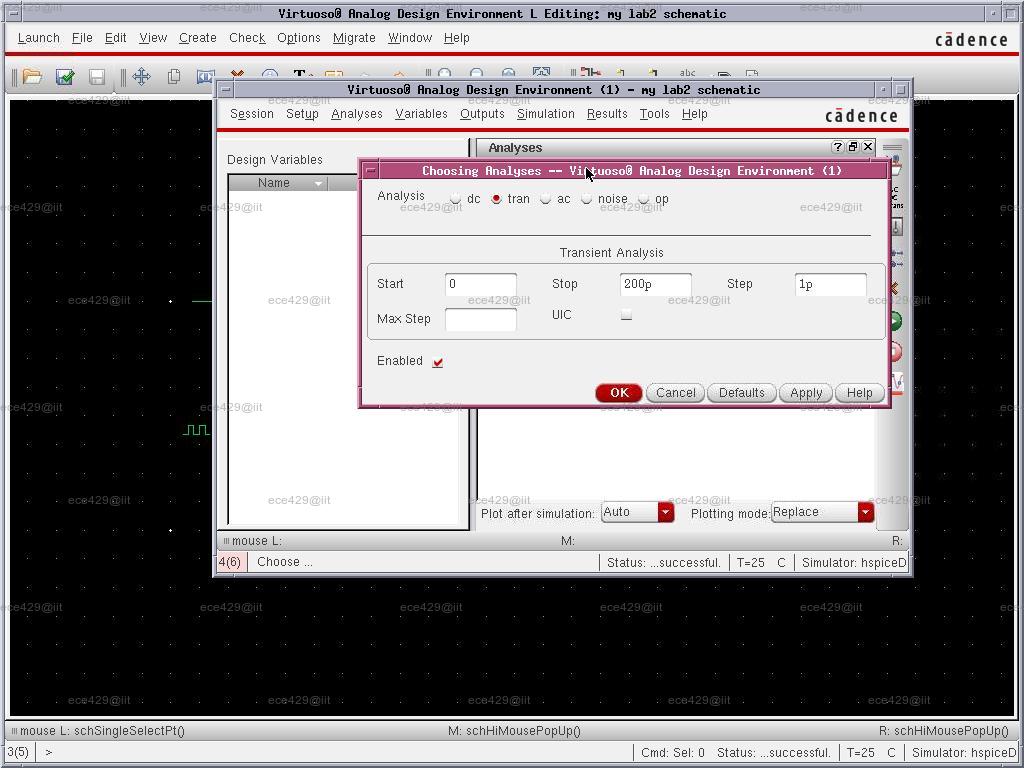


Click **Setup→Model Libraries** to bring out the Model Library Setup dialog box. Click 'Click here to add model file' and then click the '...' on the right. In the pop out window ‘Choose Model File’,

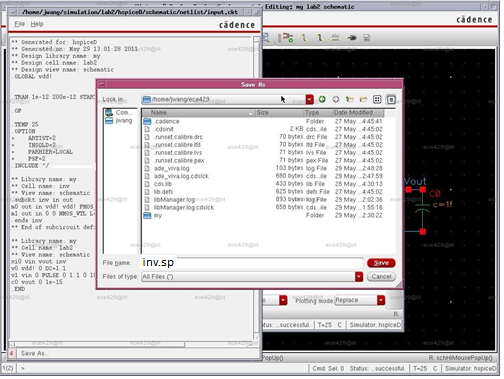
* 1. copy the following:   
   /home/ocf/peiyi/FreePDK45/ncsu\_basekit/models/hspice and **past** it into “File Name” box.
* 2. Then choose or type “hspice\_nom.include”.   
  3. Click OK to continue. to choose the file '/apps/FreePDK45/ncsu\_basekit/models/hspice/hspice\_nom.include'.



Click **Analyses→Choose** to bring out the Choosing Analyses dialog box. Choose 'tran' for 'Analysis' and modify the options for 'Transient Analysis' as follows: 'Start'=0, 'Stop'=200p, 'Step'=1p. Make sure it is 'Enabled' and click 'OK' to continue.



Click **Simulation→Netlist→Create** to generate the SPICE netlist. You should see a new window showing the netlist. Inside that window, click **File→Save As** to save it as 'inv.sp' in the directory 'simulation’.



**c) HSPICE Simulation**

In Unix command line, go to simulation folder:  
 ***cd ../simulation***

Use your favorite text editor to open 'inv.sp'; One recommended text editor is Nano (http://staffwww.fullcoll.edu/sedwards/Nano/IntroToNano.html). Add a line in inv.sp:

+ POST

just after the line

+ PSF=2

as part of the '.OPTION'. This command will instruct the HSPICE simulator to save the waveforms for every node in your circuit. You may also notice the line just below the added line

.INCLUDE '/home/ocf/peiyi/FreePDK45/ncsu\_basekit/models/hspice/hspice\_nom.include'

That's the model file we added a while ago.

In Unix command line run the simulation with the command:   
    **hspice inv.sp | tee lab2.hspice.output**  
This will at the same time show the progress in the terminal and save it to the file 'inv.hspice.output' for your future study.

Note: if after hspice command, the last line shows “hspice job concluded”, it means the simulation works. If the last line shows “hspice job aborted,” then check the error message. Sometimes it will say something like “error at line 7.”

**Next lab is verification of your schematic. We will check the waveform. The waveform tutorial is in anther file.**

**To exit Virtuoso, you must use File/exit to avoid a lock file.  
Warning: exit Cadence using File/Exit at Virtuoso 6.1.7-Log window to avoid lock of your account.**

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**Source:***Modified from* [*http://people.ece.umn.edu/help/cadence2/Cadence\_tutorial.html*](http://people.ece.umn.edu/help/cadence2/Cadence_tutorial.html)*,* [*http://www.ece.iit.edu/~jwang/ece429-2017s/tut01/schematic-spice.html*](http://www.ece.iit.edu/~jwang/ece429-2017s/tut01/schematic-spice.html)*.  
Other reference:* [*http://www.doe.carleton.ca/%7Eshams/ELEC4708/Lab1SchematicTut2014.pdf*](http://www.doe.carleton.ca/%7Eshams/ELEC4708/Lab1SchematicTut2014.pdf)*,* [*www.doe.carleton.ca/~shams/ELEC4708/Lab1LayoutTut2014.pdf*](http://www.doe.carleton.ca/~shams/ELEC4708/Lab1LayoutTut2014.pdf) *(to use later)*

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## Appendix. 1.Hotkeys for Schematic Editing

Here is the list of the hotkeys that would speed up your schematic drawing within Virtuoso Schematic Editor.

* Undo: press ‘u’; redo: press “shift + u”
* Select an object: press 'ESC' and then click it
* Edit the properties: press 'q' and then click the object
* Un-select an object: press 'ESC' and then click the background
* Press “f”: full view of current circuit
* Move an object: when no object is selected, press 'm' and then click it
* Create instances: press 'i'
* Create narrow wires: press 'w'
* Name wires: press 'l'

Note that the editor will always show the actions associated with the mouse buttons as well as the hints to complete an action at the bottom of the screen.

**2.Feedback from previous labs:**A)..If you are using B shell in your laptop, please change to C shell by typing “***csh***” in your command line  
  
B).. If you are using Mac machine, make sure XQuartz is started.  
     If you are using Windows machine, please start Xming, then Putty. In Putty, make sure that "***SSH/X11/Enable X11 forwarding***" is enabled and ***X display location is "localhost:0"***

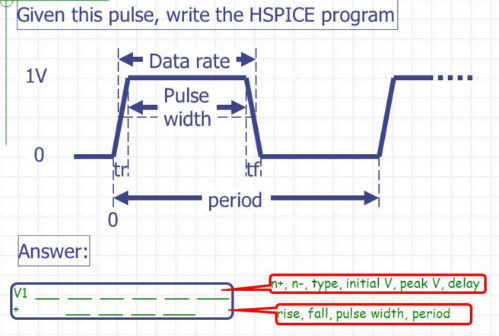
C).. When log in to Integrated Circuit Design server from command line, please use:

**ssh  -X   -Y   icd.chapman.edu**

D).. **To exit Virtuoso, you must use File/exit to avoid a lock file.**

E).. In you home directory, type "ls -al" , if you can not find .cshrc file, you have not setup your account in Lab1 correctly. Please setup your account according to instructions in Lab1:  
 *www1.chapman.edu/~zhao/CPSC330/Labs/Putty-Xming-VPN.pptx*

**2.Explanation of pulse**: start time, rise time, fall time, pulse width, period  
later in netlist you will see something like: *v1 vin gnd PULSE 0 1.1 0 10e-12 10e-12 40e-12 100e-12*



3. **When extract netlist, you may have error.**One possible error message: The property, 'connectivityLastUpdated', specified on library 'my’, cell 'inv’, view ‘schematgic', does not have an integer value. Re-extract the design (File->Check  
and Save menu option) to correct this error.  
**solution: File->Check and Save in Schematic View and Cell Symbol View respectively**