SEDRA/SMITH

Microelectronic Circuits

SEVENTH EDITION

Notes by Kevin Wang

June 12, 2023

Contents

Chapter 3

Semiconductors

Introduction

3.1 Intrinsic Semiconductors

3.2 Doped Semiconductors

3.3 Current Flow in Semiconductors

3.4 The *pn* Junction with an Applied Voltage

3.4.1 Qualitative Description of Junction Operation

3.4.2 The Current-Voltage Relationship of the Junction

3.4.3 Reverse Breakdown

3.5 Capacitive Effects in the *pn* Junction

2 ways charge can be stored in *pn* junction.

1. charge in depletion region (more visible when reverse bias)
2. minority charge in n and p material (more visible when forward bias)
   - concentration profile by injecting to n-dope
   - ” ” to p-dope

3.5.1 Depletion or Junction Capacitance

Assumption: *pn* junction reversed bias with V_R, charge on either side of junction:

$$Q_J = A\sqrt{2\epsilon_s q \frac{N_A N_D}{N_A + N_D}(V_0 + V_R)} = \alpha\sqrt{(V_0 + V_R)} \tag{3.1}$$

We denote α as $A\sqrt{2\epsilon_s q \frac{N_A N_D}{N_A+N_D}}$ and observe that $Q_J \not\propto V_R$ (also not linearly related)

- Hard to define capacitance that accounts for changing Q_J when V_R changes

  Assumption: junction operates as a point Q and define

$$C_j = \left.\frac{dQ_J}{dV_r}\right|_{V_R = V_Q} \tag{3.2}$$

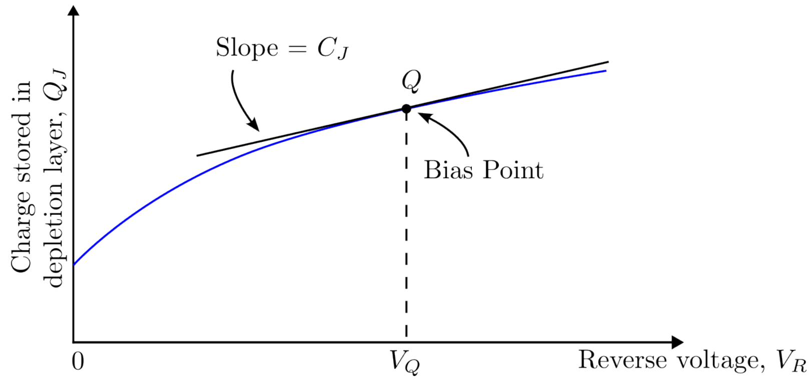

Figure 3.1: The charge stored on either side of the depletion layer as a function of the reverse voltage V_R

Note:-

The definition of capacitance

$$q = CV \implies C = q/V = \frac{\Delta q}{\Delta V}$$

- Equation 3.2 useful in electronic cct design
- This equation used in this book frequently
- Called the **"incremental-capacitance approach"**

Combining equations 3.2 with 3.1 we obtain:

$$C_j = \frac{\alpha}{2\sqrt{V_0 + V_R}} \tag{3.3}$$

We observe that C_j at reverse bias ($V_R = 0$) is $C_{j0} = \frac{\alpha}{2\sqrt{V_0}}$, so we can write C_j as

$$C_j = \frac{C_{j0}}{\sqrt{1 + \frac{V_R}{V_0}}} \tag{3.4}$$

Substituting for α, we obtain:

$$C_j = A\sqrt{\left(\frac{\epsilon_s q}{2}\right)\left(\frac{N_A N_D}{N_A + N_D}\right)\left(\frac{1}{V_0}\right)} \tag{3.5}$$

Before leaving concept of junction capacitance, we introduce

Definition 3.5.1: Terms

Abrupt junction: *pn* junction, doping concentration changes abruptly at junction boundary (this is deliberately done)
Graded junction: *pn* junction, carrier concentration changes gradually from one side to another.

If graded junction, then C_j becomes:

$$C_j = \frac{C_{j0}}{\left(1 + \frac{V_R}{V_0}\right)^m}$$

where m is the **Grading coefficient**

- m ranges from 1/3 to 1/2
- m depends on manner in which concentration changes from p to n side

Question 1: Exercise 3.14

For the pn ... cm^2.

Solution: Solution

3.5.2 Diffusion Capacitance

Consider: pn junction, forward bias:
Assume: in steady state

- Minority-carrier distributions in p and n regions as shown in ⟨Fig. 3.12⟩
  - Some minority charge carrier charges stored in p and n regions outside depletion region
- Changes in terminal voltage cause charges as mentioned ↑↑ to change before new steady state

This, completely different charge-storage phenomenon than 3.5.1

- Previous section was charge-storage of non-depletion region
- This section is charge-storage of depletion region

  We calculate excess minority-carrier charge ⟨Fig. 3.12⟩by taking shaded area under exponential
  Consider: excess hole charges in n region Q_p

$$\begin{aligned} Q_p &= Aq \times \text{shaded area under the } p_n(x) \text{ curve} \\ &= Aq \left[p_n(x_n) - p_{n0} \right] L_p \end{aligned} \tag{3.6}$$

Note:-

Recall area under exponential curve $Ae^{-x/B}$ is equal to AB

Doing some substitutions ⟨add sections⟩to Eq. (3.6):

$$Q_p = \frac{L_p^2}{D_p} I_p \tag{3.7}$$

We note that the factor $\frac{L_p^2}{D_p}$ relates Q_p to I_p is very useful parameter, and has dimensions of time (s). Thus we denote:

$$\tau_p = \frac{L_p^2}{D_p} \tag{3.8}$$

So:

$$Q_p = \tau_p I_p \tag{3.9}$$

Definition 3.5.2: Terms

Minority-carrier (hole) lifetime: Average time it takes for a hole injected into the n region to recombine with a majority electron, denoted τ_p

This definition has the following implications:

- Entire charge, Q_p disappears
- Q_p has to be replenished every τ_p seconds
- The current responsible for replenishing is I_p

Similarly for electrons charge in p region:

$$Q_n = \tau_n I_n \tag{3.10}$$

Where τ_n is electron lifespan in p region. Thus, the total excess minority-carrier charge:

$$Q = \tau_p I_p + \tau_n I_n \tag{3.11}$$

In terms of $I = I_p + I_n$, the diode current

$$Q = \tau_T I \tag{3.12}$$

Definition 3.5.3: Term

Mean transit time: For the junction, is equal to τ_T

We recognize that one side of junction more heavily doped than another. If $N_A >> N_D$:

- $I_p >> I_n$
- $I \approx I_p$
- $Q_p >> Q_n$
- $Q \approx Q_p$
- $\boxed{\tau_T \approx \tau_p}$

Definition 3.5.4: Term

Incremental diffusion capacitance: Defined C_d, for small changes around a bias point:

$$C_d = \frac{dQ}{dV} = \left(\frac{\tau_T}{V_T}\right) I \tag{3.13}$$

Where I is the forward-bias current

Note:

- $C_d \propto I$
  - Because of this, C_d negligibly small when reverse bias
- To keep C_d small, transit time must be small
  - Important requirement for pn junction for high-speed or high-frequency

Question 2: Exercise 3.15

Use the definition . . .
Solution: Solution

Question 3: Exercise 3.16

For the pn . . .
Solution: Solution

Chapter 4

Diodes

Introduction

- Diodes are the most simple and fundamental non-linear CCT
- Similar to resistor: 2 terminals
- Dissimilar to resistor: nonlinear $i - v$

Roadmap:

1. Ideal diode
2. Silicon junction diode
   (a) Terminal characteristics
   (b) Analysis diode CCT
3. Device modelling
4. Rectifiers
5. Photodiodes and LEDs
6. $\boxed{\text{Diode is nothing more than a } pn\text{-junction}}$

4.1 The Ideal Diode