



# TLC5947 24-Channel, 12-Bit PWM LED Driver With Internal Oscillator

## 1 Features

- 24 Channels, Constant-Current Sink Output
- 30-mA Capability (Constant-Current Sink)
- 12-Bit (4096 Steps) PWM Grayscale Control
- LED Power-Supply Voltage Up to 30 V
- $V_{CC} = 3.0\text{ V to }5.5\text{ V}$
- Constant-Current Accuracy:
  - Channel-to-Channel =  $\pm 2\%$  (Typical)
  - Device-to-Device =  $\pm 2\%$  (Typical)
- CMOS Logic Level I/O
- 30-MHz Data Transfer Rate (Standalone)
- 15-MHz Data Transfer Rate (Cascaded Devices, SCLK Duty = 50%)
- Shift Out Data Changes With Falling Edge to Avoid Data Shift Errors
- Auto Display Repeat
- 4-MHz Internal Oscillator
- Thermal Shutdown (TSD):
  - Automatic Shutdown at OverTemperature Conditions
  - Restart Under Normal Temperature
- Noise Reduction:
  - 4-Channel Grouped Delay to Prevent Inrush Current
- Operating Temperature:  $-40^{\circ}\text{C to }85^{\circ}\text{C}$

## 2 Applications

- Static LED Displays
- Message Boards
- Amusement Illumination
- TV Backlighting

## 3 Description

The TLC5947 is a 24-channel, constant-current sink LED driver. Each channel is individually adjustable with 4096 pulse-width modulated (PWM) steps. PWM control is repeated automatically with the programmed grayscale (GS) data. GS data are written via a serial interface port. The current value of all 24 channels is set by a single external resistor.

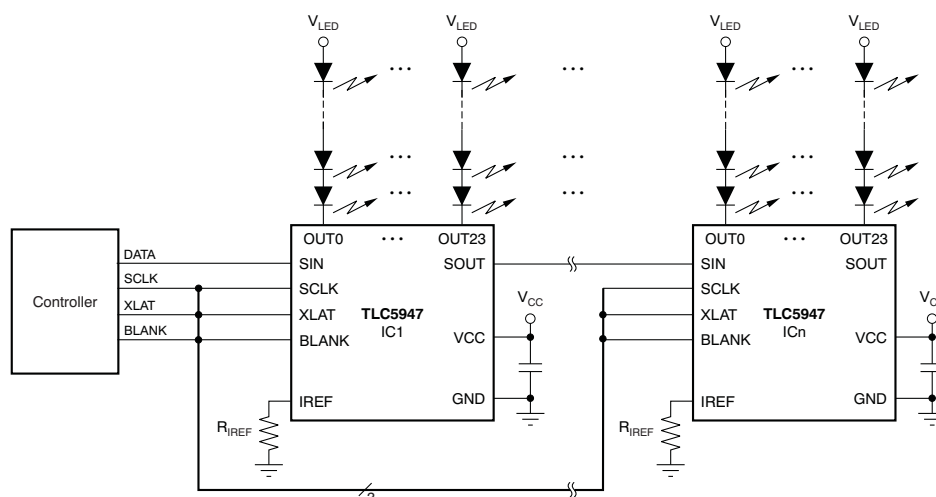
The TLC5947 has a thermal shutdown (TSD) function that turns off all output drivers during an over-temperature condition. All of the output drivers automatically restart when the temperature returns to normal conditions.

### Device Information<sup>(1)</sup>

PART NUMBER	PACKAGE	BODY SIZE (NOM)
TLC5947	HTSSOP (32)	11.00 mm × 6.20 mm
	VQFN (32)	5.00 mm × 5.00 mm

(1) For all available packages, see the orderable addendum at the end of the datasheet.

### Application Circuit



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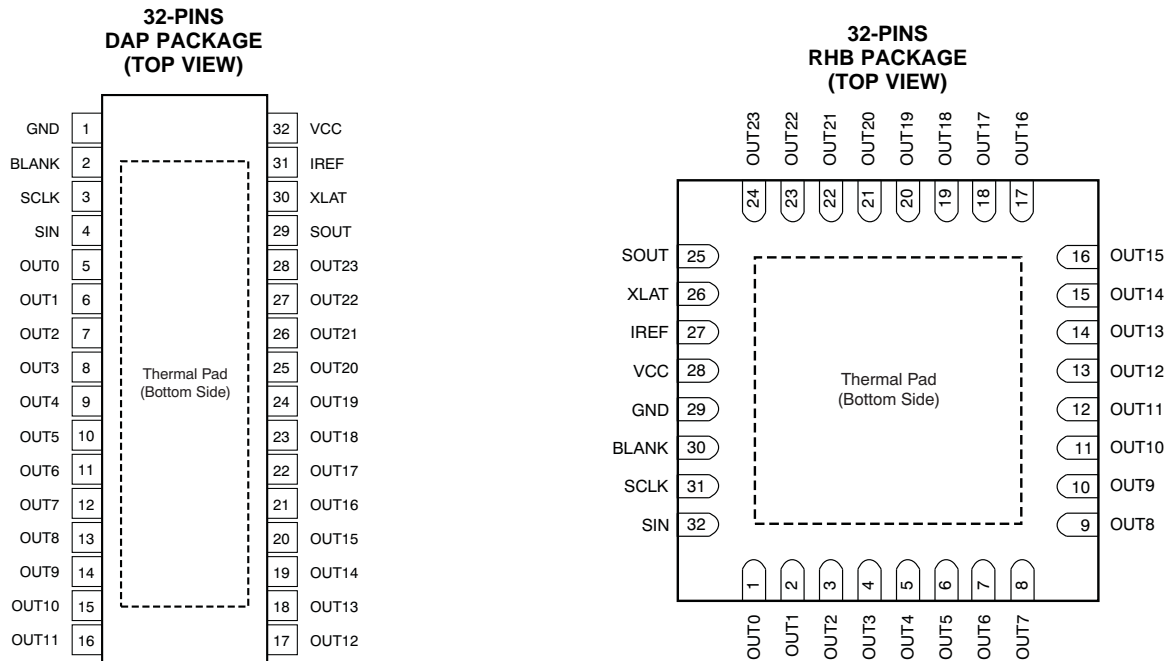
## 4 Revision History

### Changes from Revision A (September 2008) to Revision B

Page

- Added *Pin Configuration and Functions* section, *ESD Ratings* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section ..... **1**

## 5 Pin Configuration and Functions



### Pin Functions

PIN			I/O	DESCRIPTION
NAME	RHB NO.	DAP NO.		
BLANK	30	2	I	Blank (all constant-current outputs off). When BLANK is high, all constant-current outputs (OUT0 through OUT23) are forced off, the grayscale PWM timing controller initializes, and the grayscale counter resets to '0'. When BLANK is low, all constant-current outputs are controlled by the grayscale PWM timing controller.
GND	29	1	—	Power ground
IREF	27	31	I/O	This pin sets the constant-current value. OUT0 through OUT23 constant sink current is set to the desired value by connecting an external resistor between IREF and GND.
OUT0	1	5	O	Constant-current output. Multiple outputs can be tied together to increase the constant-current capability. Different voltages can be applied to each output.
OUT1	2	6	O	Constant-current output
OUT2	3	7	O	Constant-current output
OUT3	4	8	O	Constant-current output
OUT4	5	9	O	Constant-current output
OUT5	6	10	O	Constant-current output
OUT6	7	11	O	Constant-current output
OUT7	8	12	O	Constant-current output
OUT8	9	13	O	Constant-current output
OUT9	10	14	O	Constant-current output
OUT10	11	15	O	Constant-current output
OUT11	12	16	O	Constant-current output
OUT12	13	17	O	Constant-current output
OUT13	14	18	O	Constant-current output
OUT14	15	19	O	Constant-current output
OUT15	16	20	O	Constant-current output
OUT16	17	21	O	Constant-current output

## Pin Functions (continued)

PIN			I/O	DESCRIPTION
NAME	RHB NO.	DAP NO.		
OUT17	18	22	O	Constant-current output
OUT18	19	23	O	Constant-current output
OUT19	20	24	O	Constant-current output
OUT20	21	25	O	Constant-current output
OUT21	22	26	O	Constant-current output
OUT22	23	27	O	Constant-current output
OUT23	24	28	O	Constant-current output
SCLK	31	3	I	Serial data shift clock. Schmitt buffer input. Data present on the SIN pin are shifted into the shift register with the rising edge of the SCLK pin. Data are shifted to the MSB side by 1-bit synchronizing of the rising edge of SCLK. The MSB data appears on SOUT at the falling edge of SCLK. A rising edge on the SCLK input is allowed 100 ns after an XLAT rising edge.
SIN	32	4	I	Serial input for grayscale data
SOUT	25	29	O	Serial data output. This output is connected to the shift register placed after the MSB of the grayscale shift register. Therefore, the MSB data of the grayscale shift register appears at the falling edge of SCLK. This function reduces the data shifting errors caused by small timing margins between SIN and SCLK.
VCC	28	32	—	Power-supply voltage
XLAT	26	30	I	The data in the grayscale shift register are moved to the grayscale data latch with a low-to-high transition on this pin. When the XLAT rising edge is input, all constant-current outputs are forced off until the next grayscale display period. The grayscale counter is not reset to zero with a rising edge of XLAT.

## 6 Specifications

### 6.1 Absolute Maximum Ratings

Over operating free-air temperature range, unless otherwise noted.<sup>(1)(2)</sup>

		MIN	MAX	UNIT
V <sub>CC</sub>	Supply voltage: V <sub>CC</sub>	−0.3	6.0	V
I <sub>O</sub>	Output current (dc)	OUT0 to OUT23		38
				mA
V <sub>I</sub>	Input voltage	−0.3	V <sub>CC</sub> + 0.3	V
V <sub>O</sub>	Output voltage	SOUT		−0.3
		OUT0 to OUT23		V <sub>CC</sub> + 0.3
		−0.3	33	V
T <sub>J(MAX)</sub>	Operating junction temperature		150	°C
T <sub>stg</sub>	Storage temperature	−55	150	°C

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) All voltage values are with respect to network ground terminal.

### 6.2 ESD Ratings

		VALUE	UNIT
V <sub>(ESD)</sub>	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins <sup>(1)</sup>	±2500
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins <sup>(2)</sup>	±500
			V

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
- (2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

### 6.3 Recommended Operating Conditions

At  $T_A = -40^{\circ}\text{C}$  to  $85^{\circ}\text{C}$ , unless otherwise noted.

		MIN	NOM	MAX	UNIT
<b>DC CHARACTERISTICS: <math>V_{CC} = 3\text{ V}</math> to <math>5.5\text{ V}</math></b>					
$V_{CC}$	Supply voltage	3.0		5.5	V
$V_O$	Voltage applied to output OUT0 to OUT23			30	V
$V_{IH}$	High-level input voltage	$0.7 \times V_{CC}$		$V_{CC}$	V
$V_{IL}$	Low-level input voltage	GND		$0.3 \times V_{CC}$	V
$I_{OH}$	High-level output current SOUT			-3	mA
$I_{OL}$	Low-level output current SOUT			3	mA
$I_{OLC}$	Constant output sink current OUT0 to OUT23	2		30	mA
$T_A$	Operating free-air temperature range	-40		85	$^{\circ}\text{C}$
$T_J$	Operating junction temperature	-40		125	$^{\circ}\text{C}$
<b>AC CHARACTERISTICS: <math>V_{CC} = 3\text{ V}</math> to <math>5.5\text{ V}</math></b>					
$f_{SCLK}$	Data shift clock frequency	SCLK, Standalone operation		30	MHz
		SCLK, Duty 50%, cascade operation		15	MHz
$T_{WH0}$	Pulse duration	SCLK = High-level pulse width		12	ns
$T_{WL0}$		SCLK = Low-level pulse width		10	ns
$T_{WH1}$		XLAT, BLANK High-level pulse width		30	ns
$T_{SU0}$	Setup time	SIN-SCLK $\uparrow$		5	ns
$T_{SU1}$		XLAT $\uparrow$ -SCLK $\uparrow$		100	ns
$T_{SU2}$		XLAT $\uparrow$ -BLANK $\downarrow$		30	ns
$T_{H0}$	Hold time	SIN-SCLK $\uparrow$		3	ns
$T_{H1}$		XLAT $\uparrow$ -SCLK $\uparrow$		10	ns

### 6.4 Thermal Information

THERMAL METRIC <sup>(1)</sup>		TLC5947	UNIT
		DAP	
		32 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	32.8	$^{\circ}\text{C}/\text{W}$
$R_{\theta JC(\text{top})}$	Junction-to-case (top) thermal resistance	17.1	
$R_{\theta JB}$	Junction-to-board thermal resistance	17.9	
$\Psi_{JT}$	Junction-to-top characterization parameter	0.4	
$\Psi_{JB}$	Junction-to-board characterization parameter	17.8	
$R_{\theta JC(\text{bot})}$	Junction-to-case (bottom) thermal resistance	1.3	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, [SPRA953](#).

### 6.5 Dissipation Ratings

PACKAGE	OPERATING FACTOR ABOVE $T_A = 25^{\circ}\text{C}$	$T_A < 25^{\circ}\text{C}$ POWER RATING	$T_A = 70^{\circ}\text{C}$ POWER RATING	$T_A = 85^{\circ}\text{C}$ POWER RATING
HTSSOP-32 with PowerPAD™ soldered <sup>(1)</sup>	42.54 mW/ $^{\circ}\text{C}$	5318 mW	3403 mW	2765 mW
HTSSOP-32 with PowerPAD not soldered <sup>(2)</sup>	22.56 mW/ $^{\circ}\text{C}$	2820 mW	1805 mW	1466 mW
QFN-32 <sup>(3)</sup>	27.86 mW/ $^{\circ}\text{C}$	3482 mW	2228 mW	1811 mW

(1) With PowerPAD soldered onto copper area on printed circuit board (PCB); 2 oz. copper. For more information, see [SLMA002](#).

(2) With PowerPAD not soldered onto copper area on PCB.

(3) The package thermal impedance is calculated in accordance with JESD51-5.

## 6.6 Electrical Characteristics

At  $V_{CC} = 3.0\text{ V}$  to  $5.5\text{ V}$  and  $T_A = -40^\circ\text{C}$  to  $85^\circ\text{C}$ . Typical values at  $V_{CC} = 3.3\text{ V}$  and  $T_A = 25^\circ\text{C}$ , unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{OH}$	High-level output voltage	$I_{OH} = -3\text{ mA}$ at SOUT	$V_{CC} - 0.4$		$V_{CC}$	V
$V_{OL}$	Low-level output voltage	$I_{OL} = 3\text{ mA}$ at SOUT			0.4	V
$I_{IN}$	Input current	$V_{IN} = V_{CC}$ or GND at SIN, XLAT, and BLANK	-1		1	$\mu\text{A}$
$I_{CC1}$	Supply current ( $V_{CC}$ )	SIN/SCLK/XLAT = low, BLANK = high, $V_{OUTn} = 1\text{ V}$ , $R_{IREF} = 24\text{ k}\Omega$		0.5	3	mA
$I_{CC2}$		SIN/SCLK/XLAT = low, BLANK = high, $V_{OUTn} = 1\text{ V}$ , $R_{IREF} = 3.3\text{ k}\Omega$		1	6	mA
$I_{CC3}$		SIN/SCLK/XLAT = low, BLANK = low, $V_{OUTn} = 1\text{ V}$ , $R_{IREF} = 3.3\text{ k}\Omega$ , $GSn = \text{FFH}$		15	45	mA
$I_{CC4}$		SIN/SCLK/XLAT = low, BLANK = low, $V_{OUTn} = 1\text{ V}$ , $R_{IREF} = 1.6\text{ k}\Omega$ , $GSn = \text{FFH}$		30	90	mA
$I_{OLC}$	Constant output current	All $OUTn = \text{ON}$ , $V_{OUTn} = 1\text{ V}$ , $V_{OUTfix} = 1\text{ V}$ , $R_{IREF} = 1.6\text{ k}\Omega$	27.7	30.75	33.8	mA
$I_{OLK}$	Output leakage current	BLANK = high, $V_{OUTn} = 30\text{ V}$ , $R_{IREF} = 1.6\text{ k}\Omega$ , At $OUT0$ to $OUT23$			0.1	$\mu\text{A}$
$\Delta I_{OLC}$	Constant-current error (channel-to-channel) <sup>(1)</sup>	All $OUTn = \text{ON}$ , $V_{OUTn} = 1\text{ V}$ , $V_{OUTfix} = 1\text{ V}$ , $R_{IREF} = 1.6\text{ k}\Omega$ , At $OUT0$ to $OUT23$	-4%	$\pm 2\%$	4%	
$\Delta I_{OLC1}$	Constant-current error (device-to-device) <sup>(2)</sup>	All $OUTn = \text{ON}$ , $V_{OUTn} = 1\text{ V}$ , $V_{OUTfix} = 1\text{ V}$ , $R_{IREF} = 1.6\text{ k}\Omega$	-7%	$\pm 2\%$	7%	
$\Delta I_{OLC2}$	Line regulation <sup>(3)</sup>	All $OUTn = \text{ON}$ , $V_{OUTn} = 1\text{ V}$ , $V_{OUTfix} = 1\text{ V}$ , $R_{IREF} = 1.6\text{ k}\Omega$ , At $OUT0$ to $OUT23$		$\pm 1$	$\pm 3$	%/V
$\Delta I_{OLC3}$	Load regulation <sup>(4)</sup>	All $OUTn = \text{ON}$ , $V_{OUTn} = 1\text{ V}$ to $3\text{ V}$ , $V_{OUTfix} = 1\text{ V}$ , $R_{IREF} = 1.6\text{ k}\Omega$ , At $OUT0$ to $OUT23$		$\pm 2$	$\pm 6$	%/V
$T_{DOWN}$	Thermal shutdown threshold	Junction temperature <sup>(5)</sup>	150	162	175	$^\circ\text{C}$
$T_{HYS}$	Thermal error hysteresis	Junction temperature <sup>(5)</sup>	5	10	20	$^\circ\text{C}$
$V_{IREF}$	Reference voltage output	$R_{IREF} = 1.6\text{ k}\Omega$	1.16	1.20	1.24	V

- (1) The deviation of each output from the average of  $OUT0$ – $OUT23$  constant-current. Deviation is calculated by the formula:

$$\Delta (\%) = \left[ \frac{\frac{I_{OUTn}}{(I_{OUT0} + I_{OUT1} + \dots + I_{OUT22} + I_{OUT23})} - 1}{24} \right] \times 100$$

- (2) The deviation of the  $OUT0$ – $OUT23$  constant-current average from the ideal constant-current value. Deviation is calculated by the following formula:

$$\Delta (\%) = \left[ \frac{\frac{(I_{OUT0} + I_{OUT1} + \dots + I_{OUT22} + I_{OUT23})}{24} - (\text{Ideal Output Current})}{\text{Ideal Output Current}} \right] \times 100$$

Ideal current is calculated by the formula:

$$I_{OUT(\text{IDEAL})} = 41 \times \left[ \frac{1.20}{R_{IREF}} \right]$$

- (3) Line regulation is calculated by this equation:

$$\Delta (\%/V) = \left[ \frac{(I_{OUTn} \text{ at } V_{CC} = 5.5\text{ V}) - (I_{OUTn} \text{ at } V_{CC} = 3.0\text{ V})}{(I_{OUTn} \text{ at } V_{CC} = 3.0\text{ V})} \right] \times \frac{100}{5.5\text{ V} - 3\text{ V}}$$

- (4) Load regulation is calculated by the equation:

$$\Delta (\%/V) = \left[ \frac{(I_{OUTn} \text{ at } V_{OUTn} = 3\text{ V}) - (I_{OUTn} \text{ at } V_{OUTn} = 1\text{ V})}{(I_{OUTn} \text{ at } V_{OUTn} = 1\text{ V})} \right] \times \frac{100}{3\text{ V} - 1\text{ V}}$$

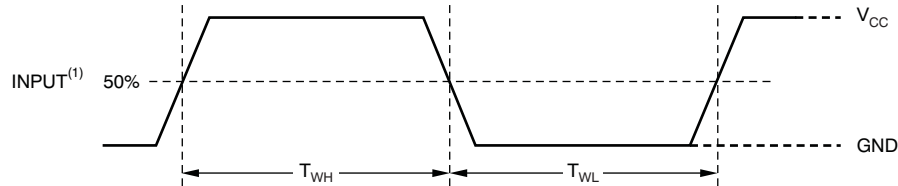
- (5) Not tested. Specified by design.

## 6.7 Switching Characteristics

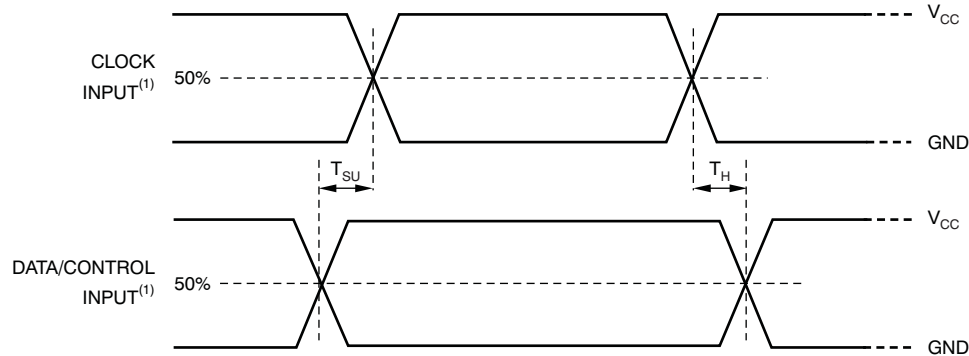
At  $V_{CC} = 3.0\text{ V}$  to  $5.5\text{ V}$ ,  $T_A = -40^\circ\text{C}$  to  $85^\circ\text{C}$ ,  $C_L = 15\text{ pF}$ ,  $R_L = 150\ \Omega$ ,  $R_{REF} = 1.6\text{ k}\Omega$ , and  $V_{LED} = 5.5\text{ V}$ . Typical values at  $V_{CC} = 3.3\text{ V}$  and  $T_A = 25^\circ\text{C}$ , unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{R0}$	Rise time	SOUT		10	15	ns
$t_{R1}$		OUTn		15	40	ns
$t_{F0}$	Fall time	SOUT		10	15	ns
$t_{F1}$		OUTn		100	300	ns
$f_{OSC}$	Internal oscillator frequency		2.4	4	5.6	MHz
$t_{D0}$	Propagation delay time	SCLK↓ to SOUT		15	25	ns
$t_{D1}$		BLANK↑ to OUT0 sink current off		20	40	ns
$t_{D2}$		OUT0 current on to OUT1/5/9/13/17/21 current on	15	24	33	ns
$t_{D3}$		OUT0 current on to OUT2/6/10/14/18/22 current on	30	48	66	ns
$t_{D4}$		OUT0 current on to OUT3/7/11/15/19/23 current on	45	72	99	ns

$T_{WH0}$ ,  $T_{WL0}$ ,  $T_{WH1}$ :

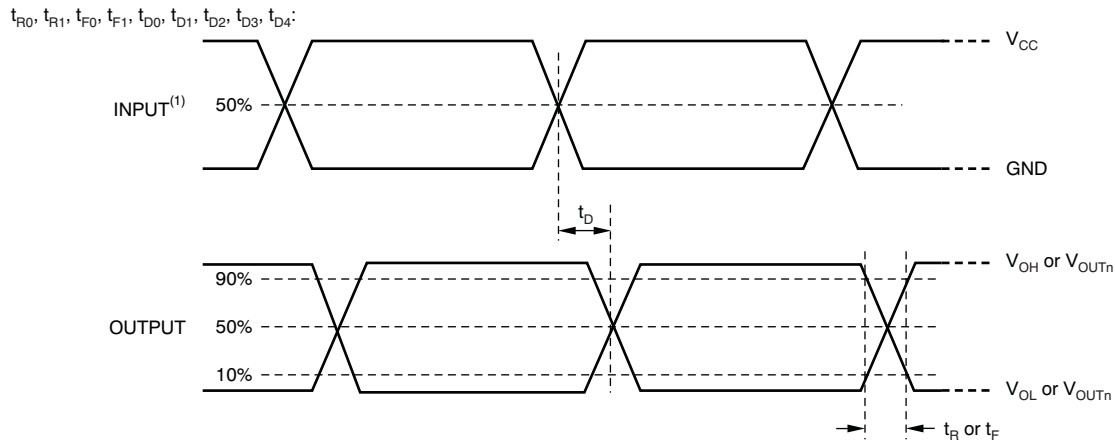


$T_{SU0}$ ,  $T_{SU1}$ ,  $T_{SU2}$ ,  $T_{H0}$ ,  $T_{H1}$ :

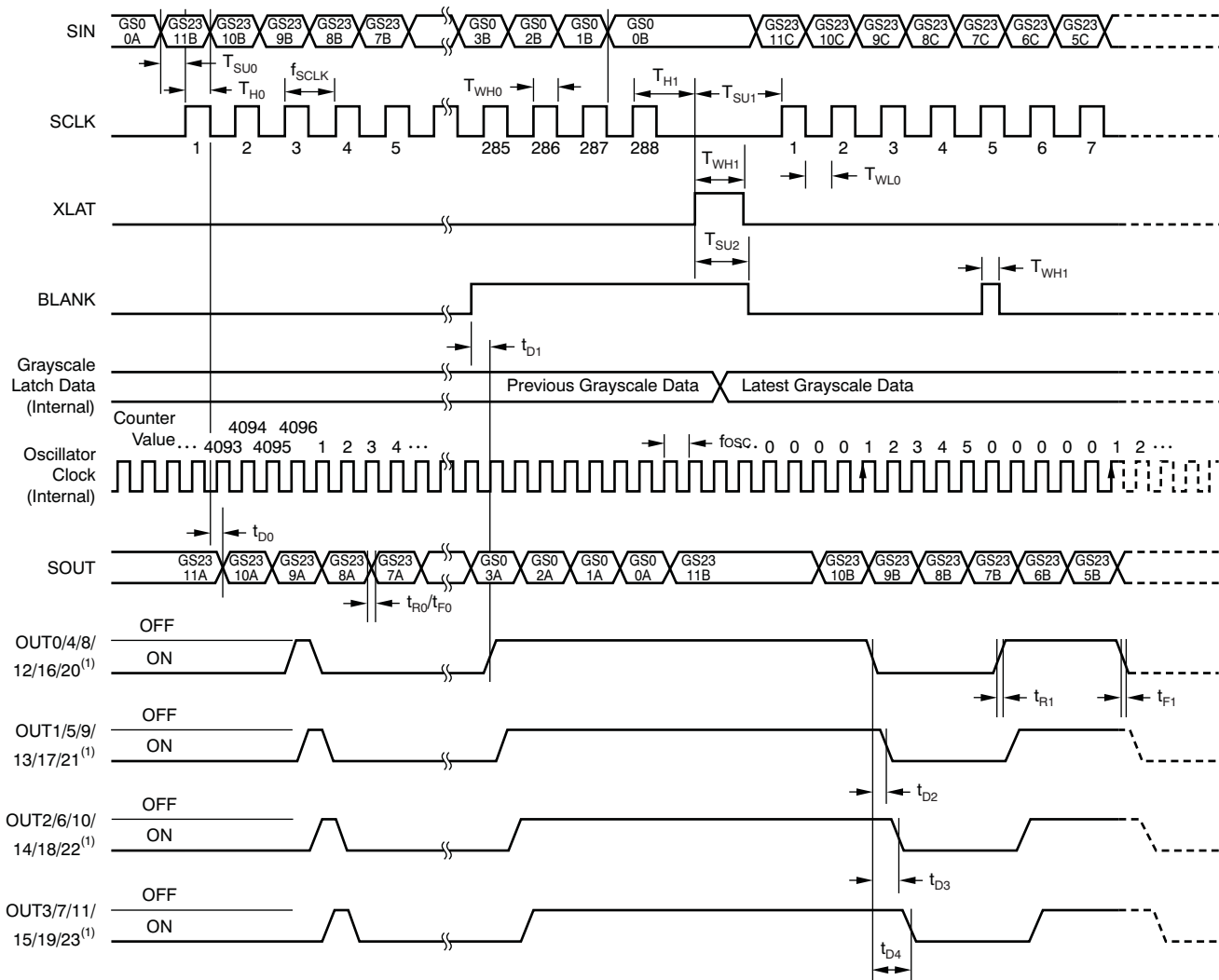


(1) Input pulse rise and fall time is 1 ns to 3 ns.

**Figure 1. Input Timing**



(1) Input pulse rise and fall time is 1 ns to 3 ns.

**Figure 2. Output Timing**


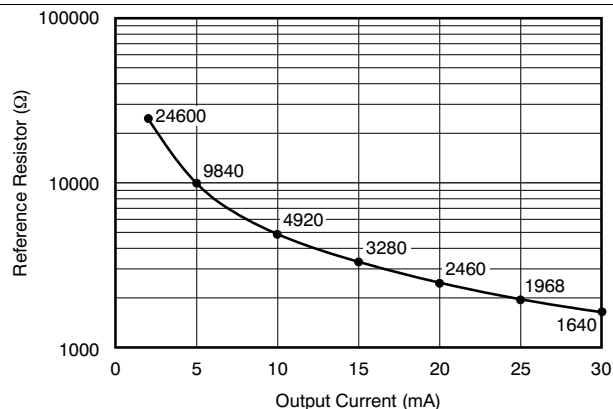
(1) GS data = FFFh.

**Figure 3. Grayscale Data Write and OUTn Operation Timing**

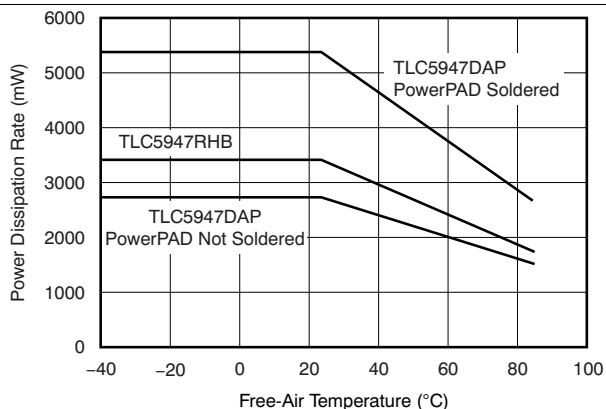


## 6.8 Typical Characteristics

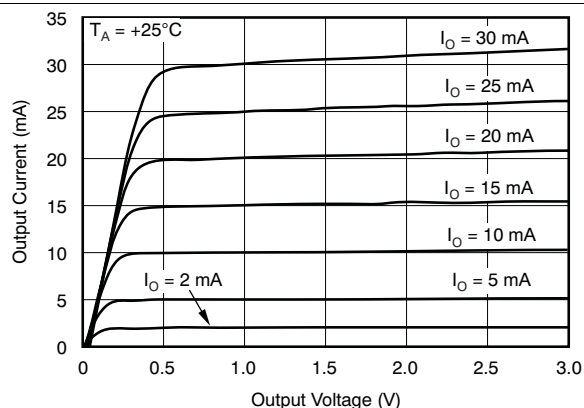
At  $V_{CC} = 3.3\text{ V}$  and  $T_A = 25^\circ\text{C}$ , unless otherwise noted.



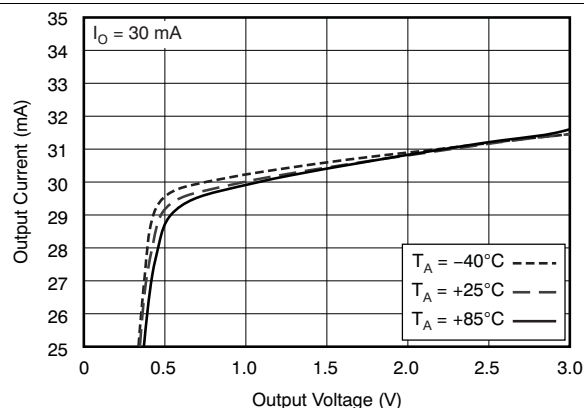
**Figure 4. Reference Resistor vs Output Current**



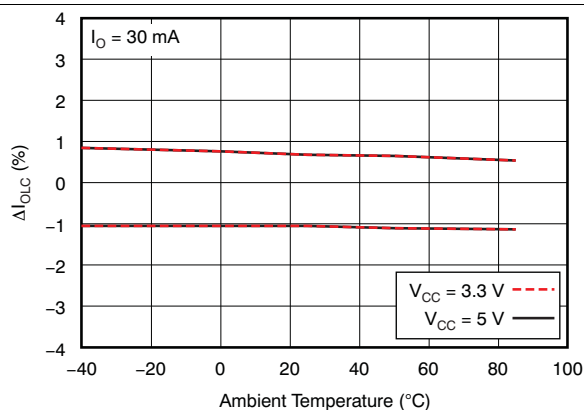
**Figure 5. Power Dissipation Rate vs Free-Air Temperature**



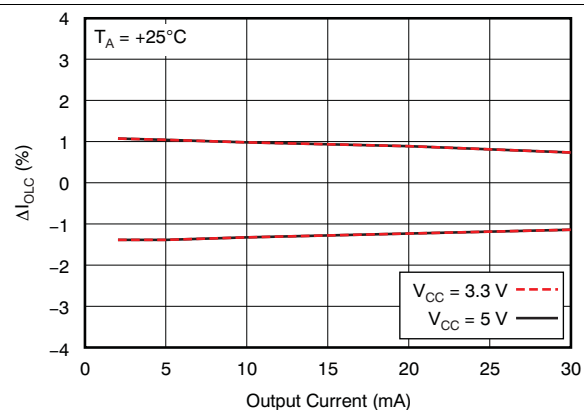
**Figure 6. Output Current vs Output Voltage**



**Figure 7. Output Current vs Output Voltage**



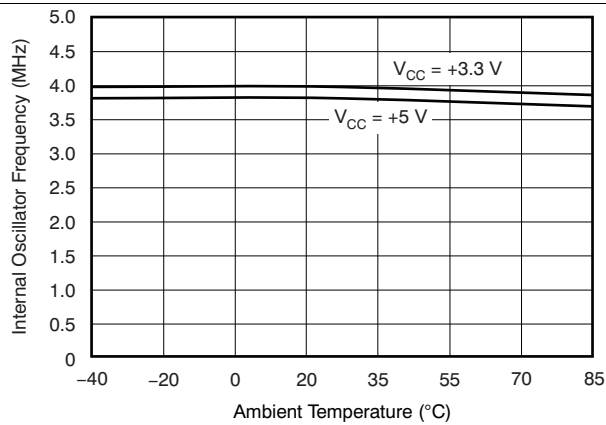
**Figure 8.  $\Delta I_{OLC}$  vs Ambient Temperature**



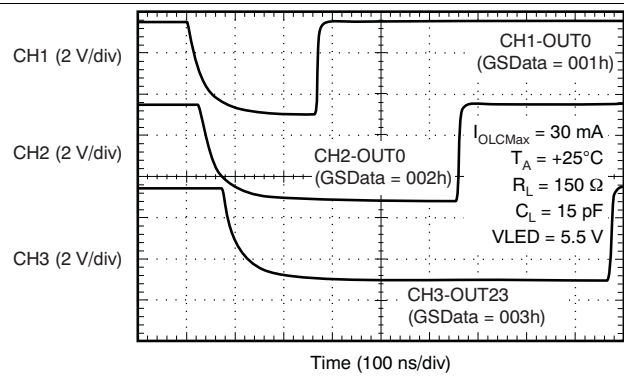
**Figure 9.  $\Delta I_{OLC}$  vs Output Current**

## Typical Characteristics (continued)

At  $V_{CC} = 3.3\text{ V}$  and  $T_A = 25^\circ\text{C}$ , unless otherwise noted.



**Figure 10. Internal Oscillator Frequency vs Ambient Temperature**



**Figure 11. Constant-Current Output Voltage Waveform**

## 7 Parameter Measurement Information

### 7.1 Pin Equivalent Input and Output Schematic Diagrams

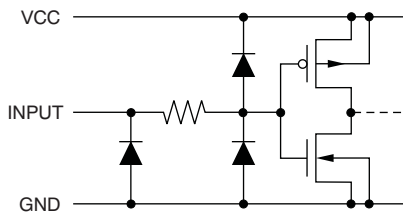


Figure 12. SIN, SCLK, XLAT, BLANK

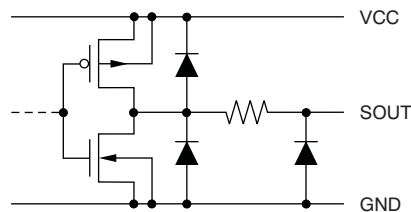


Figure 13. SOUT

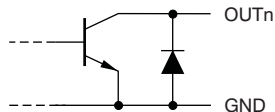


Figure 14. OUT0 Through OUT23

### 7.2 Test Circuits

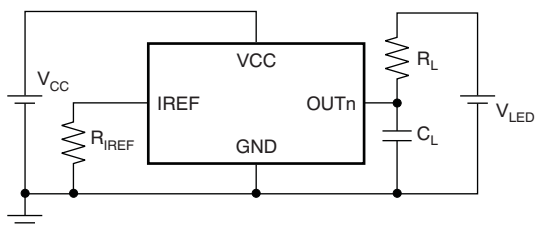


Figure 15. Rise Time and Fall Time Test Circuit for OUTn

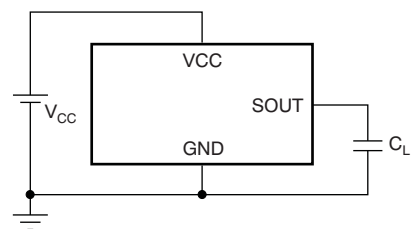


Figure 16. Rise Time and Fall Time Test Circuit for SOUT

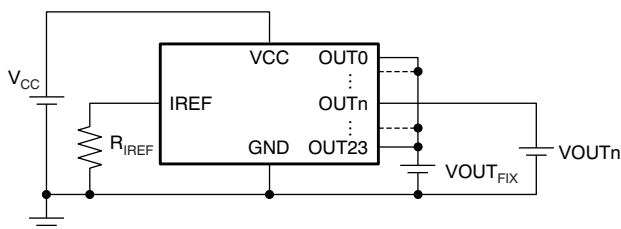
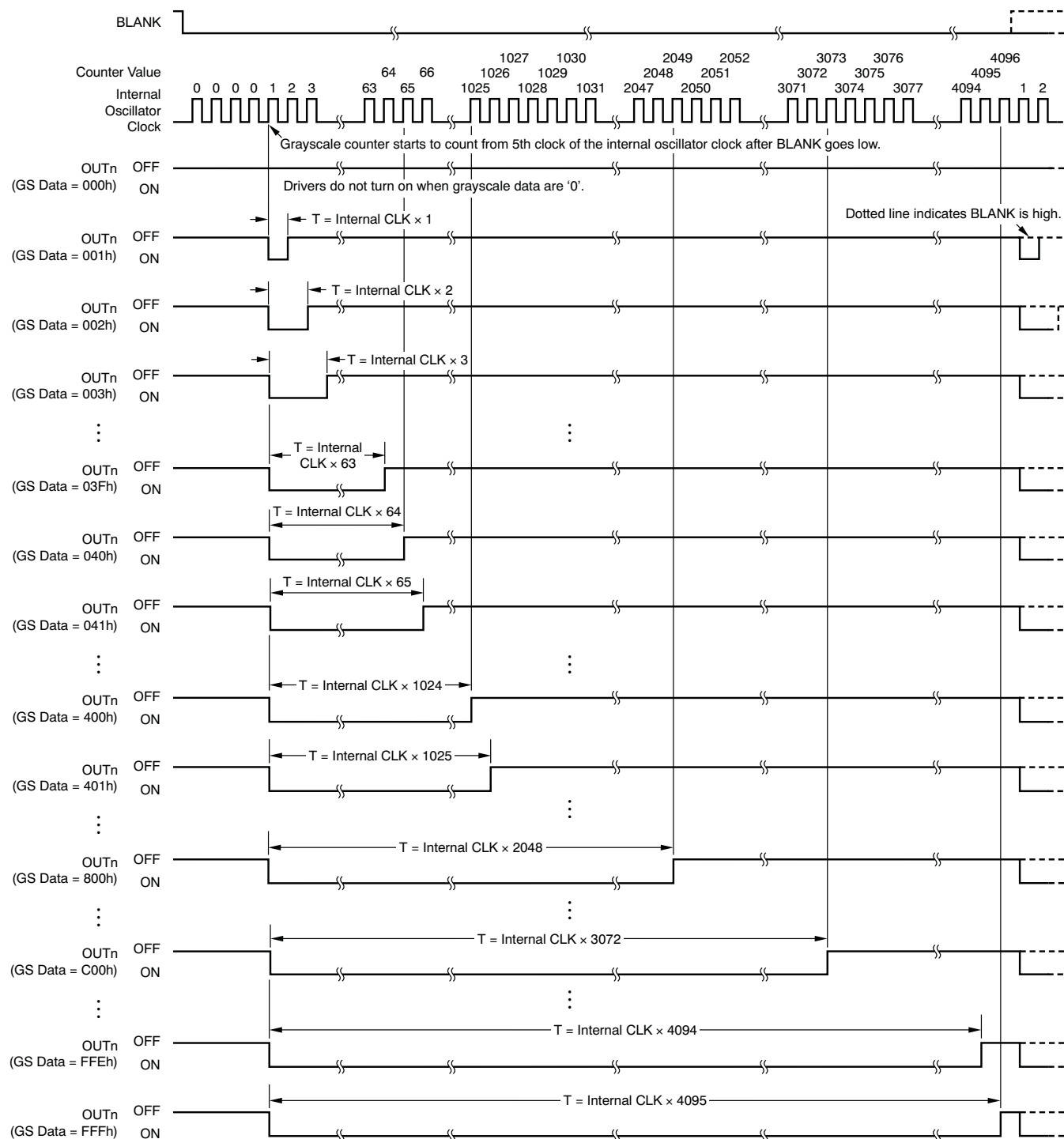


Figure 17. Constant-Current Test Circuit for OUTn



## Feature Description (continued)

When the IC is powered on, the data in the grayscale data shift register and latch are not set to default values. Therefore, grayscale data must be written to the GS latch before turning on the constant-current output. BLANK should be at a high level when powered on to keep the outputs off until valid grayscale data are written to the latch. This avoids the LED being randomly illuminated immediately after power-up. If having the outputs turn on at power-up is not a problem for the application, then BLANK does not need to be held high. The grayscale functions can be controlled directly by grayscale data writing, even though BLANK is connected to GND.

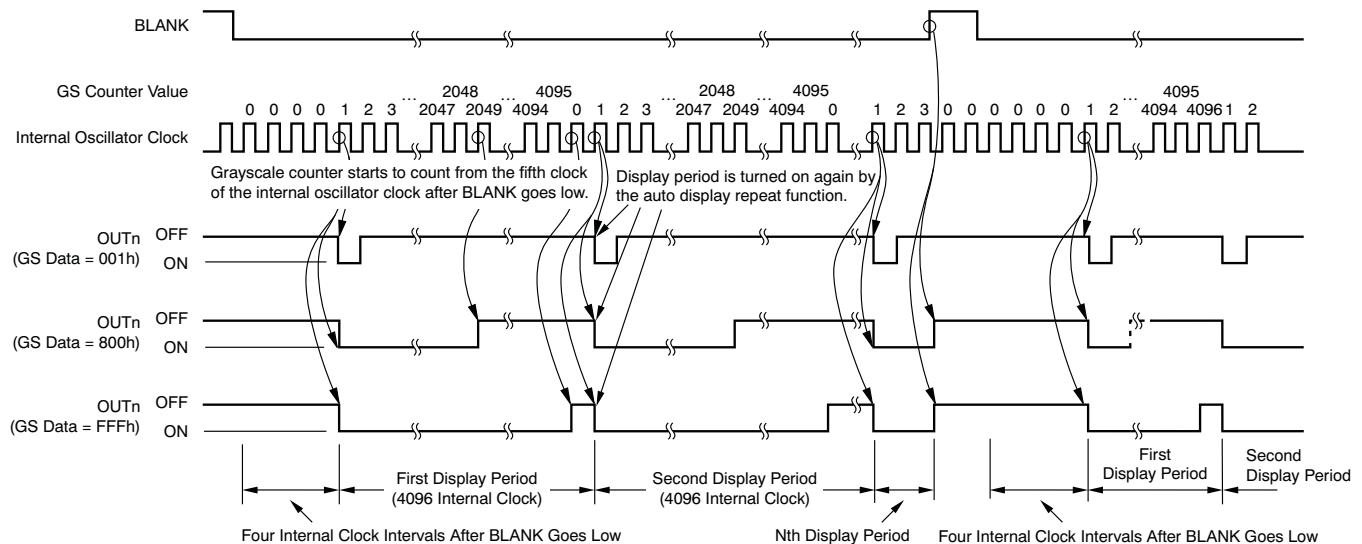


**Figure 18. PWM Operation**

## Feature Description (continued)

### 8.3.2 Auto Display Repeat Function

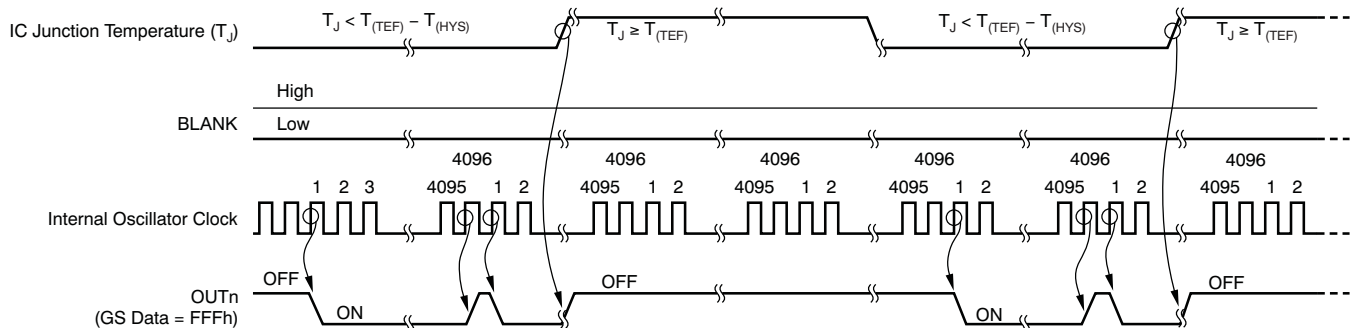
This function can repeat the total display period without any timing control signal, as shown in [Figure 19](#).



**Figure 19. Auto Display Repeat Operation**

### 8.3.3 Thermal Shutdown (TSD)

The thermal shutdown (TSD) function turns off all constant-current outputs immediately when the IC junction temperature exceeds the high temperature threshold ( $T_{(TEF)} = +162^{\circ}\text{C}$ , typ). The outputs will remain disabled as long as the over-temperature condition exists. The outputs are turned on again at the first clock after the IC junction temperature falls below the temperature of  $T_{(TEF)} - T_{(HYS)}$ . [Figure 20](#) shows the TSD operation.



**Figure 20. TSD Operation**

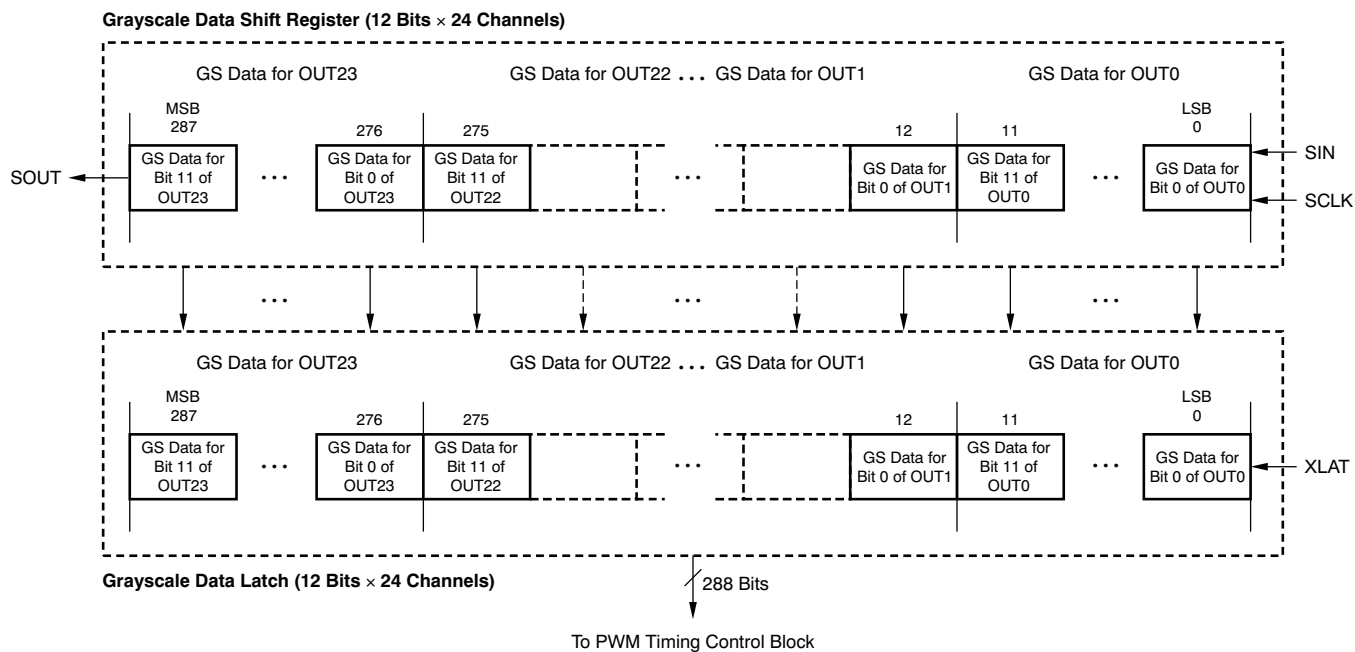
### 8.3.4 Noise Reduction

Large surge currents may flow through the IC and the board on which the device is mounted if all 24 LED channels turn on simultaneously at the start of each grayscale cycle. These large current surges could introduce detrimental noise and electromagnetic interference (EMI) into other circuits. The TLC5947 turns on the LED channels in a series delay, to provide a current soft-start feature. The output current sinks are grouped into four groups of six channels each. The first group is OUT0, 4, 8, 12, 16, 20; the second group is OUT1, 5, 9, 13, 17, 21; the third group is OUT2, 6, 10, 14, 18, 22; and the fourth group is OUT3, 7, 11, 15, 19, 23. Each group turns on sequentially with a small delay between groups; see [Figure 3](#). Both turn-on and turn-off are delayed.

## 8.4 Programming

### 8.4.1 Register Configuration

The TLC5947 has a grayscale (GS) data shift register and data latch. Both the GS data shift register and latch are 288 bits long and are used to set the PWM timing for the constant-current driver. [Table 1](#) shows the on duty cycle for each GS data. [Figure 21](#) shows the shift register and data latch configuration. The data at the SIN pin are shifted to the LSB of the shift register at the rising edge of the SCLK pin; SOUT data are shifted out on the falling edge of SCLK. The timing diagram for data writing is shown in [Figure 22](#). The driver on duty is controlled by the data in the GS data latch.



**Figure 21. Grayscale Data Shift Register and Latch Configuration**

## Programming (continued)

**Table 1. GS Data versus On Duty**

GS DATA (Binary)	GS DATA (Decimal)	GS DATA (Hex)	DUTY OF DRIVER TURN-ON TIME (%)
0000 0000 0000	0	000	0.00
0000 0000 0001	1	001	0.02
0000 0000 0010	2	002	0.05
0000 0000 0011	3	003	0.07
—	—	—	—
0111 1111 1111	2047	7FF	49.98
1000 0000 0000	2048	800	50.00
1000 0000 0001	2049	801	50.02
—	—	—	—
1111 1111 1101	4093	FFD	99.93
1111 1111 1110	4094	FFE	99.95
1111 1111 1111	4095	FFF	99.98

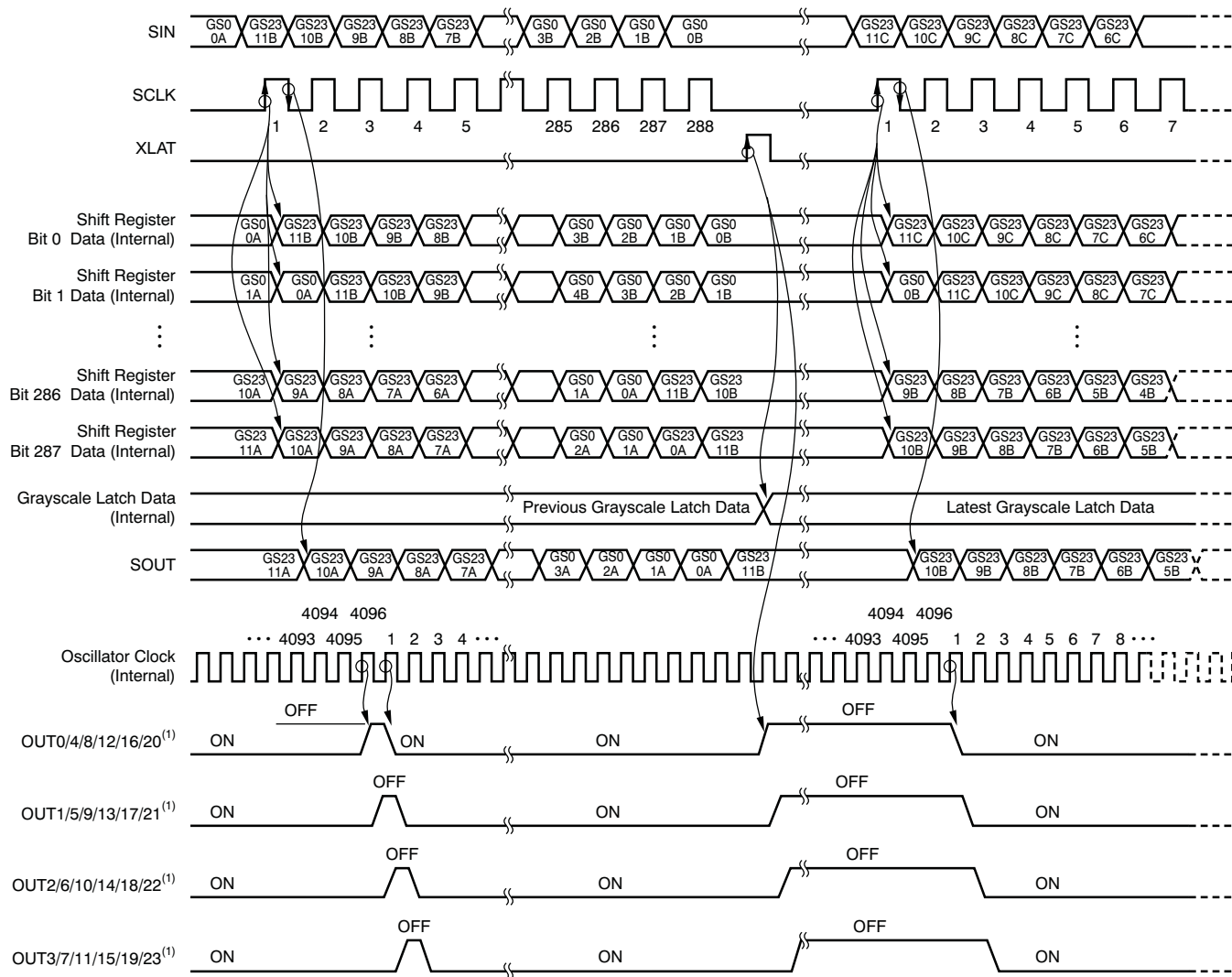
GS data are transferred from the shift register to the latch by the rising edge of XLAT. When powered up, the data in the grayscale shift register and data latch are not set to default values. Therefore, grayscale data must be written to the GS latch before turning on the constant-current output. BLANK should be at a high level when powered on to avoid falsely turning on the constant-current outputs due to random values in the latch at power-up. All of the constant-current outputs are forced off when BLANK is high. However, if the random values turning on at power-up is not a concern in the application, BLANK can be at any level. GS can be controlled correctly with the grayscale data writing functions, even if BLANK is connected to GND. [Equation 1](#) determines each output on duty.

$$\text{On Duty (\%)} = \frac{\text{GS}_n}{4096} \times 100$$

where

- GS<sub>n</sub> = the programmed grayscale value for OUT<sub>n</sub> (GS<sub>n</sub> = 0 to 4095) (1)





(1) GS data = FFFh.

**Figure 22. Grayscale Data Write Operation**

## 9 Application and Implementation

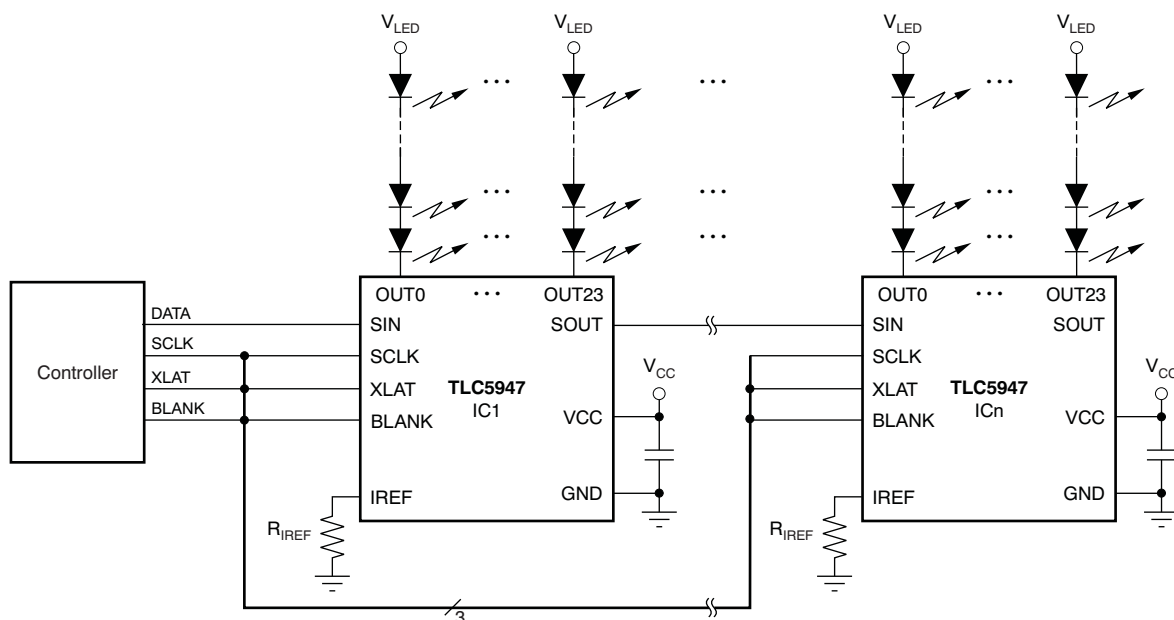
### NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

### 9.1 Application Information

The device is a 24-channel, constant sink current, LED driver. This device can be connected in series to drive many LED lamps with only a few controller ports. Output current control data and PWM control data can be written from the SIN input terminal. The PWM timing reference clock can be supplied from the internal oscillation.

### 9.2 Typical Application



**Figure 23. Typical Application Circuit (Multiple Daisy Chained TLC5947s)**

#### 9.2.1 Design Requirements

For this design example, use [Table 2](#) as the input parameters.

**Table 2. Design Parameters**

DESIGN PARAMETER	EXAMPLE VALUE
VCC input voltage range	3 V to 5.5 V
LED lamp ( $V_{LED}$ ) input voltage range	Maximum LED forward voltage ( $V_F$ ) + IC knee voltage
SIN, SCLK, LAT, and BLANK voltage range	Low level = GND, High level = VCC

#### 9.2.2 Detailed Design Procedure

##### 9.2.2.1 Define Basic Parameters

To begin the design process, a few parameters must be decided as following:

- Maximum output constant-current value for each color LED lamp
- Maximum LED forward voltage ( $V_F$ )
- Are auto display function used

### 9.2.2.2 Grayscale (GS) Data

There are a total of 24 sets of 12-bit GS data for the PWM control of each output. Select the GS data of each LED lamp and write the GS data to the register following the signal timing.

### 9.2.2.3 Auto-Display Function

There are a total of 24 sets of 12-bit GS data for the PWM control of each output. Select the GS data of each LED lamp and write the GS data to the register following the signal timing.

### 9.2.2.4 Setting for the Constant Sink Current Value

The constant-current value for all channels is set by an external resistor ( $R_{IREF}$ ) placed between IREF and GND. The resistor ( $R_{IREF}$ ) value is calculated by [Equation 2](#).

$$R_{IREF} (\Omega) = 41 \times \frac{V_{IREF} (V)}{I_{OLC} (mA)}$$

where

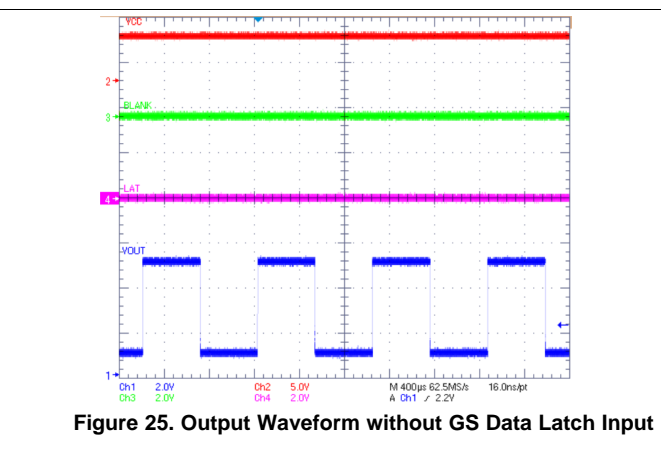
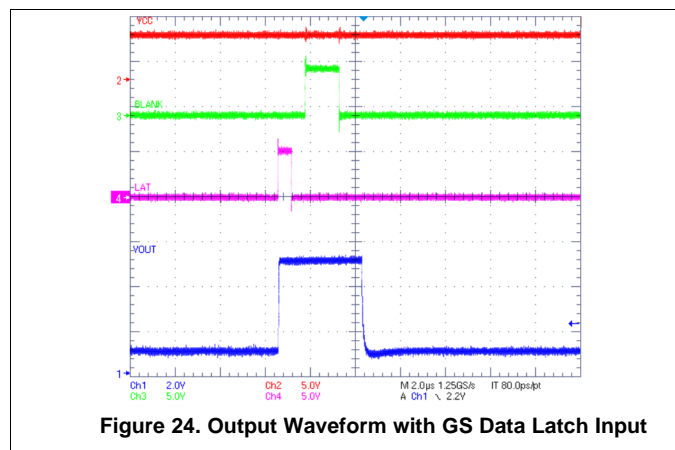
- $V_{IREF}$  = the internal reference voltage on the IREF pin (typically 1.20 V). (2)

$I_{OLC}$  must be set in the range of 2 mA to 30 mA. The constant sink current characteristic for the external resistor value is shown in [Figure 4](#). [Table 3](#) describes the constant-current output versus external resistor value.

**Table 3. Constant-Current Output versus External Resistor Value**

$I_{OLC}$ (mA, Typical)	$R_{IREF}$ ( $\Omega$ )
30	1640
25	1968
20	2460
15	3280
10	4920
5	9840
2	24600

### 9.2.3 Application Curves



## 10 Power Supply Recommendations

The VCC power supply voltage should be decoupled by placing a 0.1- $\mu$ F ceramic capacitor close to the VCC pin and GND plane. Depending on the panel size, several electrolytic capacitors must be placed on the board equally distributed to get a well regulated LED supply voltage ( $V_{LED}$ ). The  $V_{LED}$  voltage ripple must be less than 5% of its nominal value. Furthermore, the  $V_{LED}$  must be set to the voltage calculated by [Equation 3](#):

$$V_{LED} > V_F + 0.4 \text{ V (10-mA constant-current example)}$$

where

- $V_F$  = maximum forward voltage of all LEDs. (3)

## 11 Layout

### 11.1 Layout Guidelines

- Place the decoupling capacitor near the VCC pin and GND plane.
- Place the current programming resistor  $R_{IREF}$  close to the IREF pin and the IREFGND pin.
- Route the GND pattern as widely as possible for large GND currents.
- The routing wire between the LED cathode side and the device OUTXn pin must be as short and straight as possible to reduce wire inductance.
- When several ICs are chained, symmetric placements are recommended.

### 11.2 Layout Example

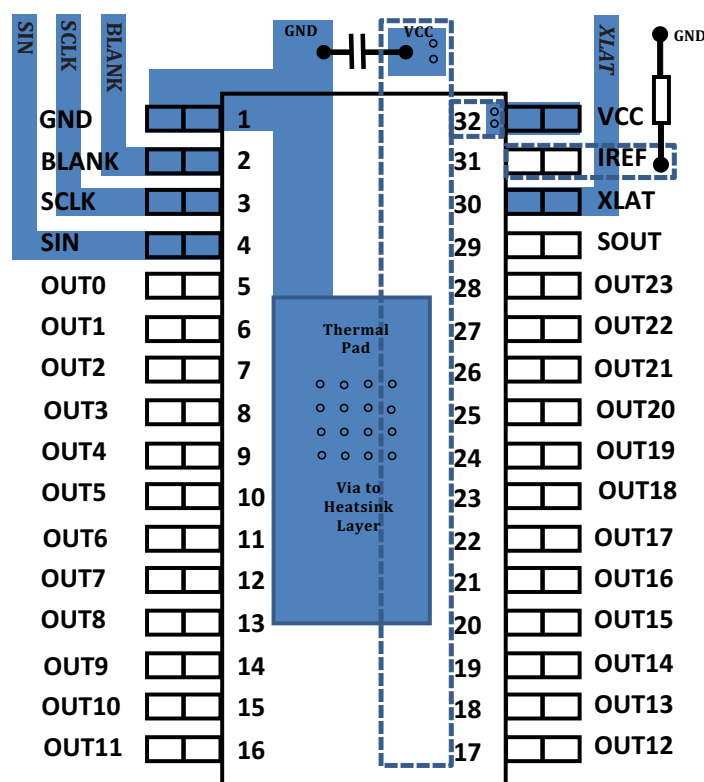


Figure 26. Layout Schematic

### 11.3 Power Dissipation

The device power dissipation must be below the power dissipation rate of the device package (illustrated in [Figure 5](#)) to ensure correct operation. [Equation 4](#) calculates the power dissipation of the device:

$$P_D = (V_{CC} \times I_{CC}) + (V_{OUT} \times I_{OLC} \times N \times d_{PWM})$$

where

- $V_{CC}$  = device supply voltage
- $I_{CC}$  = device supply current
- $V_{OUT}$  = OUTn voltage when driving LED current
- $I_{OLC}$  = LED current adjusted by  $R_{IREF}$  resistor
- $N$  = number of OUTn driving LED at the same time
- $d_{PWM}$  = duty ratio defined by GS value

(4)

## 12 Device and Documentation Support

### 12.1 Trademarks

PowerPAD is a trademark of Texas Instruments.  
All other trademarks are the property of their respective owners.

### 12.2 Electrostatic Discharge Caution



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

### 12.3 Glossary

[SLYZ022](#) — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

## 13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

## PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package   Pins	Package qty   Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
<a href="#">TLC5947DAP</a>	Active	Production	HTSSOP (DAP)   32	46   TUBE	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 85	TLC5947
TLC5947DAP.A	Active	Production	HTSSOP (DAP)   32	46   TUBE	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 85	TLC5947
TLC5947DAP.B	Active	Production	HTSSOP (DAP)   32	46   TUBE	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 85	TLC5947
TLC5947DAPG4	Active	Production	HTSSOP (DAP)   32	46   TUBE	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 85	TLC5947
<a href="#">TLC5947DAPR</a>	Active	Production	HTSSOP (DAP)   32	2000   LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 85	TLC5947
TLC5947DAPR.A	Active	Production	HTSSOP (DAP)   32	2000   LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 85	TLC5947
TLC5947DAPR.B	Active	Production	HTSSOP (DAP)   32	2000   LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 85	TLC5947
TLC5947DAPRG4	Active	Production	HTSSOP (DAP)   32	2000   LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 85	TLC5947
<a href="#">TLC5947RHBR</a>	Active	Production	VQFN (RHB)   32	3000   LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	TLC 5947
TLC5947RHBR.B	Active	Production	VQFN (RHB)   32	3000   LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	TLC 5947
<a href="#">TLC5947RHBT</a>	Active	Production	VQFN (RHB)   32	250   SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	TLC 5947
TLC5947RHBT.B	Active	Production	VQFN (RHB)   32	250   SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	TLC 5947
TLC5947RHBTG4	Active	Production	VQFN (RHB)   32	250   SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	TLC 5947
TLC5947RHBTG4.B	Active	Production	VQFN (RHB)   32	250   SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	TLC 5947

<sup>(1)</sup> **Status:** For more details on status, see our [product life cycle](#).

<sup>(2)</sup> **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

<sup>(3)</sup> **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

<sup>(4)</sup> **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

<sup>(5)</sup> **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

<sup>(6)</sup> **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

**Important Information and Disclaimer:**The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.



## TAPE AND REEL INFORMATION



\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TLC5947DAPR	HTSSOP	DAP	32	2000	330.0	24.4	8.6	11.5	1.6	12.0	24.0	Q1
TLC5947RHBR	VQFN	RHB	32	3000	330.0	12.4	5.3	5.3	1.5	8.0	12.0	Q2
TLC5947RHBT	VQFN	RHB	32	250	180.0	12.4	5.3	5.3	1.5	8.0	12.0	Q2
TLC5947RHBTG4	VQFN	RHB	32	250	180.0	12.4	5.3	5.3	1.5	8.0	12.0	Q2

## TAPE AND REEL BOX DIMENSIONS



\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TLC5947DAPR	HTSSOP	DAP	32	2000	350.0	350.0	43.0
TLC5947RHBR	VQFN	RHB	32	3000	353.0	353.0	32.0
TLC5947RHBT	VQFN	RHB	32	250	213.0	191.0	35.0
TLC5947RHBTG4	VQFN	RHB	32	250	213.0	191.0	35.0

## TUBE



\*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (μm)	B (mm)
TLC5947DAP	DAP	HTSSOP	32	46	530	11.89	3600	4.9
TLC5947DAP.A	DAP	HTSSOP	32	46	530	11.89	3600	4.9
TLC5947DAP.B	DAP	HTSSOP	32	46	530	11.89	3600	4.9
TLC5947DAPG4	DAP	HTSSOP	32	46	530	11.89	3600	4.9

## GENERIC PACKAGE VIEW

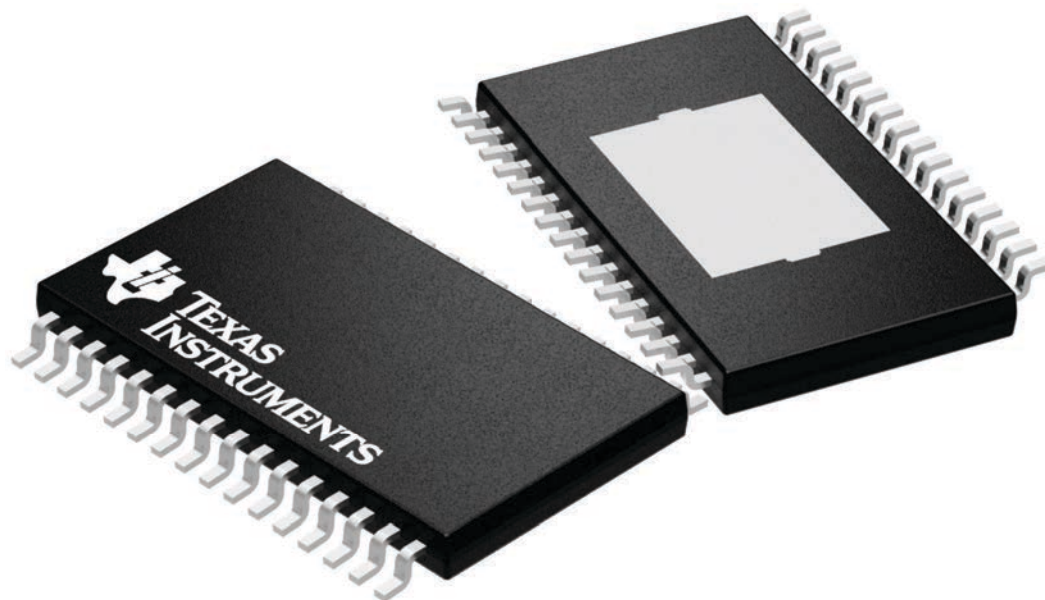
**DAP 32**

**PowerPAD™ TSSOP - 1.2 mm max height**

8.1 x 11, 0.65 mm pitch

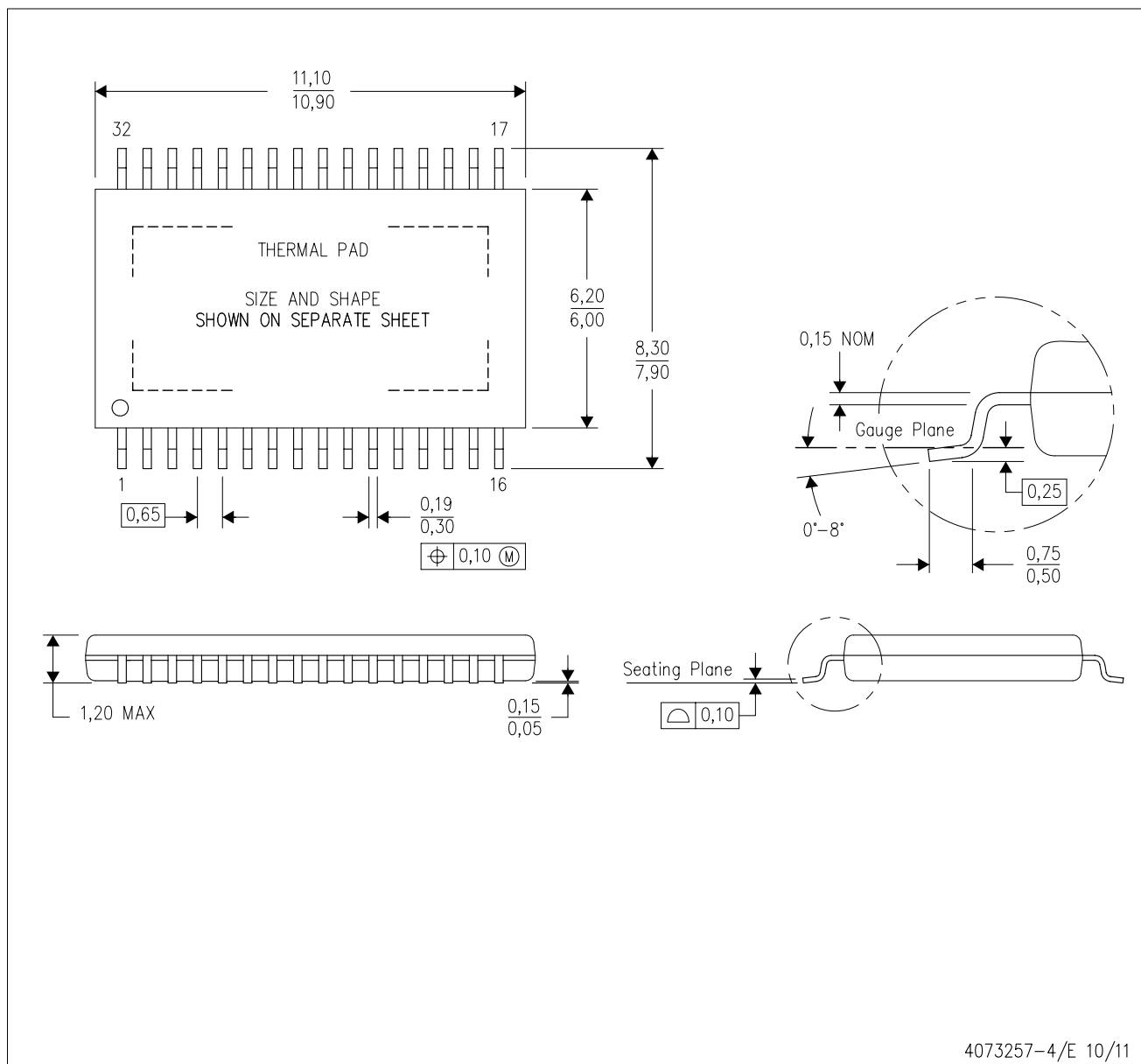
PLASTIC SMALL OUTLINE


This image is a representation of the package family, actual package may vary.  
Refer to the product data sheet for package details.



4225303/A

## DAP (R-PDSO-G32) PowerPAD™ PLASTIC SMALL-OUTLINE PACKAGE



- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
  - D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 for information regarding recommended board layout. This document is available at [www.ti.com](http://www.ti.com) <<http://www.ti.com>>.
-  Falls within JEDEC MO-153 Variation DCT.

DAP (R-PDSO-G32)

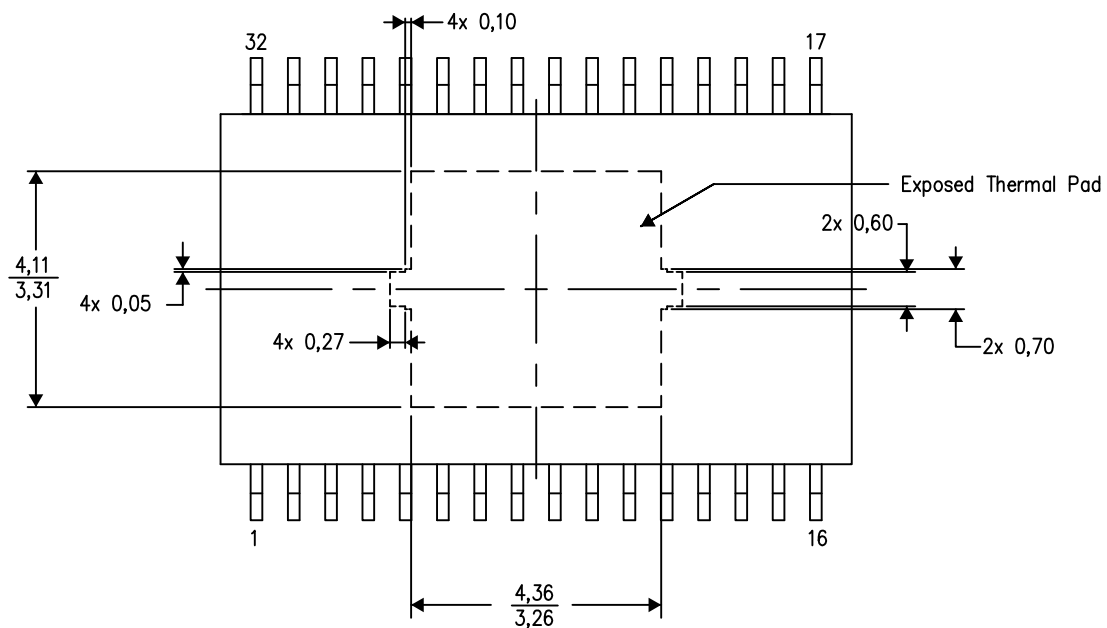
PowerPAD™ PLASTIC SMALL OUTLINE

## THERMAL INFORMATION

This PowerPAD™ package incorporates an exposed thermal pad that is designed to be attached to a printed circuit board (PCB). The thermal pad must be soldered directly to the PCB. After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For additional information on the PowerPAD package and how to take advantage of its heat dissipating abilities, refer to Technical Brief, PowerPAD Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 and Application Brief, PowerPAD Made Easy, Texas Instruments Literature No. SLMA004. Both documents are available at [www.ti.com](http://www.ti.com).

The exposed thermal pad dimensions for this package are shown in the following illustration.



Top View

Exposed Thermal Pad Dimensions

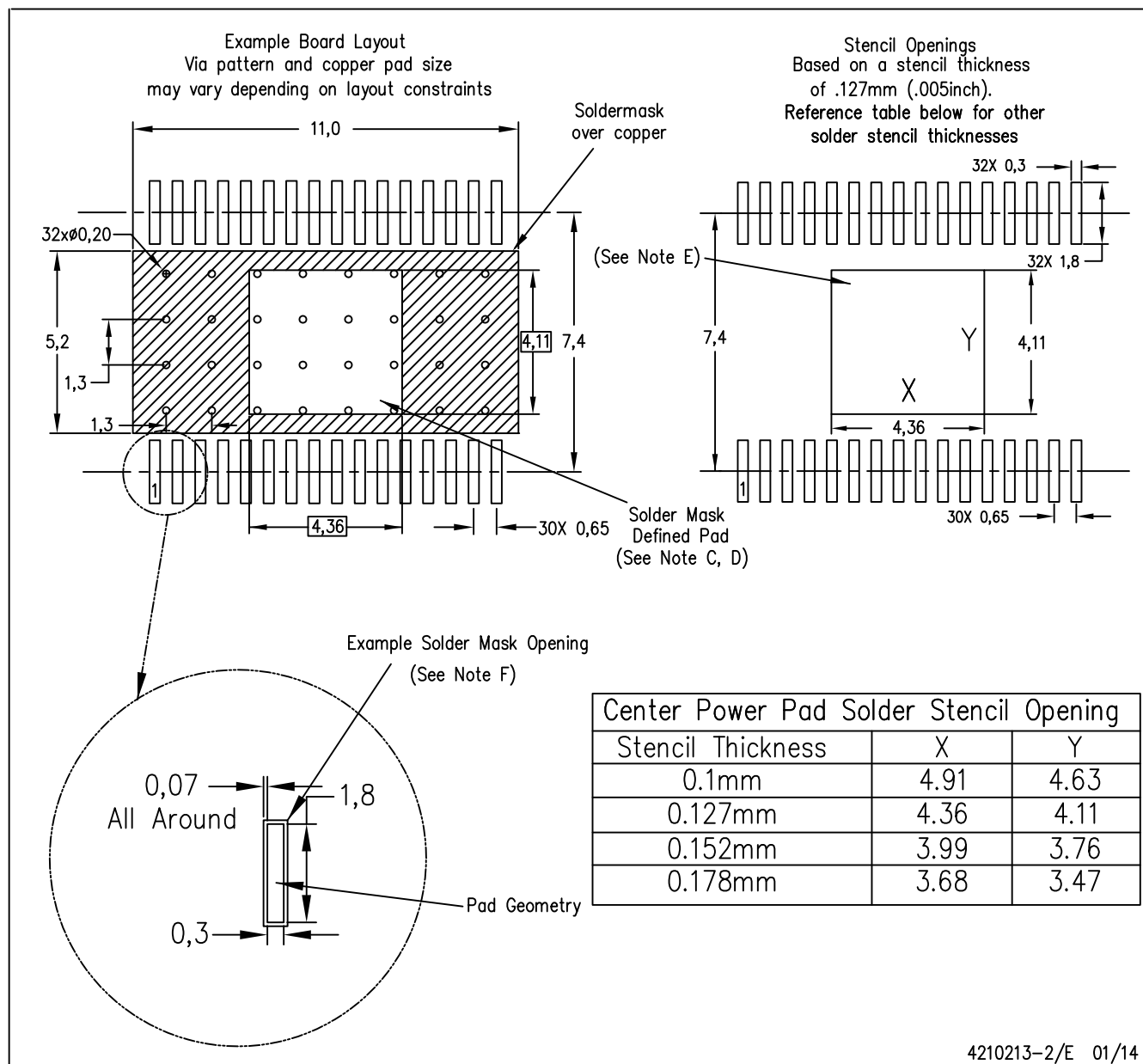
4206319-3/M 09/13

NOTE: All linear dimensions are in millimeters

PowerPAD is a trademark of Texas Instruments.

# LAND PATTERN DATA

## DAP (R-PDSO-G32) PowerPAD™ PLASTIC SMALL OUTLINE PACKAGE



- NOTES:
- All linear dimensions are in millimeters.
  - This drawing is subject to change without notice.
  - Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
  - This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002, SLMA004, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at [www.ti.com](http://www.ti.com) <<http://www.ti.com>>. Publication IPC-7351 is recommended for alternate designs.
  - Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
  - Contact the board fabrication site for recommended soldermask tolerances.

PowerPAD is a trademark of Texas Instruments



## PowerPAD™ TSSOP - 1.2 mm max height

## PLASTIC SMALL OUTLINE



PowerPAD is a trademark of Texas Instruments.

- 
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INSTRUMENTS  
www.ti.com

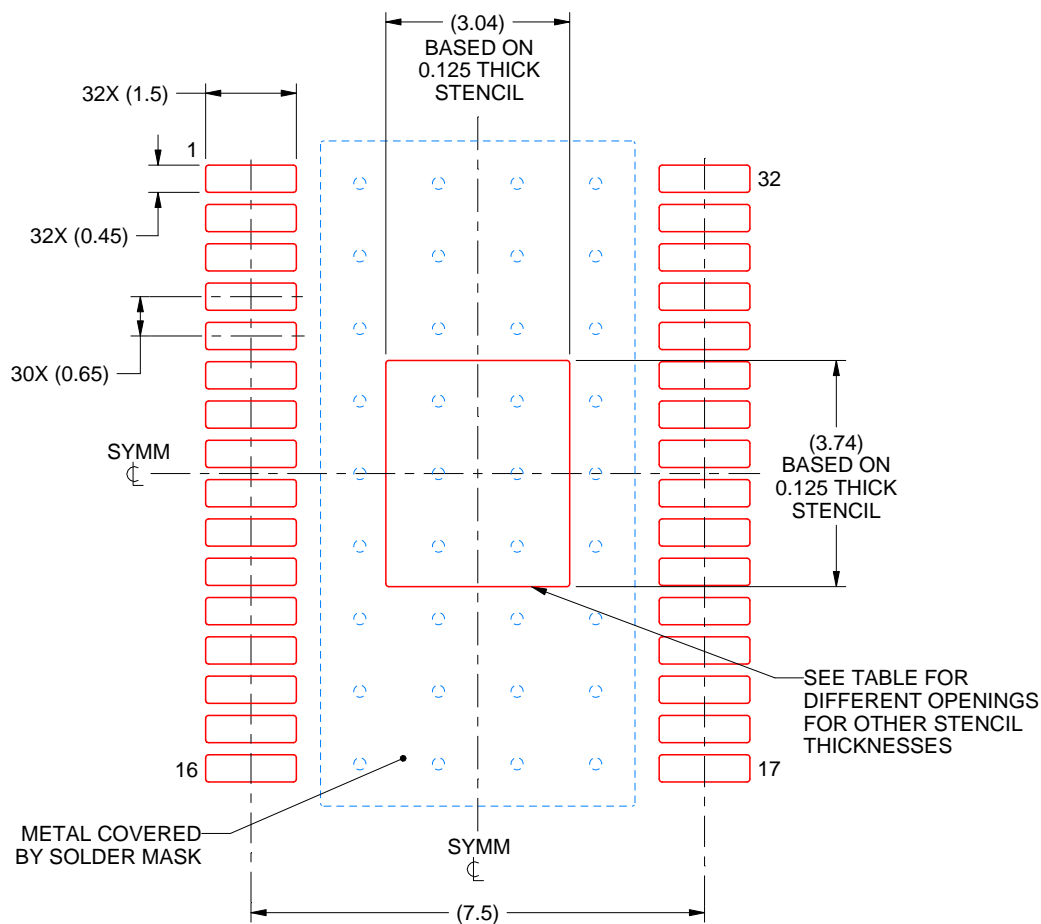




**DAP0032C**

**PowerPAD™ TSSOP - 1.2 mm max height**

## PLASTIC SMALL OUTLINE



SOLDER PASTE EXAMPLE  
EXPOSED PAD  
100% PRINTED SOLDER COVERAGE BY AREA  
SCALE:8X

STENCIL THICKNESS	SOLDER STENCIL OPENING
0.1	3.40 X 4.18
0.125	3.04 X 3.74 (SHOWN)
0.15	2.78 X 3.41
0.175	2.57 X 3.16

4223691/A 05/2017

NOTES: (continued)

10. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
11. Board assembly site may have different recommendations for stencil design.

## GENERIC PACKAGE VIEW

**RHB 32**

**VQFN - 1 mm max height**

5 x 5, 0.5 mm pitch

PLASTIC QUAD FLATPACK - NO LEAD



Images above are just a representation of the package family, actual package may vary.  
Refer to the product data sheet for package details.

4224745/A



### VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



NOTES:

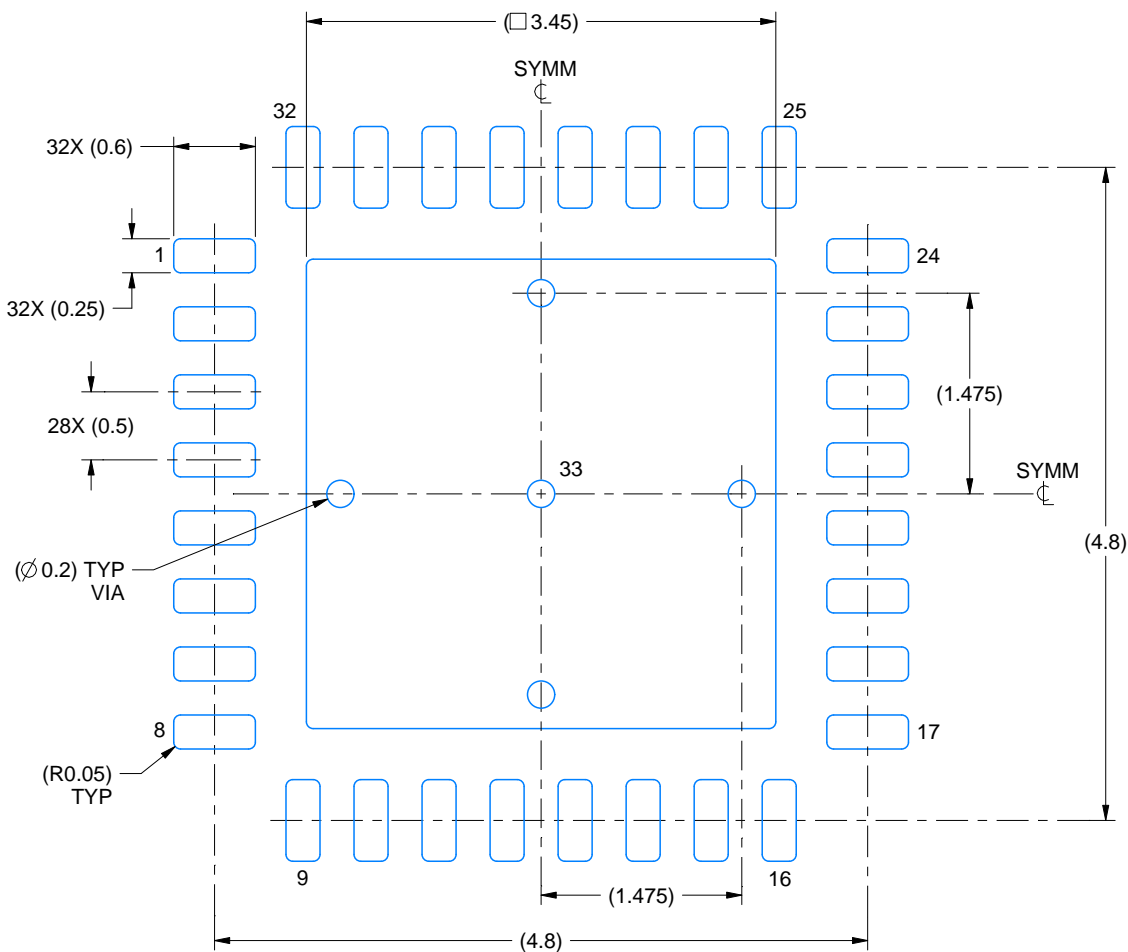
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.

# EXAMPLE BOARD LAYOUT

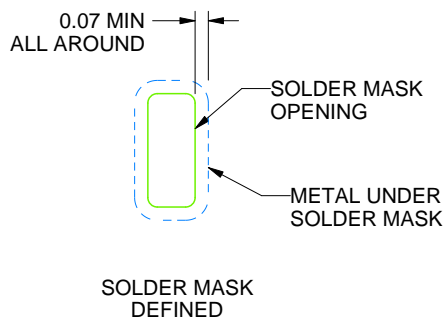
RHB0032E

VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



LAND PATTERN EXAMPLE  
SCALE:18X



SOLDER MASK DETAILS

4223442/B 08/2019

NOTES: (continued)

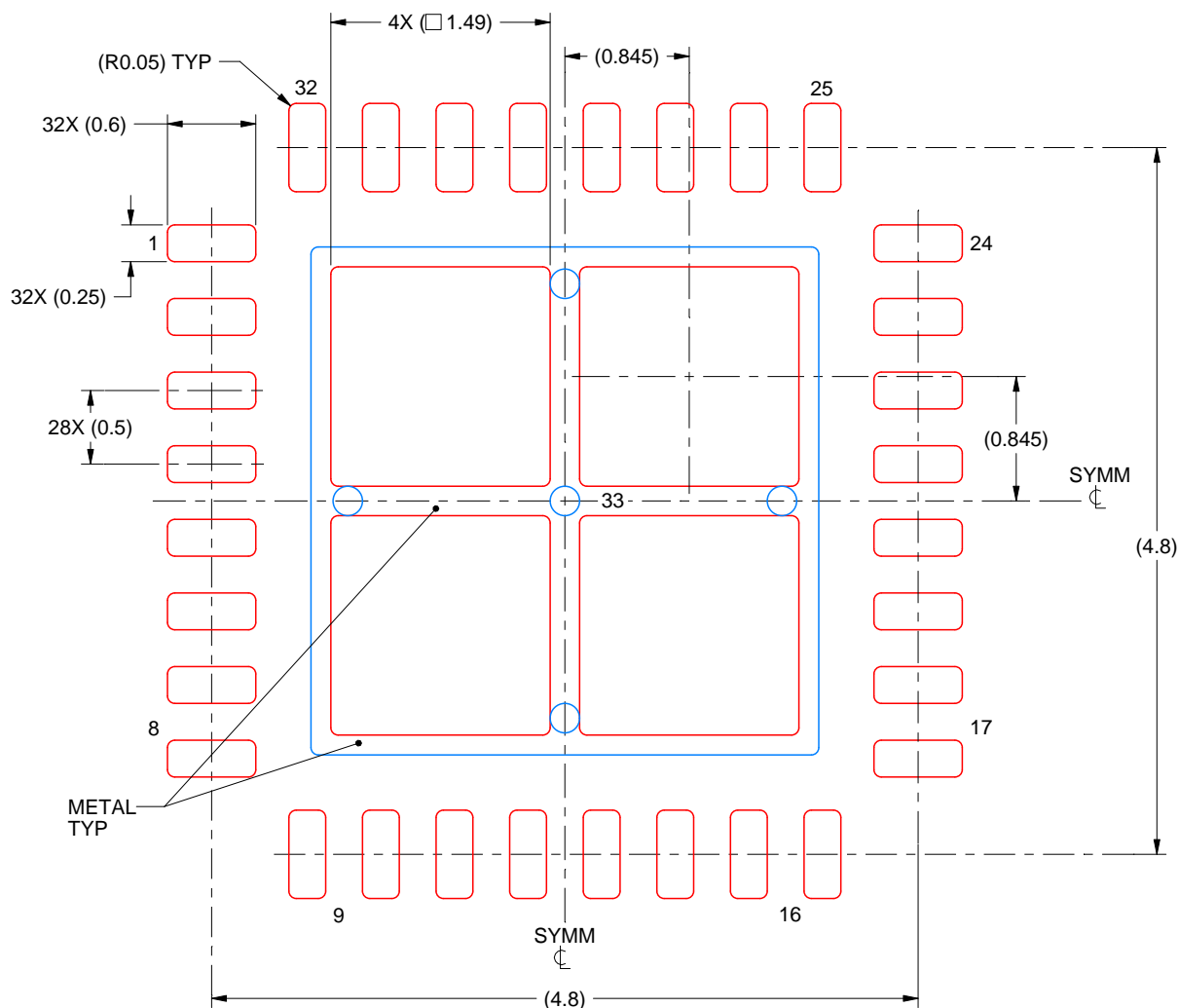
- This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 ([www.ti.com/lit/sluea271](http://www.ti.com/lit/sluea271)).
- Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

# EXAMPLE STENCIL DESIGN

RHB0032E

VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



**SOLDER PASTE EXAMPLE**  
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 33:  
75% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE  
SCALE:20X

4223442/B 08/2019

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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