SHAO-HUNG CHIU

• shaohunc@andrew.cmu.edu • (412) 889-1745 • https://tomchiu5566.github.io/

EDUCATION

Carnegie Mellon University — Pittsburgh, PA
Master of Science in Electrical and Computer Engineering — December 2020
GPA: 3.89/4.0
Courseworks: Foundations of Computer Systems, HPC, Analytical Modeling and Designs of Computer Systems

National Tsing Hua University — Hsinchu, Taiwan
Bachelor of Electrical Engineering — January 2019
Overall GPA: 4.0/4.3 Major GPA: 4.19/4.3
Relevant Courses: Computer Architecture, OS, Algorithms, Digital Systems Design, Microprocessor Systems

SKILLS

Programming Languages	C/C++, Python, MATLAB
Tools	Verilog, Linux OS
Languages	English, Chinese (Native)

WORK EXPERIENCE

ASPEED Technology Inc. — Hsinchu, Taiwan
Intern — July 2018 - August 2018
• Researched Super Resolution algorithms within recent 2 years with low computation complexity and assisted ASPEED to evaluate potential IP usage
• Introduced Efficient Inference Engine Design to illustrate domain-specific algorithms and architecture by giving a talk to 30 staff members in ASPEED
• Built machine learning models and clarified analytical tools on several frameworks such as Caffe and Tensorflow for ASPEED's further research

BIIC Lab — Hsinchu, Taiwan
Research Assistant — October 2017 - January 2018
• Utilized machine learning techniques on Human Behavioral Analysis, reaching almost 70% accuracy on image data
• Performed various feature extraction methods with Python package OpenCV for further analysis and better accuracy

ACADEMIC PROJECTS

Self-Driving Car with Raspberry Pi — Hsinchu, Taiwan
National Tsing Hua University — January 2018 - January 2019
• Developed a lane following algorithm achieving prompt controls up to 6 frames per seconds by utilizing OpenCV and fitting polynomials with Python3.5
• Scheduled entire 2-semester project and led discussion in routine meetings
• Coordinated 4 teammates' work into 1 stable system involving XBEE, MobileNet, lane following and positioning

Traveling Salesperson Accelerator — Hsinchu, Taiwan
National Tsing Hua University — December 2018 - January 2019
• Transferred C code to RISCV simulator with elaborate memory management and specific data structures for accurate profiling and further co-processor designs
• Designed RTL-level accelerator to boost up computations with co-processor interface, reducing 59% cycle numbers of bottleneck function