

# SHAO-HUNG CHIU

• shaohunc@andrew.cmu.edu • (412) 889-1745 • <https://tomchiu5566.github.io/>

## EDUCATION

---

### Carnegie Mellon University

Master of Science in Electrical and Computer Engineering

GPA: 3.89/4.0

Courseworks:

(2019 Fall) Foundations of Computer Systems, How to Write Fast Code (HPC), Analytical Modeling and Designs of Computer Systems

(2020 Spring) Computer Architecture and Systems, Java programming, Cloud Computing

### National Tsing Hua University

Bachelor of Electrical Engineering

Overall GPA: 4.0/4.3      Major GPA: 4.19/4.3

Relevant Courses: Computer Architecture, OS, Algorithms, Digital Systems Design, Microprocessor Systems

Pittsburgh, PA

December 2020

Hsinchu, Taiwan

January 2019

## SKILLS

---

### Programming Languages

C/C++, Java, Python, MATLAB

### Tools

Verilog, Linux OS

### Languages

English, Chinese (Native)

## WORK EXPERIENCE

---

### ASPEED Technology Inc.

Intern

Hsinchu, Taiwan

July 2018 - August 2018

- Researched Super Resolution algorithms within recent 2 years with low computation complexity and assisted ASPEED to evaluate potential IP usage
- Introduced Efficient Inference Engine Design to illustrate domain-specific algorithms and architecture by giving a talk to 30 staff members in ASPEED
- Built machine learning models and clarified analytical tools on several frameworks such as Caffe and Tensorflow for ASPEED's further research

### BIIC Lab

Research Assistant

Hsinchu, Taiwan

October 2017 - January 2018

- Collaborated with Gamania to operate on real-world video data up to hundreds of GB and innovated on potential interview assisting products
- Utilized machine learning techniques on Human Behavioral Analysis, reaching almost 70% accuracy on image data
- Performed various feature extraction methods with Python package OpenCV for further analysis and better accuracy

## ACADEMIC PROJECTS

---

### Fast Kernel of G3PCX

Carnegie Mellon University

Pittsburgh, PA

September 2019 - December 2019

- Analyzed genetic algorithms and identified bottleneck operations and independent chains to achieve instruction-level parallelism
- Designed fast kernels and corresponding data structures to accelerate computations to over 80% of theoretical peak
- Utilized SIMD instructions of intel AVX architecture to avoid dependent chains throughout computations and reached 2x speed for crucial functions

## **Self-Driving Car with Raspberry Pi**

National Tsing Hua University

Hsinchu, Taiwan

January 2018 - January 2019

- Developed a lane following algorithm achieving prompt controls up to 6 frames per seconds by utilizing OpenCV and fitting polynomials with Python3.5
- Scheduled entire 2-semester project and led discussion in routine meetings
- Coordinated 4 teammates' work into 1 stable system involving XBEE, MobileNet, lane following and positioning

## **Traveling Salesperson Accelerator**

National Tsing Hua University

Hsinchu, Taiwan

December 2018 - January 2019

- Transferred C code to RISCV simulator with elaborate memory management and specific data structures for accurate profiling and further co-processor designs
- Designed RTL-level accelerator to boost up computations with co-processor interface, reducing 59% cycle numbers of bottleneck function