

ENGG 4080: Project

Sec 0102

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Instructor's Name: Stefano Gregori

Names of Group Members:

Thomas Green (#1048389)

Riley McCarthy (#1054625)

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Design and Calculations

Inverter

The following figure present the symbol and schematic of the inverter, a basic component that was used throughout the design of the ECG interface:

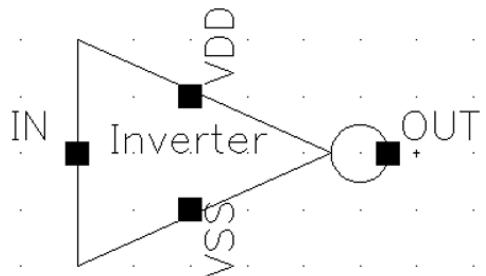


Figure 1: Inverter symbol.

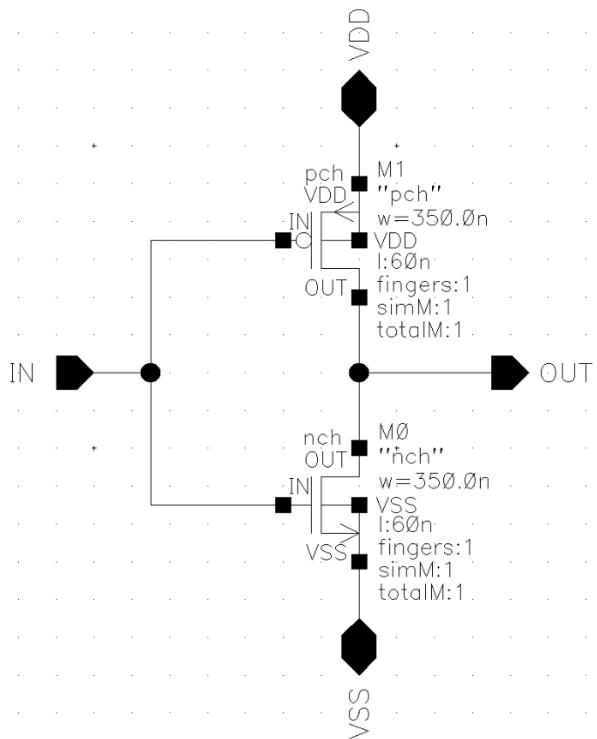


Figure 2: Inverter schematic.

As can be seen, the inverter is composed of transistors with lengths of 60nm and widths of 350nm. The transistor sizes were made as small as possible to ensure that the inverters do not take up too much space.

Switch (Transmission Gate)

The following figures present the symbol and schematic of the switch, another basic component that was also used throughout the design:

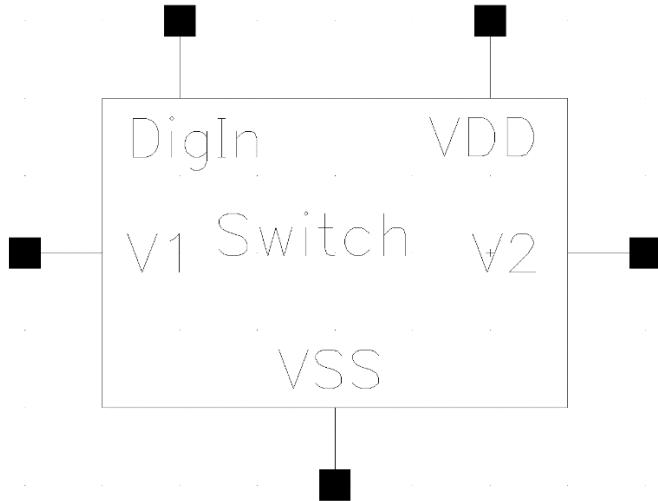


Figure 3: Switch (transmission gate) symbol.

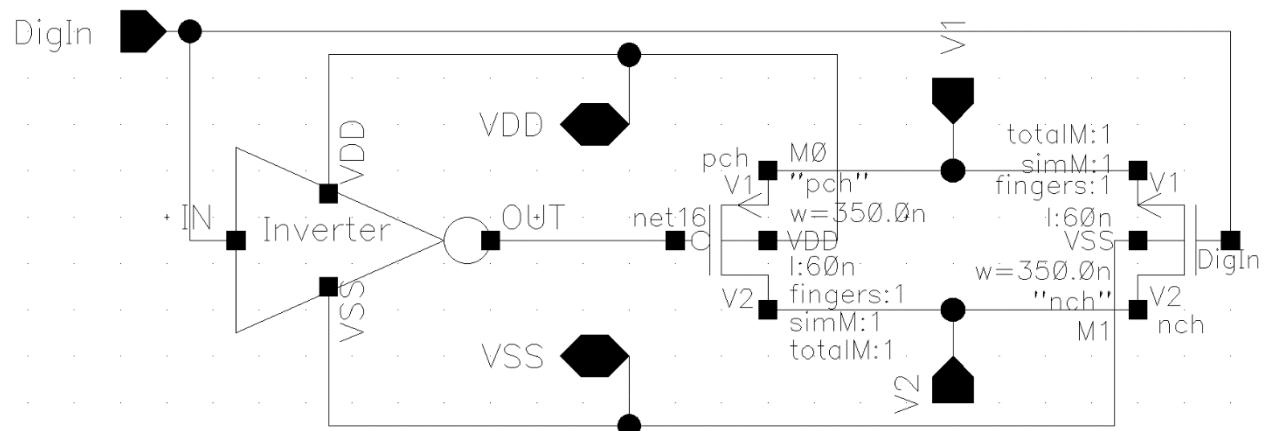


Figure 4: Switch (transmission gate) schematic.

Like the inverter, the transistors were sized so that they would take up as little space as possible. A transmission gate was used to implement the switch, as opposed to its simpler single transistor counterparts because it offers a full range for V1 to be passed to V2 (i.e., between 0V and 1V). The main advantage of the transmission gate is using both PMOS and NMOS to pass strong '0' and strong '1'.

Multiplexer

The first major component that makes up the ECG interface is the analogue multiplexer. The following figures present the multiplexer's symbol and schematic:

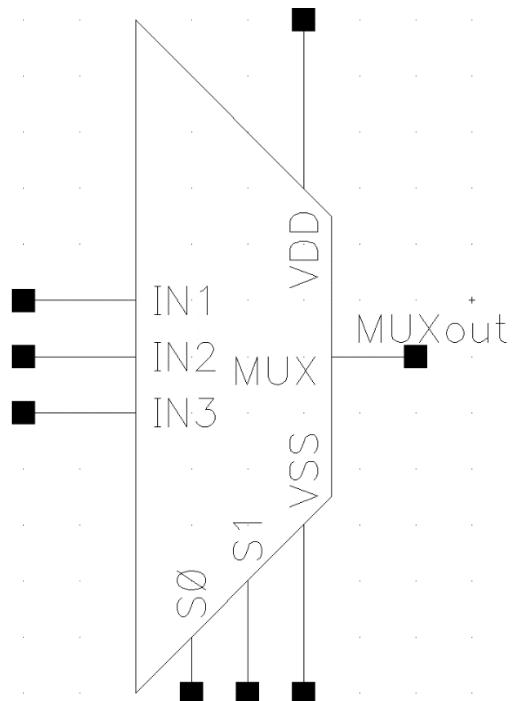


Figure 5: Multiplexer symbol.

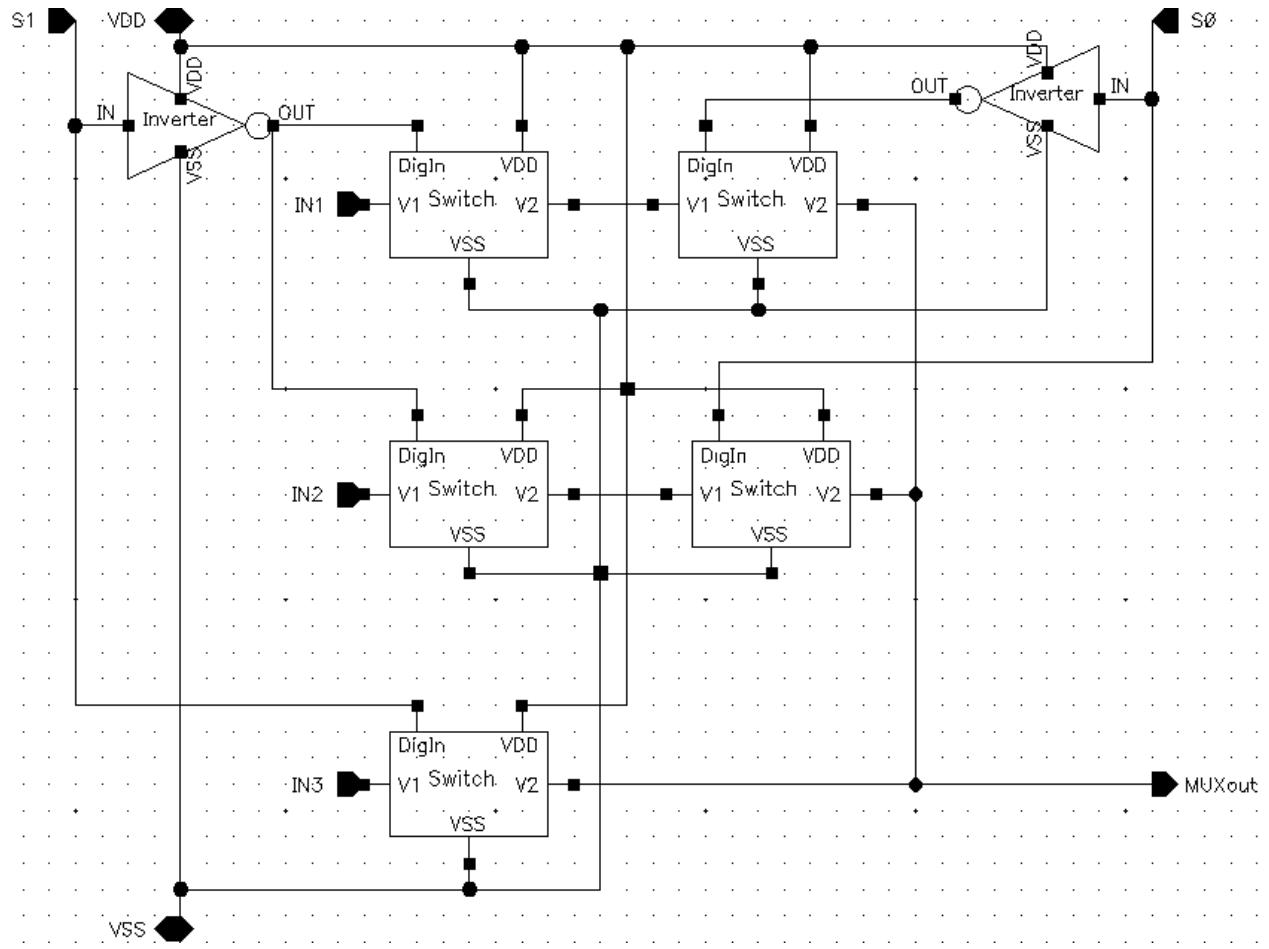


Figure 6: Multiplexer schematic.

As is the case with any multiplexer, the purpose of this component is to allow the ECG interface to select which input it processes, as controlled by select lines S1 and S0. Unlike a digital multiplexer, an analogue multiplexer passes the selected input to the output without turning it into a strong 0 or 1. As such, it is composed of switches rather than logic gates. The following truth table describes the behavior of the multiplexer that was implemented:

Table 1: Multiplexer truth table.

S1	S0	MUX_{out}
0	0	IN1
0	1	IN2
1	X	IN3

As can be seen, IN3 does not depend on S0, which omits the cost of creating an additional, unneeded switch.

Programmable Gain Amplifier

The programmable gain amplifier (PGA) was implemented using a Capacitive Reset Gain Circuit. The following figures present the PGA's symbol and schematic:

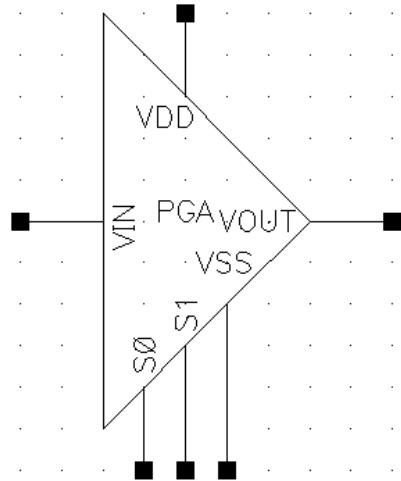


Figure 7: Programmable gain amplifier symbol.

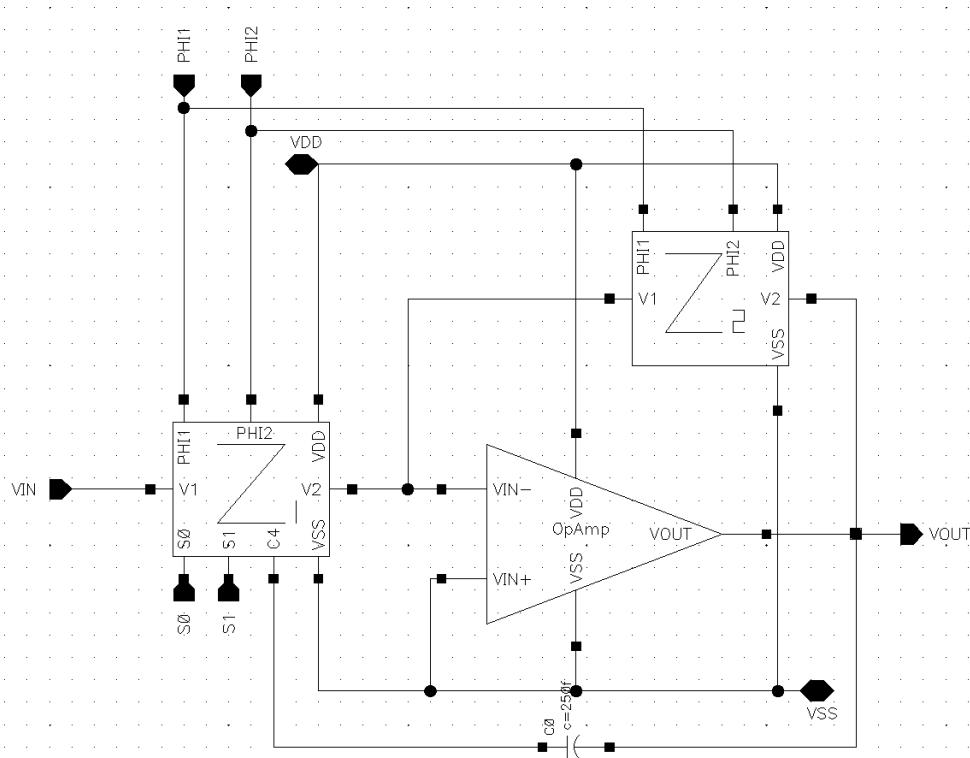


Figure 8: Programmable gain amplifier schematic.

As can be seen, the PGA was compartmentalized into the following three subblocks: impedance 1, impedance 2, and the opamp. The opamp is the core unit of the PGA, as it is what provides the circuit with gain, while impedance 1 and impedance 2 are used to achieve the desired closed loop gain. Each sub block will be described in the following sub sections.

Opamp

The following figure presents the op amp schematic:

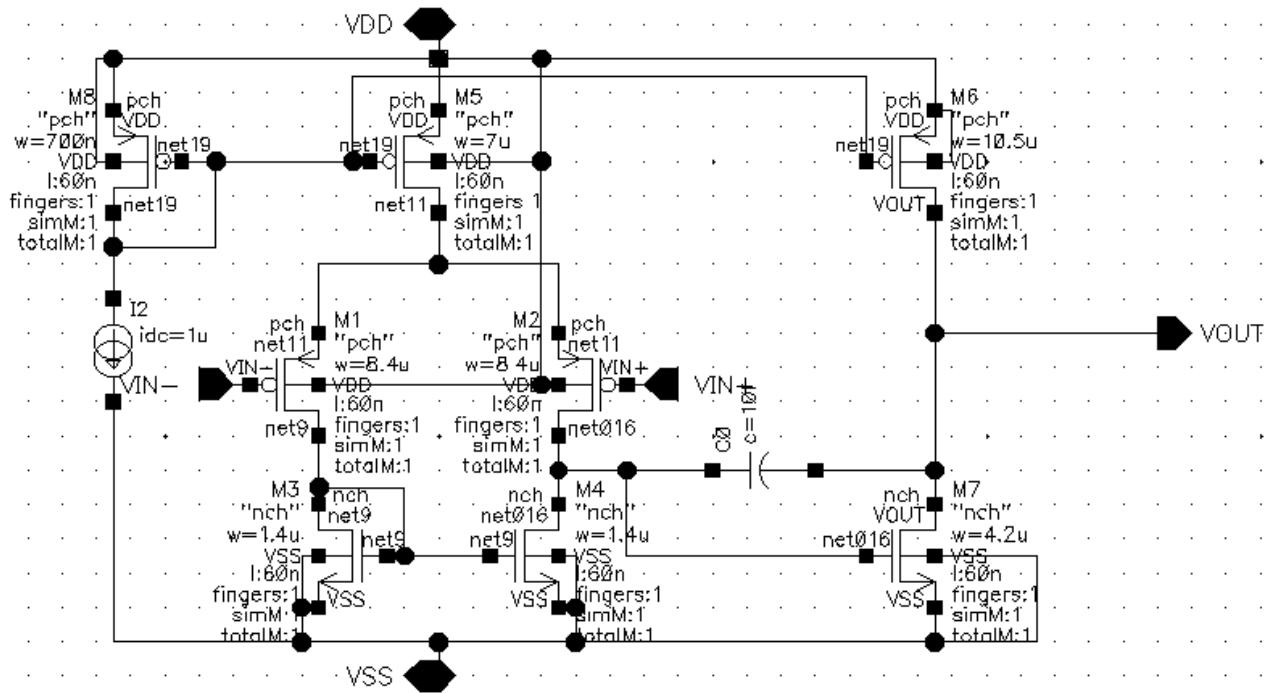


Figure 9: Opamp schematic.

Desirable Characteristics

The opamp above possesses many desirable characteristics. For one, it can be biased using only 1uA, which leads to very small current and subsequently, little power is consumed. Moreover, a wide range of voltage inputs and outputs allow all the transistors to operate in saturation, thus allowing for the proper operation of the op amp. Finally, it takes up a very small amount of area, as the transistor lengths are all set to the smallest they can be (see cost analysis). The following subsection provide calculations that validate the first two statements.

NOTES:

Values for unCox, upCox, and gain resistances were also found in cadence using Beta_eff values from simulations (Beta_eff = unCox(W/L)).

Mosfet	Type	β_{eff}	(W/L)	$\mu_{n/p}Cox$	g_m	r_{on}
M1	P-channel	20780u	8400/60	148.40u	591.0n	3.014M
M2	P-channel	20780u	8400/60	148.40u	592.1n	3.012M
M3	N-channel	12190u	1400/60	522.43u	606.1n	15.66M
M4	N-channel	12200u	1400/60	522.85u	604.3n	15.71K
M5	P-channel	17170u	7000/60	147.17u	861.6n	6.110K
M6	P-channel	25710u	10500/60	146.91u	15.90u	3.917K
M7	N-channel	40470u	4200/60	578.14u	21.71u	498.6K
M8	P-channel	827.6u	700/60	70.93u	20.50u	325.7K

$I_{out,max}$

The maximum output current is when M7 is off and all the current is flowing through the output. M6 acts as a current follower with M8 limiting the max output current equal to the current flowing through M6.

$$I_{out,max} = I_{D6} = (W/L)_6 / (W/L)_8 \cdot I_{out,max} = I_{D6} = \frac{I_{bias} \cdot \left(\frac{W}{L}\right)_6}{\left(\frac{W}{L}\right)_8} = 1uA \cdot \frac{\left(\frac{10500}{60}\right)}{\left(\frac{700}{60}\right)} = 15uA$$

V_{inmin}

$$V_{inmin} = V_{tn} + V_{ov3} - |V_{tp}|$$

$$V_{inmin} = V_{tn} + \sqrt{\frac{2 * I_{D3}}{\mu_n C_{ox} \left(\frac{W}{L}\right)_8 \left(\frac{W}{L}\right)_3}} - |V_{tp}|, \quad \text{where } I_{D3} = \frac{\left(\frac{W}{L}\right)_5 I_{bias}}{2 \left(\frac{W}{L}\right)_8}$$

$$V_{inmin} = V_{tn} + \sqrt{\frac{\left(\frac{W}{L}\right)_5 I_{bias}}{\mu_n C_{ox} \left(\frac{W}{L}\right)_8 \left(\frac{W}{L}\right)_3}} - |V_{tp}|$$

$$V_{inmin} = 360mV + \sqrt{\frac{\left(\frac{7000n}{60n}\right)_5 * 1\mu}{240\mu \left(\frac{700n}{60n}\right)_8 \left(\frac{1400n}{60n}\right)_3}} - 300mV$$

$$V_{inmin} = 0.1023V$$

V_{inmax}

$$V_{inmax} = V_{DD} - |V_{tp}| - |V_{ov5}| - |V_{ov1}|$$

$$V_{inmax} = V_{DD} - |V_{tp}| - \sqrt{\frac{2 * I_{D5}}{\mu_p C_{ox} \left(\frac{W}{L}\right)_5}} - \sqrt{\frac{2 * I_{D1}}{\mu_p C_{ox} \left(\frac{W}{L}\right)_1}}, \text{ where } I_{D5} = \frac{\left(\frac{W}{L}\right)_5 I_{bias}}{\left(\frac{W}{L}\right)_8}, I_{D1} = I_{D3}$$

$$V_{inmax} = V_{DD} - |V_{tp}| - \sqrt{\frac{2 * I_{bias}}{\mu_p C_{ox} \left(\frac{W}{L}\right)_8}} - \sqrt{\frac{\left(\frac{W}{L}\right)_5 * I_{bias}}{\mu_p C_{ox} \left(\frac{W}{L}\right)_1 \left(\frac{W}{L}\right)_8}}$$

$$V_{inmax} = 1 - 0.3 - \sqrt{\frac{2 * 1\mu}{70\mu \left(\frac{700n}{60n}\right)_8}} - \sqrt{\frac{\left(\frac{7000n}{60n}\right)_5 * 1\mu}{70\mu \left(\frac{8400n}{60n}\right)_1 \left(\frac{700n}{60n}\right)_8}}$$

$$V_{inmax} = 0.6186V$$

V_{outmin}

$$V_{outmin} = V_{ov7}$$

$$V_{outmin} = \sqrt{\frac{2 * I_{D7}}{\mu_n C_{ox} \left(\frac{W}{L}\right)_7}}, \text{ where } I_{D7} = \frac{\left(\frac{W}{L}\right)_6 I_{bias}}{\left(\frac{W}{L}\right)_8}$$

$$V_{outmin} = \sqrt{\frac{2 \left(\frac{W}{L}\right)_6 I_{bias}}{\mu_n C_{ox} \left(\frac{W}{L}\right)_7 \left(\frac{W}{L}\right)_8}}$$

$$V_{outmin} = \sqrt{\frac{2 \left(\frac{10500n}{60n}\right)_6 * 1\mu}{240\mu \left(\frac{4200n}{60n}\right)_7 \left(\frac{700n}{60n}\right)_8}}$$

$$V_{outmin} = 0.0423V$$

V_{outmax}

$$V_{outmax} = V_{DD} - |V_{ov6}|$$

$$V_{outmax} = V_{DD} - \sqrt{\frac{2 * I_{D6}}{\mu_p C_{ox} \left(\frac{W}{L}\right)_5}}, \quad \text{where } I_{D6} = I_{D7}$$

$$V_{outmax} = V_{DD} - \sqrt{\frac{2 \left(\frac{W}{L}\right)_6 I_{bias}}{\mu_p C_{ox} \left(\frac{W}{L}\right)_6 \left(\frac{W}{L}\right)_8}}$$

$$V_{outmax} = 1 - \sqrt{\frac{2 * 1\mu}{(70\mu) \left(\frac{700n}{60n}\right)_8}}$$

$$V_{outmax} = 0.9505V$$

Power Consumption

$$P = V_{DD} I_{tot}$$

$$P = V_{DD} (I_{D5} + I_{D6})$$

$$P = V_{DD} \left(\frac{\left(\frac{W}{L}\right)_5}{\left(\frac{W}{L}\right)_8} + \frac{\left(\frac{W}{L}\right)_6}{\left(\frac{W}{L}\right)_8} \right) I_{bias}$$

$$P = 1 \left(\frac{\left(\frac{7000n}{60n}\right)_5}{\left(\frac{700n}{60n}\right)_8} + \frac{\left(\frac{10500n}{60n}\right)_6}{\left(\frac{700n}{60n}\right)_8} \right) 1\mu$$

$$P = 25\mu W$$

Undesirable Characteristic

Evidently, because all of the opamp's transistors were given lengths of 60nm (more specifically, M1, M2, M3, M4, M6, and M7), and because of the small bias current, the closed loop gain of the op amp is small, which is undesirable. The following calculations show the computation for the closed loop gain; we begin by computing the transconductance of M1 and M7:

$$g_{M1} = \sqrt{2\mu_p C_{ox} \left(\frac{W}{L}\right)_1 I_{D1}}, \quad \text{where } I_{D1} = \frac{\left(\frac{W}{L}\right)_5 I_{D8}}{2 \left(\frac{W}{L}\right)_8}$$

$$g_{M1} = \sqrt{\frac{\mu_p C_{ox} \left(\frac{W}{L}\right)_1 \left(\frac{W}{L}\right)_5 I_{D8}}{\left(\frac{W}{L}\right)_8}}$$

$$g_{M1} = \sqrt{\frac{70\mu \left(\frac{8400n}{60n}\right)_1 \left(\frac{7000n}{60n}\right)_5 1\mu}{\left(\frac{700n}{60n}\right)_8}}$$

$$g_{M1} = 313.05 \mu A/V$$

$$g_{M7} = \sqrt{2\mu_n C_{ox} \left(\frac{W}{L}\right)_7 I_{D7}}, \quad \text{where } I_{D7} = \frac{\left(\frac{W}{L}\right)_6 I_{D8}}{\left(\frac{W}{L}\right)_8}$$

$$g_{M7} = \sqrt{\frac{\mu_n C_{ox} \left(\frac{W}{L}\right)_7 \left(\frac{W}{L}\right)_6 I_{D8}}{\left(\frac{W}{L}\right)_8}}$$

$$g_{M7} = \sqrt{\frac{240\mu \left(\frac{4200n}{60n}\right)_1 \left(\frac{10500n}{60n}\right)_5 1\mu}{\left(\frac{700n}{60n}\right)_8}}$$

$$g_{M7} = 501.996 \mu A/V$$

Let's now find the drain-source resistances of transistors M2, M4, M6, and M7:

$$r_{ds2} = r_{ds4} = \frac{L_2}{\lambda L I_2}, \quad \text{where } I_2 = \frac{\left(\frac{W}{L}\right)_5 I_{D8}}{2 \left(\frac{W}{L}\right)_8}$$

$$r_{ds2} = r_{ds4} = \frac{2L_2 \left(\frac{W}{L}\right)_8}{\lambda L \left(\frac{W}{L}\right)_5 I_{D8}}$$

$$r_{ds2} = r_{ds4} = \frac{2(60n) \left(\frac{700n}{60n}\right)_8}{(0.06\mu) \left(\frac{7000n}{60n}\right)_5 1\mu}$$

$$r_{ds2} = r_{ds4} = 200 k\Omega$$

$$r_{ds6} = r_{ds7} = \frac{L_6}{\lambda L I_6}, \quad \text{where } I_6 = \frac{\left(\frac{W}{L}\right)_6 I_{D8}}{\left(\frac{W}{L}\right)_8}$$

$$r_{ds6} = r_{ds7} = \frac{L_6 \left(\frac{W}{L}\right)_8}{\lambda L \left(\frac{W}{L}\right)_6 I_{D8}}$$

$$r_{ds6} = r_{ds7} = \frac{(60n) \left(\frac{700n}{60n}\right)_8}{(0.06\mu) \left(\frac{10500n}{60n}\right)_6 1\mu}$$

$$r_{ds6} = r_{ds7} = 66.67k\Omega$$

Finally, let's compute the closed loop gain:

$$A_v = g_{M1}(r_{ds2} || r_{ds4}) g_{M7}(r_{ds6} || r_{ds7})$$

$$A_v = g_{M1} \left(\frac{r_{ds2}}{2} \right) g_{M7} \left(\frac{r_{ds6}}{2} \right)$$

$$A_v = 313.05\mu \left(\frac{200k}{2} \right) 501.996\mu \left(\frac{66.67k}{2} \right)$$

$$A_v = 523.83V/V$$

Evidently, this value is bound to have poor accuracy, as the equations used to compute the drain source resistances are about 50% accuracy, and it is likely that the values for K_n , K_p , and λ simulated by spice are different from those used in the computation above.

Closed Loop Impedance Units

The following equation represents the input-output relationship of the Capacitive Reset Gain Circuit during the sampling phase (assuming an ideal opamp is used):

$$v_{out}(n) = -\left(\frac{C_1}{C_2}\right) v_{in}(n)$$

Evidently, to make the PGA programmable, one needs to enable the values for C_1 and/or C_2 to be programmable as well. For simplicity, it was decided that C_2 would have a constant value of 500fF, while C_1 would be programmable.

Impedance 1

The following figure presents the schematic of the impedance 1 unit:

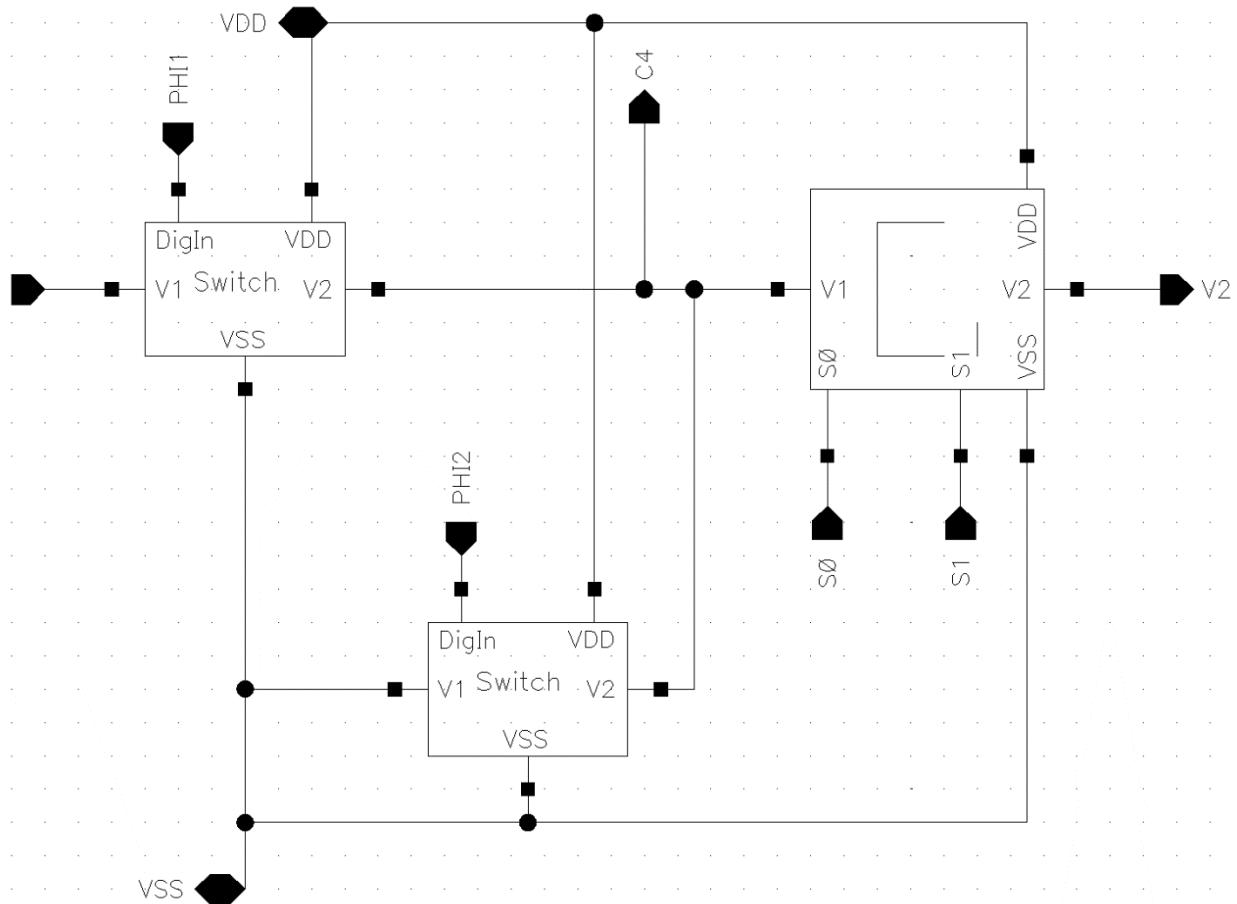


Figure 10: Impedance 1 unit schematic.

When phi2 is high, the input output relation (mentioned above) is invalid, as the circuit resets during this phase. However, when phi1 is high, the input voltage charges C_1 (which is programmable), and the same current is seen across C_2 . This gives rise to the circuits input output relation during the sampling phase. The following figure presents the schematic of the programmable C_1 unit:

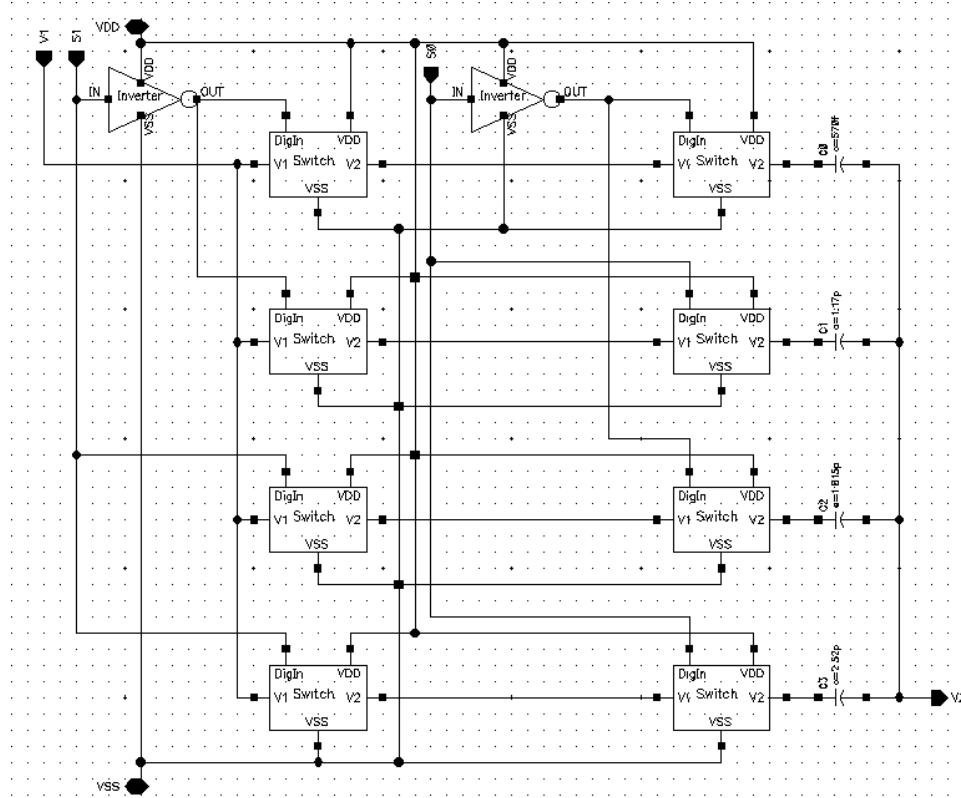


Figure 11: Programmable C_1 unit schematic.

As can be seen, this circuit uses the same idea behind that of the analogue multiplexer. Only one branch of the circuit can allow current to flow through at a time; select lines S_1 and S_0 choose which branch is active. Subsequently, the equivalent capacitance across the circuit is approximately that of the capacitor at the end of the active branch. Given the information above, the following truth table describes the behavior of this circuit:

Table 2: Programmable C_1 unit truth table.

S_1	S_0	C_1 (F)	Gain (V/V)
0	0	570f	1
0	1	1.170p	2
1	0	1.815p	3
1	1	2.520p	4

As can be seen, the values for C_1 are higher than those for the corresponding ideal circuit. Given that C_2 is equal to 500f, one might expect C_1 to be programmable to have values of 500f, 1000f, 1500f, and 2000f. However, as was seen earlier, the opamp's gain is finite, and as such, there is some error in the circuit's closed loop gain. Granted, in the case of a capacitive-reset gain circuit operating at low frequencies, this error is proportional to $1 / A^2$ rather than the usual $1 / A$. Regardless, the values for C_1

are different from those of the ideal circuit because they were tuned to compensate for the reduction in the circuit's closed loop gain caused by the opamp's finite open loop gain.

A tuning procedure was performed to derive the appropriate values of C_1 . The PGA test bench (see Test Benches and Simulations - PGA) was used to assess the various peak to peak voltage values of V_{out} for each gain level under ideal conditions. After a given iteration of the tuning procedure, the capacitor values were changed in accordance with the following equation:

$$C_{new} = C_{old} \left(\frac{V_{outp-pideal}}{V_{outp-p}} \right)$$

Where V_{outp-p} denotes the peak-to-peak voltage of V_{out} seen in the simulation, and $V_{outp-pideal}$ denotes the ideal peak to peak voltage of V_{out} . For an input having a peak-to-peak voltage of 40mV, $V_{outp-pideal}$ would have values of 40mV, 80mV, 120mV, and 160mV respectively for each level of gain.

Impedance 2

The following figure presents the schematic of the impedance 2 unit:

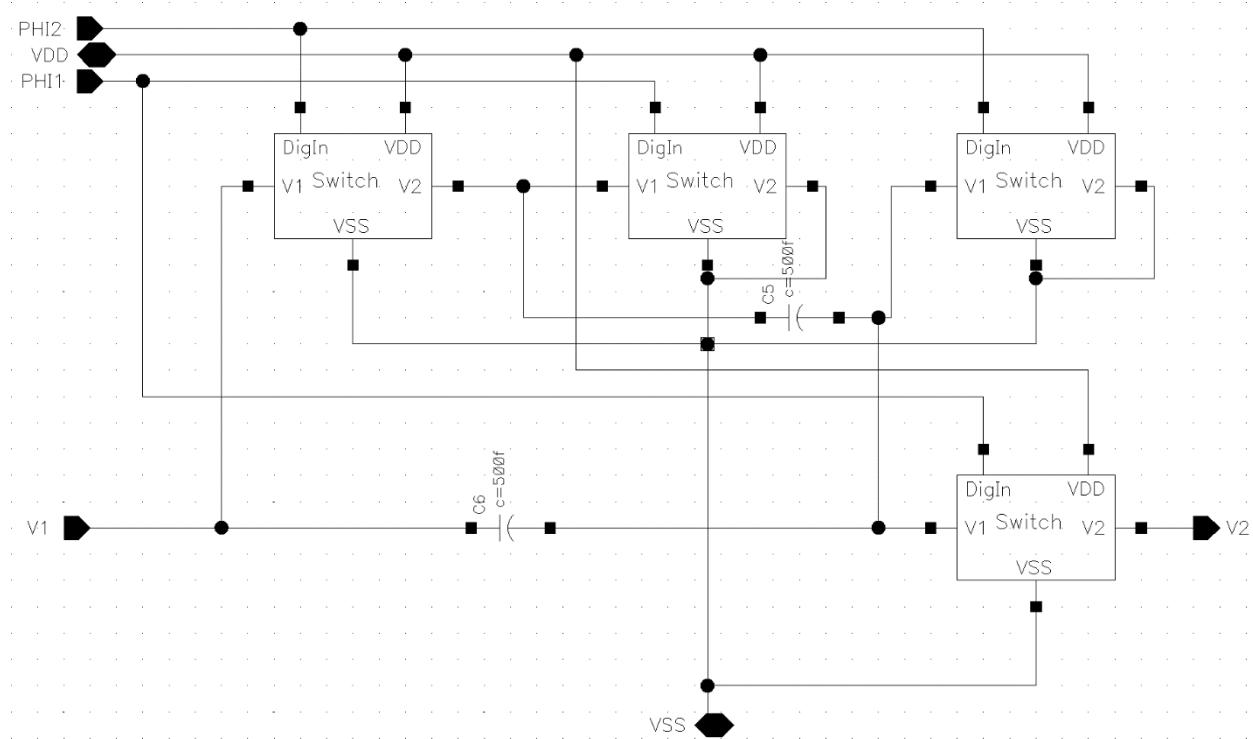


Figure 12: Impedance 2 unit schematic.

As can be seen, it contains a pin for the “deglitching” capacitor (C_4), which has a value of $250f$. Moreover, as was mentioned previously C_2 has a value $500f$.

ADC

We decided to implement a successive approximation charge redistribution analog to digital converted (SAR ADC). This decision was made because of its low power consumption, high resolution, and precision. Due to the many steps required to go from sampling the voltage to reading a digital value this type of ADC is slower than other types like flash. We will show that this limitation will not be an issue for our purposes and the benefits of its power and resolution will make it a great fit.

Double Throw CMOS Switch

The ADC uses many double throw CMOS switches that are controlled by the SAR to toggle the capacitors used between different voltages at different stages. These switches use two CMOS transfer gates to achieve strong connection at full-scale voltage ranges. Figure 13 is the design used for these switches, an inverter is used so a single input of ‘0’ or ‘1’ will select between powering either of the switches.

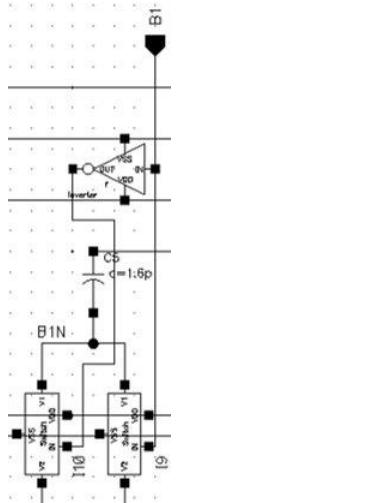


Figure 13 - Double throw CMOS switch

Overall Design

Figure 14 shows the final schematic of our implementation of the ADC. The design uses a binary weighted array of capacitors that are charged/discharged sequentially to determine the binary equivalent value. The process is achieved in three stages: sample, hold, and bit cycling.

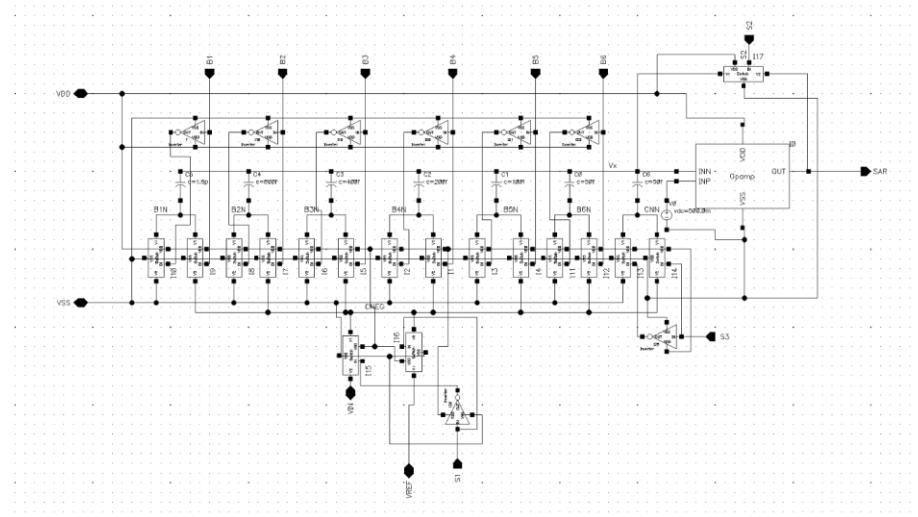


Figure 14 - ADC schematic

The first stage sampling is done to store the input voltage we want to determine its binary equivalent of. Figure 15 shows the connections made in sample mode (yellow lines show paths of closed switches), S2 is closed making the Op-amp a buffer for the 500mV voltage reference on the positive input. At this stage the negative input (V_x) is 500mV (for an ideal Op-amp). This voltage reference is set such that the Op-amp is always working within its active region. Next the capacitors are connected to V_{IN} using B1-B6 and S1, this samples the voltage onto the capacitors.

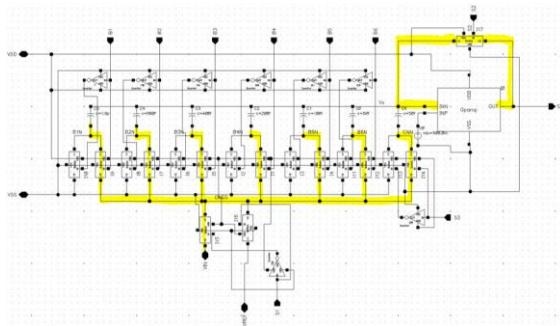


Figure 15 - ADC sample mode

After the voltage is sampled the ADC moves onto the hold stage. During this stage S2 is opened running the Op-amp open loop as a comparator. Next the capacitors are connected to ground as we can see in Figure 16. This causes V_x to become biased by $-V_{in}$ changing the new voltage to:

$$V_x = 500mV - V_{in}$$

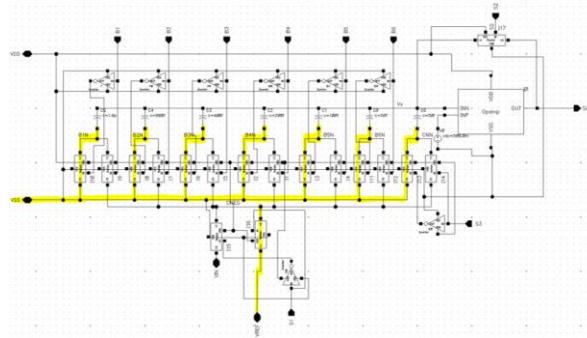


Figure 16 - ADC hold mode

The final stage is bit cycling, this stage uses successive approximation to determine bit by bit a precise binary representation. Figure 17 shows the connections made when the MSB is being cycled. This means that our largest capacitor of size 32C ($C=5fF$) is connected to V_{ref} , because our capacitor array has a total capacitance of 64C we get a capacitive divider of $\frac{1}{2}$. Making our new V_x :

$$V_x = 500mV - V_{in} + \frac{V_{ref}}{2}$$

V_x is connected to our negative Op-amp terminal while the positive is connected to 500mV. If the negative input > positive input then the Op-amp comparator has an output of VDD, otherwise it will be zero (for ideal Op-amp). The SAR will read this output and if a VDD is read then the capacitor stays connected to V_{ref} otherwise it will be returned to ground. If it returns to ground V_x will return to its previous value. This process will repeat for each bit changing the V_x by each bit's weight reflected by the capacitor ratios.

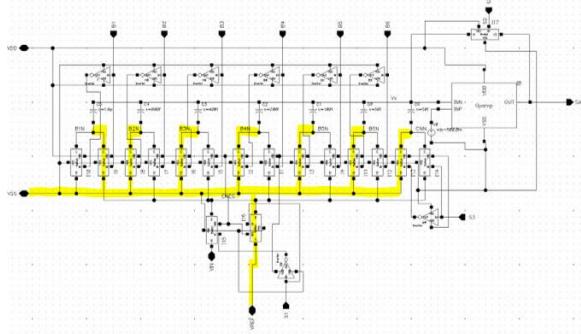


Figure 17 - ADC bit cycling

SAR

To control the switches for the ADC to operate in different modes a successive approximation register was implemented using VerilogA. Figure 44 and Figure 45 is the VerilogA code used to implement the SAR.

Parameters

The heart of the ADC is the comparator, we decided to implement it using an Op-amp because our sampling frequency is not high enough to require a specialized comparator. This saves cost by allowing the Op-amp layout and design to be reused.

The capacitors we used in the array have the smallest capacitor of 50fF, this value was chosen because the smallest capacitor size (limited by manufacturing) of 5fF would introduce a significant amount of error due to voltage loss from leakage current. Having the capacitors too large will be costly due to the large amount of area they take up and if the capacitance is too high the Op-amp won't be able to supply enough current. This will slow the rate the capacitors charge/discharge and will cause issues at high frequency's because it won't have enough time to settle. The operation precision of the ADC requires accurate ratios between capacitors, to achieve this we will use capacitor matching techniques. The main source of error for small capacitors is due to over etching, this causes the actual areas to be smaller than the mask. This effect can be combated in two ways, the first is using larger capacitors because this will reduce the effect the mismatch has on error but as we discussed earlier size is expensive. Thus, we need to use unit sized capacitors of C=50fF, this works by creating the ratios by adding together many C sized capacitors in parallel to get 2C,4C,8C,16C, and 32C sizes. Unit sized capacitors have the advantage of each containing the same relative error that becomes irrelevant when used for ratios.

Test Benches and Simulations

Inverter and Switch

The test benches and simulations for the inverter and switch can be found in the appendix (Figure 39Figure 42).

Multiplexer

The following figures present the test bench and simulation results for the multiplexer:

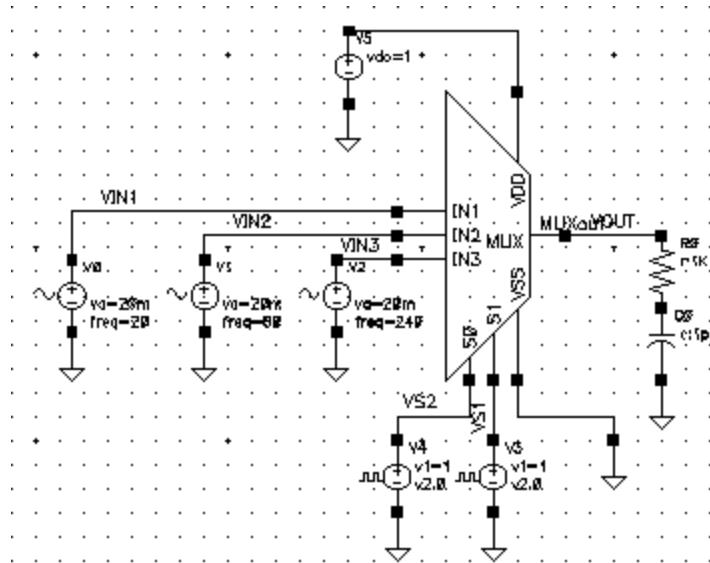


Figure 18: Multiplexer test bench.

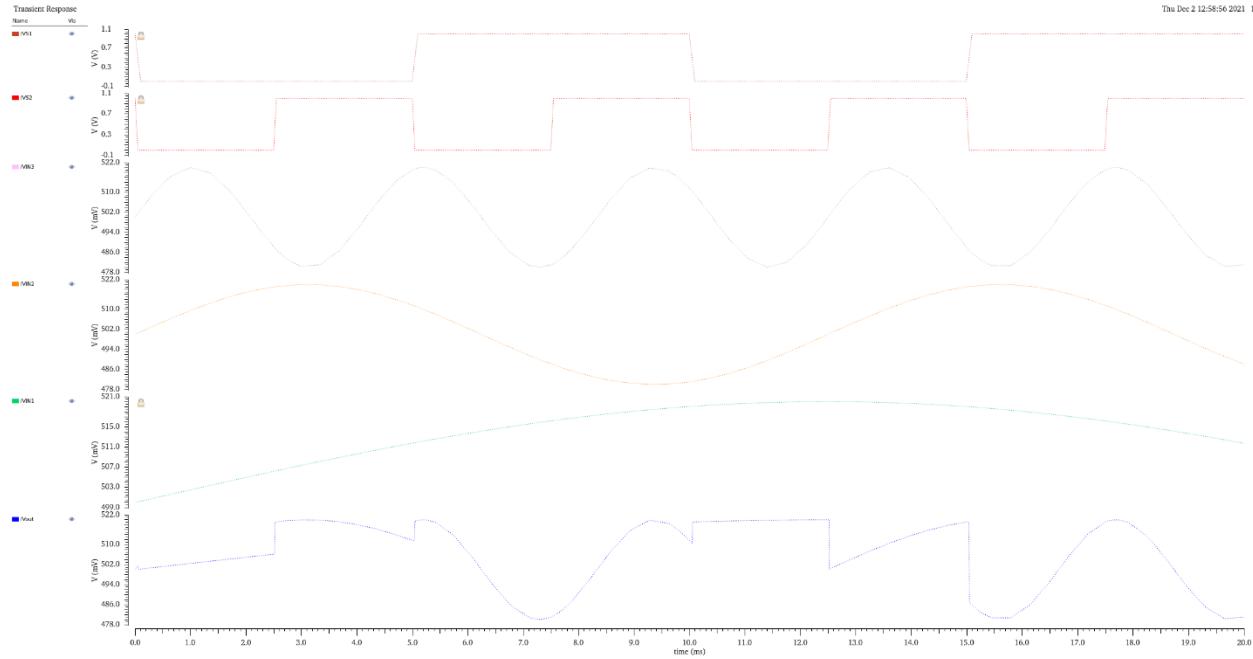


Figure 19: Multiplexer simulation results.

As can be seen, the simulation results show that the multiplexer exhibits the correct behavior, as it follows the same logic outlined in Table 1. During each permutation of clock 1 and clock 2 (i.e. S1 and S0), the correct input gets passed to the output.

Open Loop Opamp

The following figure presents the test bench that was to validate the Opamp in an open loop setting:

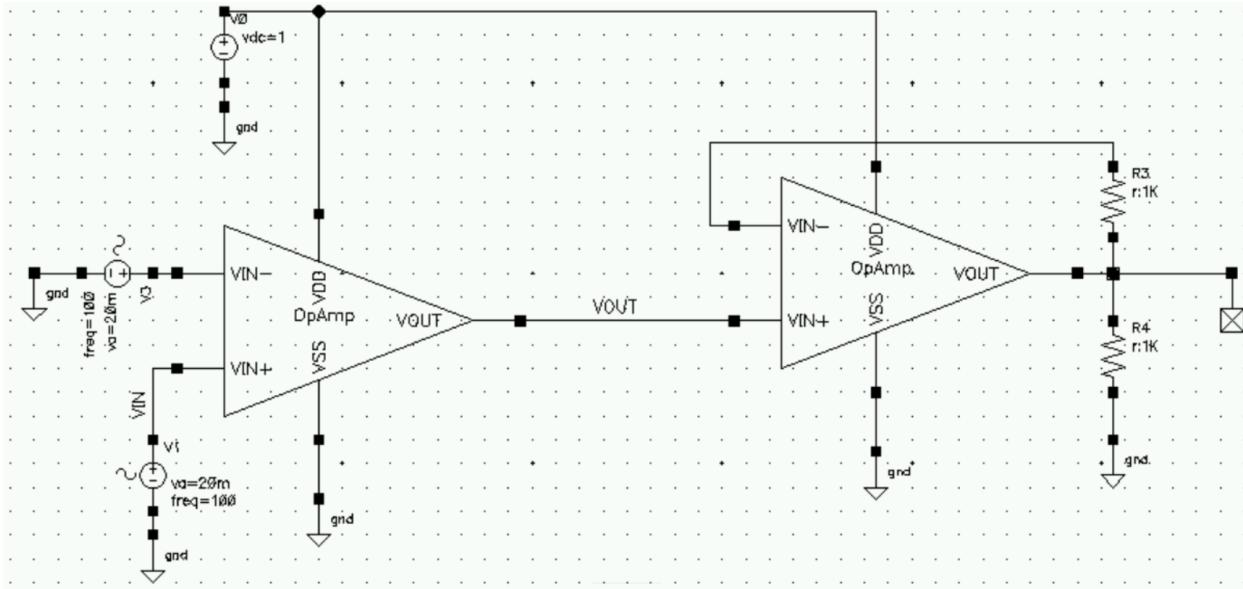


Figure 20: Open loop Opamp test bench.

This test bench was used to analyze the opamp's bode plot and temperature versus open loop gain relation.

Opamp Stability

The following figure presents the opamp's magnitude and phase response (bode plot):

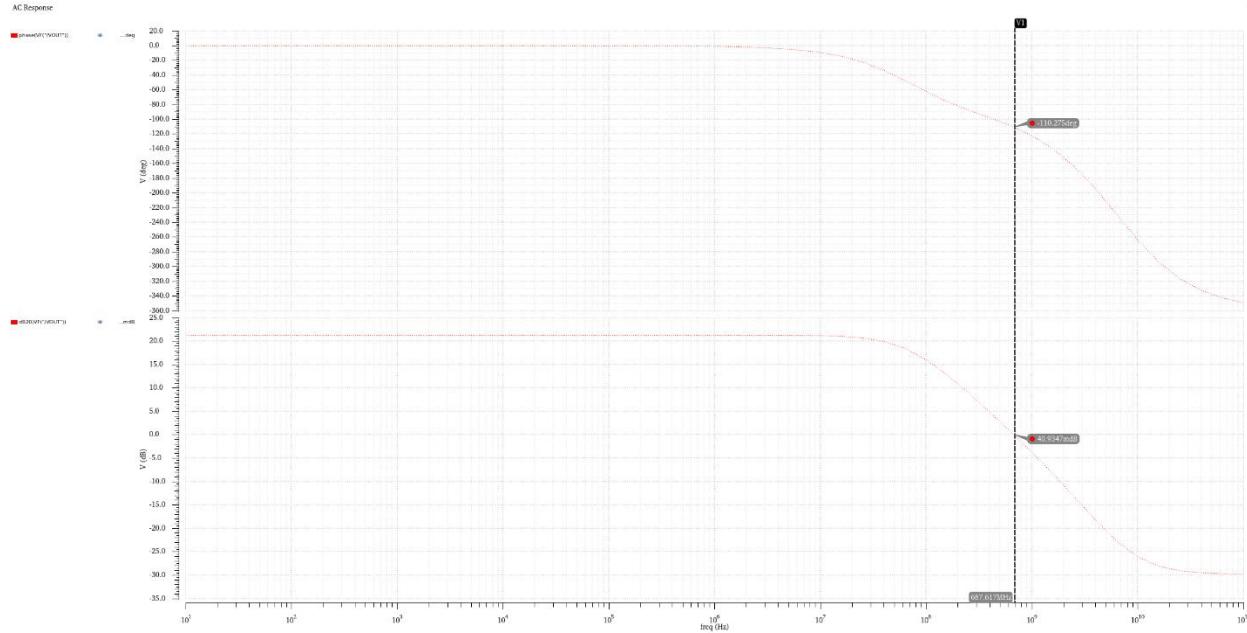


Figure 21: Opamp magnitude and phase response (bode plot).

As can be seen, the opamp has the following phase margin:

$$PM = \angle L(\omega_t) + 180^\circ$$

$$PM = -110.275^\circ + 180^\circ$$

$$PM = 69.7^\circ$$

A phase margin of 69.7° indicates that the opamp is rather stable, as it is well within the range of 45° and 90° . A modest compensating capacitor value of 10fF was used to shift the first pole ω_{p1} to the left such that this phase margin could be achieved.

Opamp Gain Versus Temperature

The following figure presents the opamp's open loop gain as a function of temperature (assuming an input frequency of 100Hz):

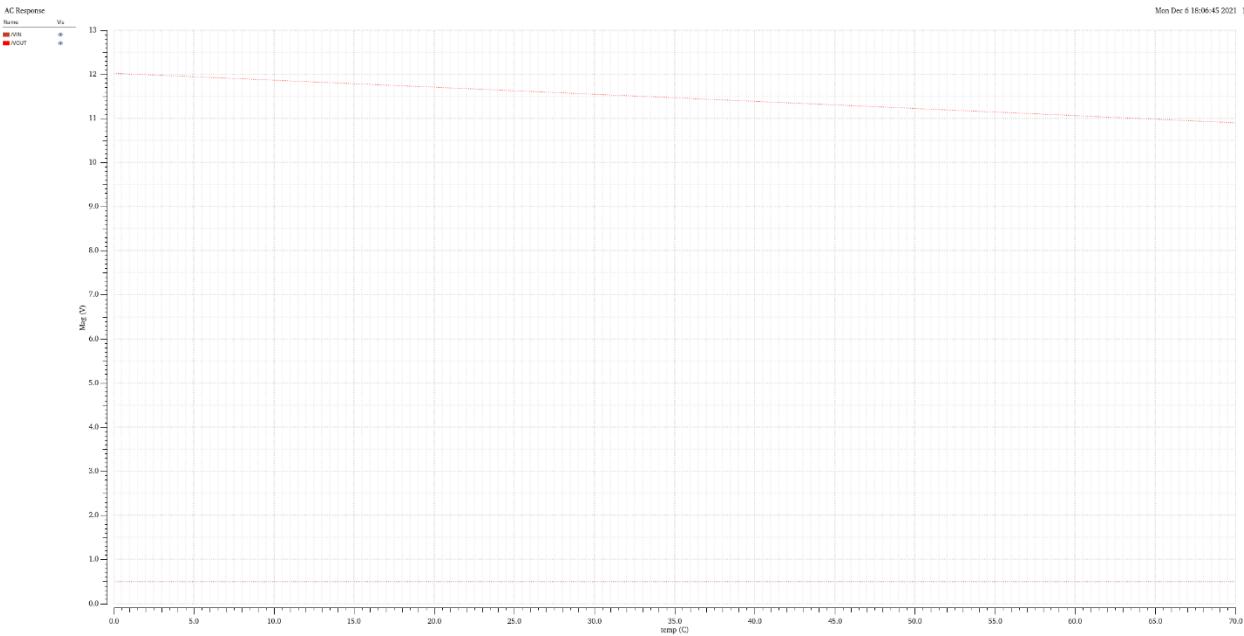


Figure 22: Opamp gain versus temperature, where the input frequency is set to 100Hz.

As can be seen, a change in temperature from 0° to 70° causes the gain to change by about 10%. Coupled with the fact that the gain is small to begin with ($\sim 12V/V$), this gives rise to an unfavorable response to temperature changes, as will be discussed in the following subsection.

PGA

The following figure presents the test bench that was to validate the PGA:

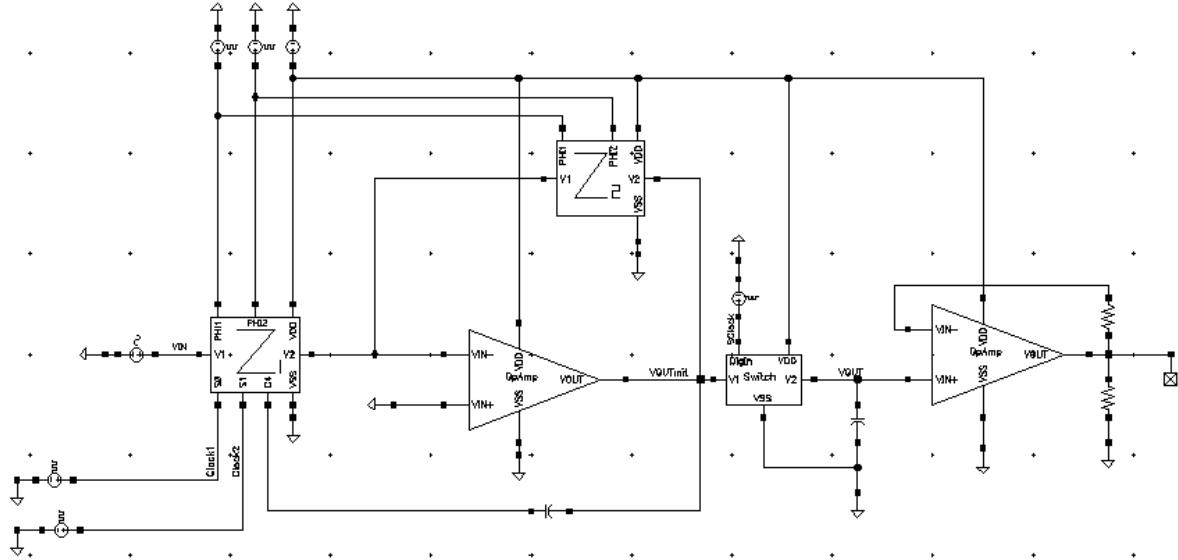


Figure 23: Programmable gain amplifier test bench.

This test bench contains a simple sample and hold circuit at the output, which samples the PGA's output during the correct periods (as would the ADC). In this test bench, the switch capacitor clocks have frequencies set to 1us. As such, the switch capacitors in this circuit have equivalent resistances on the order of a few hundred kilo-ohms to a few mega-ohms (e.g. 1us / 1pF = 1MΩ). This test bench was used in a variety of conditions, and the results from such will be discussed in the following sub sections.

Ideal Conditions

The following figure presents the PGA's performance when V_{DD} is set to 1 V and when the temperature is set to 27° Celsius:

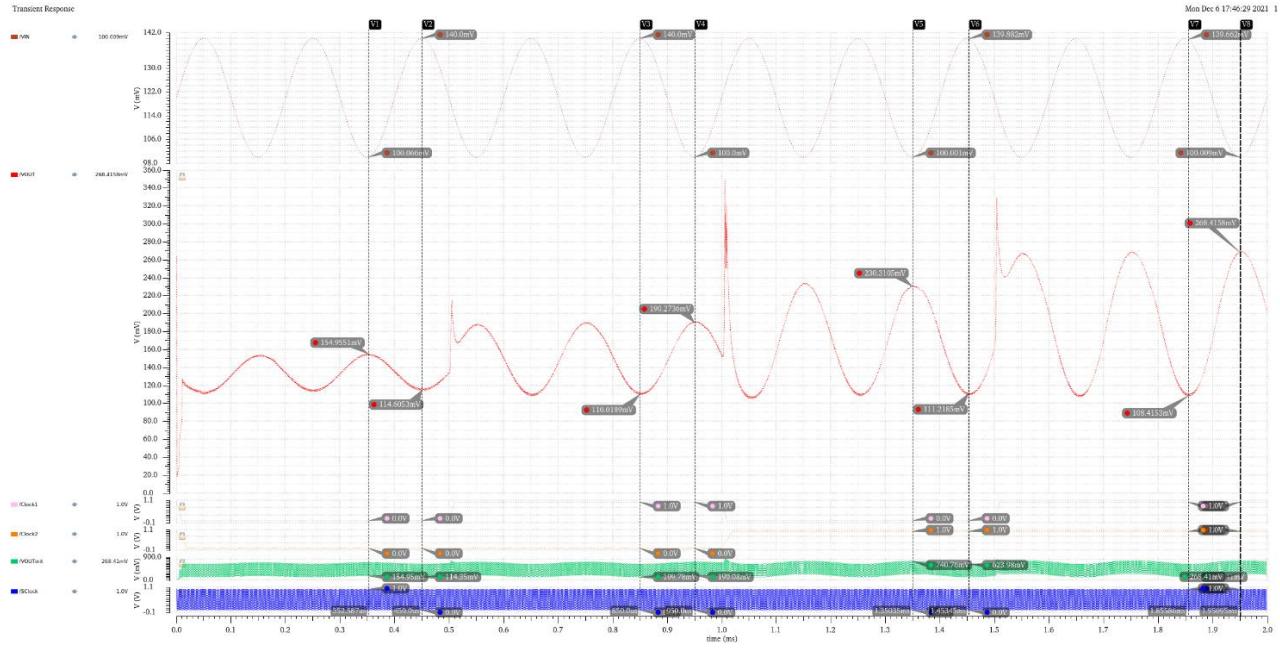


Figure 24: PGA output when V_{DD} is set to 1 V and when the temperature is set to 27° Celsius.

The following table presents the peak-to-peak voltage of V_{out} for each gain level under these conditions, and the corresponding error associated with such:

Table 3: PGA accuracy when V_{DD} is set to 1 V and when the temperature is set to 27° Celsius.

Gain setting (V/V)	$V_{out,p}$ observed (V)	Error $((V_{out,p}/V_{out,pideal}) - 1) * 100\%$
1	40.34	+0.850%
2	80.25	+0.313%
3	119.092	-0.757%
4	160.0005	+0.0003%

As can be seen, the PGA works within 1% accuracy for each level of gain under ideal conditions.

70° Celsius

The following presents the PGA's performance when V_{DD} is set to 1 V and when the temperature is set to 70° Celsius:

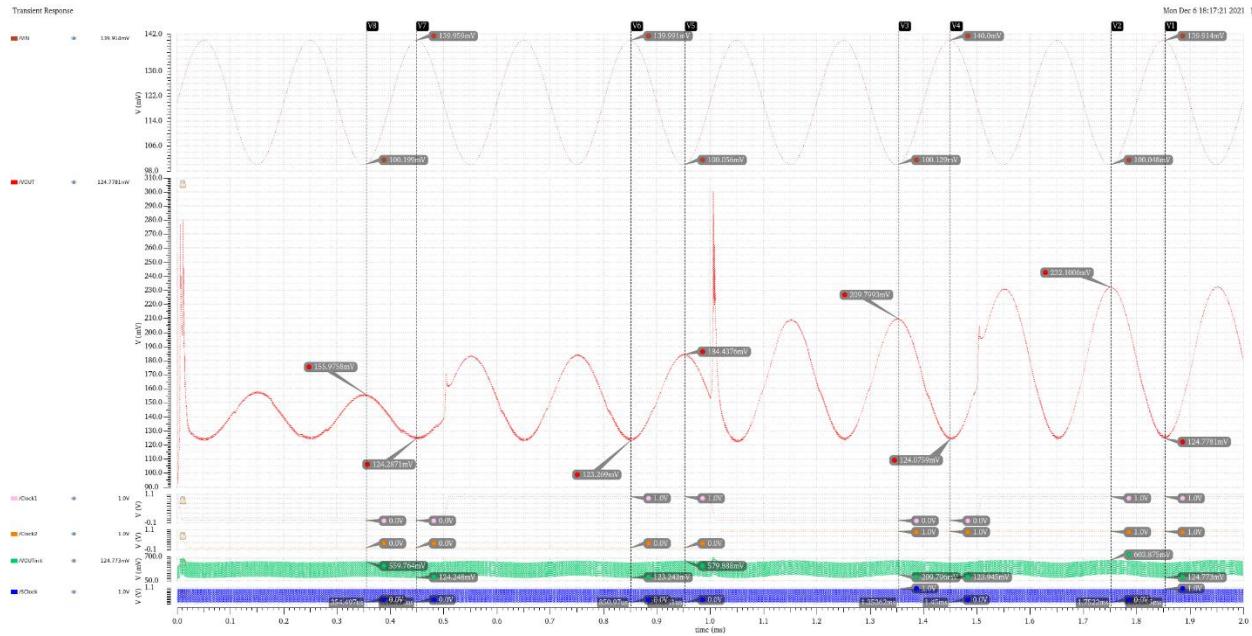


Figure 25: PGA output when V_{DD} is set to 1 V and when the temperature is set to 70° Celsius.

The following table presents the peak-to-peak voltage of V_{out} for each gain level under these conditions, and the corresponding error associated with such:

Table 4: PGA accuracy when V_{DD} is set to 1 V and when the temperature is set to 70° Celsius.

Gain setting (V/V)	V_{outp-p} observed (V)	Error $((V_{outp-p}/V_{outp-pideal}) - 1) * 100\%$
1	31.6887	-20.8%
2	61.1686	-23.5%
3	85.7234	-28.6%
4	107.3226	-33.0%

Evidently, the PGA does not perform very well when the temperature is different from 27° Celsius. This is because a change in temperature changes the open loop gain, which subsequently changes the closed loop gain. Moreover, the open loop gain is rather small, so the amount by which the open loop gain changes is larger than it would be if the closed loop gain was larger.

0° Celsius

The following presents the PGA's performance when V_{DD} is set to 1 V and when the temperature is set to 0° Celsius:

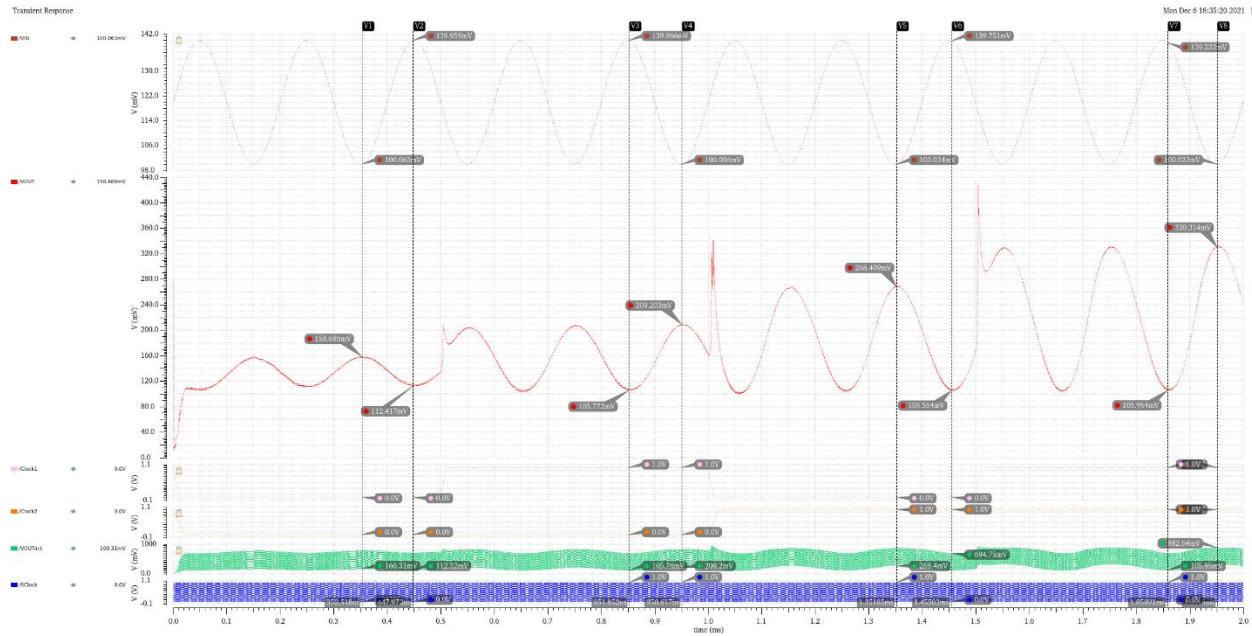


Figure 26: PGA output when V_{DD} is set to 1 V and when the temperature is set to 0° Celsius.

The following table presents the peak-to-peak voltage of V_{out} for each gain level under these conditions, and the corresponding error associated with such:

Table 5: PGA accuracy when V_{DD} is set to 1 V and when the temperature is set to 70° Celsius.

Gain setting (V/V)	$V_{out,p}$ observed (V)	Error $((V_{out,p}/V_{out,pideal}) - 1) * 100\%$
1	46.269	+15.67%
2	103.845	+29.81%
3	162.845	+35.70%
4	224.36	+40.23%

For similar reasons to those discussed for the case where the temperature is set to 70° Celsius, the performance of the PGA is degraded when the temperature is set to 0° Celsius.

$$V_{DD} = 1.05V$$

The following presents the PGA's performance when V_{DD} is set to 1.05 V and when the temperature is set to 27° Celsius:

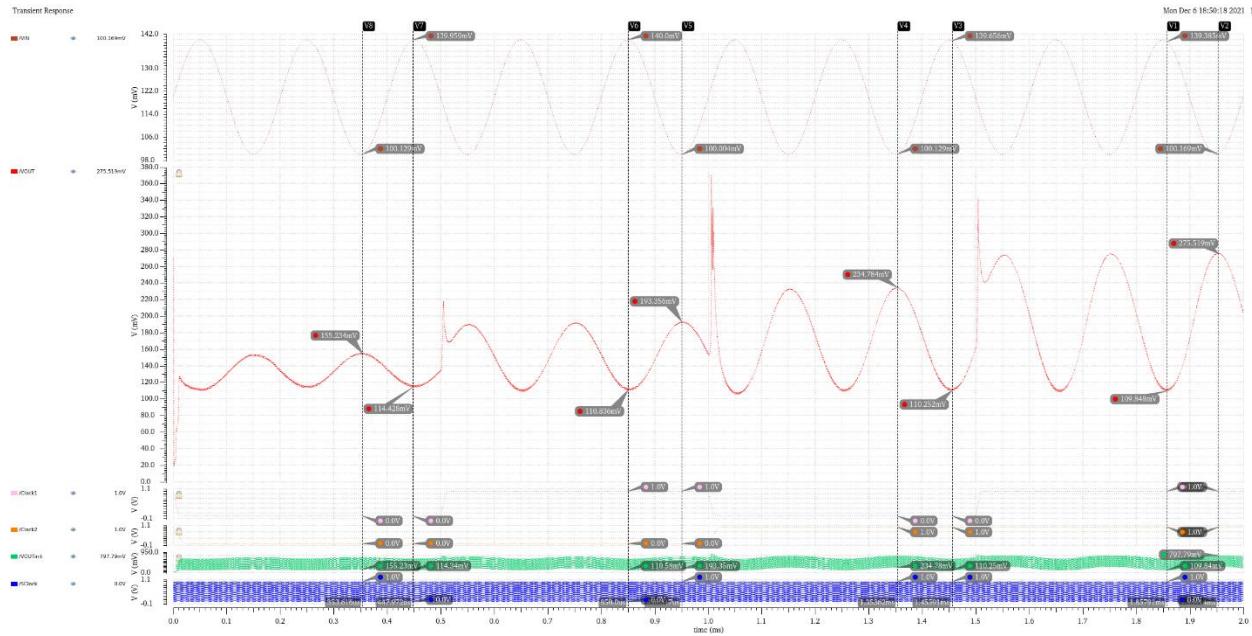


Figure 27: PGA output when V_{DD} is set to 1.05 V and when the temperature is set to 27° Celsius.

The following table presents the peak-to-peak voltage of V_{out} for each gain level under these conditions, and the corresponding error associated with such:

Table 6: PGA accuracy when VDD is set to 1.05 V and when the temperature is set to 27° Celsius.

Gain setting (V/V)	$V_{out,p}$ observed (V)	Error $((V_{out,p}/V_{out,pideal}) - 1) * 100\%$
1	39.806	-0.485%
2	82.52	+3.15%
3	124.532	+3.78%
4	165.671	+3.54%

As can be seen, the accuracy of the PGA is slightly diminished when V_{DD} is altered, but not nearly as much as is the case when the temperature is altered. This may be partly because $V_{in,max}$ and $V_{out,max}$ (which are dependent of V_{DD}) are large relative to the bias voltage of the input signal. As such, the transistors can stay in saturation, even when large variations in V_{DD} are considered and thus, the opamp is able to operate relatively effectively.

$$V_{DD} = 0.95V$$

The following presents the PGA's performance when V_{DD} is set to 0.95 V and when the temperature is set to 27° Celsius:

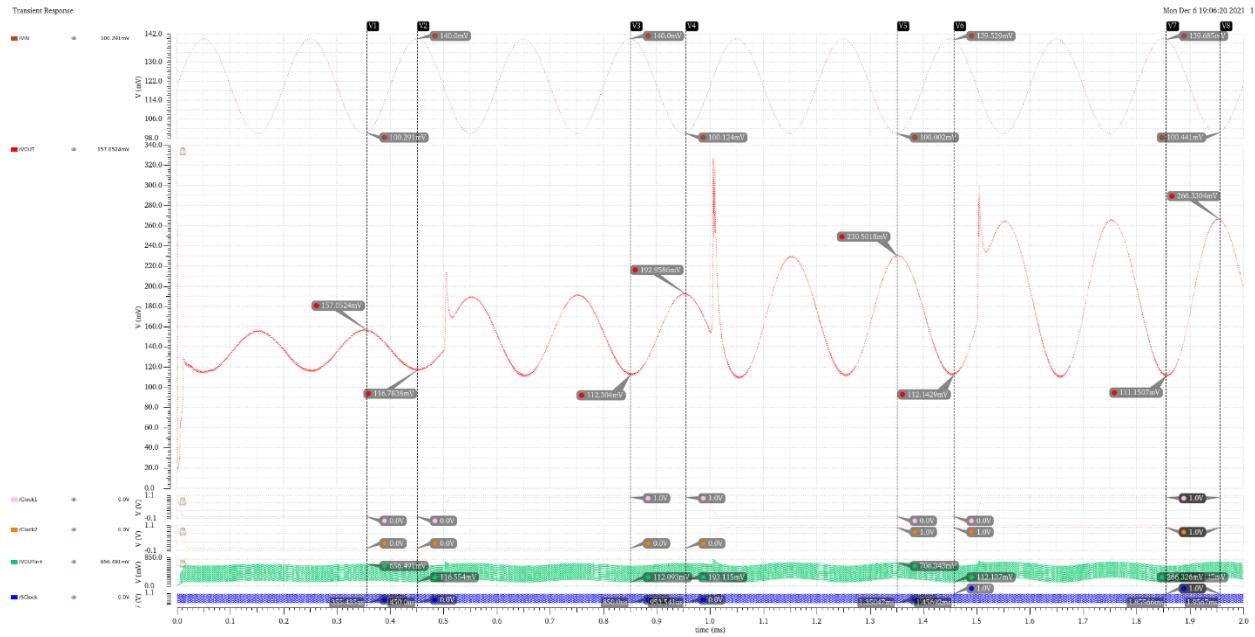


Figure 28: PGA output when V_{DD} is set to 0.95 V and when the temperature is set to 27° Celsius.

The following table presents the peak-to-peak voltage of V_{out} for each gain level under these conditions, and the corresponding error associated with such:

Table 7: PGA accuracy when V_{DD} is set to 0.95 V and when the temperature is set to 27° Celsius.

Gain setting (V/V)	$V_{out,p}$ observed (V)	Error $((V_{out,p}/V_{out,pideal}) - 1) * 100\%$
1	40.2702	+0.675%
2	80.6546	+0.818%
3	118.3589	-1.37%
4	155.1797	-3.01%

For similar reasons to those discussed for the case where V_{DD} is set to 1.05V, the performance of the PGA is only slightly degraded when V_{DD} is set to 0.95V.

ADC

The following figures are test benches showing the ADC operating in different conditions.

Ideal Conditions

Figure 29 is the test bench used to demonstrate the ADC's functionality. The ADC is using a 1V voltage reference that is regulated independently from VDD. We are also supplying a 240mV voltage to the input of the ADC. As we can see the SAR controls B1-B6, S1,S2, and S3 then monitors the SAR output to calculate the output bits (out<0:5>). To control the SAR a clock with a period of 1us is used.

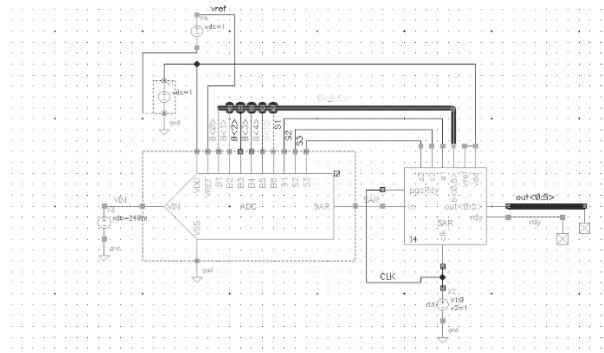


Figure 29 - ADC Test Bench

Figure 30 is the simulation results for the ADC test bench shown in Figure 29. This simulation is sampling 240mV. Label M1 is the negative opamp voltage (V_x) while the ADC is sampling. According to theory this should be 500mV but due to the Op-amp being non-ideal we have a voltage of 518.321mV. This seems like a large source of error but due to the method of determining the voltage this offset of 18mV is compensated for. The next stage is hold, here we can see label M2 gives a V_x of 279mV. We know this value should be:

$$518.321 - V_{in} = 518.321 - 240mV = 278.321mV$$

Next the ADC enters bit cycling, when B6 is connected to vref we expect V_x to shift up by 500mV and shown by M3 to M4 we get a shift of 499mV. We find the output value SAR is about zero (less than 500mV) so the SAR connect B6 back to ground and connect B5 to vref. This switch will change V_x by:

$$-\frac{V_{ref}}{2} + \frac{V_{ref}}{4} = -500mV + 250mV = -250mV$$

The change in voltage seen between M4 and M5 is -250mV in the simulation. This process continues for each bit until $t=9.5\mu s$ when the rdy signal is set high. At this point we know that the ADC output is valid, reading the bits out<0:5> we get a binary number of 001111 = 15 decimal. We can calculate the binary represented voltage using:

$$V_{eq} = \frac{out_{dec}}{2^6} * FS_{voltage} = \frac{15}{64} * 1V = 234mV$$

The accuracy of our ADC is within one LSB:

$$V_{lsb} = \frac{1}{64} * 1V = 15.6mV$$

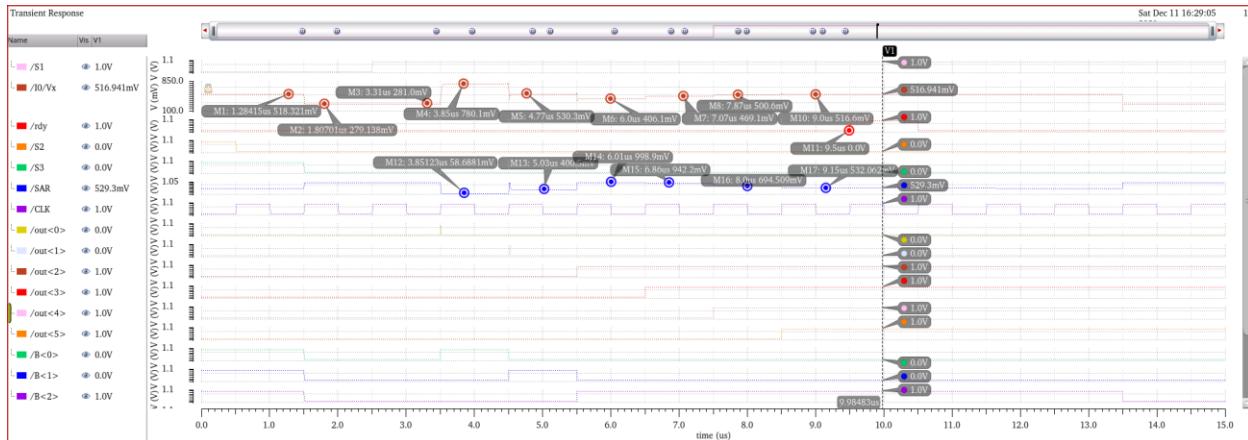


Figure 30 - ADC ideal simulation

70 Degrees

Simulating at 70 degrees our output value stays accurate within 1 LSB. While our VerilogA SAR can achieve consistent resolution at 70 degrees this will be more difficult in a real-world scenario. The output of the Op-amp (SAR output) in the ADC depends on the difference between its input pins, with an infinite gain (ideal) we get strong '0' and '1's but our Op-amp has a low gain making a '1' anything greater than 500mV while a '0' is anything below 500mV. With the temperature effecting mostly the gain of the Op-amp we will have a harder time distinguishing between HIGH and LOW. Our SAR doesn't is able to decode this fine but in the real world these soft values can cause issues.

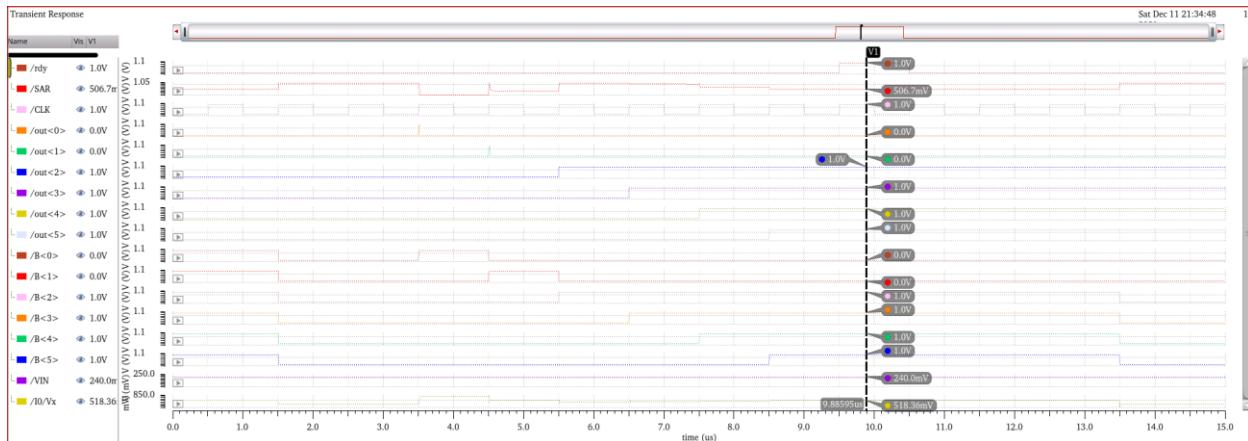


Figure 31 - ADC at 70 degrees

0 Degrees

Simulating at 0 degrees our output value stays accurate within 1 LSB.

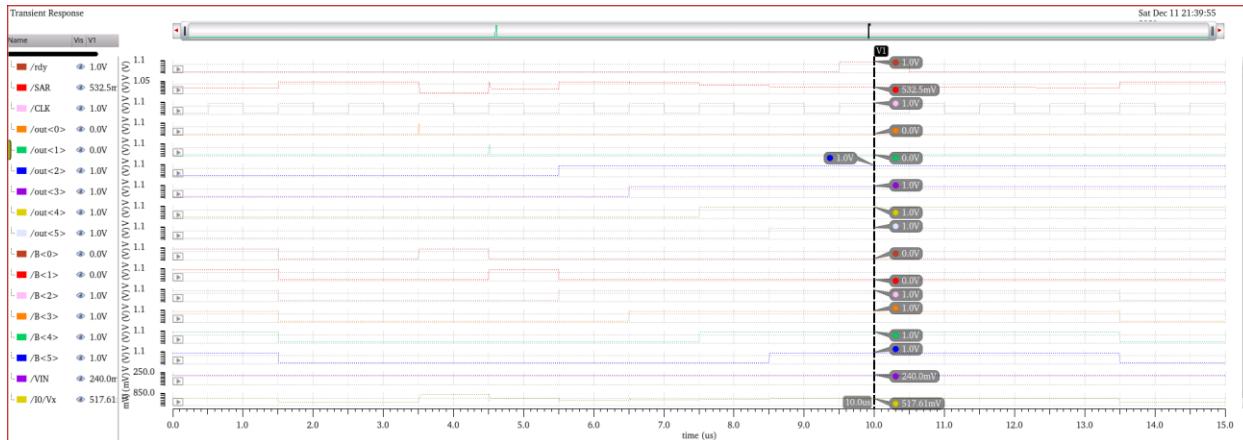


Figure 32 - ADC at 0 degrees

1.05V VDD

Once again, we get an output equal to that in the ideal schematic. This is due to the voltage reference being independent from the VDD.

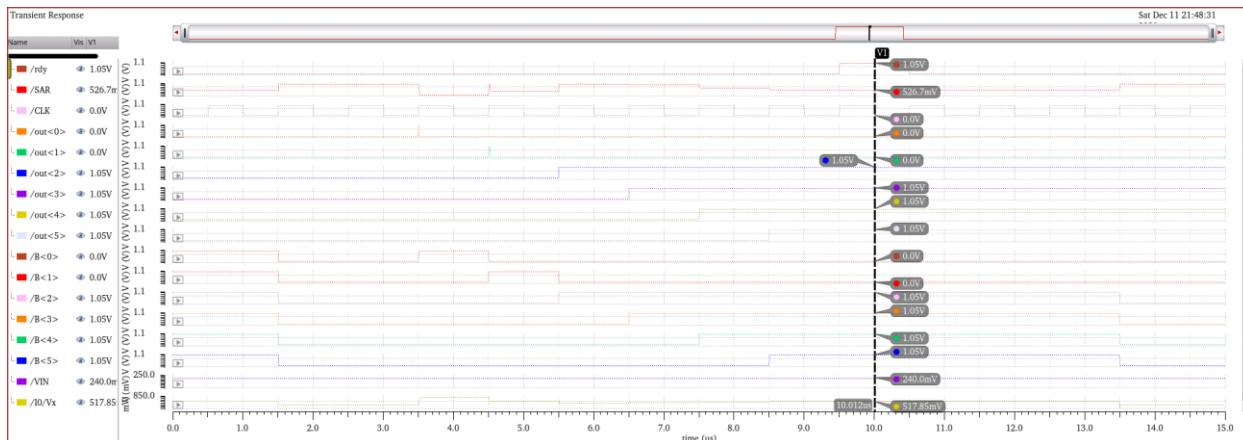


Figure 33 - ADC simulation, VDD=1.05V

Complete Design

The complete design was implemented as seen in Figure 34. This test bench takes three ECG signals and selected one using the MUX. The Mux output feeds into the PGA which applies a programmable gain which is finally sent to the ADC for reading.

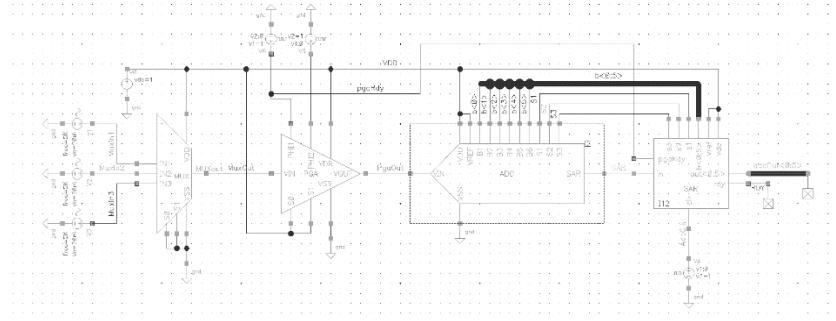


Figure 34 - Complete design

Figure 35 and Figure 36 is the complete simulation of the overall design. We can see the Mux, PGA, and ADC's respective values. Figure 36 is zoomed in on V1 market seen on Figure 35, this marker shows the PGA output voltage of 142.9mV. This voltage is sampled by the ADC and market V2 is located when the ready signal is HIGH. We can read the bits of $\text{adcOut}<0:5> = 001001 = 9$ decimal.

$$V_{eq} = \frac{9}{64} * 1V = 141mV$$

The results are very close to the PGA outputs actual value.

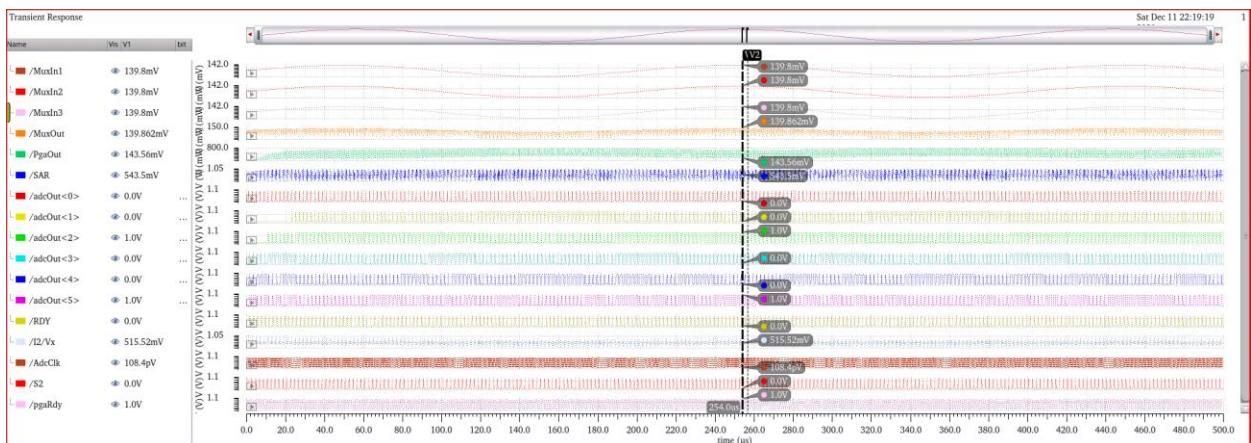


Figure 35 - Complete simulation

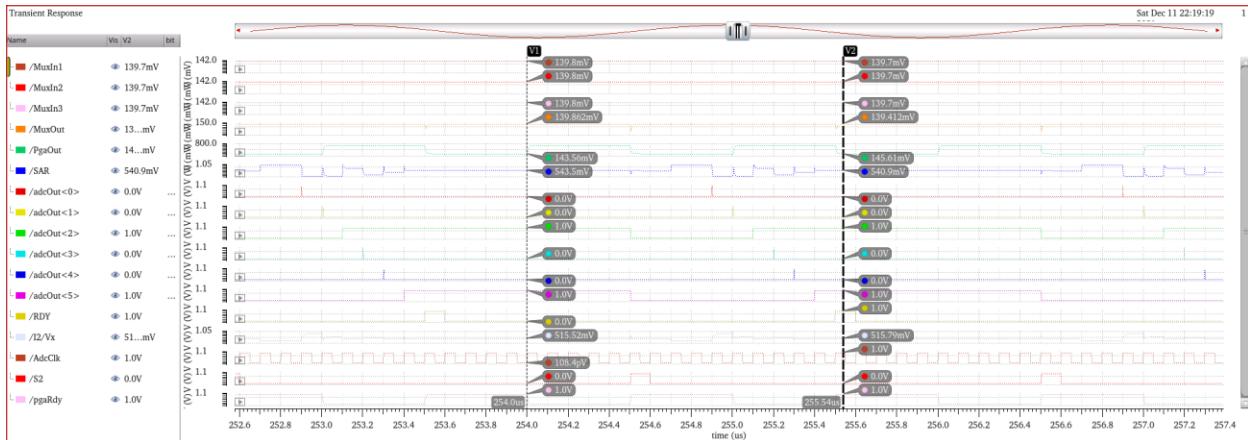


Figure 36 - Complete simulation results

Cost Estimation

For the following discussion, it is assumed that the cost of the overall ECG interface is proportional to the area of the physical PCB. Because the design is composed of transistors and capacitors, the area taken up by each type of element will be analyzed in the following subsections.

Transistor Area Estimation

The following figure presents the layout of the inverter:

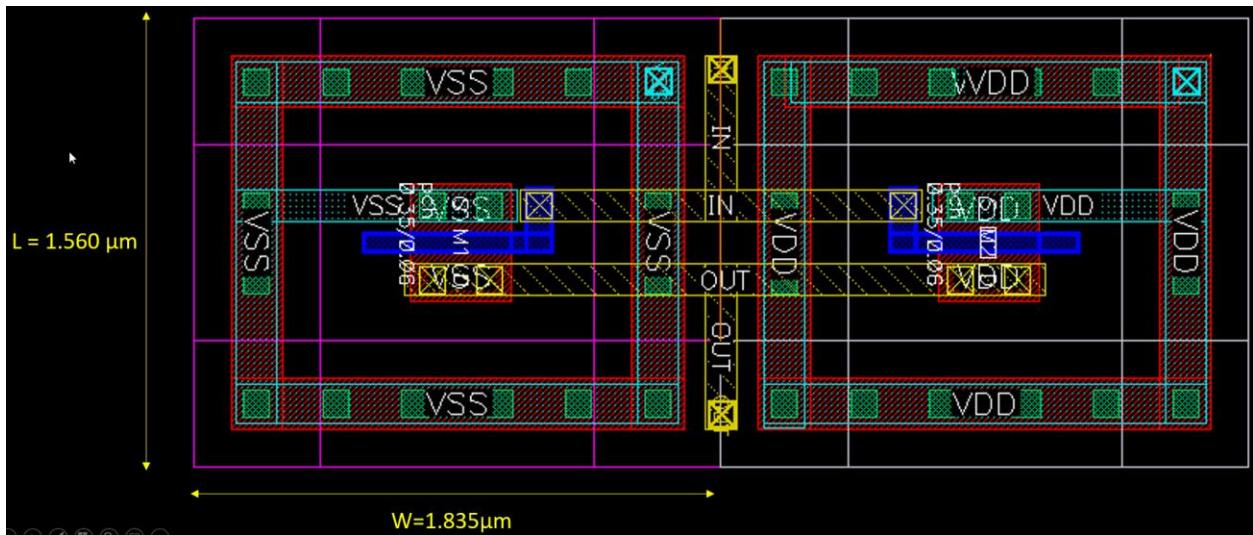


Figure 37: Inverter layout.

The DRC for this layout can be found in the appendix (Figure 43). As can be seen, the transistors are surrounded by connections made to either V_{SS} or V_{DD} . This is to ensure that the transistors are completely electrically isolated and to prevent conduction between the transistor terminals and the substrate. This does come with the cost of taking up more area and the introduction of an additional metal layer. The overall area taken up by transistors can be estimated by considering the following figure:

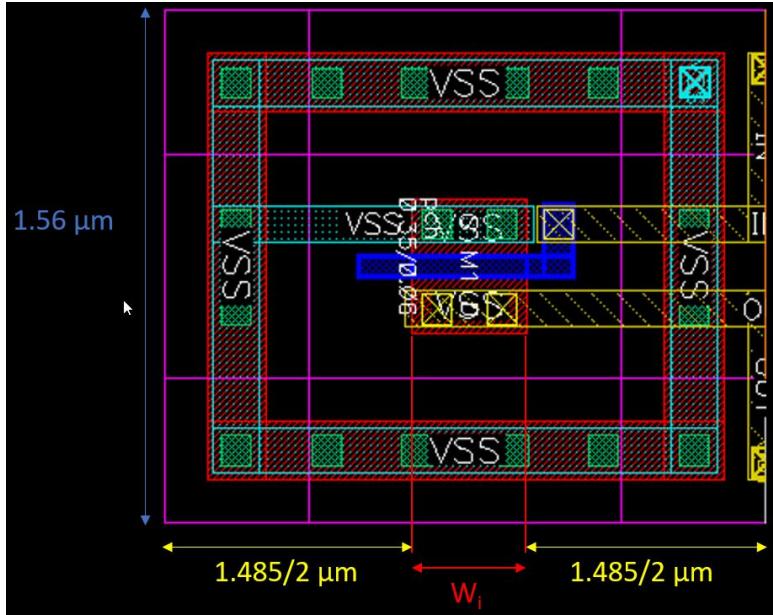


Figure 38: Dimensions of a basic transistor cell.

Because the transistors all have a fixed length of 60nm, the area taken up by any given transistor is only dependent on its width. More specifically, the area of a given transistor cell is defined as the following:

$$A_{ci} = W_{ci}L_{ci}$$

$$A_{ci} = (1.485 + W_i)(1.56)\mu m^2$$

Where A_{ci} , W_{ci} , and L_{ci} denote the area, width, and length of transistor cell i . Given this, the overall area taken up by transistor is simply the summation of the area from each transistor in the design. Given that there are 64 transistors in the overall design, the total area taken up by transistors (A_{Mtot}) is equal to the following:

$$A_{Mtot} = \sum_{i=1}^{64} W_{ci}L_{ci}$$

$$A_{Mtot} = \sum_{i=1}^{64} (1.485 + W_i)(1.56)\mu m^2$$

$$A_{Mtot} = \sum_{i=1}^{64} (64)(1.485)(1.56) + \sum_{i=1}^{64} (1.485 + W_i)(1.56) \mu m^2$$

The following table shows the width of each transistor in the design, and subsequently, the computation of A_{Mtot} :

Table 8: Computation of the total area taken up by transistors.

Transistor(s)	$W_i (\mu m^2)$
PGA/OpAmp/M1	8.4
PGA/OpAmp/M2	8.4
PGA/OpAmp/M3	1.4
PGA/OpAmp/M4	1.4
PGA/OpAmp/M5	7
PGA/OpAmp/M6	10.5
PGA/OpAmp/M7	4.2
PGA/OpAmp/M8	0.7
PGA/Z1/S<1:2>	2.8
PGA/Z1/Programmable C1/S<1:8>	11.2
PGA/Z1/Programmable C1/I<1:2>	1.4
PGA/Z2/S<1:4>	5.6
MUX/S<1:5>	7
MUX/I<1:2>	1.4
ADC/I<1:8>	5.6
ADC/S<1:17>	23.8
ADC/OpAmp (same as that from the pga)	42

$\sum(1.485)(1.56) = (64)(1.485)(1.56)$	148.2624
$\sum 1.56Wi$	142.8
Total area (μm^2)	291.0624

Capacitor Area Estimation

For the following discussion, it is assumed that C_{ox} has a value of $21.5 \text{ fF}/\mu m^2$; this value was derived from an interpolation polynomial composed of the C_{ox} values in table 5 of the textbook. Given this, the area of one 5fF capacitor is the following:

$$C_1 = C_{ox}A$$

$$A = \frac{C_1}{C_{ox}}$$

$$A = \frac{5f}{21.5 \frac{f}{\mu m^2}}$$

$$A = 0.23 \mu m^2$$

Therefore, for any given capacitor with capacitance C , the area taken up by such is equal to the following:

$$A = 0.23 \frac{C}{5f} \mu m^2$$

Subsequently, following table shows the computation of the total area taken up by capacitors in the design:

Table 9: Computation of the total area taken up by capacitors.

Capacitors	Number of 5fF capacitors needed for equivalence:
PGA/C1: 250f	50
PGA/OpAmp: 10f	2
PGA/Z1/Programmable C1/C1: 610f	122
PGA/Z1/Programmable C1/C2: 1295f	259
PGA/Z1/Programmable C1/C3: 1825f	364

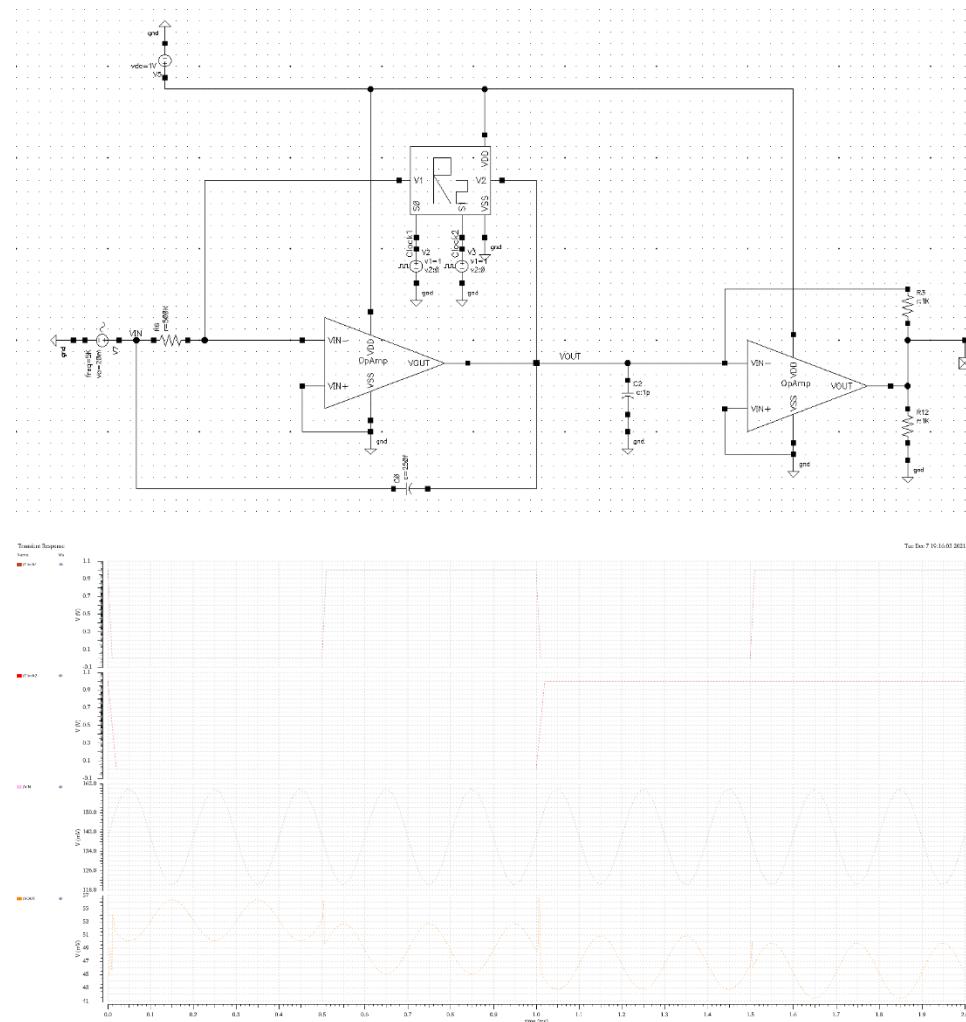
PGA/Z1/Programmable C1/C4: 2515f	503
PGA/Z2/C1: 500f	100
PGA/Z2/C2: 500f	100
ADC/C1: 50f	10
ADC/C2: 50f	10
ADC/C3: 100f	20
ADC/C4: 200f	40
ADC/C5: 400f	80
ADC/C6: 800f	160
ADC/C7: 1.6p	320
Total Number of 5f capacitor needed for equivalents:	2140
Area ($0.23\sum C_i (\mu m^2)$):	492.2

Therefore, the total area of the design, which includes that taken up by transistors and capacitors, is $783.26 \mu m^2$. Moreover, the final design does not contain any off board elements such as large capacitors or resistors.

Design Challenges

Opamp

Given that in the capacitive reset circuit, the switch capacitors have equivalent resistances on the order of $100k\text{-}M$ (I.e. $1\text{us}/500\text{fF} = 2\text{M}$),



Observations

Through completing this design project, many important lessons have been learned. Perhaps the most important, is that PCB design is not a simple matter and that special techniques need to be used throughout the design process. To contextualize, changing one design variable in an attempt to change a behavioral aspect of the circuit (e.g., open loop gain of an opamp) often introduces unwanted changes to another aspect (e.g. DC operating point of an opamp). Moreover, the results of making changes to certain design parameters often has unknown effects without rigorous computation and/or simulation. For instance, increasing the length of transistor 6 decreases the transconductance of transistor 7, but increases the drain source resistance of transistor 6 and 7. As such, increasing this length has opposite effects on 2 variables that open loop gain is proportional to. From a mathematical perspective, the results of increasing this parameter may be unclear without a lengthy derivation, and it is often easier to make the change and to simulate the circuit to learn what the true effects are (i.e., making use of special design techniques).

Although the opamp that was implemented works well in ideal conditions, is compact, relatively inexpensive, and does not draw much power, its main shortcoming is its small open loop gain of 20V/V. As was discussed, the lack of gain makes the overall design unreliable in less-than-ideal conditions. Several attempts were made to increase this gain, however, in doing so the opamp's operating point in the closed loop setting would change to undesirable values (i.e., negative voltage values). As outlined in chapter 5, the analysis of closed loop gain can be complicated. However, the use of calculations in the S domain could have allowed for the design of a high gain circuit with a desirable operating point.

Appendix

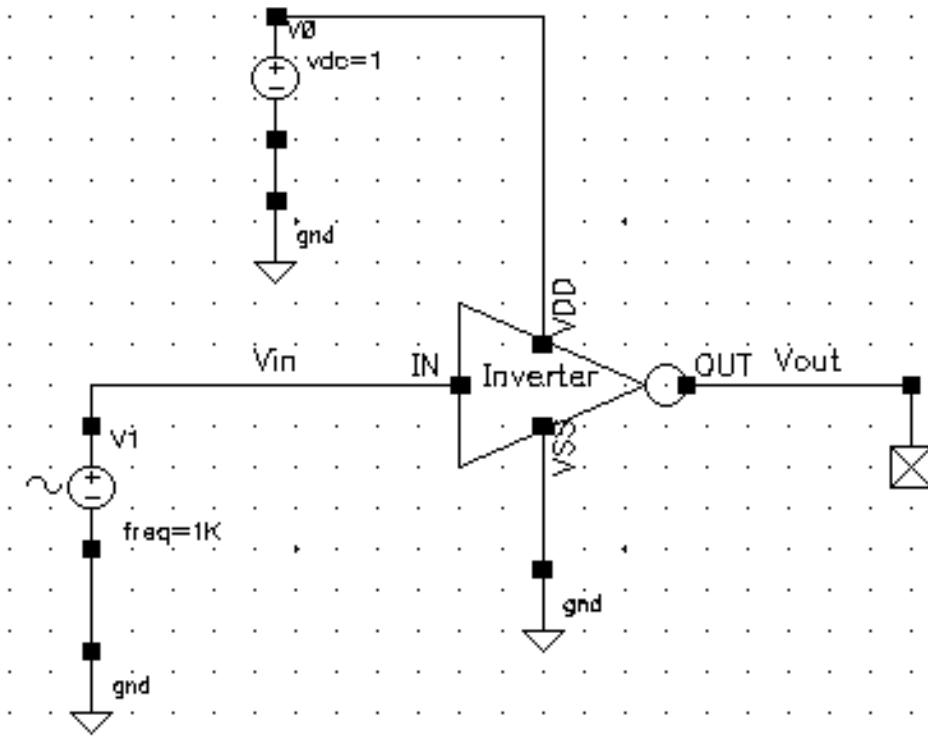


Figure 39: Inverter test bench.

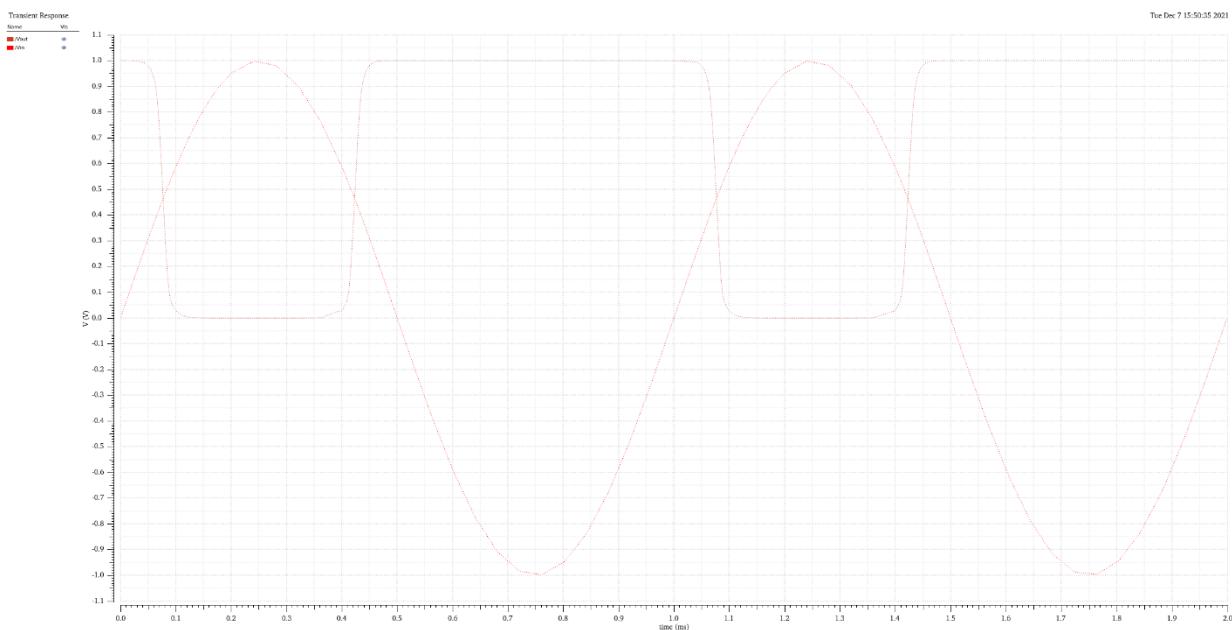


Figure 40: Inverter simulation.

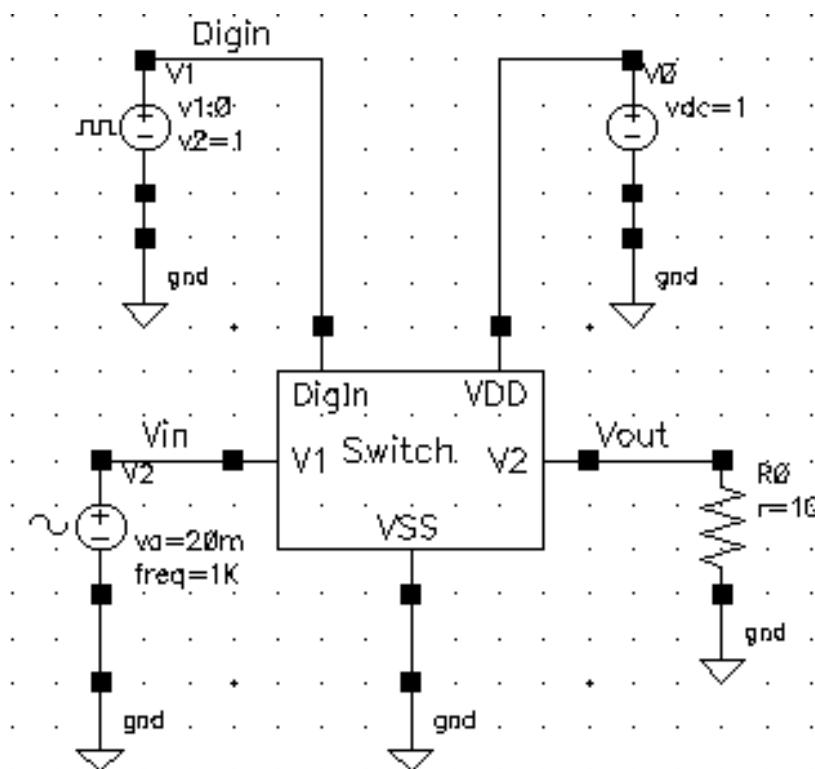


Figure 41: Switch test bench.

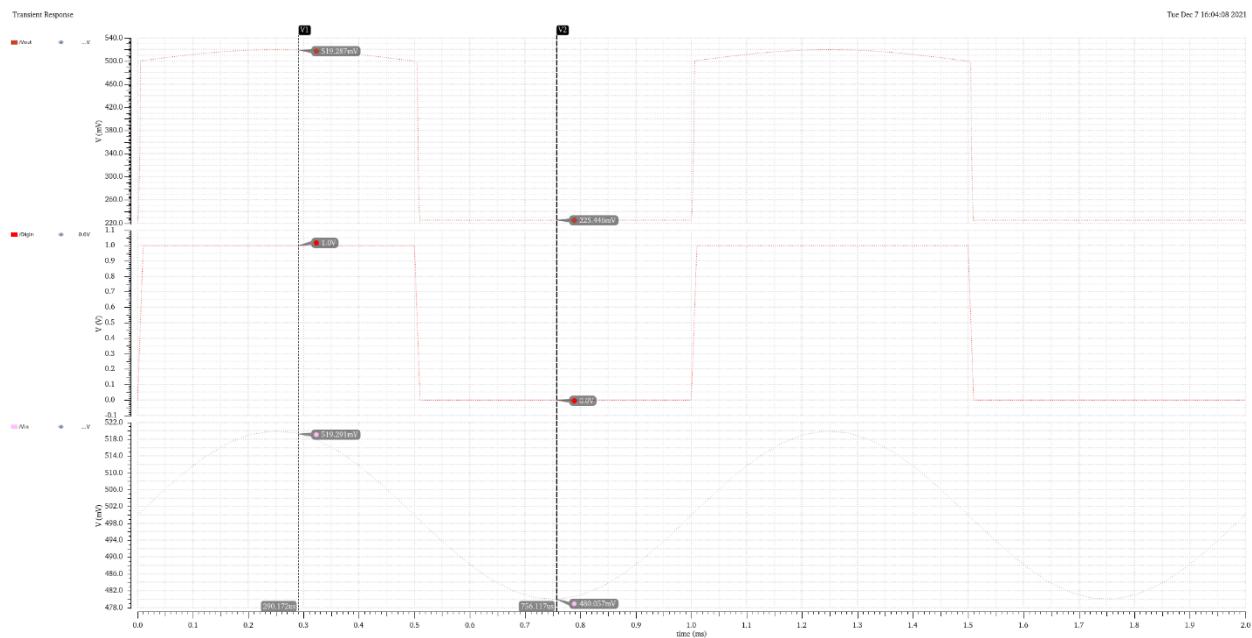


Figure 42: Switch simulation.

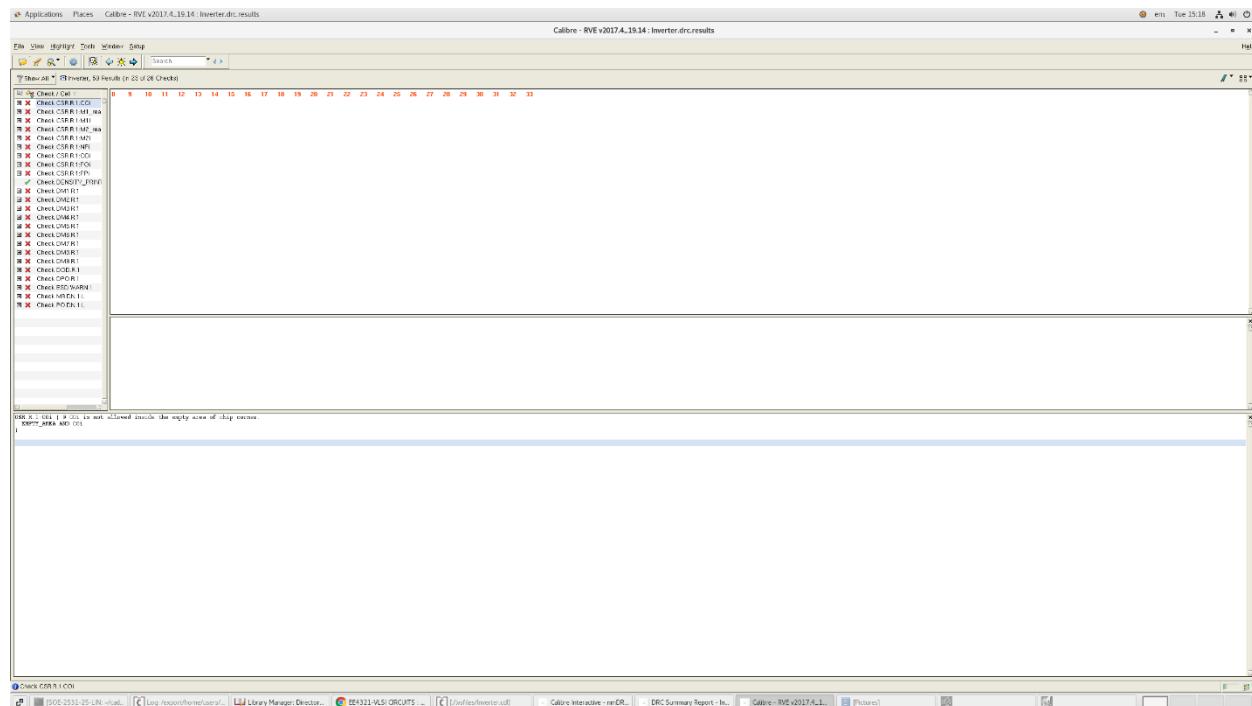


Figure 43: Inverter layout DRC.

```

// VerilogA for FinalProject, SAR, verilogA

`include "constants.vams"
`include "disciplines.vams"

module SAR(vdd,vref,clk,in,pgaRdy,b, s1,s2,s3,out,rdy);

//rising and falling times
parameter real td = 0;
parameter real tt = 0;

input vdd,vref,clk,in,pgaRdy;
output s1,s2,s3,rdy;
output [0:5] b;
output [0:5] out;
voltage vdd,vref,clk,in,pgaRdy;
voltage s1,s2,s3,rdy;
voltage [0:5] b;
voltage [0:5] out;

integer btemp [0:5];
integer outtemp [0:5];
integer s1temp,s2temp,s3temp,rdytemp;

real fullscale , supply;
integer i,j,sample;
genvar k;
analog begin
    fullscale = V(vref); //get voltage from vref pin
    supply = V(vdd); //get supply voltage from vdd
    @(initial_step) begin
        sample = supply;
        i=15;
        for (k=0;k<6;k=k+1) begin
            btemp[k] = 1;
            outtemp[k] = 0;
        end
        s1temp=0;
        s2temp=1;
        s3temp=1;
    end
    @(cross(V(pgaRdy) - V(vdd) / 2, +1)) begin //wait for rising edge of pga ready clock, this ensures we
sample only when pga output is valid
        if(>11) begin
            i=0;
            sample = supply;
        end
    end
    @(cross(V(clk) - V(vdd) / 2, +1)) begin //wait for rising edge of clock
        i = i+1;
    end
end
if (i==0) begin //sample
    for (k=0;k<6;k=k+1) begin
        btemp[k] = 1;
        outtemp[k] = 0;
    end
    s1temp=0;

```

1

Figure 44 - SAR VerilogA 1

```

        s2temp=1;
        s3temp=1;
    end      else if (i==1) begin //disconnect out and Vx
        s2temp = 0;
    end else if (i==2) begin //connect the caps to gnd
        for (k=0;k<6;k=k+1) begin
            btemp[k] = 0;
        end
        s3temp=0;
    end else if (i==3) begin //connect s1 to vref
        s1temp = 1;
    end else if (i>=4 && i<=9) begin //bit cycling
        if (i!=4) begin
            btemp[i-5] = outtemp[i-5];
        end
        btemp[i-4]= 1;
        outtemp[i-4]=floor(V(in)/supply +0.5);
    end

    //update the output variables
    for (k=0;k<6;k=k+1) begin
        V(b[k]) <+ btemp[k]*supply;
        V(out[k]) <+ outtemp[k]*supply;
    end
    V(rdy) <+ i==10 ? supply:0;
    V(s1) <+ s1temp*supply;
    V(s2) <+ s2temp*supply;
    V(s3) <+ s3temp*supply;
end
endmodule

```

Figure 45 - SAR VerilogA 2