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Special Issue Paper

Statistical Analysis on the Effect of Capacitance Mismatch in a High-Resolution Successive-Approximation ADC

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This paper describes the statistical analysis of the effect of capacitance mismatch on the accuracy of a high-resolution successive-approximation analog-to-digital converter (ADC), which employs a split capacitor array to achieve high resolution. An analysis has been made for the following two types of capacitor digital-to-analog converters (DACs). One is the capacitor DAC with binary-weighted capacitor array. The other is that which uses the segmented capacitor array for the upper bits to relax the matching requirement. The analysis was verified using the Monte-Carlo simulation with capacitance mismatch. This analysis clarifies the required capacitance matching for a given ADC resolution and provides with a guideline for the optimum design.

Keywords: SAR ADC, capacitor DAC, capacitor array, capacitor mismatch

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1. Introduction

The resolution of a successive-approximation (SAR) analog-to-digital converter (ADC) that employs a capacitor digital-to-analog converter (DAC) is limited by a capacitance mismatch. The effect of the capacitance mismatch on the SAR ADC accuracy is analyzed in Ref. [1]. However, it seems to be a little complex and is based on the maximum capacitance mismatch instead of the standard deviation. The required capacitance accuracy in the worst case is analyzed in Ref. [2] for the SAR ADC using a binary-weighted capacitor array. In this analysis, it is assumed that all the unit capacitors used for the most significant bit (MSB) capacitor have the maximum error in the same direction and the rest of the unit capacitors have the maximum error in the opposite direction. This assumption seems to be too tight. The data of the capacitance mismatch, which depend on the integrated circuit (IC) fabrication process, its structure and dimensions, are usually available as a statistical data, such as standard deviation [3, 4]. Therefore, it is more practical to clarify the relationship between the standard deviation of the capacitance mismatch and the achievable ADC accuracy. In this paper, a statistical analysis has been made on the effect of capacitance mismatch on the SAR ADC accuracy.

A SAR ADC basic configuration is reviewed in Section 2 and the statistical analysis is described in Section 3. The analytical results are compared with the Monte-Carlo simulation in Section 4 and the results are summarized in Section 5.

2. SAR ADC Basic Configuration

A block diagram of the SAR ADC employing a DAC capacitor array is shown in Fig. 1. The input signal is sampled on the capacitor array and then the DAC code that produces the same voltage as the sampled input voltage is searched using the SAR control logic to complete the conversion.

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An example of the DAC capacitor array for a high-resolution SAR ADC is shown in Fig. 2(a). The capacitor array is split into the M-bit main DAC array and the L-bit sub-DAC array to keep the total capacitance in an achievable value to be integrated [2]. These two arrays are connected with an attenuation capacitor to form the N-bit ($N = M + L$) capacitor DAC. A unit capacitance (C) is used for the attenuation capacitor in order to keep good capacitance matching. For a high-resolution ADC, a poly-poly capacitor or an metal-insulator-metal (MIM) capacitor is usually used to have better capacitance matching and better linearity. The capacitance mismatch decreases as the capacitor size increases. The capacitor size is determined based on the required matching to achieve the ADC resolution. The parasitic capacitance on both side of the attenuation capacitor also causes a conversion error. Employing a poly-poly capacitor or an MIM capacitor with smaller parasitic capacitance than other types of capacitors helps reduce the conversion error although a special care must be paid for the layout. $D_{M,i}$ and $D_{S,i}$ are the digital codes for the main and sub-DACs. V_{IN} and V_R are the input and reference voltages. The input voltage is sampled on the main DAC capacitors during the sampling phase and the DAC code that produces the same voltage as the sampled one is searched using both the main and sub-DACs during the bit trial phase.

The sub-DAC side capacitance seen from node A (C_S) is given by

$$C_S = \frac{(2^L - 1)C^2}{(2^L - 1)C + C} = (1 - 2^{-L})C \tag{1}$$

When all capacitors in the sub-DAC are connected to ground, the voltage at node A (V_A) is given by

$$\sum_{i=0}^{M-1} 2^i C (V_A - D_{M,i} V_R) + C_S V_A = 0 \tag{2}$$

From (1) and (2),

$$V_A = \frac{V_R}{2^M (1 - 2^{-N})} \sum_{i=0}^{M-1} 2^i D_{M,i} \tag{3}$$

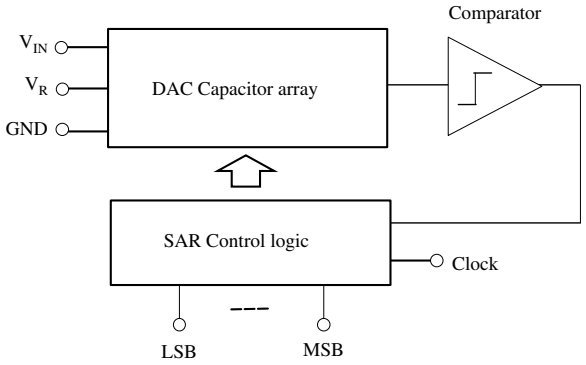

Fig. 1. Block diagram of the SAR ADC

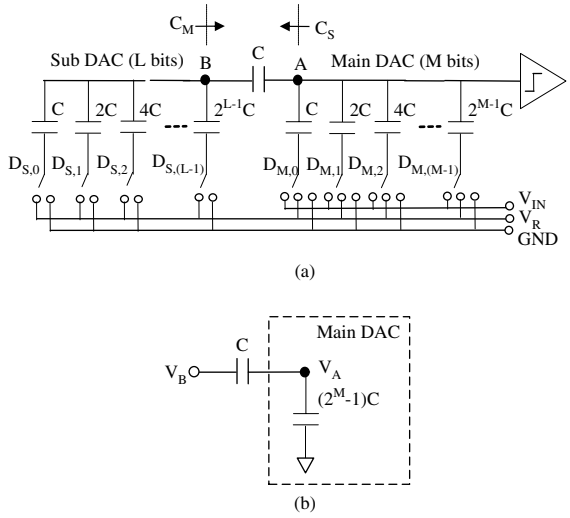

Fig. 2. DAC capacitor array. (a) DAC capacitor array and (b) voltage attenuation

Similarly, the main DAC side capacitance seen from node B (C_M) is given by

$$C_M = \frac{(2^M - 1)C^2}{(2^M - 1)C + C} = (1-2^{-M})C \tag{4}$$

When all capacitors in the main DAC are connected to the ground, the voltage at node B (V_B) is given by

$$\sum_{i=0}^{L-1} 2^i C\,(V_B - D_{S,i} V_R) + C_M V_B = 0 \tag{5}$$

From (4) and (5),

$$V_B = \frac{V_R}{2^L(1-2^{-N})} \sum_{i=0}^{L-1} 2^i D_{S,i} \tag{6}$$

Then, referring to the equivalent circuit shown in Fig. 2(b), this voltage is attenuated to V_A' at node A which is given by

$$V_A' = \frac{C}{(2^M - 1)C + C} V_B = \frac{V_B}{2^M} \tag{7}$$

Because the weight of each bit in the sub-DAC is scaled to $1/2^M$ at node A, the DAC output voltage (V_O) at node A is given by

$$V_O = \frac{V_R}{2^M(1-2^{-N})} \sum_{i=0}^{M-1} 2^i D_{M,i} + \frac{V_R}{2^M 2^L(1-2^{-N})} \sum_{i=0}^{L-1} 2^i D_{S,i}$$
$$= \frac{V_R}{2^M(1-2^{-N})} \left(\sum_{i=0}^{M-1} 2^i D_{M,i} + \frac{1}{2^L} \sum_{i=0}^{L-1} 2^i D_{S,i} \right) \tag{8}$$

The term $(1-2^{-N})$ in the denominator shows the gain error that can be calibrated in a digital domain. As the effect of the capacitance mismatch in the sub-DAC is reduced to $1/2^M$, the one in the main DAC dominates. In Section 3, the capacitance mismatch effect in the main DAC is analyzed.

3. Statistical Analysis on the Effect of Capacitance Mismatch upon the SAR ADC Accuracy

In this section, the effect of the capacitance mismatch on the ADC accuracy is analyzed for the following two cases. One is the case where the main DAC consists of a binary-weighted capacitor array. The other is the case where the segmented capacitor array is used for several upper bits of the main DAC to relax the matching requirement.

3.1. Case I: Binary-weighted capacitor array First, the capacitance mismatch effect in the main DAC shown in Fig. 3 is analyzed. This is the case where the binary-weighted capacitor array is used. For simplicity, it is assumed that all sub-DAC capacitors are connected to the ground and the initial charge is zero. The maximum error occurs during the code transition from '011…1' to '100…0' at the midpoint where the number of capacitors that change their state is maximal as shown in Fig. 3(a). To meet the ADC accuracy, this error must be smaller than a half least significant bit (LSB) ($V_R/2^{(N+1)}$). The capacitor arrangement for this code transition is shown in Fig. 3(b) and (c).

V_X is the voltage at node A before the code transition and V_X' is that after the transition. Before the code transition, the MSB capacitor in the main DAC and all capacitors in the sub-DAC are connected to the ground, and all other capacitors are connected to the reference as shown in Fig. 3(b). Using (1), V_X is given by

$$V_X \approx \frac{(2^{M-1} - 1)C}{2^M(1-2^{-N})C} V_R \approx \frac{(2^{M-1} - 1)C}{2^M C} V_R \tag{9}$$

After the code transition, the MSB capacitor in the main DAC is connected to the reference, and all other capacitors are connected to the ground as shown in the figure. Due to the code transition, the charge on node A is redistributed to each capacitor and the resulting voltage (V_X') at node A is given by

$$V_X' = \frac{2^{M-1}C}{2^M C} V_R \tag{10}$$

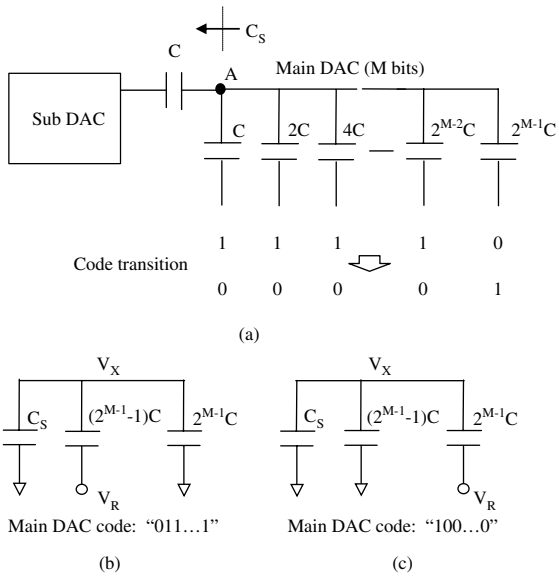

Fig. 3. Binary-weighted capacitor array. (a) Code transition, (b) before the code transition and (c) after the code transition

In an ideal case, $(V_X' - V_X)$ is equal to one LSB ($V_R/2^M$) of the M-bit main DAC as shown below:

$$(V_X' - V_X)_{\text{IDEAL}} = \frac{2^{M-1}C_U - (2^{M-1}-1)C_U}{2^M C_U} V_R = \frac{V_R}{2^M} \quad (11)$$

However, the mismatch in the capacitor array causes an error. It is assumed that a unit capacitor (C) is given by

$$C = C_U + \Delta C_U \quad (12)$$

where C_U is the average unit capacitance, and ΔC_U is the standard deviation. Each capacitor in the array consists of unit capacitors connected in parallel. When the number of unit capacitor connected in parallel is N_C, the average of the total capacitance is $N_C C_U$, whereas the standard deviation is $\sqrt{N_C}\Delta C_U$, assuming that they are not correlated. From (9), (10) and (12), the standard deviation of $(V_X' - V_X)$ with capacitance mismatch is given by

$$\begin{aligned}
&(V_X' - V_X)_{\text{STD}} \\
&= \frac{2^{M-1}C - (2^{M-1}-1)C}{2^M C} V_R \\
&= \frac{2^{M-1}C_U + \sqrt{2^{M-1}}\Delta C_U - (2^{M-1}-1)C_U - \sqrt{2^{M-1}-1}\Delta C_U}{2^M C_U + \sqrt{2^M}\Delta C_U} V_R \\
&\approx \frac{C_U + \sqrt{2^{M-1}}\Delta C_U - \sqrt{2^{M-1}-1}\Delta C_U}{2^M C_U} V_R \quad (13)
\end{aligned}$$

as $2^M C \gg \sqrt{2^M}\Delta C_U$. From (11) and (13), the standard deviation of the differential nonlinearity error voltage, $V_{\text{DNL,STD}}$, during the code transition is given by

$$\begin{aligned}
V_{\text{DNL,STD}} &= (V_X' - V_X)_{\text{STD}} - (V_X' - V_X)_{\text{IDEAL}} \\
&= \frac{\sqrt{2^{M-1}}\Delta C_U - \sqrt{2^{M-1}-1}\Delta C_U}{2^M C_U} V_R \\
&\approx \frac{\sqrt{2^M - 1}}{2^M} \frac{\Delta C_U}{C_U} V_R \quad (14)
\end{aligned}$$

since the terms in the numerator are statistical data. To achieve the ADC accuracy, α times $V_{\text{DNL,STD}}$ must be smaller than a half LSB of the N-bit ADC ($V_R/2^{N+1}$). This results in

$$\frac{\Delta C_U}{C_U} < \frac{1}{\alpha 2^{(N+1-M)}\sqrt{2^M - 1}} \quad (15)$$

As a practical value, $\alpha = 3.3$ is often used [5]. When the ADC resolution is 14 bits (N = 14) and the main DAC resolution is 7 bits (M = 7), the standard deviation of the capacitance mismatch must be smaller than 0.011% with $\alpha = 3.3$.

The relationship between the standard deviation of the acceptable capacitance mismatch and the main DAC resolution (M) is shown in Fig. 4, for the ADC resolution of 14 bits ($N = 14$). Accordingly, the sub-sub DAC has $L(=14-M)$ bits. This graph is based on (15). The total capacitance including the main and sub-sub DACs is $(2^M - 1)C + 2^{14-M}C$ in the case where the binary-weighted capacitor array is used in both main and sub-sub DACs. The total capacitance normalized by the unit capacitance is also shown in Fig. 4. The main DAC capacitance dominates with large M, whereas the sub-sub DAC capacitance dominates with small M. As can be seen in the figure, the acceptable mismatch increases with M and becomes maximal with $M = 14$. As the practical unit capacitance is often around 100 fF; however, the total capacitance becomes 1600 pF with $M = 14$. This capacitance is too large to be integrated. There is a trade-off between the required accuracy and the total capacitance. When the main DAC resolution is reduced to 7 bits ($M = 7$), the total capacitance is reduced to about 26 pF, which is a practical value to be integrated at the expense of tighter matching requirement.

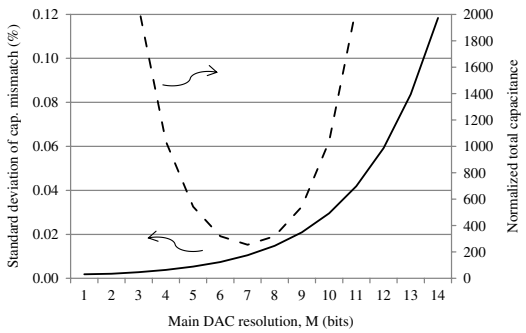

Fig. 4. Required capacitance matching and the total capacitance normalized by the unit capacitance versus the main DAC resolution ($N = 14, \alpha = 3.3$)

Since sometimes the required accuracy of the MSB capacitance (C_{MSB}) is argued, it would be worthwhile to show how it is related to the mismatch in a unit capacitance. The percentage of the mismatch of this capacitance is much smaller than that of the unit capacitance as shown below because it consists of 2^{M-1} unit capacitors connected in parallel.

$$C_{\text{MSB}} = 2^{M-1}C = C_{\text{MSBO}} + \Delta C_{\text{MSB}} \quad (16)$$

$$C_{\text{MSBO}} = 2^{M-1}C_U, \Delta C_{\text{MSB}} = \sqrt{2^{M-1}}\Delta C_U \quad (17)$$

$$\frac{\Delta C_{\text{MSB}}}{C_{\text{MSBO}}} = \frac{\sqrt{2^{M-1}}\Delta C_U}{2^{M-1}C_U} = \frac{1}{\sqrt{2^{M-1}}} \frac{\Delta C_U}{C_U} \quad (18)$$

In the case of $M = 7$, the mismatch of the MSB capacitance is eight times smaller than that of the unit capacitance. Although this requirement seems to be very tight, it is equivalent to the requirement given by (15) as shown here.

Next, the integral nonlinearity (INL) is analyzed. The INL is defined as a departure from the line that goes through two end points where the codes are all 0s and all 1s. Although the capacitance mismatch is accumulated, the voltage at node A is equal to $(1-2^{-M})V_R$ when the code is all 1 because all capacitors are connected to the reference. This results in the ideal voltage of $V_R/2$ at the midpoint. The INL becomes maximal at the midpoint due to the accumulation of the capacitance mismatch. Referring to (10), the standard deviation of the INL error voltage, $V_{\text{INL,STD}}$, is given by

$$\begin{aligned}
V_{\text{INL,STD}} &= \left(\frac{2^{M-1}C}{2^M C} - \frac{1}{2}\right) V_R \\
&\approx \left(\frac{2^{M-1}C_U + \sqrt{2^{M-1}}\Delta C_U}{2^M C_U} - \frac{1}{2}\right) V_R \approx \frac{\sqrt{2^{M-1}}}{2^M} \frac{\Delta C_U}{C_U} V_R
\end{aligned} \quad (19)$$

In comparison with (14), the INL is about $\sqrt{2}$ times smaller than the differential nonlinearity (DNL) in this case. Even with the segmented capacitor array or the mixture of the segmented and binary-weighted capacitor arrays which is described later, the INL becomes maximal at the midpoint because the departure from the ideal line due to the accumulation of the mismatch becomes maximal at that point. Therefore, the INL in these cases is also given by (19). The DNL is usually required to be less than a half LSB and at least one LSB to avoid a missing code. In contrast, the INL requirement could be less critical than the DNL depending on the application. To keep the INL error small, the focus must also be on the layout to reduce the effect of oxide thickness gradient [2]. The DNL for the other type of capacitor array is analyzed in the following section.

3.2. Case II: Segmented capacitor array for upper bits The required capacitance mismatch can be relaxed using

a segmented capacitor array as shown in Fig. 5(a) as the number of capacitors to be switched at the same time is reduced. In this case, the segmented capacitor array is used for the upper 5 bits and the binary-weighted capacitor array is used for the lower 2 bits. In this configuration, the maximum error occurs during the code transition from '00...0011' to '00...0100' because the number of capacitors that change their state is maximal during this transition. The capacitor array before and after the code transition is shown in Fig. 5(b) and (c).

In Fig. 5(b), 2 binary-weighted capacitors are connected to the reference and all other capacitors are connected to the ground. In Fig. 5(c), one of the 31 segmented capacitors are connected to the reference, and all other capacitors are connected to the ground.

Similar to the previous case, the voltages at node A (V_X) before the code transition and after the transition (V_X') are given by

$$V_X = \frac{3C}{2^7 C} V_{\mathrm{R}} \tag{20}$$

$$V_X' = \frac{4C}{2^7 C} V_{\mathrm{R}} \tag{21}$$

Then, the standard deviation of the differential nonlinearity error voltage, $V_{\mathrm{DNL,STD}}$, due to capacitance mismatch is given by

$$\begin{aligned} V_{\mathrm{DNL,STD}} &= (V_X' - V_X)_{\mathrm{STD}} - (V_X' - V_X)_{\mathrm{IDEAL}} \\ &\approx \frac{\sqrt{4}\Delta C_{\mathrm{U}} - \sqrt{3}\Delta C_{\mathrm{U}}}{2^7 C_{\mathrm{U}}} V_{\mathrm{R}} \\ &\approx \frac{\sqrt{7}}{2^7} \frac{\Delta C_{\mathrm{U}}}{C_{\mathrm{U}}} V_{\mathrm{R}} \end{aligned} \tag{22}$$

To achieve the ADC accuracy, α times $V_{\mathrm{DNL,STD}}$ must be smaller than a half LSB ($V_{\mathrm{R}}/2^{14+1}$). With $\alpha = 3.3$, this results in

$$\frac{\Delta C_{\mathrm{U}}}{C_{\mathrm{U}}} < \frac{1}{3.3 \times 2^8 \sqrt{7}} = 0.045\% \tag{23}$$

The required standard deviation of the capacitance mismatch is 0.045%. Compared to the binary-weighted capacitor array case, the required matching is 4.1 times relaxed. However, a segmented capacitor array requires much more digital control signals than a binary-weighted one, although the total capacitance is the same. For example, a 7-bit segmented capacitor array requires 127 ($=2^7 - 1$) control signals, whereas a 7-bit binary-weighted array

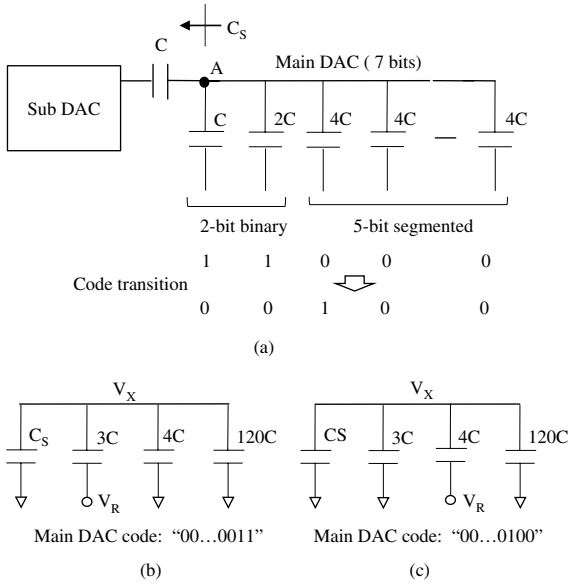

Fig. 5. Binary-weighted and segment capacitor array. (a) Code transition, (b) before the code transition and (c) after the code transition

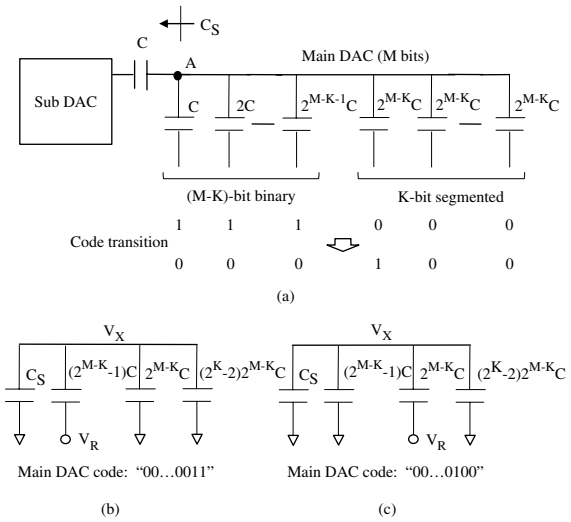

Fig. 6. More general case: binary-weighted and segmented capacitor array. (a) Code transition, (b) before the code transition and (c) after the code transition

requires only 7. Therefore, the combination of these capacitor arrays is usually used to reduce the number of control signals based on the trade-offs between the required capacitance matching and the complexity of signal routing in the IC layout. In the case in Fig. 5(a), the number of the required control signals is 33 ($=2 + 2^5 - 1$).

A more generalized case of the capacitor array in Fig. 5(a) is shown in Fig. 6(a). Here, the upper K bits consist of a segmented capacitor array, whereas the lower $(M - K)$ bits consist of a binary-weighted capacitor array. In this configuration, the maximum error occurs during the code transition where the binary capacitor array changes its state from all 1s to all 0s because the number of capacitors that change the state is maximal. The capacitor array before and after the code transition is shown in Fig. 6(b) and (c). Similar to the previous case, the voltage at node A (V_X) before the code transition, the one after the transition (V_X') and the standard deviation of the INL error voltage are given by

$$V_X = \frac{(2^{M-K} - 1)C}{2^M C} V_{\mathrm{R}} \tag{24}$$

$$V_X' = \frac{2^{M-K} C}{2^M C} V_{\mathrm{R}} \tag{25}$$

$$\begin{aligned} V_{\mathrm{DNL,STD}} &= (V_X' - V_X)_{\mathrm{STD}} - (V_X' - V_X)_{\mathrm{IDEAL}} \\ &\approx \frac{\sqrt{2^{M-K}}\Delta C_{\mathrm{U}} - \sqrt{2^{M-K} - 1}\Delta C_{\mathrm{U}}}{2^M C_{\mathrm{U}}} V_{\mathrm{R}} \\ &\approx \frac{\sqrt{2^{M-K+1} - 1}}{2^M} \frac{\Delta C_{\mathrm{U}}}{C_{\mathrm{U}}} V_{\mathrm{R}} \end{aligned} \tag{26}$$

Since α times $V_{\mathrm{DNL,STD}}$ must be smaller than a half LSB ($V_{\mathrm{R}}/2^{N+1}$),

$$\frac{\Delta C_{\mathrm{U}}}{C_{\mathrm{U}}} < \frac{1}{\alpha 2^{N-M+1}\sqrt{2^{M-K+1} - 1}} \tag{27}$$

This is a more generalized expression of the case in Fig. 5. When $N = 14, M = 7$ and $K = 5$, the standard deviation of the capacitance mismatch must be smaller than 0.045%. This is the same result as with the case shown in Fig. 5 as expected because the condition is the same.

4. Simulation Results

To verify the analysis of the capacitance mismatch effect on the SAR ADC accuracy, the analyzed value was compared with the

Monte-Carlo simulation results. In simulation it was assumed that the unit capacitance has a Gaussian distribution and 1000 trials were carried out. The results for the binary-weighted capacitor array in Fig. 3 are shown in Fig. 7. This shows the relationship between the required capacitance matching and the main DAC resolution for each ADC resolution. The solid lines show the value calculated using (15) and the dots show the values obtained from the Monte-Carlo simulation. The simulation results agree with the analytical results fairly well. As the main DAC resolution increases, the required capacitance accuracy is relaxed at the expense of increased total capacitance. When the ADC resolution is 14 bits and the main DAC resolution is 7 bits, the acceptable capacitance mismatch is 0.011% with $\alpha = 3.3$.

The simulation results for the case where the main DAC resolution is 7 bits and the segmented capacitor array was used for the upper K bits are shown in Fig. 8. The solid line shows the value calculated using (27) and the dots show the value obtained from Monte-Carlo simulation. Simulation results agree with the analyzed value as shown in the figure. As the number of segmented capacitors increases, the required capacitance matching is relaxed because the number of capacitors whose states change reduces. As mentioned in the previous section, this results in increased control signals. Therefore, the optimum segmented capacitor array needs to be determined based on this trade-off. In the case where the ADC resolution is 14 bits, the main DAC resolution is 7 bits and the upper 5 bits are segmented, the standard deviation of the acceptable capacitance mismatch is 0.045% with $\alpha = 3.3$.

The discussion so far is for the single-ended case. In the case of the differential configuration with two sets of capacitor arrays, the capacitance matching requirement is $\sqrt{2}$ times relaxed because the signal amplitude becomes twice while the voltage error due to capacitance mismatch increases $\sqrt{2}$ times.

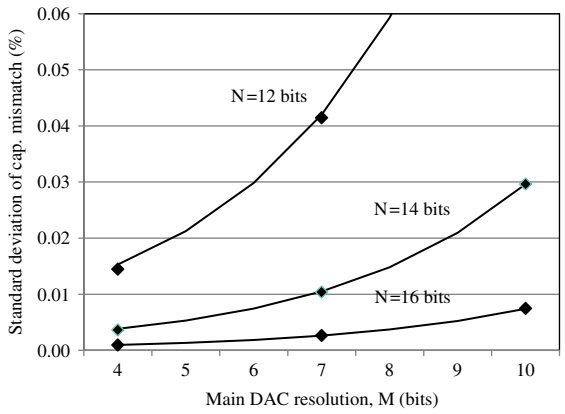

Fig. 7. Required capacitance matching versus the main DAC resolution ($\alpha = 3.3$)

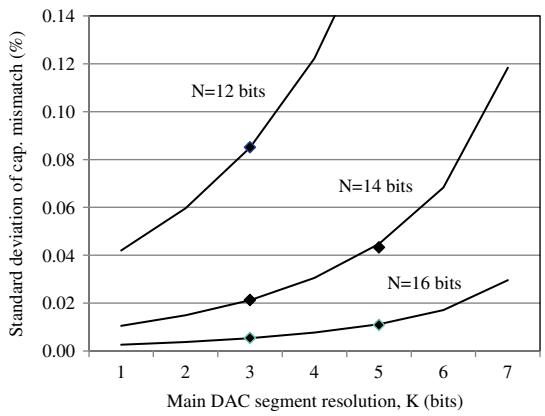

Fig. 8. Required capacitance matching versus the main DAC resolution ($M = 7, \alpha = 3.3$)

5. Conclusions

The required capacitance matching to achieve a high-resolution SAR ADC was analyzed. Statistical analysis was made for the internal DACs with the binary-weighted capacitor array and a mixture of the segmented and binary-weighted capacitor arrays. The latter case relaxes the capacitance matching requirement for the DNL at the expense of the increased complexity of signal routing in the layout. The analytical results were verified by comparing with the Monte-Carlo simulation results, and provide with a clear trade-off between the standard deviation of the capacitance mismatch and an achievable ADC resolution.

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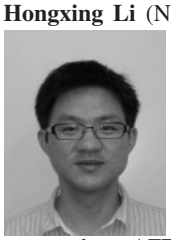

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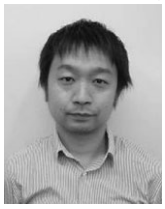

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