

02-22-2016

* Re-label L1 & L2 from 2.5A to 7A

03-09-2016 (Rev 2C)

* Add pin 17 (GND) to PTN5110

03-12-2016

- * Replace Q6, Q7, Q8, Q9, Q12, Q13, Q14, Q14 with correct part
- * Replace J5 with correct part number from Mouser
- * Replace D20, D22, D23, D25, D26 with low reverse current version

03-13-2016

- * Rename signal DC_BARREL_ON to nDC_BARREL_ON
- * Add Q22 to indicate VBAT_PRESENT

08-02-2016

- * change C107 to 1uF
- * remove U4, change pullup on R30/R31 to BYPASS * R54 is DNS, R59 is 3.6K instead of 100K
- * Added R138
- * R51 is DNS
- * C48 is 4.7uF instead of 10uF
- * U11 and its components are DNS
- * Added Q23, Q24, R139, R140
- * R123 is 30K and R125 is 3.6K instead of 100K
- * R72 and R90 are 1K instead of 100K
- * Remove Q16, D45, R98, R99, Q17, R100
- * Changed U15 (3290) to correct footprint
- * Remove footnote to control Q17
- * Changed VARIABLE_PS_LS_ENA to nVARIABLE_PS_LS_ENA

08-16-2016

* Add J23 for VBUS load or LCD connection

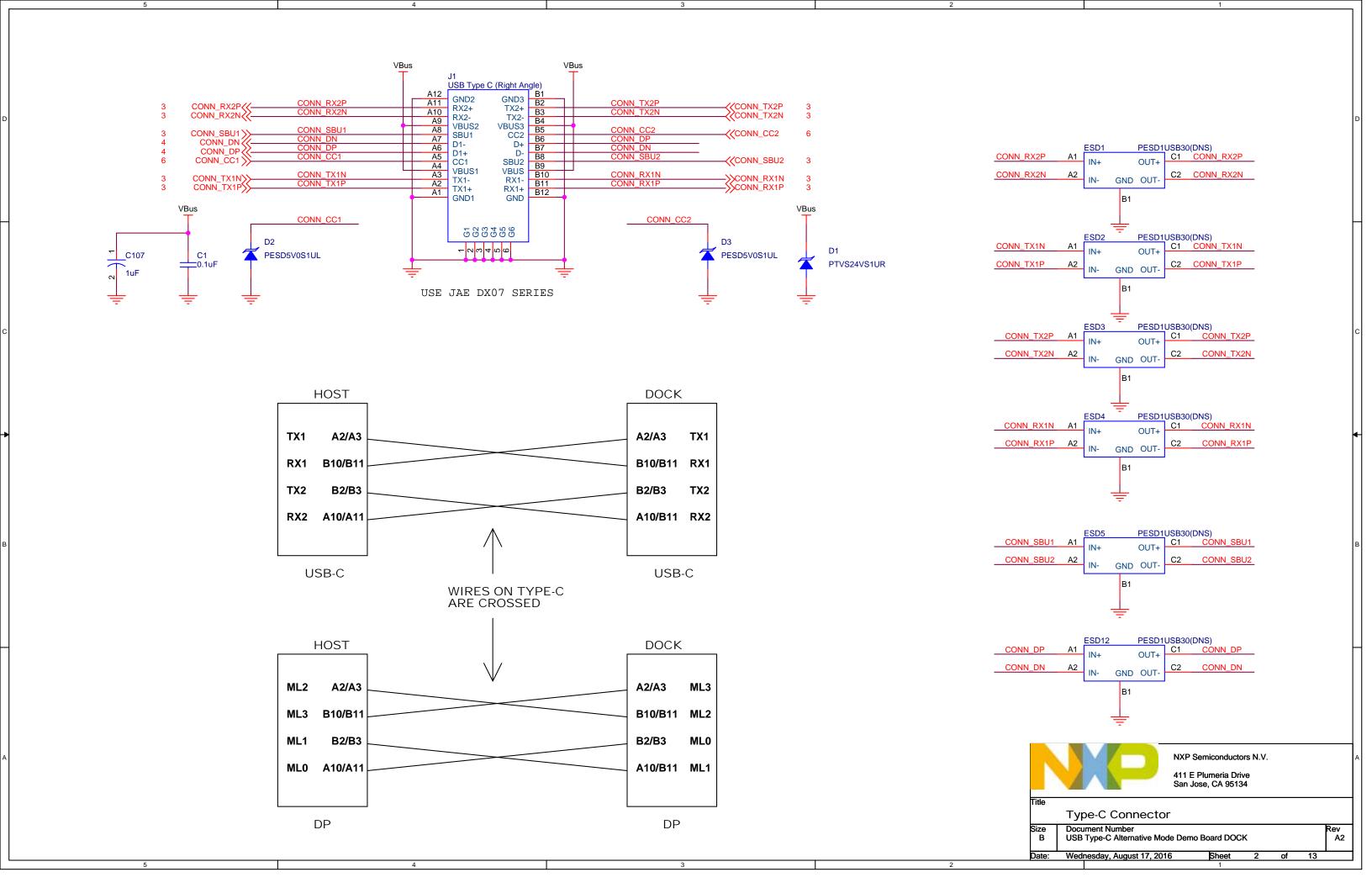
08-17-2016

* Change U7 footprint from SOT996-2 to SOT833-1

02-16-2017

* Added loading options

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4LANE_DP=1: Select DP Path 4LANE_DP=0: Select USB3 Path

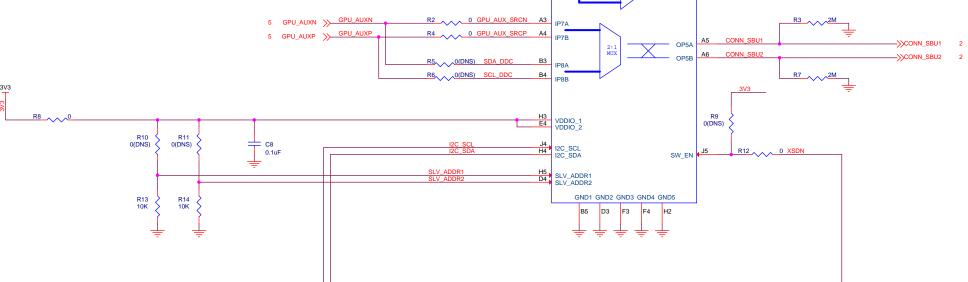
XSDN	4LANE_DP	CC_ORIENT	Function
0	X	x	All switches Hi-Z USB3 path + 2 lanes DP. Normal plug orientation
1	0	1	USB3 path + 2 lanes DP. Flipped plug orientation
1	1	0	4 lanes DP. Normal plug orientation 4 lanes DP. Flipped plug orientation

Table 3-1: USB Type-C Receptacle DFP_D Pin Assignment Summary

Receptacle Pin	Pin Assignment	A	В	С	D	E	F
Number	Cable	USB Type-C	USB Type-C	USB Type-C	USB Type-C	USB Type-C	USB Type-C
		to USB	to USB	to USB	to USB	to DP	to DP
		Type-C or	Type-C or	Type-C or	Type-C or		
		Protocol	Protocol	Protocol	Protocol		
		Converter	Converter	Converter	Converter		
	DisplayPort Signaling	GEN2_BR	GEN2_BR	DP_BR	DP_BR	DP_BR	DP_BR
A11 – A10	RX2	Open ^a / ML2	Open ^a / ML1	ML0	ML0	ML0	ML0
A2 - A3	TX1	ML1	SSTX	ML2	SSTX	ML2	SSTX
B11 – B10	RX1	Open ^a / ML3	SSRX	ML3	SSRX	ML3	SSRX
B2 - B3	TX2	ML0	ML0	ML1	ML1	ML1	ML1
A8	SBU1	AUX_CH_P	AUX_CH_P	AUX_CH_P	AUX_CH_P	AUX_CH_P	AUX_CH_P
B8	SBU2	AUX_CH_N	AUX_CH_N	AUX_CH_N	AUX_CH_N	AUX_CH_N	AUX_CH_N

a. Connections marked as optionally Open are not used when Active cables are connected.

SLV_ADDR2	SLV_ADDR1	I2C slave address
0	0	0x60/0x61
0	1	0x64/0x65
1	0	0x68/0x69
1	1	0x6C/0x6D



5 GPU_ML2_TXP >> GPU_ML2_TXP

5 GPU_ML2_TXN >> GPU_ML2_TXN

5 GPU_ML1_TXP >> GPU_ML1_TXP

5 GPU_ML1_TXN >> GPU_ML1_TXN

4 xHCI_SS_TXP >> xHCI_SS_TXP

4 xHCI_SS_TXN >> xHCI_SS_TXN

5 GPU_ML3_TXP >>> GPU_ML3_TXP

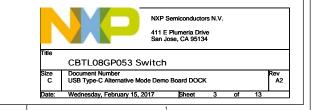
5 GPU_ML3_TXN >>> GPU_ML3_TXN

5 GPU_ML0_TXP >> GPU_ML0_TXP

5 GPU_ML0_TXN

GPU_ML0_TXN

G1

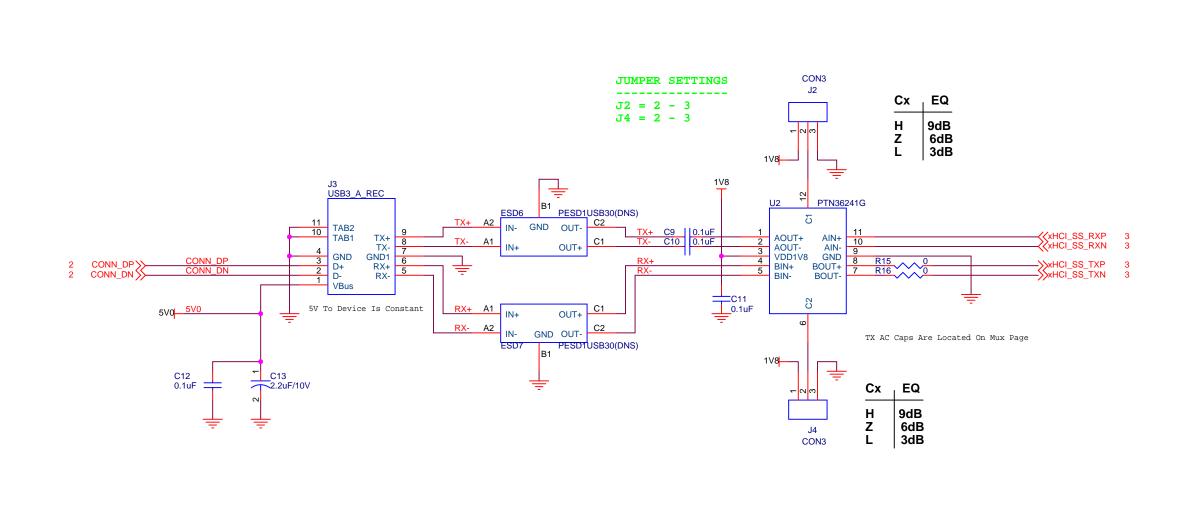


CONN_RX1P 2

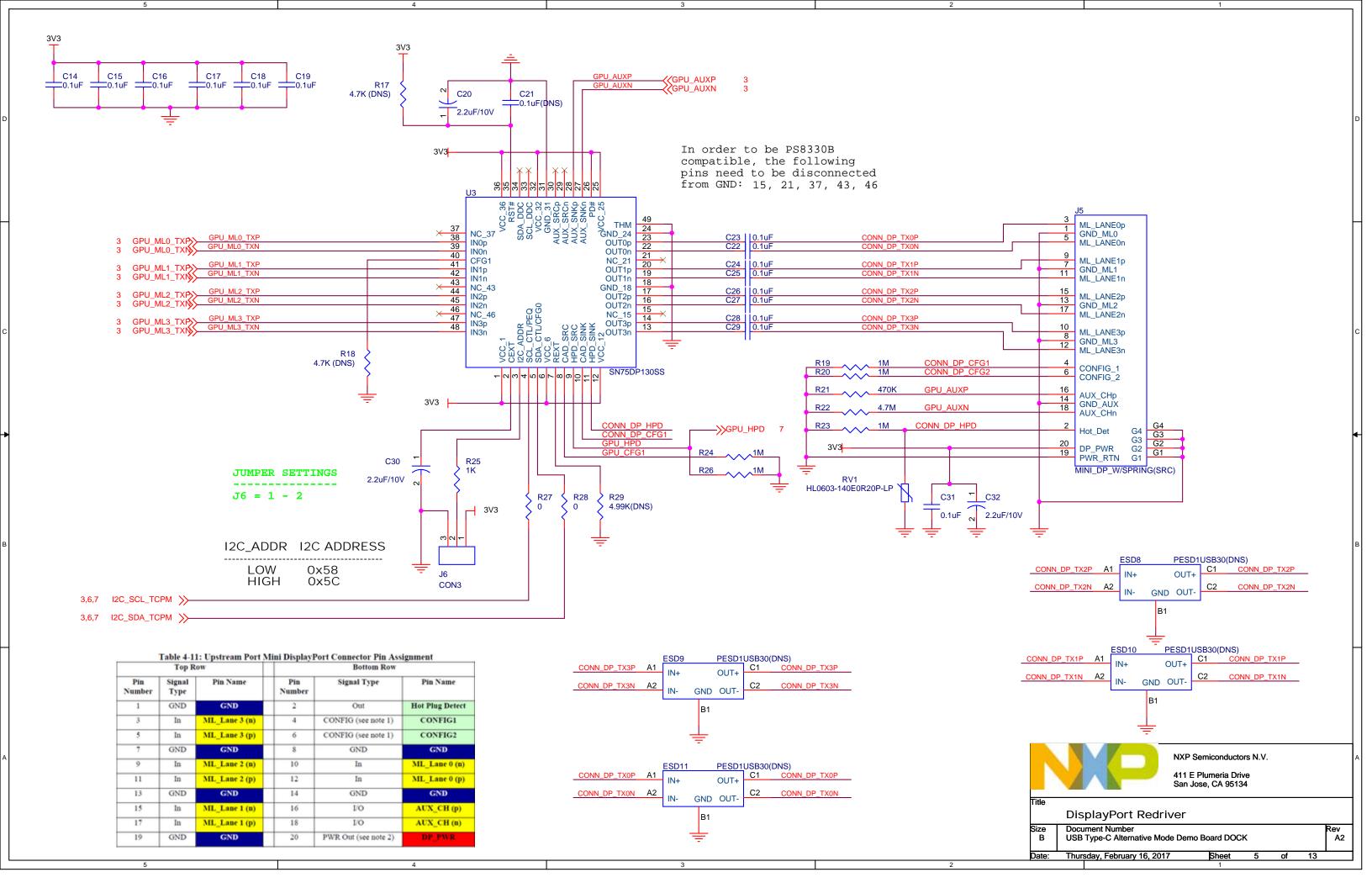
CONN_RX1N 2

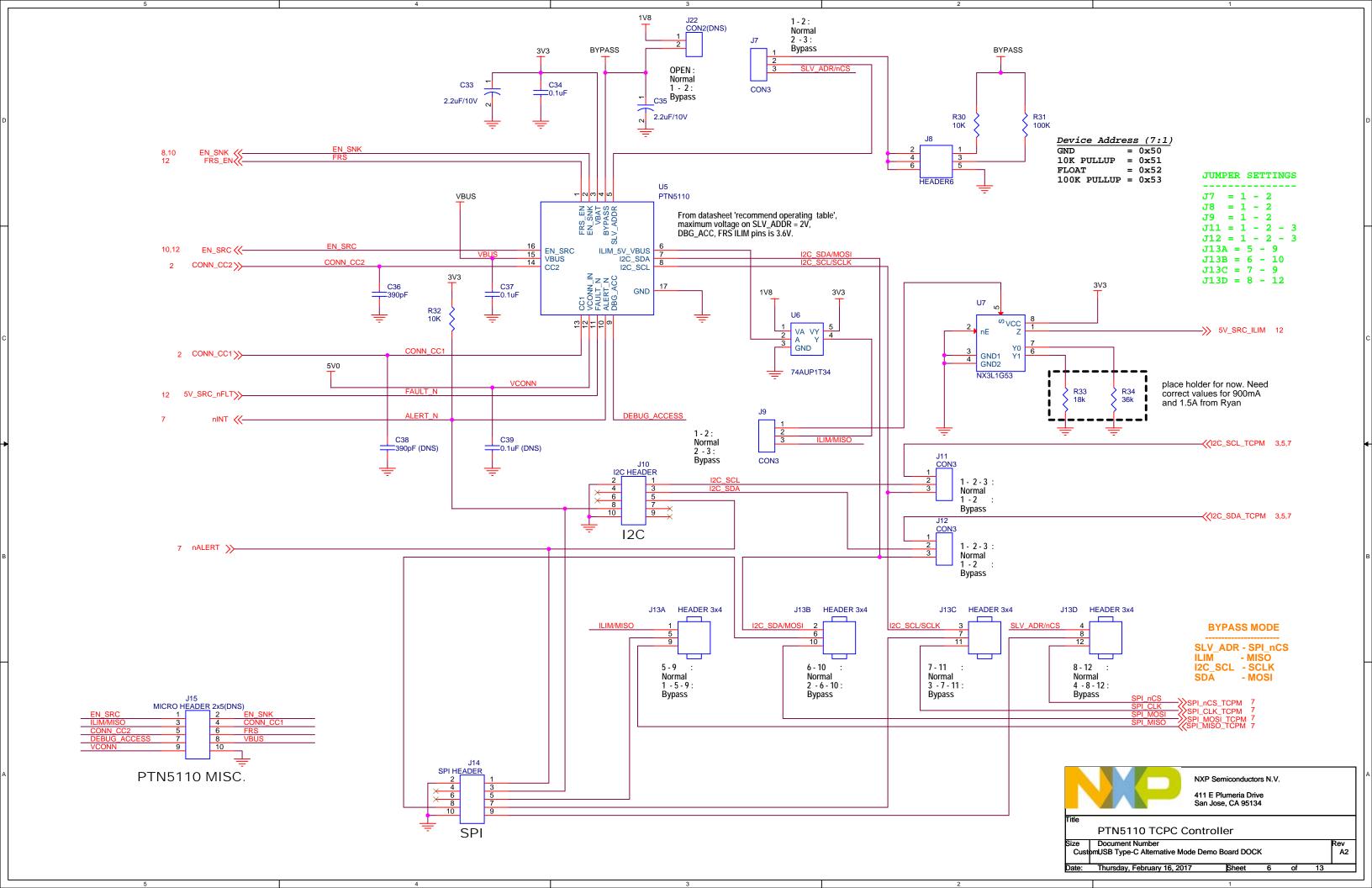
J6 CONN_RX1N

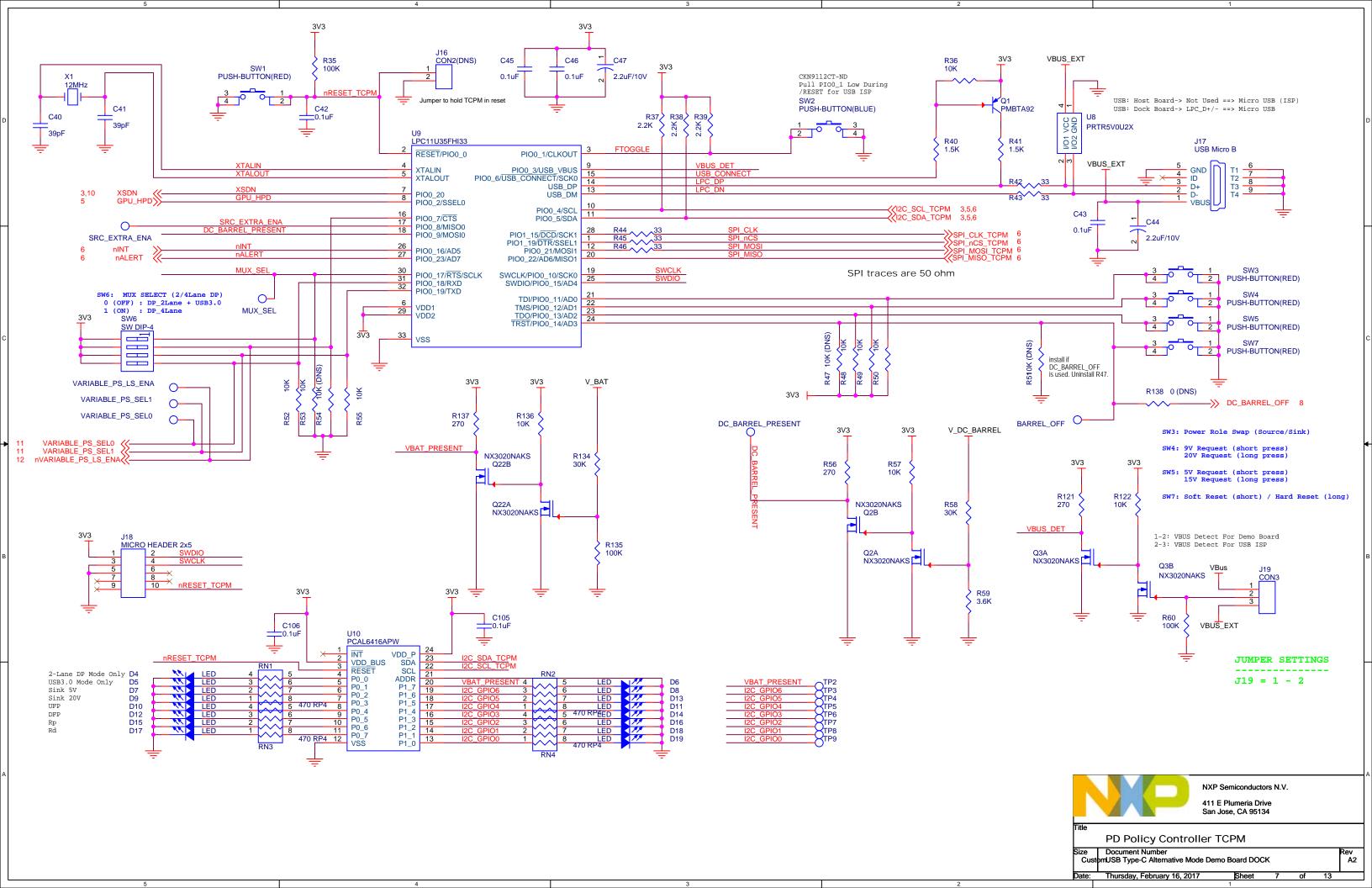
OP3+ G6 C4 0.1uF CONN_TX1P

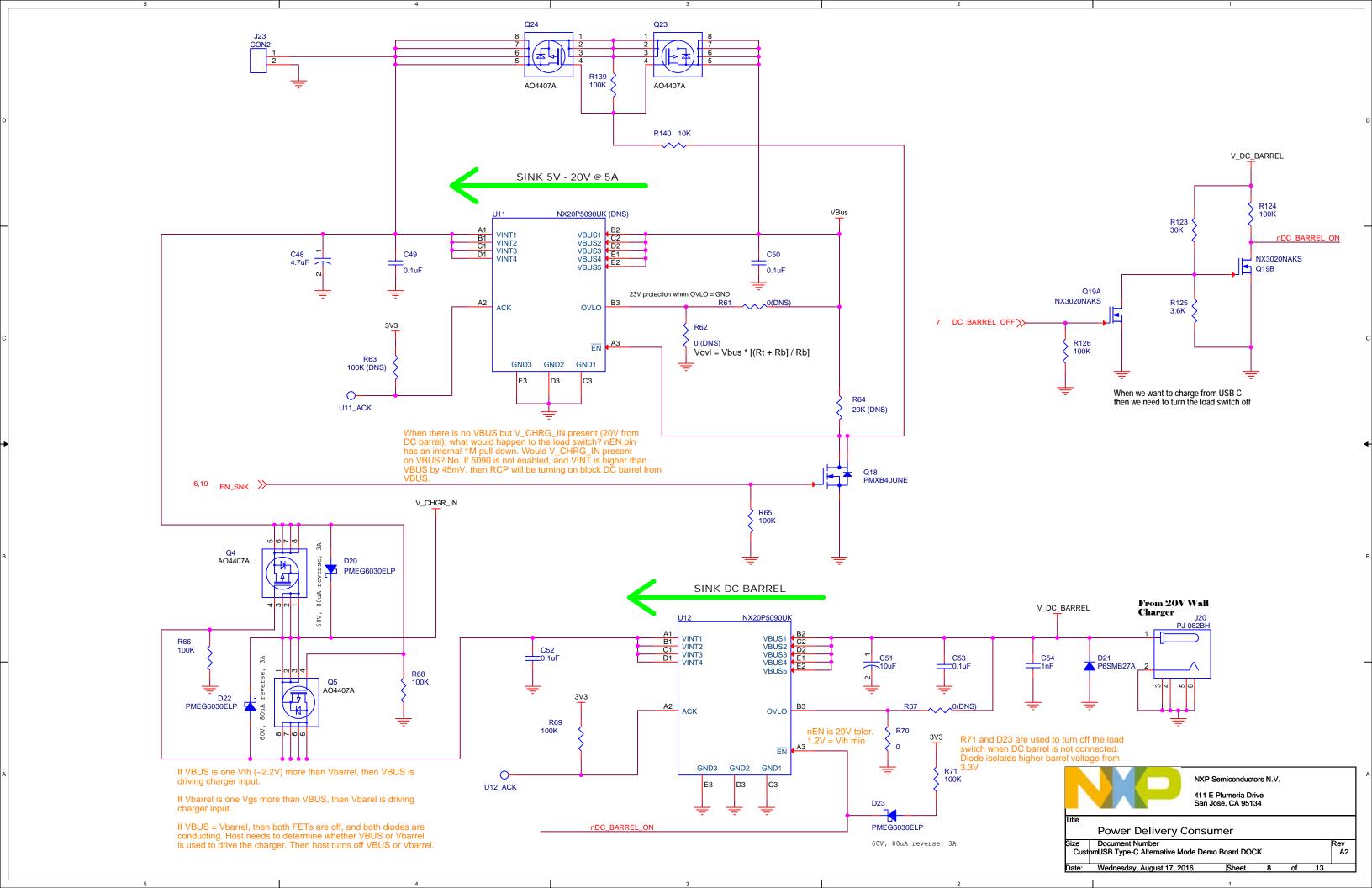


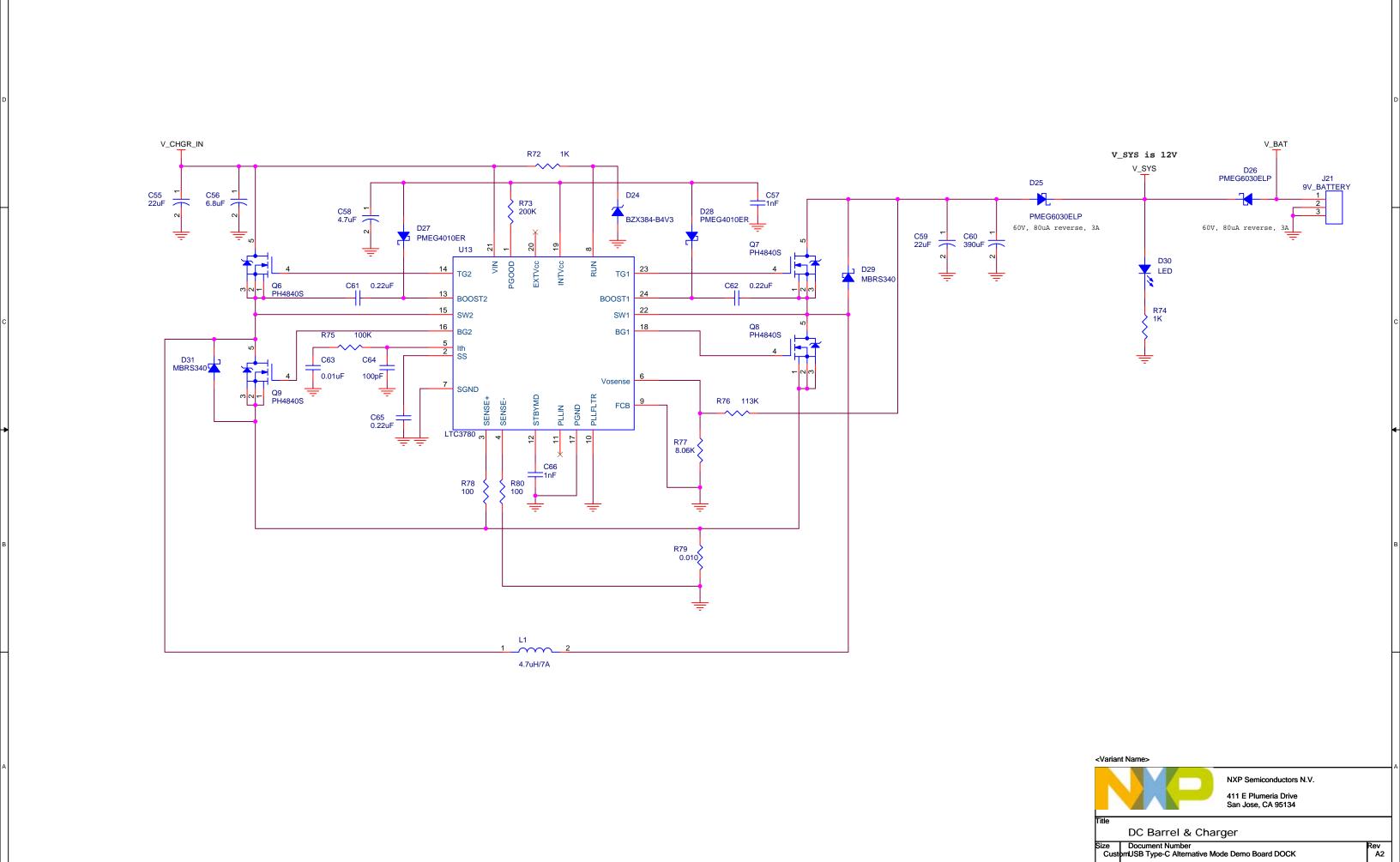
NXP Semiconductors N.V. 411 E Plumeria Drive San Jose, CA 95134 USB3.0 Redriver Size Document Number
CustomUSB Type-C Alternative Mode Demo Board DOCK Rev A2

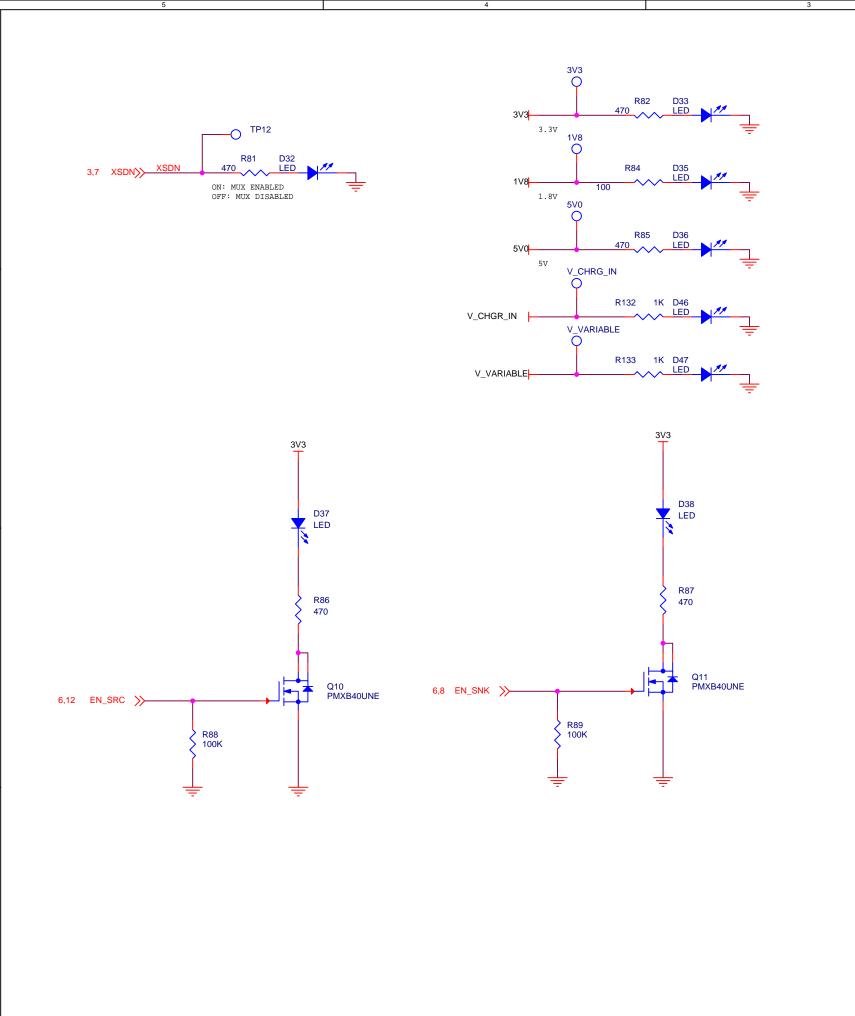


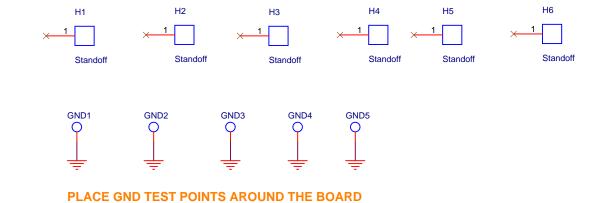


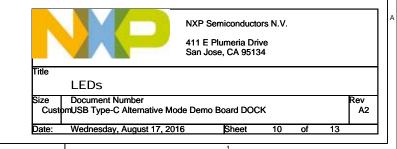


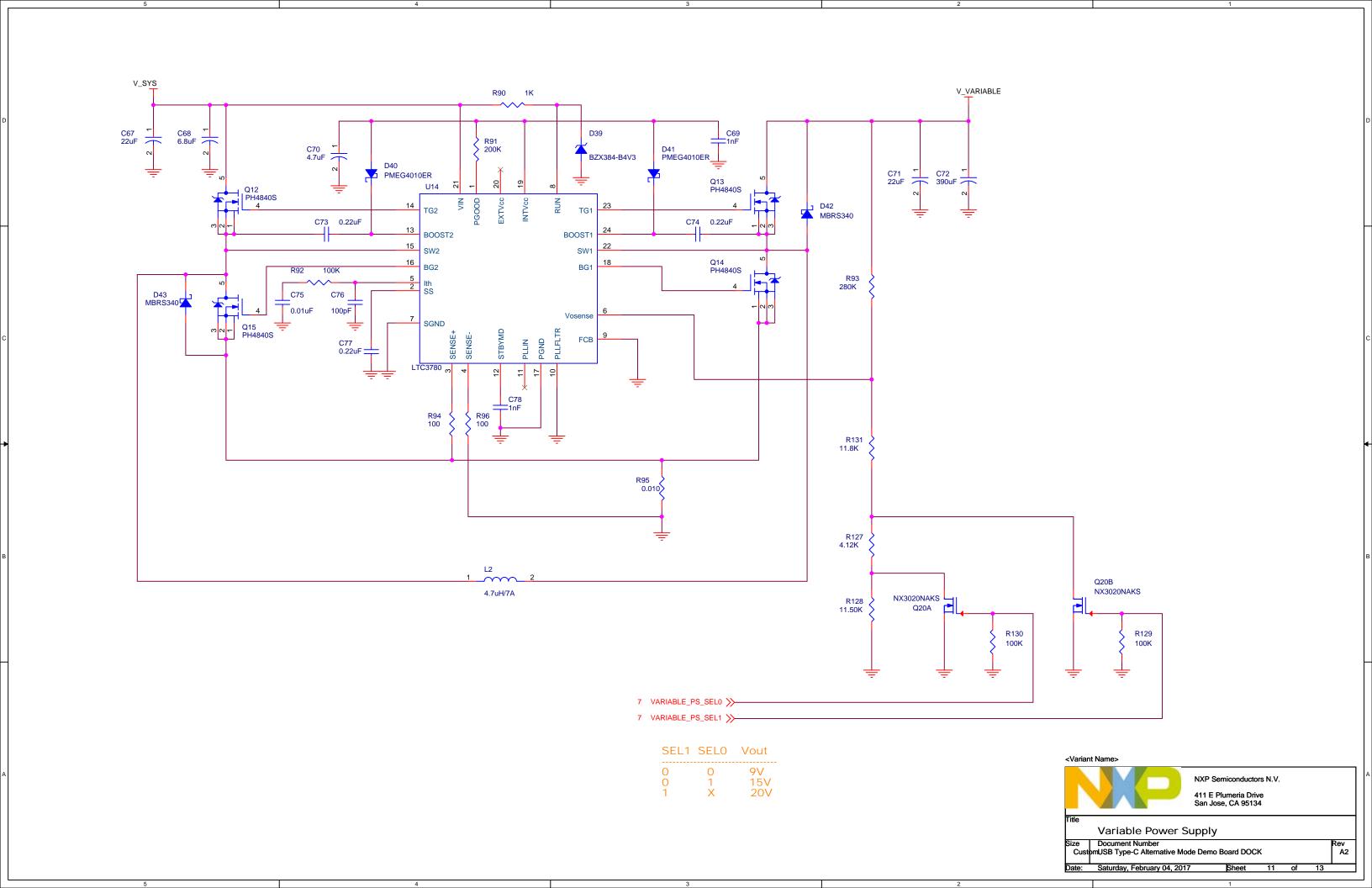


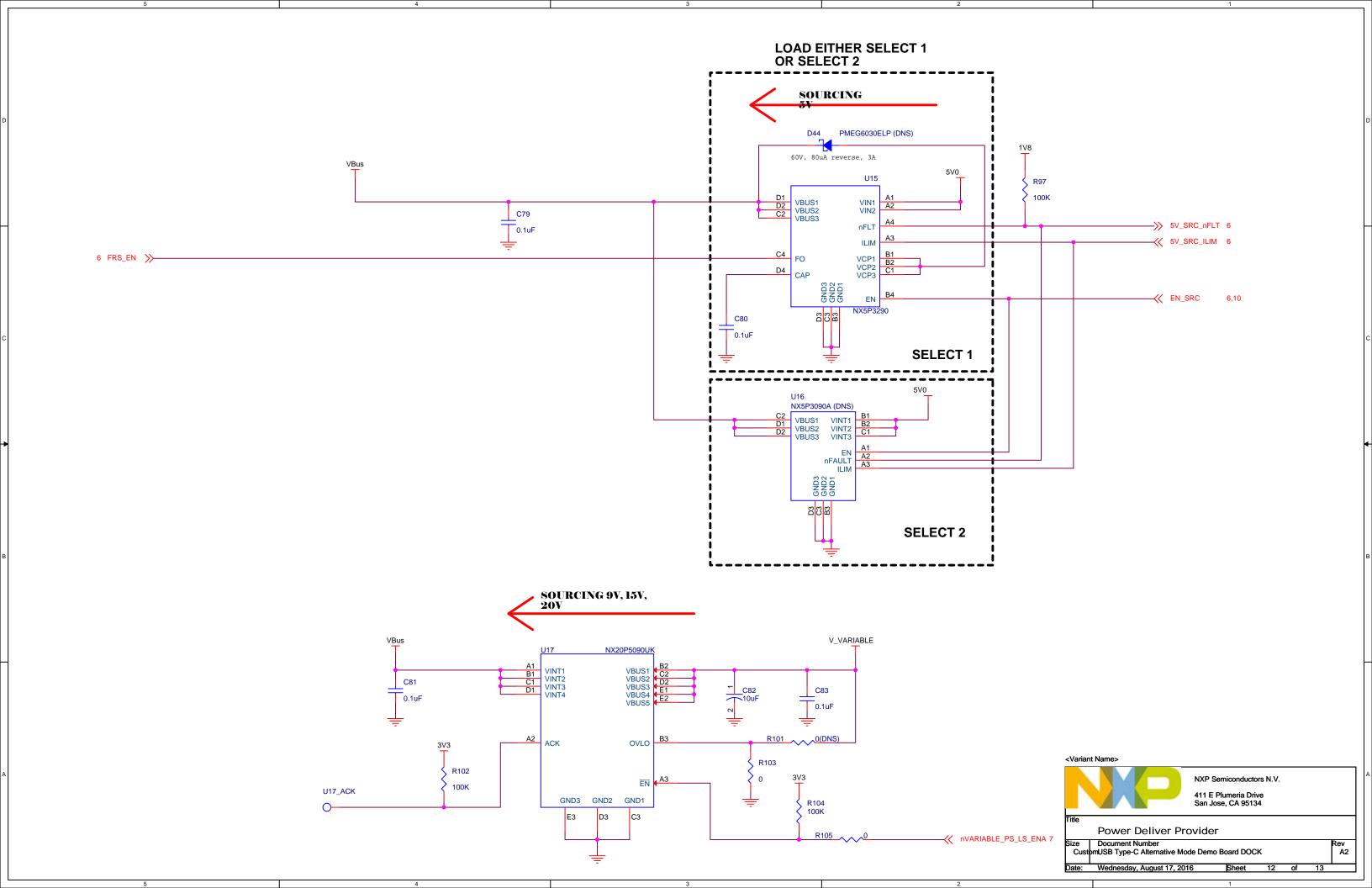


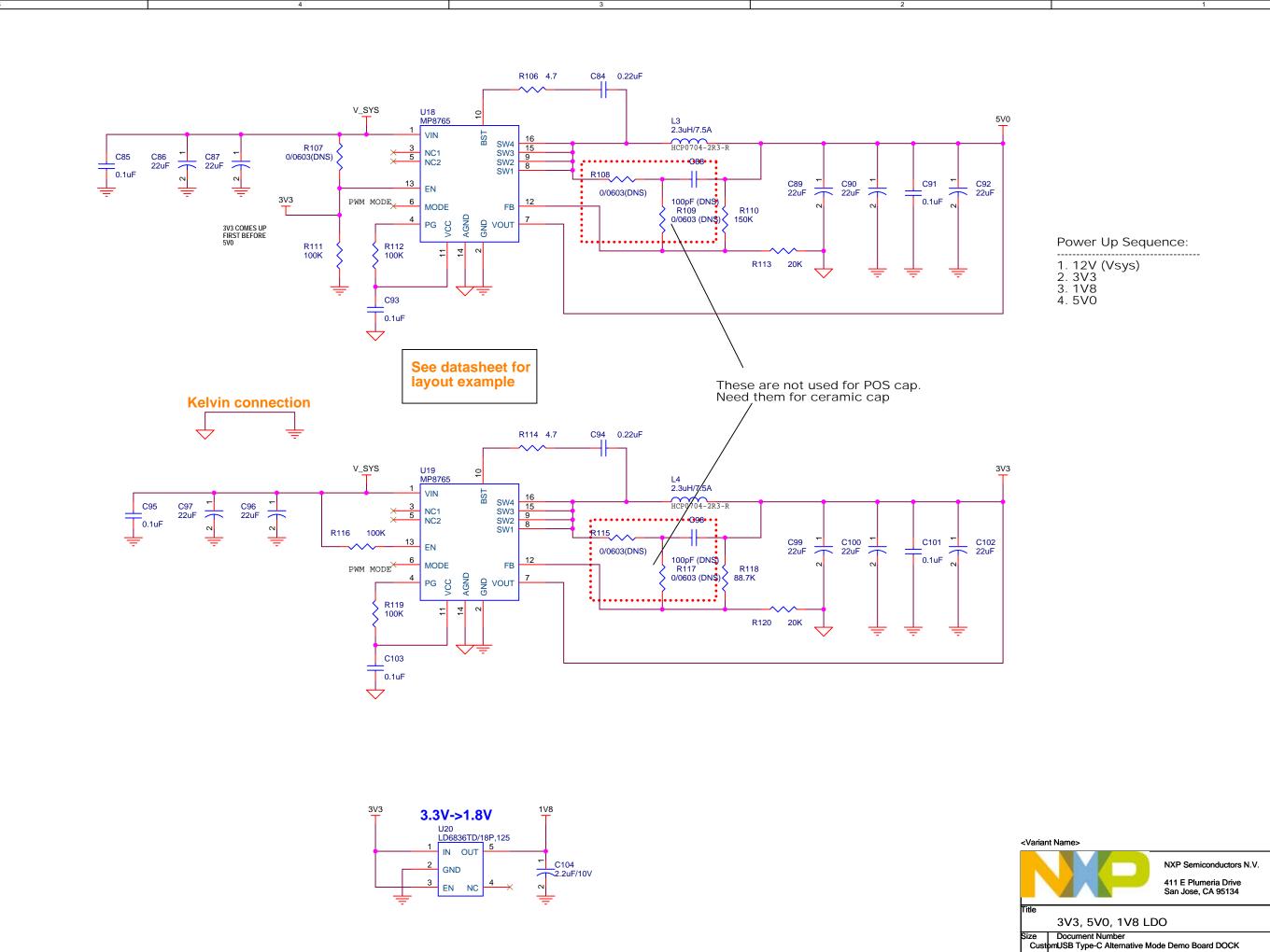












Rev A2

Date: Thursday, February 16, 2017