

Eric Vittoz

# Low-Power Crystal and MEMS Oscillators

The Experience of Watch  
Developments

# Integrated Circuits and Systems

## **Series Editor**

Anantha Chandrakasan, Massachusetts Institute of Technology  
Cambridge, Massachusetts

For other titles published in this series, go to  
[www.springer.com/series/7236](http://www.springer.com/series/7236)

Eric Vittoz

# Low-Power Crystal and MEMS Oscillators

The Experience of Watch Developments



Springer

Eric Vittoz  
Ecole Polytechnique Fédérale de Lausanne (EPFL)  
1015 Lausanne  
Switzerland  
[evittoz@ieee.org](mailto:evittoz@ieee.org)

ISSN 1558-9412  
ISBN 978-90-481-9394-3 e-ISBN 978-90-481-9395-0  
DOI 10.1007/978-90-481-9395-0  
Springer Dordrecht Heidelberg London New York

Library of Congress Control Number: 2010930852

© Springer Science+Business Media B.V. 2010  
No part of this work may be reproduced, stored in a retrieval system, or transmitted in any form or by any means, electronic, mechanical, photocopying, microfilming, recording or otherwise, without written permission from the Publisher, with the exception of any material supplied specifically for the purpose of being entered and executed on a computer system, for exclusive use by the purchaser of the work.

*Cover design:* Spi Publisher Services

Printed on acid-free paper

Springer is part of Springer Science+Business Media ([www.springer.com](http://www.springer.com))

**To my wife Monique**

# Contents

<b>Preface .....</b>	<b>xi</b>
<b>Symbols .....</b>	<b>xiii</b>
<b>1 Introduction .....</b>	<b>1</b>
1.1 Applications of Quartz Crystal Oscillators .....	1
1.2 Historical Notes .....	2
1.3 The Book Structure .....	2
1.4 Basics on Oscillators .....	4
<b>2 Quartz and MEM Resonators .....</b>	<b>7</b>
2.1 The Quartz Resonator .....	7
2.2 Equivalent Circuit .....	8
2.3 Figure of Merit .....	10
2.4 Mechanical Energy and Power Dissipation .....	15
2.5 Various Types of Quartz Resonators .....	15
2.6 MEM Resonators .....	18
2.6.1 Basic Generic Structure .....	18
2.6.2 Symmetrical Transducers .....	21
<b>3 General Theory of High-Q Oscillators .....</b>	<b>23</b>
3.1 General Form of the Oscillator .....	23
3.2 Stable Oscillation .....	25
3.3 Critical Condition for Oscillation and Linear Approximation ..	27
3.4 Amplitude Limitation .....	27
3.5 Start-up of Oscillation .....	29
3.6 Duality .....	30
3.7 Basic Considerations on Phase Noise .....	31
3.7.1 Linear Circuit .....	31

3.7.2	Nonlinear Time Variant Circuit	33
3.8	Model of the MOS Transistor	36
<b>4</b>	<b>Theory of the Pierce Oscillator</b>	<b>41</b>
4.1	Basic Circuit	41
4.2	Linear Analysis	42
4.2.1	Linearized Circuit	42
4.2.2	Lossless Circuit	46
4.2.3	Phase Stability	50
4.2.4	Relative Oscillator Voltages	51
4.2.5	Effect of Losses	52
4.2.6	Frequency Adjustment	54
4.3	Nonlinear Analysis	55
4.3.1	Numerical Example	55
4.3.2	Distortion of the Gate Voltage	57
4.3.3	Amplitude Limitation by the Transistor Transfer Function	58
4.3.4	Energy and Power of Mechanical Oscillation	68
4.3.5	Frequency Stability	69
4.3.6	Elimination of Unwanted Modes	71
4.4	Phase Noise	77
4.4.1	Linear Effects on Phase Noise	77
4.4.2	Phase Noise in the Nonlinear Time Variant Circuit	78
4.5	Design Process	84
4.5.1	Design Steps	84
4.5.2	Design Examples	89
<b>5</b>	<b>Implementations of the Pierce Oscillator</b>	<b>93</b>
5.1	Grounded-Source Oscillator	93
5.1.1	Basic Circuit	93
5.1.2	Dynamic Behavior of Bias	95
5.1.3	Dynamic Behavior of Oscillation Amplitude	97
5.1.4	Design Examples	100
5.1.5	Implementation of the Drain-to-Gate Resistor	102
5.1.6	Increasing the Maximum Amplitude	106
5.2	Amplitude Regulation	107
5.2.1	Introduction	107
5.2.2	Basic Regulator	108
5.2.3	Amplitude Regulating Loop	115
5.2.4	Simplified Regulator Using Linear Resistors	118

5.2.5	Elimination of Resistors . . . . .	120
5.3	Extraction of the Oscillatory Signal . . . . .	123
5.4	CMOS-Inverter Oscillator . . . . .	124
5.4.1	Direct Implementation . . . . .	124
5.4.2	Current-controlled CMOS-inverter oscillator. . . . .	129
5.5	Grounded-Drain Oscillator . . . . .	132
5.5.1	Basic Implementation . . . . .	132
5.5.2	Single-Substrate Implementation . . . . .	133
<b>6</b>	<b>Alternative Architectures . . . . .</b>	<b>137</b>
6.1	Introduction . . . . .	137
6.2	Symmetrical Oscillator for Parallel Resonance . . . . .	137
6.2.1	Basic Structure . . . . .	137
6.2.2	Linear Analysis with the Parallel Resonator . . . . .	139
6.2.3	Linear Analysis with the Series Motional Resonator .	140
6.2.4	Effect of Losses . . . . .	143
6.2.5	Nonlinear Analysis . . . . .	144
6.2.6	Phase Noise . . . . .	149
6.2.7	Practical Implementations . . . . .	157
6.3	Symmetrical Oscillator for Series Resonance . . . . .	164
6.3.1	Basic Structure . . . . .	164
6.3.2	Linear Analysis . . . . .	165
6.3.3	Nonlinear Analysis . . . . .	172
6.3.4	Phase Noise . . . . .	177
6.3.5	Practical Implementation . . . . .	183
6.4	Van den Homberg Oscillator . . . . .	190
6.4.1	Principle and Linear Analysis . . . . .	190
6.4.2	Practical Implementation and Nonlinear Behavior .	193
6.5	Comparison of Oscillators . . . . .	194
6.5.1	Pierce Oscillator (1) . . . . .	195
6.5.2	Van den Homberg Oscillator (2) . . . . .	196
6.5.3	Parallel Resonance Oscillator (3) . . . . .	196
6.5.4	Series Resonance Oscillator (4) . . . . .	197
<b>Bibliography . . . . .</b>	<b>201</b>	
<b>Index . . . . .</b>	<b>203</b>	

# Preface

In the early 60s, the watchmaking industry realized that the newly invented integrated circuit technology could possibly be applied to develop electronic wristwatches. But it was immediately obvious that the precision and stability required for the time base could not be obtained by purely electronic means. A mechanical resonator had to be used, combined with a transducer. The frequency of the resonator had to be low enough to limit the power consumption at the microwatt level, but its size had to be compatible with that of the watch. After unsuccessful results with metallic resonators at sonic frequencies, efforts were concentrated on reducing the size of a quartz crystal resonator. Several solutions were developed until a standard emerged with a thin tuning fork oscillating at 32 kHz and fabricated by chemical etching. After first developments in bipolar technology, CMOS was soon identified as the best choice to limit the power consumption of the oscillator and frequency divider chain below one microwatt. Low-power oscillator circuits were developed and progressively optimized for best frequency stability, which is the main requirement for timekeeping applications. More recent applications to portable communication devices require higher frequencies and a limited level of phase noise. Micro-electro-mechanical (MEM) resonators have been developed recently. They use piezoelectric or electrostatic transduction and are therefore electrically similar to a quartz resonator.

The precision and stability of a quartz is several orders of magnitude better than that of integrated electronic components. Hence, an ideal oscillator circuit should just compensate the losses of the resonator to maintain its oscillation on a desired mode at the desired level, without affecting the frequency or the phase of the oscillation. Optimum designs aim at approaching this ideal case while minimizing the power consumption.

This book includes the experience accumulated along more than 30 years by the author and his coworkers. The main part is dedicated to variants of the Pierce oscillator most frequently used in timekeeping applications. Other forms of oscillators that became important for RF applications have been added, as well as an analysis of phase noise. The knowledge is formalized in an analytical manner, in order to highlight the effect and the importance of the various design parameters. Computer simulations are limited to particular examples but have been used to crosscheck most of the analytical results.

Many collaborators of CEH (Centre Electronique Hologer, Watchmakers Electronic Center), and later of CSEM, have contributed to the know-how described in this book. Among them, by alphabetic order, Daniel Aebischer, Luc Astier, Serge Bitz, Marc Degrauwe, Christian Enz, Jean Fellrath, Armin Frei, Walter Hammer, Jean Hermann, Vincent von Kaenel, Henri Oguey, and David Ruffieux. Special thanks go to Christian Enz for the numerous discussions about oscillators and phase noise during the elaboration of this book.

Eric A. Vittoz  
Cernier, Switzerland  
February 2010

# Symbols

**Table 0.1** Symbols and their definitions.

Symbol	Description	Reference
$a$	Power factor of the flicker noise current	(6.71)
$A$	Normalized transconductance in series resonance oscillator	(6.108)
$B$	Normalized bandwidth in series resonance oscillator	(6.108)
$C_a, C_b$	Functional capacitors	Fig. 6.37
$C_D$	Capacitance between drains	Fig. 6.1
$C_L$	Load capacitance in series resonance oscillator	Fig. 6.16
$C_m (C_{m,i})$	Motional capacitance (of mode $i$ )	Fig. 2.2
$C_P$	Total parallel capacitance of the resonator	(2.22)
$C_s$	Series connection of $C_1$ and $C_2$	(4.9)
$C_S$	Capacitance between sources	Fig. 6.1
$C_0$	Parallel capacitance of the dipole resonator	(2.1)
$C_1$	Total gate-to-source capacitance	Fig. 4.1
$C_2$	Total drain-to-source capacitance	Fig. 4.1
$C_3$	Total capacitance across the motional impedance	Fig. 2.2
$E_m$	Energy of mechanical oscillation	(2.23)
$f$	Frequency	
$f_m$	Motional resonant frequency	(4.140)
$f_s$	Frequency of stable oscillation	(3.24)
$f_s(m_v)$	Fundamental function in strong inversion	(6.37)
$f_w(v_{in})$	Fundamental function in weak inversion	(6.30)
$F_a$	Flicker noise current constant	(6.71)
$G_a$	Reference conductance for the flicker noise current	(6.71)
$G_{ds}$	Residual output conductance in saturation	(3.57)
$G_m$	Gate transconductance of a transistor	(3.53)

*continued on next page*

*continued from previous page*

Symbol	Description	Reference
$G_{ms}$	Source transconductance of a transistor	(3.49)
$G_{md}$	Drain transconductance of a transistor	(3.49)
$G_{mcrit}$	Critical transconductance for oscillation	Fig. 4.4
$G_{mcrit0}$	Critical transconductance for lossless circuit	Fig. 4.6
$G_{mlim}$	Limit transconductance in series resonance oscillator	(6.109)
$G_{mmax}$	Maximum possible transconductance for oscillation	Fig. 4.4
$G_{mopt}$	Optimum value of transconductance	Fig. 4.4
$G_{m(1)}$	Transconductance for the fundamental frequency	(4.54)
$G_{vi}$	Transconductance of the regulator	(5.52)
$h_s(m_i)$	Transconductance function in strong inversion	(6.142)
$I_{B0}(x)$	Modified Bessel function of order 0	(4.59)
$I_{B1}(x)$	Modified Bessel function of order 1	(4.61)
$I_c$	Circuit current	Fig. 3.1
$I_{cs}$	Value of $I_c$ at stable oscillation	(3.6)
$I_D$	Drain current	Fig. 3.10
$I_{D0}$	DC component of drain current	(5.1.2)
$I_{D(1)}$	Fundamental component of $I_D$	Fig. 4.13
$I_F$	Forward component of drain current	(3.40)
$I_m$	Motional current	Fig. 2.2
$I_{ms}$	Value of $I_m$ at stable oscillation	(3.6)
$I_R$	Reverse component of drain current	(3.40)
$I_{spec}$	Specific current of a transistor	(3.41)
$I_0$	Bias current of the oscillator	Fig. 4.13
$I_{0start}$	Start-up value of bias current	(5.45)
$I_{0crit}$	Critical value of bias current $I_0$	Fig. 4.14
$I_{0critmin}$	Critical current in weak inversion	(4.64)
$I_1$	Complex value of the sinusoidal drain current	6.3.2.3
$IC$	Inversion coefficient of a transistor	(3.45)
$IC_0$	Inversion coefficient at $I_0 = I_{0crit}$	(4.72)
$k_c$	Capacitive attenuation factor	(4.69)
$K_f$	Flicker noise voltage constant of a transistor	(3.62)
$K_{fi}$	Flicker noise current function	(3.36)
$K_{fv}$	Flicker noise voltage function	(3.35)
$K_g$	Transconductance ratio	Fig. 6.37
$K_i$	Mirror ratio in the regulator	Fig. 5.9
$K_{iv}$	Gain parameter of $ V_1 (I_{D0})$	(5.24)
$K_l$	Level of specific current	(6.92)
$K_m$	Margin factor	(4.17)
$K_r$	Ratio of transfer parameters	Fig. 5.4

*continued on next page*

continued from previous page

Symbol	Description	Reference
$K_s$	Ratio of specific currents	(6.82)
$K_t$	Transconductance ratio	(6.175)
$K_w$	Width ratio in the regulator	(5.43)
$L_m (L_{m,i})$	Motional inductance (of mode $i$ )	Fig. 2.2
$m_i$	Index of current modulation	(6.133)
$m_v$	Index of voltage modulation	(4.122)
$m_{vd}$	Index of voltage modulation for a differential pair	(6.35)
$M$	Figure of merit	(2.9)
$M_D$	Figure of merit of the resonator used as a dipole	(2.22)
$M_L$	Figure of merit of the resonator used as a loaded dipole	(6.7)
$M_0$	Intrinsic figure of merit of the resonator	(2.10)
$n$	Slope factor of a transistor	(3.40)
$p$	Frequency pulling	(2.7)
$p_c$	Frequency pulling at critical condition for oscillation	(3.10)
$p_{pa}$	Frequency pulling at parallel resonance	(2.15)
$p_s$	Frequency pulling at stable oscillation	(3.7)
$p_{se}$	Frequency pulling at series resonance	(2.14)
$P_m$	Power dissipated in the resonator	(2.24)
$Q (Q_i)$	Quality factor (of mode $i$ )	(2.3)
$Q_b$	Quality factor of the bias circuit	(5.12)
$R_{iv}$	Slope of the amplitude $ V_1 (I_0)$	Fig. 5.3
$R_L$	Load resistance	Fig. 6.16
$R_m (R_{m,i})$	Motional resistance (of mode $i$ )	Fig. 2.2
$R_n$	Negative resistance of the circuit	(3.2)
$R_{n0}$	Value of $R_n$ for the linear circuit	(3.12)
$s_{vi}$	Normalized slope of the regulator	Fig. 5.10
$s_{iv}$	Normalized slope of the amplitude	Fig. 4.17
$S_{I_n^2}$	Current noise spectrum	(4.107)
$S_{I_{nD}^2}$	Drain current channel noise spectrum	(3.59)
$S_{I_{nL}^2}$	Loop Current noise spectrum	(3.27)
$S_{V_n^2}$	Voltage noise spectrum	(4.107)
$S_{V_{nG}^2}$	Gate voltage flicker noise spectrum	(3.62)
$S_{\phi_n^2}$	Phase noise power spectrum	(3.29)
$t$	Time	
$U_T$	Thermodynamic voltage	(3.40)
$V$	Voltage across the resonator	Fig. 2.2
$V_B$	Supply voltage (battery voltage)	Fig. 5.1
$v_c$	Value of $ V_c $ normalized to $nU_T$	(6.130)
$V_c$	Control voltage of a transistor	(6.129)

continued on next page

continued from previous page

Symbol	Description	Reference
$V_D$	Drain voltage	Fig. 3.10
$V_{Dsat}$	Saturation value of drain voltage	(3.46)
$v_e$	Normalized effective DC gate voltage	(4.57)
$V_G$	Gate voltage	Fig. 3.10
$V_{G0}$	DC component of gate voltage	(4.52)
$v_{in}$	Value of $ V_{in} $ normalized to $nU_T$	(6.31)
$V_{in}$	Differential input voltage	Fig. 6.5
$V_M$	Channel length modulation voltage	(3.57)
$V_n$	Open-loop noise voltage of the circuit	3.7.1
$V_S$	Source voltage	Fig. 3.10
$V_{T0}$	Threshold voltage of a transistor	(3.40)
$V_{(1)}$	Complex value of fundamental component of $V$	(3.1)
$v_1$	value of $ V_1 $ normalized to $nU_T$	(4.57)
$V_1$	Complex value of gate-to-source voltage	Fig. 4.8
$V_2$	Complex value of drain-to-source voltage	Fig. 4.8
$V_3$	Complex value of drain-to-gate voltage	Fig. 4.8
$Z_c$	Impedance of the linear circuit	(3.8)
$Z_{c(1)}$	Circuit impedance for fundamental frequency	(3.1)
$Z_{c0}$	Circuit impedance without parallel capacitance	(6.3)
$Z_D$	Impedance between drains	Fig. 6.3
$Z_L$	Load impedance	Fig. 6.16
$Z_m$ ( $Z_{m,i}$ )	Motional impedance (of mode $i$ )	Fig. 2.2
$Z_p$	Total parallel impedance	(2.12)
$Z_S$	Impedance between sources	Fig. 6.3
$Z_1$	Total gate-to-source impedance	Fig. 4.3
$Z_2$	Total drain-to-source impedance	Fig. 4.3
$Z_3$	Total drain-to-gate impedance	Fig. 4.3
$\alpha$	Ratio of critical transconductance	(4.98)
$\alpha_i$	Noise current modulation function	Fig. 3.9
$\alpha_v$	Noise voltage modulation function	Fig. 3.9
$\alpha_0$	Value of $\alpha$ for the lossless case	(4.99)
$\beta$	Transfer parameter of a transistor	(3.44)
$\Delta\omega$	Noise frequency offset	(3.28)
$\epsilon_{max}$	Maximum relative mismatch	(6.15)
$\epsilon_0$	Permittivity of free space	(2.27)
$\gamma$	Noise excess factor of the oscillator	Fig. 3.7
$\gamma_t$	Channel noise excess factor of a transistor	(3.60)
$\Gamma_i$	Effective impulse sensitivity function for noise current	(3.34)
$\Gamma_v$	Effective impulse sensitivity function for noise voltage	(3.32)

continued on next page

*continued from previous page*

Symbol	Description	Reference
$\tau$	Time constant of oscillation growth	(3.16)
$\tau_0$	Start-up value of $\tau$	(3.15)
$\omega$	Approximate angular frequency of oscillation	
$\omega_m$ ( $\omega_{m,i}$ )	angular frequency of resonance (of mode $i$ )	(2.2)
$\omega_n$	Angular frequency at which noise is considered	(4.106)
$\omega_s$	Angular frequency at stable oscillation	(3.24)
$\Omega_{civ}$	Cut-off angular frequency of $ V_1 (I_{D0})$	(5.26)
$\Omega_0$	Resonant angular frequency of bias circuit	(5.10)
$\Omega_1$	Unity gain frequency of the regulation loop	(5.71)

# Chapter 1

## Introduction

### 1.1 Applications of Quartz Crystal Oscillators

Relevant time durations for modern science range from the femtosecond of very fast electronics to the age of the universe, 15 billion years. This corresponds to a range of about 32 orders of magnitude. Moreover, this variable can be controlled and measured with an accuracy better than  $10^{-14}$  by modern atomic clocks. However, the accuracy that can be obtained by purely electronic circuits, such as integrated circuits, is only of the order of  $10^{-3}$ . This is because there is no combination of available electronic components (like a RC time constant for example) that is more precise and constant with time and temperature. Now,  $10^{-3}$  corresponds to an error of about 1.5 minute per day, which is totally unacceptable for timekeeping applications. The same is true for applications to modern telecommunications, which exploits the frequency spectrum up to 300 Ghz.

Quartz crystal oscillators offer the range of accuracy required by these applications by combining the electronic circuit with a simple electromechanical resonator that essentially controls the frequency.

Timekeeping devices like wristwatches need a long-term precision better than  $10^{-5}$ , possibly  $10^{-6}$  that corresponds to 30 s/year. Additional requirements for watches include a very low power consumption, of the order of 0.1  $\mu\text{W}$  in the range of indoor and outdoor temperatures. The frequency should be as low as possible, to minimize the additional power consumed by the frequency divider (period counter).

The same level of long-term precision is needed for telecommunications, with less demanding requirements on power consumption. However, higher or much higher frequencies are needed, and there is an additional important requirement on phase noise (or short-time stability).

Crystal oscillators are also often used for generating the clock of digital systems or analog circuits. The precision needed is then of the order of  $10^{-4}$ , which makes the quartz oscillator very uncritical, but problems may arise if it is not properly designed, the worst one being oscillation on an parasitic resonance of the resonator.

## 1.2 Historical Notes

The first quartz crystal oscillator was invented by Walter Guyton Cady in 1921 [1], as a way to produce an electrical signal of very constant frequency. Soon after, George Washington Pierce developed a very elegant oscillator circuit using a single vacuum tube [2, 3], that has been easily adapted to integrated circuits, some 40 years later. Quartz oscillators have since been used extensively to produce the accurate and stable frequency needed for the carrier of telecommunication circuits.

Artificial quartz, first produced in 1958, progressively replaced natural quartz crystal. Quartz production was boosted in the seventies by a surge of demand for the 40-channel of citizen band transceivers. It was alleviated by the introduction of frequency synthesizers made possible by the evolution of VLSI circuits.

The application of quartz oscillators to timekeeping devices started in 1927 with the first quartz clock developed by Morrison and Horton [4]. Portable clocks became possible with the invention of the transistor, but integrated circuits were needed to develop the first quartz wristwatch presented in 1967 [5].

## 1.3 The Book Structure

After this short introductory chapter, Chapter 2 is essentially dedicated to the quartz crystal resonator and to its electrical equivalent circuit. By exploiting the very large value of quality factor  $Q$ , the electrical impedance of the resonator is described by a bilinear function of the relative amount  $p$  of frequency difference with the mechanical resonant frequency, called frequency

pulling. After a brief description of the various types of quartz resonators, a last section shows how the equivalent circuit of a MEM resonator using an electrostatic transducer can be reduced qualitatively to that of the quartz resonator.

Chapter 3 describes a general theory that applies to all oscillators based on a high- $Q$  series resonant circuit (or parallel resonant circuit by swapping currents for voltages). By adequately splitting conceptually the oscillator into a frequency-independent nonlinear part and a frequency-dependent linear series resonator, this approach allows to predict the amplitude and the precise value of frequency pulling by including nonlinear effects. This chapter also introduces some basic considerations on phase noise. An analysis of the effect of cyclostationary noise sources is proposed, based on the effective impulse sensitivity function (ISF) [6], with the approximation of sinusoidal waveforms made possible by the high value of  $Q$ . The chapter ends with a short introduction to the EKV analytical model of the MOS transistor that is used in all subsequent circuit analyses.

Chapter 4 concentrates on the theory of the Pierce oscillator [3], which is the only possible architecture with a single active transistor. The linear analysis (valid at the critical condition for oscillation or for sufficiently small amplitudes) capitalizes on the circular locus resulting from the bilinear dependency of the circuit impedance on the transconductance of the transistor. The amplitude of oscillation is obtained analytically from the DC transfer function of the transistor, using the fact that the gate voltage remains almost sinusoidal. The important problem of frequency stability and that of avoiding oscillation on a parasitic resonant mode of the resonator are also discussed. Phase noise is then approached analytically, using the concept of effective impulse sensitivity function (ISF) to treat the effect of the cyclostationary white and flicker noise produced by the active transistor. A design process is presented and illustrated by two numerical examples.

Chapter 5 deals with the practical realization of the Pierce oscillator. The dynamic behavior of the grounded source implementation with respect to variations of its bias current is analyzed. The oscillator is then embedded in an amplitude regulating loop based on a particular amplitude regulator scheme. The results are then applied to the two numerical examples presented in Chapter 4. The Pierce oscillator is frequently realized by means of a simple CMOS inverter. A qualitative analysis supported by circuit simulations demonstrates the many drawbacks of this solution. A better way to reduce the power consumption by means of complementary transistors is presented. The chapter ends with the grounded-drain implementation, which has the advantage of requiring only one pin to connect the external reson-

ator. Its performance is shown to be lower than that of the grounded-source solution, especially if the active transistor is not put in a separate well.

Many architectures become possible when two or more active transistors are considered. Chapter 6 describes and analyzes three of them. The first one is a symmetrical circuit that exploits the parallel resonance of the resonator, and delivers symmetrical output voltages [25]. The power consumption of this circuit can be made very low, at the cost of an increased sensitivity of the frequency to electrical parameters. The second circuit is also symmetrical and based on two active transistors. It produces a current stable DC negative resistance compatible with a series resonator. Compared to other solutions, the power consumption of this circuit is lower for low- $Q$  resonators and/or for very low values of frequency pulling. In the third architecture [27], one side of the resonator is grounded (one-pin oscillator). This more complex circuit uses a full operational transconductance amplifier (OTA) combined with two grounded capacitors. The chapter ends with a comparison of the four types of oscillators analyzed in the book.

An analytical approach is favored all along the chapters, with a list of all the variables at the beginning of the book. Results are simple equations illustrated by normalized graphs. The advantage is to explicit clearly the effect of each design parameter on the circuit performance. The drawback is that some approximations are sometimes necessary, leading to approximative results. Computer simulations can then be used to obtain more precision. Most of the analytical results have been cross-checked by circuit simulations, with the notable exception of phase noise. These simulations have been carried out with the LTspice circuit simulator of Linear Technology and the EKV model of the MOS transistor.

## 1.4 Basics on Oscillators

As depicted in Fig. 1.1, the most general way of describing an oscillator is by a frequency-dependent nonlinear circuit block connected in closed loop. The transfer function of the block is  $G(\omega, A)$ , where  $\omega$  is the angular frequency and  $A$  is the input amplitude.

If the circuit is strongly nonlinear with a large bandwidth, it results in a relaxation oscillator, the waveform of which is far from being sinusoidal.

On the contrary, if the circuit has a narrow bandwidth, the system becomes a harmonic oscillator and the oscillatory signal is approximately sinusoidal. Stable oscillation may take place at frequency  $\omega_s$  with an amplitude  $A_s$  for



**Figure 1.1** General representation of an oscillator.

$$G(\omega_s, A_s) = 1. \quad (1.1)$$

However, this is only possible if two fundamental conditions are fulfilled. The first condition is that for *phase stability* [7]

$$\frac{d(\arg G)}{d\omega} \Big|_{\omega_s, A_s} < 0. \quad (1.2)$$

No periodic solution can be maintained if this condition is not fulfilled. The second condition is that of *amplitude stability*

$$\frac{d|G|}{dA} \Big|_{\omega_s, A_s} < 0. \quad (1.3)$$

This condition requires that the circuit block contains some *nonlinearity* to fix the amplitude of oscillation.

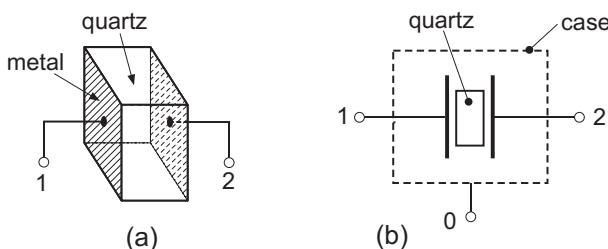
Although this approach of a closed loop is applicable to all kinds of oscillators, we will show in Chapter 3 that, for the case of oscillators including a resonator with very high quality factor, more insight can be obtained by separating this resonator from the rest of the circuit.

# Chapter 2

## Quartz and MEMS Resonators

### 2.1 The Quartz Resonator

As illustrated by Fig. 2.1(a), a quartz resonator is essentially a capacitor, the dielectric of which is silicon dioxide ( $\text{SiO}_2$ ), the same chemical compound as used in integrated circuits. However, instead of being a glass, it is a monocrystal, a quartz crystal, which exhibits piezoelectric properties. Therefore, a part of the electrical energy stored in the capacitor is converted into mechanical energy.



**Figure 2.1** Quartz crystal resonator: (a) Schematic structure; (b) symbol.

Whatever the shape of the piece of quartz, it has some mass and some elasticity; it can therefore oscillate mechanically. Unlike simple  $LC$  electrical resonators, mechanical resonators always possess several resonance frequencies, corresponding to different possible modes of oscillation (eigenmodes).

Now, if an AC voltage is applied to the capacitor at a frequency close to that of a possible mode, it can possibly excite this mode and drive the quartz resonator into mechanical oscillation.

In addition to its piezoelectric properties, quartz has the advantage of being an excellent mechanical material, with very small internal friction. It has therefore a very high intrinsic quality factor, of the order of  $10^6$ .

The resonant frequency depends essentially on the shape and the dimensions of the piece of quartz. Possible frequencies range from 1 kHz for large cantilever resonators to hundreds of MHz for very thin thickness-mode resonators.

The exact frequency and its variation with temperature depend on the orientation with respect to the 3 crystal axes. By choosing the optimum mode with an optimum orientation, the linear and quadratic components of the variation of the frequency with temperature can be cancelled, leaving at best a residual dependency of about  $10^{-6}$  from -20 to +80 °C.

## 2.2 Equivalent Circuit

The equivalent circuit of a quartz resonator is shown in Fig. 2.2(a). Although the intrinsic device is a dipole, it is very important in some circuits to model it as a 3-point component, in order to separate the electrical capacitor  $C_{12}$  from the parasitic capacitances to the packaging case  $C_{10}$  and  $C_{20}$ .

If the device is only considered as a dipole, with node 0 floating, then the lumped electrical capacitance is

$$C_0 \triangleq C_{12} + \frac{C_{10}C_{20}}{C_{10} + C_{20}}. \quad (2.1)$$

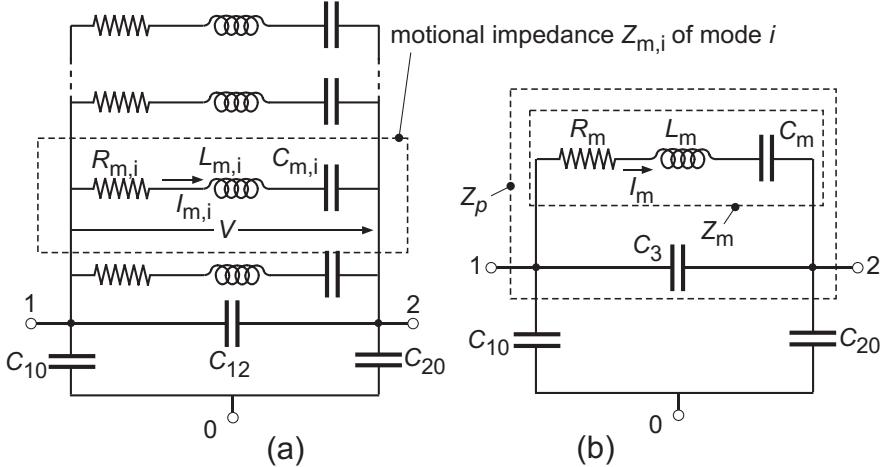
Each possible mode of oscillation  $i$  of the resonator corresponds to a *motional impedance*  $Z_{m,i}$  formed by the series resonant circuit  $R_{m,i}L_{m,i}C_{m,i}$ . The motional inductance  $L_m$  is proportional to the mass of the mechanical resonator. The motional capacitance  $C_m$  is proportional to the inverse of its stiffness. The motional resistance  $R_m$  represents the mechanical losses.

The resonant angular frequency of mode  $i$  is given by

$$\omega_{m,i} = 1 / \sqrt{L_{m,i}C_{m,i}}, \quad (2.2)$$

and its quality factor by

$$Q_i = \frac{1}{\omega_{m,i}R_{m,i}C_{m,i}} = \frac{\omega_{m,i}L_{m,i}}{R_{m,i}} = \frac{1}{R_{m,i}} \sqrt{\frac{L_{m,i}}{C_{m,i}}}. \quad (2.3)$$



**Figure 2.2** Equivalent circuit: (a) of the resonator alone with all possible modes; (b) of a single mode with  $C_{12}$  increased to  $C_3$  by external capacitors.

This factor is very large, typically ranging from  $10^4$  to  $10^6$ . Whenever needed, this relation between  $Q$ ,  $\omega_m$ ,  $R_m$  and  $C_m$  will be used implicitly throughout this book.

The motional current  $I_{m,i}$  flowing through the motional impedance  $Z_{m,i}$  is proportional to the velocity of mode  $i$ . Thus its peak value  $|I_{m,i}|$  is proportional to the peak velocity and  $|I_{m,i}|/\omega_i$  to the amplitude of oscillation of mode  $i$ .

The voltage  $V$  across the motional impedances is proportional to the force produced by the piezoelectric effect.

The ratio  $C_{m,i}/C_{12} \ll 1$  represents the electromechanical coupling to the mode  $i$ . It is always much lower than unity, since it never exceeds the intrinsic coupling coefficient of quartz, which is about 1%. If a mode  $i$  is not coupled at all, then  $C_{m,i} = 0$  and the corresponding branch disappears from the equivalent circuit.

At this point, two very important remarks must be introduced, since they will greatly simplify the nonlinear analysis of quartz oscillators:

1. Since  $Q_i \gg 1$ , the bandwidth of  $Z_m$  is very narrow. Hence, for frequencies close to the resonance of mode  $i$ , the harmonic content of the motional current  $I_{m,i}$  is always negligible. Thus, this current can be considered *perfectly sinusoidal, even if the voltage  $V$  is strongly distorted*:

$$I_{m,i}(t) = |I_{m,i}| \sin(\omega t) \quad (2.4)$$

or, expressed as a complex value

$$I_{m,i} = |I_{m,i}| \exp(j\omega t). \quad (2.5)$$

2. Among the various possible modes of oscillation, we may have the “overtones”, the frequencies of which are close to multiples of that of the fundamental mode. However, because of end effects, these frequencies are not exact multiples of the fundamental. Hence, once a mode is excited, the harmonics that can be produced by the distortion of  $V$  cannot excite these overtones. Once oscillation has taken place at one mode, the *other modes* (and thus the other branches in the equivalent circuit) *can be ignored*.

From now on, let us consider only this particular “wanted” mode, and drop the index  $i$  in the notations. The equivalent circuit is then reduced to that of Fig. 2.2(b), where  $C_3$  now includes external capacitances possibly added to  $C_{12}$  of the resonator itself.

The complex motional impedance is given by

$$Z_m = R_m + j\omega L_m + \frac{1}{j\omega C_m} = R_m + \frac{j}{\omega C_m} \cdot \frac{\omega + \omega_m}{\omega_m} \cdot \frac{\omega - \omega_m}{\omega_m}, \quad (2.6)$$

where the last term has been obtained by introducing (2.2).

Now, because of the very large value of  $Q$ , the frequency of oscillation will always be very close to  $\omega_m$ . It is thus very useful to replace  $\omega$  by the relative amount of *frequency pulling* (by the circuit)

$$p \triangleq \frac{\omega - \omega_m}{\omega_m} \quad \text{with } |p| \ll 1, \quad (2.7)$$

which, introduced in (2.6), gives almost exactly

$$Z_m = R_m + j \frac{2p}{\omega C_m}, \quad (2.8)$$

where  $\omega$  can be considered constant with respect to its effect on  $Z_m$ . Hence,  $Z_m$  is a linear impedance that is *strongly dependent on p*. Indeed, its real part is constant (as long as the quality factor remains constant) but its imaginary part is proportional to  $p$ .

## 2.3 Figure of Merit

An important parameter of quartz resonators (and of all electrostatically driven resonators) is its figure of merit

$$M \triangleq \frac{1}{\omega C_3 R_m} = \frac{QC_m}{C_3}, \quad (2.9)$$

which has a maximum intrinsic value when  $C_3$  is reduced to its minimum value  $C_{12}$ , defined as

$$M_0 \triangleq \frac{1}{\omega C_{12} R_m} = \frac{QC_m}{C_{12}}. \quad (2.10)$$

Indeed,  $M$  is the maximum possible ratio of currents through  $Z_m$  and  $C_3$ . By introducing this definition in (2.8), we can express  $Z_m$  normalized to  $1/\omega C_3$  as

$$\omega C_3 Z_m = \frac{1}{M} (1 + 2Qpj). \quad (2.11)$$

We can now calculate  $Z_p$ , the impedance of the parallel connection of  $Z_m$  and  $C_3$ . Assuming  $\omega$  constant (since  $p \ll 1$ ), it gives, in normalized form:

$$\omega C_3 Z_p = \frac{1 + 2Qpj}{(M - 2Qp) + j} = \frac{M - [4(Qp)^2 - 2MQp + 1] j}{(M - 2Qp)^2 + 1}. \quad (2.12)$$

This impedance becomes real for

$$Qp = \frac{M \pm \sqrt{M^2 - 4}}{4}. \quad (2.13)$$

The negative sign correspond to the *series resonance* frequency, at a value of pulling

$$p_{se} = \frac{C_m}{4C_3} \left[ 1 - \sqrt{1 - 4/M^2} \right], \quad (2.14)$$

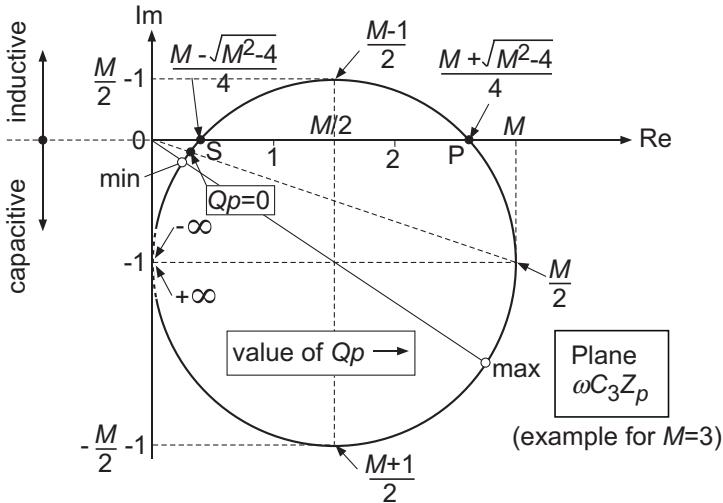
whereas the positive sign corresponds to the *parallel resonance* frequency, at a value of pulling

$$p_{pa} = \frac{C_m}{4C_3} \left[ 1 + \sqrt{1 - 4/M^2} \right], \quad (2.15)$$

For  $M \gg 1$ ,  $p_{se} = 0$ ; the series resonance frequency is the mechanical frequency of the resonator. But  $p_{pa} = C_m/2C_3$ ; the parallel resonance frequency depends on the electrical capacitance  $C_3$ .

Notice that for  $M < 2$ , (2.13) has no real solution. The impedance  $Z_p$  itself is never real but remains capacitive for all frequencies.

As shown by (2.12),  $Z_p$  is a bilinear function of  $Qp$ . Now, a property of bilinear functions is to transform circles into circles in the complex plane [8]. Therefore, the locus of  $Z_p(Qp)$  for  $p$  changing from  $-\infty$  to  $+\infty$  (circle of infinite radius) is a circle, as illustrated by Fig. 2.3 for the particular case  $M = 3$ .



**Figure 2.3** Complex plane of  $\omega C_3 Z_p(Qp)$ . Notice that this representation is no longer valid for  $Qp \rightarrow \pm\infty$ , since it assumes that  $|p| \ll 1$ .

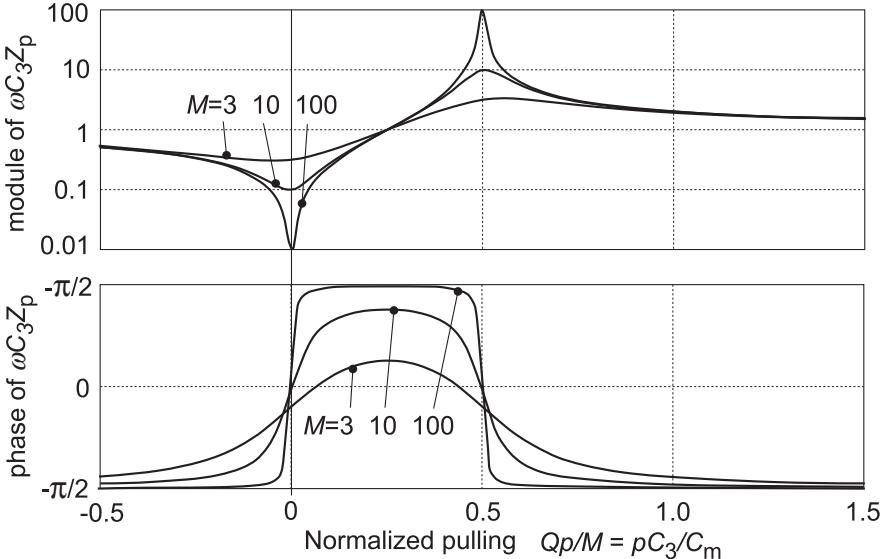
This circle of radius  $M/2$  is centered at  $(M/2; -j)$ . Since  $M > 2$  in this example, the circle crosses the real axis at points S and P corresponding to the series and parallel resonance frequencies given by (2.13). The maximum inductive (normalized) impedance (positive imaginary value) is  $M/2 - 1$  and occurs at  $Qp = (M - 1)/2$ . The maximum resistive component of the (normalized) impedance is  $M$  and occurs at  $Qp = M/2$ . Notice that the circular locus is no longer valid for  $p \rightarrow \pm\infty$ , since  $\omega$  is no longer constant. The minimum module of the impedance (min) occurs for a slightly negative value of  $Qp$ . The maximum module (max) is larger by  $M$  (diameter of the circle).

A small value of  $M$  was chosen in Fig. 2.3 in order to make the various points on the circle visible. For larger (and more realistic) values of  $M$ , this circle becomes much larger and almost centered on the real axis. The evolution of the module and phase of  $Z_p(p)$  for increasing values of  $M$  is shown in Fig. 2.4.

As can be seen, for  $M \gg 2$  the values of  $p$  at series and parallel resonance tend to 0, respectively  $M/2Q = C_m/2C_3$ , in accordance with (2.13). The corresponding values of  $Z_p$  tend to

$$Z_p = \frac{1}{\omega C_3 M} = R_m \quad \text{at series resonance} \quad (2.16)$$

$$Z_p = \frac{M}{\omega C_3} = M^2 R_m \quad \text{at parallel resonance.} \quad (2.17)$$



**Figure 2.4** Module and phase of  $Z_p$  vs. normalized frequency pulling  $pC_3/C_m$ .

According to (2.14), (2.15) and (2.9), the exact series and parallel resonance frequencies depend on the electrical capacitance  $C_3$  and the quality factor  $Q$ . The calculation of these sensitivities yields:

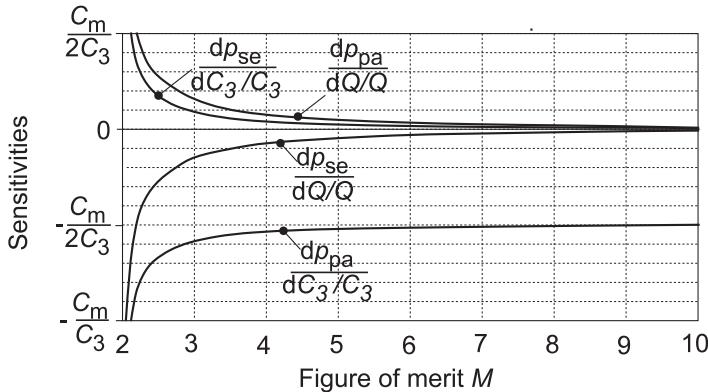
$$\frac{dp_{se}}{dC_3/C_3} = \frac{C_m}{4C_3} \left[ \frac{M}{\sqrt{M^2 - 4}} - 1 \right] \rightarrow \frac{C_m}{2M^2C_3} \text{ for } M \gg 1, \quad (2.18)$$

$$\frac{dp_{pa}}{dC_3/C_3} = -\frac{C_m}{4C_3} \left[ \frac{M}{\sqrt{M^2 - 4}} + 1 \right] \rightarrow -\frac{C_m}{2C_3} \text{ for } M \gg 1, \quad (2.19)$$

$$\frac{dp_{pa}}{dQ/Q} = -\frac{dp_{se}}{dQ/Q} = \frac{C_m}{C_3} \frac{1}{M\sqrt{M^2 - 4}} \rightarrow \frac{C_m}{M^2C_3} \text{ for } M \gg 1. \quad (2.20)$$

These sensitivities are plotted in Fig. 2.5 as functions of the figure of merit  $M$ . As can be seen, they become rapidly negligible for  $M \gg 1$ , except that of  $p_{pa}$  which tend to  $C_m/2C_3$ . Indeed, the parallel resonance frequency depends on the series connection of  $C_m$  and  $C_3$ .

If  $M$  is sufficiently larger than 2, the series resonance frequency becomes independent of the electrical capacitance and of the factor of quality  $Q$ . The latter point is important, since some quartz resonators may have a mechanical frequency  $\omega_m$  very constant with temperature variations, but large variations of their quality factor.



**Figure 2.5** Sensitivities of  $p_{se}$  and  $p_{pa}$  to  $C_3$  and  $Q$ .

In order to have a high value of  $M$ , the coupling factor  $C_m/C_3$  of the resonator should be sufficiently large according to (2.9). Hence, its intrinsic value itself  $C_m/C_{12}$  should already be sufficiently large, since  $C_3 > C_{12}$  due to additional parasitic capacitances in the circuit. The figure of merit is further degraded if one of the two “hot” terminals of the resonator is grounded, as in “1-pin” oscillators: indeed, either  $C_{10}$  or  $C_{20}$  is then connected in parallel with  $C_3$ .

As will be explained later in Chapter 4, the minimization of  $C_3$  is also useful to prevent harmonic currents to flow between nodes 1 and 2, in order to minimize the effect of nonlinearities on the frequency of oscillation.

If the resonator is used as just a dipole, then capacitors  $C_{10}$ ,  $C_{20}$  and  $C_{12}$  of Fig. 2.2(a) merge into the single parallel capacitance  $C_0$  defined by (2.1). The corresponding figure of merit is then

$$M_{D0} = \frac{1}{\omega C_0 R_m} = \frac{QC_m}{C_0}. \quad (2.21)$$

In practice, some additional parasitic capacitors will be added to the intrinsic capacitors of the resonators, and the total parallel capacitance  $C_P$  is somewhat larger than  $C_0$ , resulting in a figure of merit

$$M_D \triangleq \frac{1}{\omega C_P R_m} = \frac{QC_m}{C_P}. \quad (2.22)$$

## 2.4 Mechanical Energy and Power Dissipation

Since the quality factor is very large, the energy  $E_m$  of mechanic oscillation is almost constant along each period. It is simply exchanged from kinetic energy to potential energy. It is all kinetic energy at the peaks of velocity, and all potential energy at the peaks of amplitude.

Since the motional current  $I_m$  represents the mechanical velocity and  $L_m$  represent the equivalent mass moving at this velocity,  $E_m$  is equal to the peak value of the kinetic energy

$$E_m = \frac{L_m |I_m|^2}{2} = \frac{|I_m|^2}{2\omega^2 C_m} = \frac{Q R_m |I_m|^2}{2\omega}, \quad (2.23)$$

where the second form is obtained by introducing (2.2) and the third form by means of (2.3).

Since this energy is proportional to the square of the amplitude, it should be limited to avoid destruction and limit nonlinear effects and aging. But it should be much larger than the noise energy, in order to limit the phase noise, as will be discussed in Section 3.7.

The motional current is sinusoidal, with an RMS value  $|I_m|/\sqrt{2}$ . The power dissipated in the resonator is thus given by

$$P_m = \frac{R_m |I_m|^2}{2} = \frac{|I_m|^2}{2\omega Q C_m}. \quad (2.24)$$

This power must be provided by the sustaining circuit in order to maintain the amplitude of oscillation. Otherwise, at each period of oscillation  $2\pi/\omega$ , the energy would be reduced by

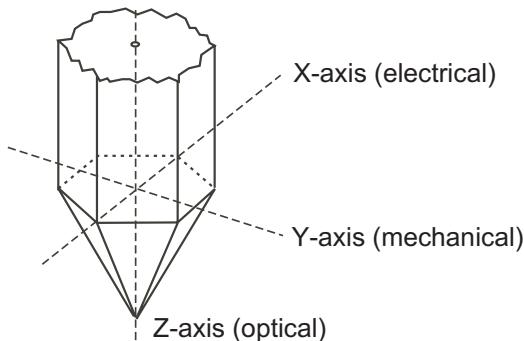
$$\Delta E_m = \frac{2\pi P_m}{\omega} = \frac{|I_m|^2}{2\omega^2 C_m} \cdot \frac{2\pi}{Q} = \frac{2\pi}{Q} E_m. \quad (2.25)$$

According to (2.23) and (2.24),  $E_m$  and  $P_m$  can be calculated as soon as  $|I_m|$  is known.

## 2.5 Various Types of Quartz Resonators

Quartz is monocrystal of  $\text{SiO}_2$  that has an hexagonal structure with 3 main axes, as illustrated in Fig. 2.6 [9]. The optical axis Z passes through the apex of the crystal. The electrical axis X is a set of three axes perpendicular to Z

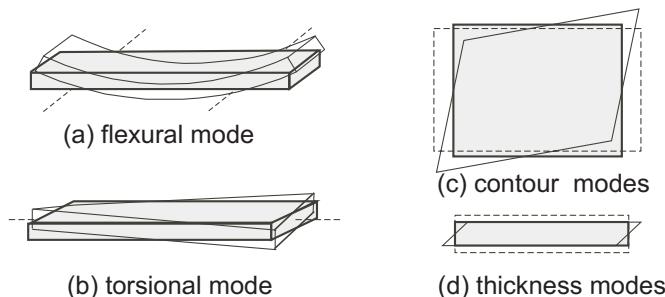
that pass through the corners of the crystal. The mechanical axis Y is a set of three axes that are perpendicular to Z and to the faces of the crystal. The electromechanical transducing property comes from the fact that an electrical field applied along one of the X axes produces a mechanical stress in the direction of the perpendicular Y axis.



**Figure 2.6** Schematic view of a quartz crystal.

Many types of quartz resonators have been developed along the years. They are essentially differentiated by their mode of oscillation, and by the orientation of their cut with respect to the axes. A precise choice of orientation for a given mode is essential to control the variation of the resonant frequency  $\omega_m$  with that of the temperature.

The variety of possible modes of oscillation is depicted in Fig. 2.7. Each of them corresponds to a practical range of frequency.



**Figure 2.7** Possible modes of oscillation of a quartz resonator.

The flexural mode of Fig. 2.7(a) provides the lowest possible frequencies (down to a few kHz). To minimize losses, it is suspended at its two nodes of

oscillation. The electric field is applied by deposited metallic electrodes. The pattern of these electrodes is optimized to maximize the coupling  $C_m/C_{12}$  for the expected fundamental mode. The temperature dependency is a square law of about  $-35 \cdot 10^{-9} / ^\circ\text{C}^2$  that can be centered at the middle of the temperature range. A vacuum package is needed to obtain a large value of quality factor. This is the type of quartz used for the very first quartz wristwatch in the 60's, with a frequency of 8 kHz [5]. To further reduce its size, the flexural mode resonator can be split into two parallel bars supported by a foot. It becomes a tuning fork resonator [10]. Modern tuning fork resonators are fabricated in a batch process by using the patterning and etching techniques developed for integrated circuits. Their tiny 32 kHz version has become a standard for most electronic watches.

For the same dimensions, the torsional mode depicted in Fig. 2.7(b) resonates at a higher frequency. It can be applied to a tuning fork as well.

Contour modes are obtained by a plate that oscillates within its own plane, as shown by Fig. 2.7(c) (generically, they include the length-mode oscillation of a bar). Resonant frequencies are higher than for the flexural and torsional modes. Best among a large variety of known cuts, the GT-cut [11] eliminates the first, second and third order terms in the variation of  $\omega_m$  with temperature. The residual variation is of the order of 2 ppm in a  $100^\circ\text{C}$  range. But this cut requires a very precise control of the dimensions of the plate, and is therefore very expensive. A less critical solution called the ZT-cut that can be produced in batch was developed more recently [12]. It cancels the first and second order terms, leaving a third order term of only  $55 \cdot 10^{-12} / ^\circ\text{C}^3$ .

High frequencies are obtained by plates resonating in thickness modes as illustrated in Fig. 2.7(d). The most frequent is the AT-cut, that resonates in the thickness shear mode, with a frequency variation of 20 to 100 ppm in a  $100^\circ\text{C}$  temperature range. Since the frequency is inversely proportional to the thickness of the plate, very high frequencies are obtained by thinning the vibrating center area of the plate in an "inverted mesa" structure. Fundamental frequencies as high as 250 MHz can then be reached. Harmonic frequencies (overtones) may be used, but their coupling  $C_m/C_{12}$  is always smaller than that for the fundamental.

## 2.6 MEM Resonators

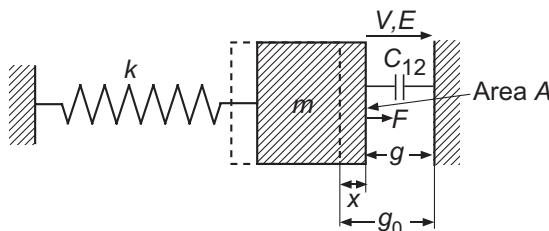
### 2.6.1 Basic Generic Structure

Very small resonators can be fabricated by using the modern etching techniques that have been developed by the microelectronics industry. For compatibility with integrated circuits, these micro-electro-mechanical (MEM) resonators can be made of polysilicon glass, of aluminum or of silicon itself. The latter exhibits excellent mechanical characteristics, in particular a very high intrinsic quality factor.

However, these material are not piezoelectric, hence the resonator must be combined with an electromechanical transducer.

The transducer may be a layer of piezoelectric material deposited on the resonator, together with electrodes. The equivalent circuit is then qualitatively the same as that of the quartz resonator illustrated in Fig. 2.2. The coupling factor  $C_m/C_{12}$  is reduced by the fact that the transducer only represents a small volume of the resonator, but this may be compensated by using a piezoelectric material with a higher coupling coefficient than that of the quartz. It is thus possible to obtain a sufficiently high value of the intrinsic figure of merit defined by (2.10). The capacitance  $C_{12}$  of the transducer should be large enough to limit the reduction of the figure of merit  $M$  defined by (2.9) by parasitic capacitors.

Another interesting solution that avoids the need for piezoelectric material is to use an electrostatic transducer. Consider the lumped spring-mass equivalent of such a MEM resonator shown in Fig. 2.8 with its capacitive transducer.



**Figure 2.8** Spring-mass equivalent of a MEM resonator with electrostatic transduction.

The equivalent mass of the resonator is  $m$  and  $k$  is the stiffness of the spring. The angular frequency of mechanical resonance is then given by

$$\omega_m = \sqrt{k/m}, \quad (2.26)$$

whereas the electrical capacitance of the transducer is

$$C_{12} = A\epsilon_0/g, \quad (2.27)$$

where  $A$  is the area,  $g$  is the gap and  $\epsilon_0$  the permittivity of free space.

Statically, the force  $F$  due to the electrical field should compensate the force  $kx$  of the spring for any value of  $x$ , hence:

$$F = QE = C_{12}V^2/g = A\epsilon_0V^2/g^2, \quad (2.28)$$

For a small variation  $\delta V$  of the voltage  $V$  around its DC value  $V_0$ , the variation of the force is

$$\delta F = 2A\epsilon_0V_0\delta V/g^2, \quad (2.29)$$

which moves the mass by

$$\delta x = \eta_d \delta F/k, \quad (2.30)$$

where  $\eta_d \leq 1$  is a measure of the efficiency of the force to displace the mass, that depends on the mode of oscillation considered ( $\eta_d = 1$  in the schematic case of Fig. 2.8). The corresponding variation of the stored mechanical energy  $E_m$  is then

$$\delta E_m = \frac{1}{2}\delta F \cdot \delta x = \frac{\eta_d \delta F^2}{2k} = \underbrace{\frac{2\eta_d A^2 \epsilon_0^2 V_0^2}{kg^4}}_{C_m/2} \delta V^2. \quad (2.31)$$

The value of the motional capacitor is then given by

$$C_m = \frac{4\eta_d A^2 \epsilon_0^2 V_0^2}{kg^4}. \quad (2.32)$$

The intrinsic figure of merit of the resonator is then obtained by combining (2.32) and (2.27):

$$M_0 = \frac{QC_m}{C_{12}} = \frac{4\eta_d QA\epsilon_0 V_0^2}{kg^3}, \quad (2.33)$$

or, by replacing the elastic constant by the mass according to (2.26)

$$M_0 = \frac{4\eta_d QA\epsilon_0 V_0^2}{m\omega_m^2 g^3}. \quad (2.34)$$

It can be increased by decreasing the gap or by increasing the bias voltage  $V_0$ . However, the latter is limited by the effect of electrostatic pulling. Indeed,

since  $V$  creates a force  $F$  that moves the mass by a distance  $x$ , the gap  $g$  is reduced with respect to its unbiased value  $g_0$  and (2.28) can be rewritten as

$$F = \frac{A\epsilon_0 V^2}{(g_0 - x)^2} = kx/\eta_s, \quad (2.35)$$

where  $\eta_s$  is a measure the efficiency of the force to statically displace the mass ( $\eta_s = 1$  in the schematic case of Fig. 2.8). By introducing the normalized position  $\xi = x/g_0$ , this equation becomes

$$\xi(1-\xi)^2 = \frac{\eta_s A \epsilon_0}{kg_0^3} V^2 \quad \text{or} \quad V = \sqrt{\frac{kg_0^3}{\eta_s A \epsilon_0}} (1-\xi) \sqrt{\xi}. \quad (2.36)$$

The system becomes unstable when  $\xi$  reaches the limit value  $\xi_l$  for which  $dV/d\xi = 0$ ; indeed, for  $\xi > \xi_l$ , the electrostatic force increases faster than the force of the spring and the mass moves to  $x = g_0$ . This critical value is reached for

$$\frac{dV}{d\xi}|_{\xi=\xi_l} = 0 \quad \text{giving} \quad \xi_l = 1/3. \quad (2.37)$$

Introducing this value in (2.36) gives the limit value  $V_l$  of  $V$

$$V_l = \sqrt{\frac{4kg_0^3}{27\eta_s A \epsilon_0}}, \quad (2.38)$$

or, by replacing  $k$  by  $m$  according to (2.26)

$$V_l = \omega_m \sqrt{\frac{4mg_0^3}{27\eta_s A \epsilon_0}}. \quad (2.39)$$

The bias voltage  $V_0$  can only be some fraction of this limit voltage:

$$V_0 = \alpha V_l \quad \text{with} \quad \alpha < 1. \quad (2.40)$$

By introducing (2.40) and (2.38) in (2.33), we obtain an interesting expression for the all-important figure of merit:

$$M_0 = \frac{QC_m}{C_{12}} = \frac{16}{27} \cdot \frac{\eta_d}{\eta_s} \alpha^2 Q \frac{g_0^3}{g^3} \cong \frac{16}{27} \cdot \frac{\eta_d}{\eta_s} \alpha^2 Q \quad (2.41)$$

where the second expression is a good approximation if  $\alpha \ll 1$ . Thus, for a given ratio  $\eta_d/\eta_s$  (which depends on the structure of the resonator), the

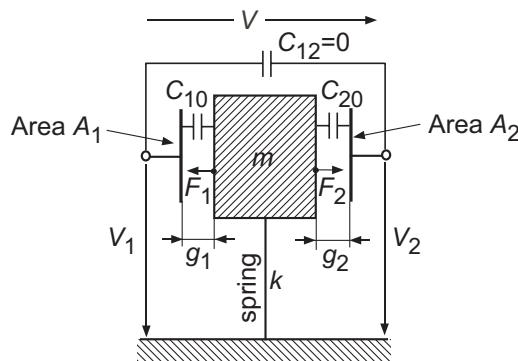
intrinsic figure of merit *only depends* on the quality factor and on the fraction  $\alpha$  of the limit voltage at which the device is biased. The square of this fraction is the equivalent of the coupling factor of piezoelectric resonators.

According to (2.39), the limit voltage is proportional to the frequency and increases with  $g_0^{3/2}$  and  $m^{1/2}$ . It can be decreased by increasing the area  $A$  of the transducer.

For a given frequency, the impedance level (and the value of motional resistor  $R_m$  for a given value of  $Q$ ) is inversely proportional to  $C_{12}$  given by (2.27). Hence, it decreases as  $g/A$ . Because of the small value of area  $A$  possible with a thin resonator and of the difficulty to reduce the gap  $g$  much below  $1\text{ }\mu\text{m}$ , the value of  $C_{12}$  is expected to be at least one order of magnitude smaller than for quartz resonators.

## 2.6.2 Symmetrical Transducers

In many practical cases, the metallic MEM resonator is grounded and is driven by two electrostatic transducers operating in opposite phase according to the spring-mass equivalent depicted in Fig. 2.9. The spring of stiffness  $k$  is here represented by a massless flexible blade.



**Figure 2.9** Spring-mass equivalent with symmetrical electrostatic transduction.

Using (2.28), the forces produced by the two transducers are given by

$$F_1 = A_1 \epsilon_0 V_1^2 / g_1^2 \text{ and } F_2 = A_2 \epsilon_0 V_2^2 / g_2^2. \quad (2.42)$$

The variation of net force  $F_1 - F_2$  produced by small variations of  $V_1$  and  $V_2$  around their bias values  $V_{10}$  and  $V_{20}$  is thus

$$\delta F = \delta F_1 - \delta F_2 = 2\epsilon_0 \left( \frac{A_1 V_{01}}{g_1^2} \delta V_1 - \frac{A_2 V_{02}}{g_2^2} \delta V_2 \right). \quad (2.43)$$

Let us assume that the bias situation is adjusted for no net force by imposing

$$\frac{A_1 V_{01}}{g_1^2} = \frac{A_2 V_{02}}{g_2^2} = \frac{AV_0}{g^2}. \quad (2.44)$$

Then

$$\delta F = 2A\epsilon_0 V_0 (\delta V_1 - \delta V_2)/g^2, \quad (2.45)$$

This result is identical to (2.29), since  $\delta V_1 - \delta V_2 = \delta V$ . Therefore, (2.31) also applies to this symmetrical transducer, for which the motional capacitor is also given by (2.32).

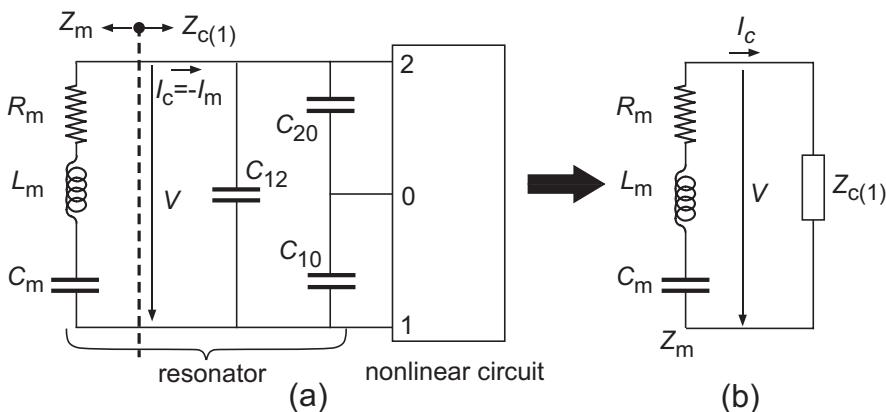
However, there is a major important difference with respect to the non symmetrical case. Indeed, since the body of the resonator is grounded, no capacitive coupling exists between nodes 1 and 2 in Fig. 2.2(a), hence  $C_{12} = 0$ . The intrinsic figure of merit  $M_0$  is therefore infinite and the overall figure of merit  $M$  defined by (2.9) is only limited by all parasitic capacitors contributing to  $C_3$ .

# Chapter 3

## General Theory of High-Q Oscillators

### 3.1 General Form of the Oscillator

In order to sustain the oscillation of the resonator, it must be combined with a circuit to form a full oscillator, as illustrated in Fig. 3.1(a).



**Figure 3.1** General form of an oscillator: (a) combination of the resonator with a nonlinear circuit ; (b) splitting into motional impedance  $Z_m$  and circuit impedance  $Z_{c(1)}$ .

It is important to point-out that the *circuit must be nonlinear*, in order to impose the level of oscillation. Indeed, a linear circuit would be independ-

ent of the amplitude and would therefore not be capable of controlling this amplitude.

Now, as discussed in Chapter 2, the current  $I_m$  flowing through the motional impedance  $Z_m$  is always sinusoidal, thanks to the high value of quality factor  $Q$ . Therefore the best way to analyze the behavior of the oscillator, while including the necessary nonlinearity of the circuit, is to split it conceptually into the motional impedance  $Z_m$  and a circuit impedance containing all electronic components, including capacitors  $C_{12}$ ,  $C_{10}$  and  $C_{20}$  of the resonator, as depicted in Fig. 3.1(b) [13, 14]. The current flowing through the electronic part  $I_c = -I_m$  is then also sinusoidal.

Since  $I_c$  is sinusoidal, no energy can be exchanged with the circuit at multiples of the oscillating frequency (harmonics). The nonlinear circuit can therefore be characterized by its impedance  $Z_{c(1)}$  for the fundamental frequency defined by

$$Z_{c(1)} = \frac{V_{(1)}}{I_c}, \quad (3.1)$$

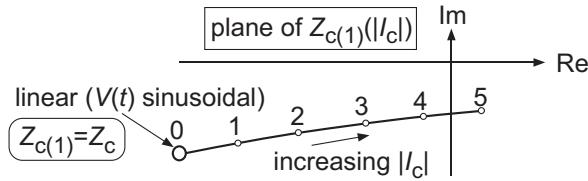
where  $I_c$  is the complex value of the sinusoidal current, and  $V_{(1)}$  the corresponding complex value of the *fundamental component* of voltage  $V$ . Since the circuit is nonlinear  $Z_{c(1)} = Z_{c(1)}(|I_c|)$ : it is a *function of the amplitude* oscillation  $|I_c|$ . But it is practically *independent of p*  $\ll 1$ . It should be mentioned that this approach is a particular case of the general approach of oscillators proposed by H.J. Reich (see Section 75 of [15]).

In general, the locus of  $Z_{c(1)}(|I_c|)$  cannot be calculated analytically. But it can be obtained by means of a circuit simulator according to the following procedure:

- (a) The circuit is first fully described including its bias.
- (b) A source of sinusoidal current of amplitude  $|I_{c1}|$  is connected across terminals 1 and 2.
- (c) The resulting stationary voltage  $V(t)$  is calculated by the simulator.
- (d) The fundamental component  $V_{(1)}$  of  $V(t)$  is calculated by Fourier analysis and  $Z_{c(1)}(|I_{c1}|)$  is calculated according to (3.1).
- (e) A new value  $|I_{c2}|$  of the current source is selected and the process is iterated from step (c).

The result is the locus of  $Z_{c(1)}(|I_c|)$  in the complex plane as illustrated by the qualitative example of Fig. 3.2. In this putative example,  $Z_{c(1)}$  has been calculated (according to the above procedure) for 6 increasing values of  $|I_c|$  corresponding to points 0 to 5.

As long as the sinusoidal current is small enough, the circuit remains linear and the voltage  $V(t)$  remains sinusoidal with a complex value  $V_{(1)} = V$ .



**Figure 3.2** Qualitative example of the locus of  $Z_{c(1)}(|I_c|)$ .

This corresponds to point 0, where  $Z_{c(1)}$  is identical to the small-signal impedance  $Z_c$  of the circuit. The real part of  $Z_c$  should be negative (as is the case in this example) to be able to compensate the losses of the resonator.

When the current is large enough to produce harmonic components of  $V(t)$ , the amplitude  $|V_{(1)}|$  of its fundamental component is normally progressively reduced, thereby reducing the negative real part of  $Z_{c(1)}$ , as is the case for points 1 to 4.

Too much current may produce so much nonlinearities that the real part of  $Z_{c(1)}$  becomes positive, as shown by point 5.

In this example, the imaginary part of  $Z_{c(1)}$  is negative, and corresponds to a circuit that contains only capacitors (functional or parasitic). Notice that, as shown in this example, this imaginary value is usually also affected by nonlinear effects.

### 3.2 Stable Oscillation

With the definition of  $Z_{c(1)}$  introduced in the previous section, the equivalent circuit of the full oscillator can be represented by the resonant circuit shown in Fig. 3.3(a).

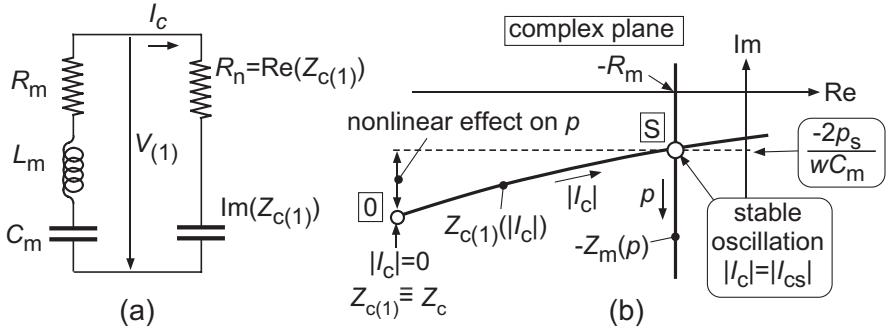
Let us define the negative resistance provided by the circuit

$$R_n \triangleq \text{Re}(Z_{c(1)}). \quad (3.2)$$

The total resistance is thus  $R_m + R_n$ . It can easily be shown that any existing oscillation will therefore decay exponentially with a time constant

$$\tau \triangleq \frac{-2L_m}{R_m + R_n}. \quad (3.3)$$

But if this net resistance is negative, the value of  $\tau$  is positive and the amplitude grows exponentially. Thus, stable oscillation is obtained for



**Figure 3.3** Oscillation: (a) equivalent circuit ; (b) intersection of the locus of  $Z_{c(1)}(|I_c|)$  with that of  $-Z_m(p)$ .

$$R_n = \text{Re}(Z_{c(1)}) = -R_m \quad \text{corresponding to } \tau = \infty. \quad (3.4)$$

At that point, the imaginary parts must also balance each other, thus the general condition for stable oscillation is simply given by

$$Z_{c(1)}(|I_c|) = -Z_m(p), \quad (3.5)$$

that is at the intersection point S of the locus of  $Z_{c(1)}(|I_c|)$  with that of  $-Z_m(p)$ , as illustrated in Fig. 3.3(b). According to (2.8), the locus of  $-Z_m(p)$  is a vertical line at the distance  $-R_m$  from the imaginary axis.

At point S, the stable amplitude of motional current has the value

$$|I_{ms}| = |I_{cs}| = |I_c|_S \quad (3.6)$$

Equating the imaginary part of  $Z_{c(1)}$  at point S with that of  $-Z_m$  expressed by (2.8) gives the amount of frequency pulling at stable oscillation

$$p_s = -\frac{\omega C_m}{2} \text{Im}(Z_{c(1)}|_S). \quad (3.7)$$

This relation provides the exact relative difference between the frequency of oscillation and the mechanical resonant frequency of the resonator. The effect of nonlinearities on the amount of frequency pulling is shown in Fig. 3.3(b) as the difference between the imaginary parts of  $Z_{c(1)}$  at point S and at point 0 (linear case). It would be zero if the locus of  $Z_{c(1)}(|I_c|)$  would be an horizontal line.

### 3.3 Critical Condition for Oscillation and Linear Approximation

The *critical condition for oscillation* occurs when points S and O coincide in Fig. 3.3(b), corresponding to  $Z_{c(1)} \equiv Z_c$ . It is thus simply expressed as

$$Z_c = -Z_m(p), \quad (3.8)$$

or, by separating the real and imaginary parts and according to (2.8)

$$\text{Re}(Z_c) = -\text{Re}(Z_m) = -R_m, \quad (3.9)$$

and

$$\text{Im}(Z_c) = -\text{Im}(Z_m) = -\frac{2p_c}{\omega C_m}, \quad (3.10)$$

where  $p_c$  is the amount of frequency pulling at the critical condition for oscillation.

Although these equations are only strictly valid at the verge of oscillation, when the amplitude is so small that the circuit remains linear, equations (3.8) to (3.10) can be used for a *linear approximation* of the real nonlinear case. In particular, equation 3.10 can be used to obtain an approximative value of frequency pulling  $p_s$  for larger amplitudes. This approximation gives a negligible error if the circuit is designed to eliminate the effect of nonlinearities on the frequency pulling  $p$  (see Fig. 3.3(b)).

### 3.4 Amplitude Limitation

As already pointed out, any oscillator must be nonlinear, in order to define the amplitude of oscillation. The resonator itself should be kept in its linear range of operation, in order to avoid aging or even destruction. Hence, the nonlinearity must be provided by the circuit. This nonlinearity must cause a progressive reduction of the negative resistance with the increase of oscillation current, which can be expressed as

$$R_n = R_{n0}F(|I_c|) \quad (3.11)$$

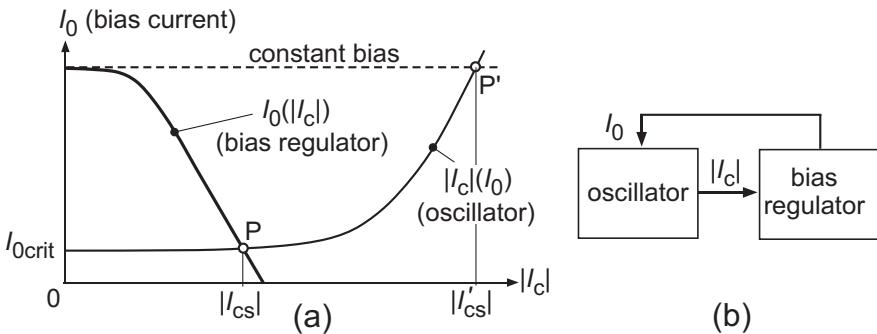
where  $F(|I_c|)$  is a monotonously decreasing function with  $F(0) = 1$ , and

$$R_{n0} = \text{Re}(Z_c) \quad (3.12)$$

is the real part of the impedance of the linear circuit.

If the circuit is designed with a fixed amount of bias current, the amplitude limitation will be caused by instantaneous nonlinearities. These nonlinearities will reduce the amount of negative resistance by increasing the losses, while creating harmonic components of voltages. Intermodulation of these components will eventually create a new fundamental component of  $I_c$  with a different phase, which will affect the imaginary part of  $Z_{c(1)}$  and therefore  $p_s$ .

This problem can be solved by using a bias regulator as illustrated by Fig. 3.4. Instead of maintaining a fixed value of bias current  $I_0$ , the bias regulator reduces this current as the amplitude increases, as shown by the curve  $I_0(|I_c|)$  in Fig. 3.4(a).



**Figure 3.4** Amplitude limitation by bias regulator; (a) qualitative transfer function; (b) closed loop system.

For the oscillator itself, the critical condition is reached for a value  $I_{0crit}$  of  $I_0$ . For any slight increase of  $I_0$  above this value the oscillation grows, until it is limited by nonlinear effects. A further growth of the oscillation requires more bias current, as illustrated by the curve  $|I_c|(I_0)$ .

When the two blocks are connected in a closed loop as shown by Fig. 3.4(b), stable oscillation is given by the intersection point P of the two transfer functions. The amplitude  $|I_{cs}|$  can be controlled to impose  $I_0$  just above  $I_{0crit}$ , thereby producing a negligible amount of voltage distortion across the resonator.

Without regulator, and with the same start-up bias current, the amplitude would be stabilized at point P' by instantaneous nonlinearities (voltage distortion).

### 3.5 Start-up of Oscillation

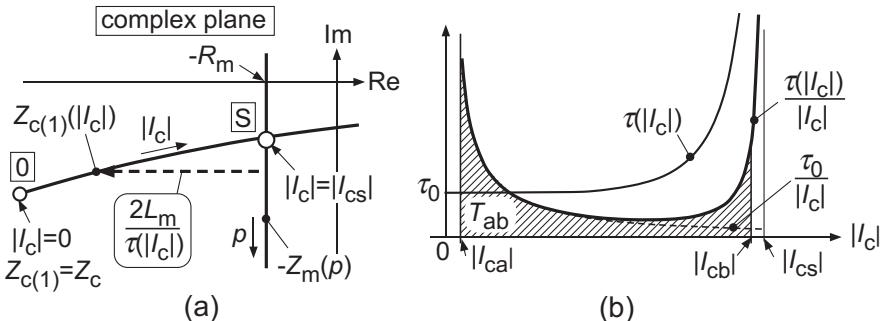
As already established from Fig. 3.3(a), any existing motional current of amplitude  $|I_{ca}|$  will grow exponentially according to

$$|I_c| = |I_{ca}| \exp \frac{t}{\tau} \quad (3.13)$$

where  $\tau$  is the time constant given by (3.3). By differentiation

$$\frac{dt}{d|I_c|} = \frac{\tau(|I_c|)}{|I_c|} \quad (3.14)$$

The value of  $2L_m/\tau$  can be obtained graphically as illustrated in Fig. 3.5(a). As long as the current is small enough, the circuit remains linear with an



**Figure 3.5** Start-up of oscillation: (a) variation of time constant  $\tau$ ; (b) evaluation of the start-up time.

impedance  $Z_c$  (point 0) and this value is maximum, corresponding to a minimum value  $\tau_0$  of the time constant given by

$$\tau_0 = \frac{-2L_m}{R_m + R_{n0}} = \frac{2}{\omega^2 C_m} \cdot \frac{1}{-R_{n0} - R_m}. \quad (3.15)$$

When nonlinearities start to appear, the margin of negative resistance decreases, thereby increasing the time constant as shown in Fig. 3.5(b). This time constant become infinite at stable oscillation.

By introducing the expression (3.11) of  $R_n(|I_c|)$  in (3.3), we obtain

$$\tau = \frac{-2L_m}{R_m + R_{n0}F(|I_c|)}, \quad (3.16)$$

which should be infinite for  $|I_c| = |I_{cs}|$  (stable oscillation). Hence, by using (3.15)

$$\tau = \tau_0 \frac{1 - F(|I_{cs}|)}{F(|I_c|) - F(|I_{cs}|)}. \quad (3.17)$$

Introducing this result in (3.14) and integrating gives the time  $T_{ab}$  needed for the oscillation to grow from  $|I_{ca}|$  to  $|I_{cb}|$ :

$$T_{ab} = \tau_0 \int_{|I_{ca}|}^{|I_{cb}|} \frac{1}{|I_c|} \frac{1 - F(|I_{cs}|)}{F(|I_c|) - F(|I_{cs}|)} d|I_c|, \quad (3.18)$$

represented by the hatched area in Fig. 3.5(b). This time tends to infinity for  $|I_{cb}| = |I_{cs}|$  (fully stable oscillation).

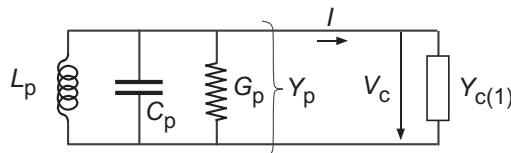
In absence of oscillation, some energy is provided by the thermal energy  $kT$ , corresponding to a total noise current of variance  $kT/L_m$ ; therefore the lower limit of  $|I_{ca}|$  is

$$|I_{ca}| > \sqrt{kT/L_m} = \omega \sqrt{kTC_m}. \quad (3.19)$$

In practice, for quartz resonators, the start-up time to reach 90% of the stable amplitude ranges from 7 to 15  $\tau_0$ .

### 3.6 Duality

The general analysis developed in the previous sections can be applied to all oscillators based on a series resonant circuit. It is applicable to high- $Q$  parallel resonant circuits as well, by using the duality principle, as shown by Fig. 3.6.



**Figure 3.6** Oscillator using a high- $Q$  parallel resonant circuit.

The motional impedance  $Z_m$  becomes a parallel admittance

$$Y_p = G_p + j \frac{2p}{\omega L_p} = G_p + 2jp\omega C_p \quad (3.20)$$

The circuit impedance for the fundamental frequency  $Z_{c(1)}$  becomes a circuit admittance for the fundamental frequency

$$Y_{c(1)} = \frac{I_{(1)}}{V_c}, \quad (3.21)$$

where  $V_c$  is the complex value of the *sinusoidal* voltage across the parallel resonant circuit and  $I_{(1)}$  is the corresponding complex value of the fundamental component of the distorted circuit current  $I$ . The condition for stable oscillation (3.5) becomes

$$Y_{c(1)}(|V_c|) = -Y_p(p), \quad (3.22)$$

provided the amplitude and phase stability conditions (1.2) and (1.3) are fulfilled.

High- $Q$  parallel resonant circuits are difficult to obtain by electrical components only, especially with small physical dimensions. But they can be part of the equivalent circuit of high- $Q$  mechanical resonators associated with an electromagnetic transducer. The other parts of this equivalent circuit are then embedded in the circuit admittance  $Y_{c(1)}$ .

## 3.7 Basic Considerations on Phase Noise

### 3.7.1 Linear Circuit

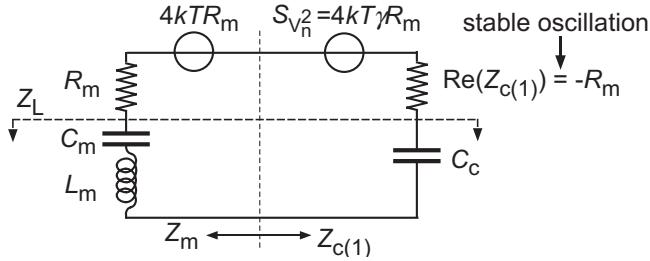
For a linear circuit with time invariant noise sources, the phase noise of the oscillator may be analyzed by using the classical approach proposed by Leeson [16]. The equivalent circuit of the oscillator at stable oscillation is shown in Fig. 3.7.

A noise voltage of spectral density  $4kTR_m$  is associated with the motional resistance  $R_m$  of the resonator. At stable oscillation, the real part of the circuit impedance is equal to  $-R_m$  and can therefore be associated with an open-loop noise voltage  $V_n$  of spectral density  $S_{V_n^2}$  that can be expressed as

$$S_{V_n^2} = 4kT\gamma R_m, \quad (3.23)$$

where  $\gamma$  is the noise excess factor that depends on the detailed noise contributions of the circuit.

At stable oscillation, the impedance  $Z_L$  that loads the total noise voltage source of spectral density  $4kTR_m(1 + \gamma)$  is that of the lossless series resonator



**Figure 3.7** Equivalent circuit at stable oscillation for noise calculation.  $Z_L$  is the impedance loading the total noise voltage source of spectral density  $4kTR_m(1 + \gamma)$ .

formed by the motional components  $L_m$  and  $C_m$  of the resonator and by the capacitance  $C_c$  of the circuit.

The frequency of stable oscillation is given by

$$\omega_s = 2\pi f_s = \frac{1}{\sqrt{L_m C_t}}, \quad (3.24)$$

where  $C_t$  is the series connection of  $C_m$  and  $C_c$ .

The loading impedance for noise sources may then be expressed as

$$Z_L = j\omega_n L_m + \frac{1}{j\omega_n C_t} = j\omega_n L_m \frac{(\omega_n + \omega_s)(\omega_n - \omega_s)}{\omega_n^2}, \quad (3.25)$$

where  $\omega_n$  is the frequency at which noise is considered.

For  $(\omega_n - \omega_s)/\omega_s \ll 1$ , this impedance is almost exactly given by

$$Z_L = 2j\omega L_m \frac{\omega_n - \omega_s}{\omega} = 2jQR_m \frac{\omega_n - \omega_s}{\omega}, \quad (3.26)$$

where the second form is obtained by applying (2.3).

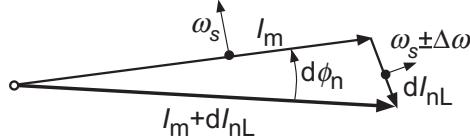
The power spectral density of the noise current  $I_{nL}$  circulating in the loop is then

$$S_{I_{nL}^2} = \frac{4kT(1 + \gamma)R_m}{|Z_L|^2} = \frac{(1 + \gamma)kT}{Q^2 R_m} \left( \frac{\omega}{\Delta\omega} \right)^2, \quad (3.27)$$

where  $\Delta\omega$  is the offset of the noise frequency  $\omega_n$  with respect to the stable frequency of oscillation  $\omega_s$ :

$$\Delta\omega = |\omega_n - \omega_s|. \quad (3.28)$$

This noise current is added to the oscillation (motional) current  $I_m$ . For an elementary bandwidth  $df$  at angular frequency  $\omega$ , the corresponding complex phasors are illustrated in Fig. 3.8 at a given instant. Notice that the length of the noise phasor  $dI_n$  is a random value of variance  $S_{I_{nL}^2} df$ .



**Figure 3.8** Complex phasors of oscillation current  $I_m$  and elementary noise currents  $dI_{nL}$  at a given instant.

Now, since the noise current is small compared to the oscillation current, the power spectrum of the phase noise  $\phi_n$  can be expressed as

$$S_{\phi_n^2} = \frac{1}{2} \frac{S_{I_{nL}^2}}{(|I_m|/\sqrt{2})^2} = \frac{(1+\gamma)kT\omega^2}{Q^2R_m|I_m|^2\Delta\omega^2}, \quad (3.29)$$

where  $|I_m|/\sqrt{2}$  is the RMS value of the oscillation current. The factor  $1/2$  introduced in the first form is due to the fact that only half of the noise power is translated into phase noise, whereas the other half becomes amplitude noise.

Using expressions (2.24) and (2.23) of the power  $P_m$  dissipated in the resonator and of the energy  $E_m$  of oscillation, (3.29) becomes

$$S_{\phi_n^2} = \frac{(1+\gamma)kT\omega^2}{2Q^2P_m\Delta\omega^2} = \frac{(1+\gamma)kT\omega}{2QE_m\Delta\omega^2}. \quad (3.30)$$

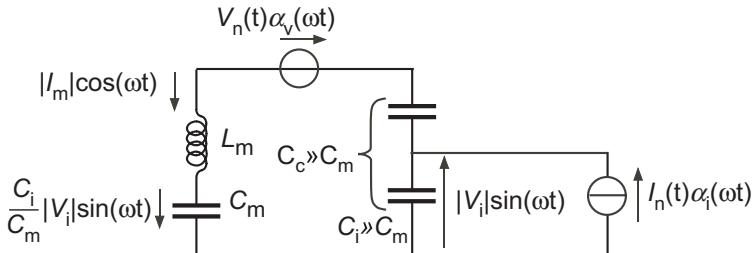
The power spectrum of phase noise is thus proportional to  $1/\Delta\omega^2$ . However, this law is no longer valid when  $\Delta\omega$  tends to zero, because of the unavoidable mechanism of amplitude limitation.

For a given oscillation frequency  $\omega$ ,  $S_{\phi_n^2}$  is inversely proportional to the energy of oscillation  $E_m$  and to the quality factor  $Q$ .

### 3.7.2 Nonlinear Time Variant Circuit

The results derived in the previous section are only valid if the amplitude of oscillation is so small that the circuit remains linear and the noise sources are time invariant. But to reduce the phase noise, the amplitude must be increased to increase the motional current  $I_m$  and the energy of oscillation  $E_m$ . As a result, the circuit becomes nonlinear and the noise produced by the active devices becomes cyclostationary (even when it remains white). Phase noise can then be analyzed by using the impulse sensitivity function (ISF) introduced by Hadjimiri and Lee [6].

Consider the equivalent circuit of a quartz oscillator at stable oscillation illustrated in Fig. 3.9 It is a second order system with two state variables.



**Figure 3.9** Equivalent circuit of the oscillator for nonlinear analysis of phase noise.

One is the current flowing through the single inductance  $L_m$ . The second is the total voltage across the capacitances that exchange their energy with the inductance at every cycle of oscillation. The loss resistance  $R_m$  and the active device that compensates for it are ignored in a first approximation. Indeed, the energy dissipation in  $R_m$  during each cycle is  $2\pi/Q$  the total energy of oscillation, thus a very small percentage for large values of the quality factor  $Q$ . Therefore, we will simplify the analysis by assuming that the voltage across all the capacitors of the loop is *perfectly sinusoidal*.

Two separate noise sources are shown, both of them possibly cyclostationary. A voltage noise source in series with the inductance and composed of a stationary noise  $V_n(t)$  multiplied by a modulation function  $\alpha_v$  synchronous with the current. A current noise source in parallel with a capacitor  $C_i \gg C_m$  and composed of a stationary noise  $I_n(t)$  multiplied by a modulation function  $\alpha_i$  synchronous with the voltage.

According to [6], the phase noise spectrum density resulting from the white noise voltage  $V_n(t)$  of spectral density  $S_{V_n^2}$  can be expressed as

$$S_{\phi_n^2} = \frac{\bar{\Gamma}_v^2 \cdot S_{V_n^2}}{2(L_m|I_m|)^2 \Delta \omega^2}, \quad (3.31)$$

where  $\bar{\Gamma}_v$  is the effective *impulse sensitivity function* (ISF) given, for the *sinusoidal* current  $|I_m| \cos \phi$ , by

$$\bar{\Gamma}_v = -\sin \phi \cdot \alpha_v(\phi). \quad (3.32)$$

The product  $L_m|I_m|$  is the maximum magnetic flux in the inductor and  $\Delta \omega$  is given by (3.28).

With a white noise current  $I_n(t)$  source of spectral density  $S_{I_n^2}$ , the phase noise spectrum is

$$S_{\phi_n^2} = \frac{\bar{\Gamma}_i^2 \cdot S_{I_n^2}}{2(C_i|V_i|)^2 \Delta \omega^2} \cdot \left( \frac{C_m}{C_i} \right)^2, \quad (3.33)$$

where  $\bar{\Gamma}_i$  is the effective impulse sensitivity function given, for the *sinusoidal* voltage  $|V_i| \sin \phi$ , by

$$\bar{\Gamma}_i = \cos \phi \cdot \alpha_i(\phi). \quad (3.34)$$

The product  $C_i|V_i|$  is the maximum charge in capacitors  $C_i$  and  $C_m$ . The factor  $(C_m/C_i)$  corresponds to the fraction of the total voltage (state variable) that appears across  $C_i \gg C_m$ .

According to [6], the phase noise spectrum density due to a  $1/f$  flicker noise voltage source of spectral density  $K_{fv}/\omega_n$  is

$$S_{\phi_n^2} = \frac{\bar{\Gamma}_v^2 \cdot K_{fv}}{(L_m|I_m|)^2 \Delta \omega^3}. \quad (3.35)$$

The effective ISF  $\bar{\Gamma}_v$  is still defined by (3.32), but may be *different* from that for white noise.

With a flicker noise current source of spectral density  $K_{fi}/\omega_n$ , the phase noise spectral density is

$$S_{\phi_n^2} = \frac{\bar{\Gamma}_i^2 \cdot K_{fi}}{(C_i|V_i|)^2 \Delta \omega^3} \cdot \left( \frac{C_m}{C_i} \right)^2. \quad (3.36)$$

The effective ISF  $\bar{\Gamma}_i$  is still defined by (3.34), but may be *different* from that for white noise.

The phase noise spectrum density due to white noise sources is proportional to  $1/\Delta \omega^2$  and to the mean square value of the corresponding ISF. For  $1/f$  flicker noise sources, this density is proportional  $1/\Delta \omega^3$  and to the square of the mean value of the effective ISF.

The phase noise due to the motional resistance  $R_m$  alone can be obtained by introducing the corresponding thermal noise density  $S_{V_n^2} = 4kT R_m$  in (3.31), with  $\alpha_v = 1$  in the expression (3.32) of the effective ISF. Replacing  $L_m$  by  $QR_m/\omega$  gives

$$S_{\phi_n^2} = \frac{kT \omega^2}{Q^2 R_m |I_m|^2 \Delta \omega^2}, \quad (3.37)$$

which is identical to (3.29) for  $\gamma = 0$  (no contribution of the circuit).

If the noise current across capacitor  $C_i$  comes from the active device that compensates for losses, the current delivered by this active device produces a change in voltage  $V_i$ . During each period of oscillation, the relative change of energy in  $C_i$  to compensate the loss in  $R_m$  must be

$$\frac{\Delta E_c}{E_c} = \frac{2\pi C_i}{QC_m}, \quad (3.38)$$

which is  $C_i/C_m$  larger than the relative loss in the resonator itself. Thus, even with a large value of  $Q$ , the assumption of a sinusoidal voltage  $V_i$  across  $C_1$  becomes a *crude approximation* when the current is strongly distorted. Without this approximation, the ISF is much more complicated and a precise calculation of the phase noise can only be obtained by numerical computation.

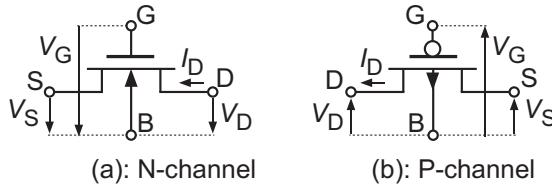
### 3.8 Model of the MOS Transistor

The most important nonlinear devices in the circuit are the transistors. Hence their proper modelling is essential for nonlinear analyses. Fig. 3.10 shows the symbols used for N-channel and P-channel MOS transistors. Unlike bipolar transistors, MOS transistors are *4-terminal devices*. They have an intrinsic symmetry that can be preserved in the model by using the local substrate B as the reference for voltages. This local substrate is normally common to all transistors of the same type, and is connected to one rail of the power supply (negative rail for the N-channel p-substrate, positive rail for the P-channel n-substate). Hence, the corresponding electrode is usually not represented in schematics, except when it is connected differently.

The static drain current  $I_D$  of a MOS transistor depends on the values of the gate voltage  $V_G$ , the source voltage  $V_S$  and the drain voltage  $V_D$ , all of them being defined with respect to the substrate B of the transistor, as defined in Fig. 3.10. According to the EKV model [17, 18], it can be expressed as the difference of two values of a function  $I(V, V_G)$ , for  $V = V_S$  and  $V = V_D$ :

$$I_D = I(V_S, V_G) - I(V_D, V_G) = I_F - I_R, \quad (3.39)$$

where the first term is called the forward (component of) current  $I_F$  and the second the reverse (component of) current  $I_R$ . A simple but sufficiently accurate expression of these symmetrical currents valid in a wide range of current is [19]



**Figure 3.10** Definitions of currents and voltages; (a) for a N-channel transistor; (b) for a P-channel transistor.

$$I_{F(R)} = I_{spec} \left[ \ln \left( 1 + \exp \frac{V_G - V_{T0} - nV_{S(D)}}{2nU_T} \right) \right]^2, \quad (3.40)$$

where  $V_{T0}$  is the threshold voltage (its value for  $V_S = 0$ ),  $n$  the slope factor (value ranging from 1.1 to 1.6) and  $U_T = kT/q$  the thermodynamic voltage (26 mV at 27°C).  $I_{spec}$  is the specific current of the transistor given by

$$I_{spec} \triangleq 2n\mu C_{ox} \frac{W}{L} U_T^2, \quad (3.41)$$

which depends on the mobility  $\mu$  of carriers in the channel, on the gate oxide capacitance per unit area  $C_{ox}$ , and on the width-to-length ratio of the channel  $W/L$ .

In normal situations ( $V_D > V_S$  for a N-channel transistor), the forward current  $I_F = I(V_S, V_G)$  is larger than the reverse current  $I_R = I(V_D, V_G)$ .

If  $I_R \ll I_F$  the transistor is in *saturation*. The drain current becomes independent on the drain voltage since  $I_F$  only depends on  $V_G$  and  $V_S$ .

If  $I_{F(R)} \ll I_{spec}$ , this component is in *weak inversion* and can be simplified to

$$I_{F(R)} = I_{spec} \exp \frac{V_G - V_{T0} - nV_{S(D)}}{nU_T} \quad (3.42)$$

If  $I_{F(R)} \gg I_{spec}$ , it is in *strong inversion* and can be simplified to

$$I_{F(R)} = I_{spec} \left( \frac{V_G - V_{T0} - nV_{S(D)}}{2nU_T} \right)^2 = \frac{\beta}{2n} (V_G - V_{T0} - nV_{S(D)})^2, \quad (3.43)$$

where

$$\beta \triangleq \mu C_{ox} W/L \quad (3.44)$$

is the transfer parameter that can be used instead of  $I_{spec}$ .

The amount of inversion in the transistor can be characterized by the inversion coefficient  $IC$  defined as

$$IC \triangleq \max \left( \frac{I_F}{I_{spec}}, \frac{I_R}{I_{spec}} \right). \quad (3.45)$$

If  $I_F$  and  $I_R$  are both in weak inversion, the transistor itself operates in weak inversion. Saturation ( $I_R \ll I_F$ ) is then obtained for

$$V_D > V_{Dsat} = V_S + 4U_T \text{ to } 6U_T \quad (\text{saturation in weak inversion}). \quad (3.46)$$

The transistor operates in strong inversion as soon as one of components is in strong inversion. Saturation ( $I_R \ll I_F$ ) is then approximately obtained for

$$V_D > V_{Dsat} = \frac{V_G - V_{T0}}{n} = V_S + 2U_T \sqrt{IC} \quad (\text{satur. in strong inversion}). \quad (3.47)$$

For small variations of the control voltages around a bias point, the device remains linear and the variation of drain current can be expressed as

$$\delta I_D = -G_{ms} \delta V_S + G_{md} \delta V_D + G_m \delta V_G, \quad (3.48)$$

where  $G_m$  is the usual small-signal gate transconductance, and  $G_{ms(d)}$  is the small-signal source (drain) transconductance given by

$$G_{ms(d)} \triangleq -\frac{dI_{F(R)}}{dV_{S(D)}}. \quad (3.49)$$

It can be obtained by differentiation of (3.40):

$$G_{ms(d)} = \frac{\sqrt{I_{F(R)} I_{spec}}}{U_T} \left( 1 - e^{-\sqrt{I_{F(R)}/I_{spec}}} \right). \quad (3.50)$$

For strong inversion, it can be expressed as a function of the voltages by differentiation of (3.43), or as a function of currents from (3.50) with  $I_{F(R)} \gg 1$ :

$$G_{ms(d)} = \beta(V_G - V_{T0} - nV_{S(D)}) = \frac{\sqrt{I_{F(R)} I_{spec}}}{U_T}. \quad (3.51)$$

In weak inversion, (3.50) becomes simply

$$G_{ms(d)} = I_{F(R)}/U_T \quad (3.52)$$

It can easily be shown that the more usual gate transconductance is related to  $G_{ms}$  and  $G_{md}$  by

$$G_m \triangleq \frac{dI_D}{dV_G} = \frac{G_{ms} - G_{md}}{n}. \quad (3.53)$$

Hence in weak inversion:

$$G_m = \frac{1}{n} \left[ \frac{I_F}{U_T} - \frac{I_R}{U_T} \right] = \frac{I_D}{nU_T} \quad (\text{weak inversion}). \quad (3.54)$$

In *forward saturation*,  $I_R \ll I_F$  and  $G_{md} \ll G_{ms}$ . The general expression of the gate transconductance is then:

$$G_m = \frac{G_{ms}}{n} = \frac{\sqrt{I_D I_{spec}}}{nU_T} \left( 1 - e^{-\sqrt{I_D/I_{spec}}} \right) = \frac{I_D}{nU_T} \cdot \frac{1 - e^{-\sqrt{IC}}}{\sqrt{IC}}, \quad (3.55)$$

In *strong inversion*, it is reduced to

$$G_m = \frac{G_{ms}}{n} = \frac{\sqrt{I_D I_{spec}}}{nU_T} = \frac{I_D}{nU_T \sqrt{IC}} = \sqrt{\frac{2\beta I_D}{n}} = \frac{\beta}{n} (V_G - V_{T0} - nV_S). \quad (3.56)$$

It should be mentioned that even in saturation (i.e. for  $I_D = I_F$ ), the drain current  $I_D$  remains slightly dependent on the drain voltage, due to the phenomenon of channel length modulation. This effect can be modelled by a source-to-drain conductance  $G_{ds}$  that can be approximated by

$$G_{ds} = I_D/V_M, \quad (3.57)$$

where  $V_M$  is the channel length modulation voltage, proportional to the length  $L$  of the channel. If the channel is not too short (sufficiently longer than the minimum length allowed by the process), the intrinsic voltage gain of the transistor in saturation

$$A_{V0} \triangleq G_m/G_{ds} = \frac{V_M}{nU_T} \cdot \frac{1 - e^{-\sqrt{IC}}}{\sqrt{IC}} \quad (3.58)$$

is much larger than unity but is reduced for large values of  $IC$ .

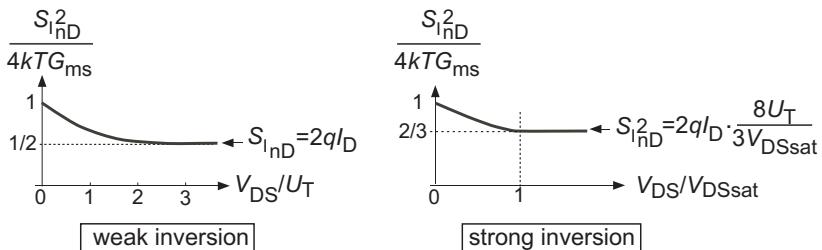
The most fundamental source of noise of the transistor is its channel noise. It can be modelled by a noise current of spectral density  $S_{I_{nD}^2}$  independent of the frequency, which is added to the drain current. For  $V_D = V_S$  (thus for  $I_D = I_F - I_R = 0$ ), this noise is the thermal noise of the channel conductance equal to  $G_{ms}$  and  $G_{md}$ :

$$S_{I_{nD}^2} = 4kTG_{ms} \quad \text{for } V_D = V_S \quad (3.59)$$

As shown by Fig. 3.11, when the transistor is saturated this spectral density is reduced to

$$S_{I_{nD}^2} = 4kT\gamma G_{ms} = 4kT\gamma nG_m \quad \text{in saturation,} \quad (3.60)$$

where  $\gamma$  is the channel noise excess factor of the transistor, of value 1/2 in weak inversion and 2/3 in strong inversion. These values can be higher in short-channel devices. Notice that in saturation, the noise of the transistor



**Figure 3.11** Variation of the channel noise spectral density with increasing  $V_{DS} = V_D - V_S$ .

in weak inversion is the shot noise associated with the forward current  $I_F = I_D \gg I_R$ :

$$S_{I_{nD}^2} = 2qI_D \quad (\text{saturated weak inversion}). \quad (3.61)$$

In strong inversion, the noise for a given value of drain current is reduced, since  $G_{ms}/I_D$  is reduced.

Flicker noise due to carrier trapping and mobility fluctuations is also important in MOS transistors. Since its spectral density is inversely proportional to the frequency, it dominates at low frequencies. It can be approximated by a noise voltage  $V_{nG}$  added to the gate voltage, with a spectral density  $S_{V_{nG}^2}$  given by

$$S_{V_{nG}^2} = \frac{K_f}{\omega_n} \quad \text{where } K_f \propto \frac{1}{WL}. \quad (3.62)$$

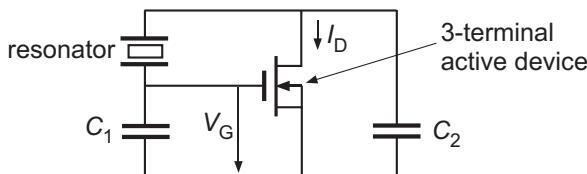
This noise voltage is minimum in moderate inversion and increases only slowly in weak and in strong inversion. Hence, in a first approximation,  $K_f$  can be considered *constant*. In a given process, it can be reduced by increasing the gate area  $WL$ .

# Chapter 4

## Theory of the Pierce Oscillator

### 4.1 Basic Circuit

The simplest possible oscillator uses a single active device to generate the required negative resistance. If no inductance is available, the only possibility is the 3-point oscillator developed in 1923 by G. W. Pierce [2, 3]. The principle of this oscillator is depicted in Fig. 4.1. The active device is assumed to



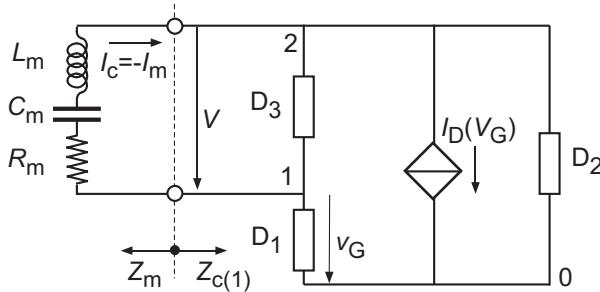
**Figure 4.1** Basic 3-point Pierce oscillator (biasing omitted).

be a MOS transistor, but it could be a bipolar transistor as well. The source of the MOS transistor is connected to its substrate, to make it a 3-terminal device. The bias circuitry needed to activate the transistor is omitted here. Capacitors  $C_1$  and  $C_2$  connected between gate and source, respectively drain and source, are functional: they must have finite values in order to obtain a negative resistance across the motional impedance of the resonator.

This oscillator is very similar to the Clapp circuit [20], except for the presence of the unavoidable capacitance in parallel with the series motional

resonator. The presence of this capacitance has important implications on the behavior of the circuit.

Assuming that the transistor is saturated, the equivalent circuit of this structure is that of Fig. 4.2.



**Figure 4.2** General equivalent circuit of the Pierce oscillator.

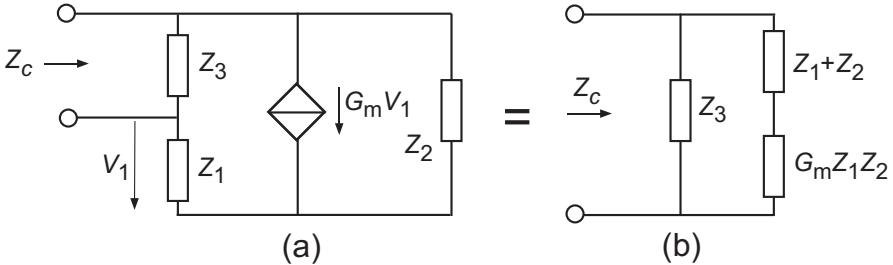
The active part of the saturated transistor is represented by the voltage-controlled current source  $I_D(V_G)$ . The three passive dipoles  $D_1$ ,  $D_2$  and  $D_3$  include all remaining parts of the equivalent circuit of the transistor itself, as well as the functional and parasitic components of the biasing circuitry. Moreover, in accordance with Fig. 3.1(a),  $D_3$  includes the capacitance  $C_{12}$  of the quartz resonator, whereas  $C_{10}$  and  $C_{20}$  are included in  $D_1$  and  $D_2$  respectively. Notice that each of these three dipole may be nonlinear, as for example  $D_1$  if the active device is a bipolar transistor. The rest of the circuit is the motional impedance  $Z_m$  of the resonator.

## 4.2 Linear Analysis

### 4.2.1 Linearized Circuit

Linearizing the general equivalent circuit of Fig. 4.2 around a biasing point of the active device results in the equivalent circuit of impedance  $Z_c$  depicted in Fig. 4.3(a). Assuming no inductance dominates, the three passive dipoles  $D_i$  becomes linear complex impedance given by

$$Z_i = \frac{1}{G_i + j\omega C_i}, \quad (4.1)$$



**Figure 4.3** Linearized equivalent circuit of the oscillator.

that are practically independent of slight amount of frequency pulling  $p \ll 1$ . The voltage-controlled current source becomes  $G_m V_1$ , where  $G_m$  is the gate transconductance of the transistor and  $V_1$  the complex voltage across  $Z_1$ .

The linear circuit impedance  $Z_c$  can easily be expressed as

$$Z_c = \frac{Z_1 Z_3 + Z_2 Z_3 + G_m Z_1 Z_2 Z_3}{Z_1 + Z_2 + Z_3 + G_m Z_1 Z_2}, \quad (4.2)$$

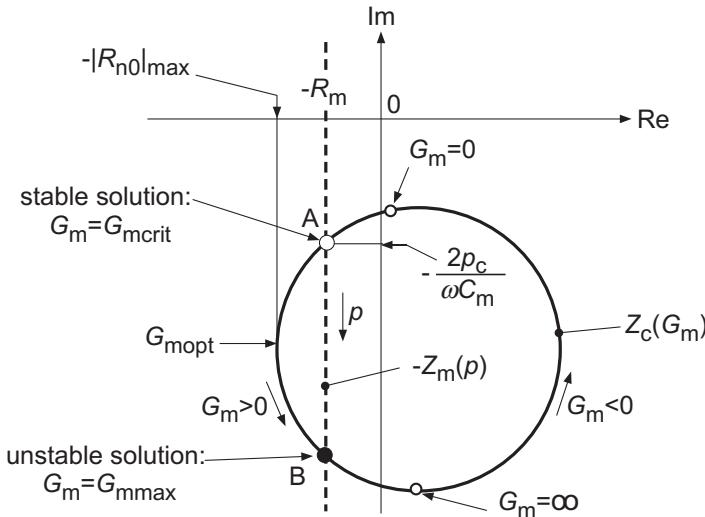
which corresponds to the compact small-signal model of Fig. 4.3(b). The circuit impedance  $Z_c$  is thus a *bilinear function of  $G_m$* . Bilinear functions transform circles into circles in the complex plane [8], therefore the locus of  $Z_c(G_m)$  for  $G_m$  changing from  $-\infty$  to  $+\infty$  (circle of infinite radius) is a circle, as illustrated in Fig. 4.4. It should not be confused with the locus of  $Z_{c(1)}(|I_c|)$  represented in Fig. 3.3.

Since the reactive components of  $Z_i$  are all capacitive, this circle is located in the lower half of the complex plane (negative imaginary part). The real part of  $Z_c$  can only be negative (providing a negative resistance) when the circuit is made active by a positive value of  $G_m$ . However, the circuit remains passive if  $G_m$  is too small to compensate the losses due to the real parts of  $Z_i$ . Moreover, as can be seen in the figure, it also remains passive if  $G_m$  is *too large*.

The real value of  $Z_c$  is minimum for a particular value  $G_{mopt}$  of transconductance. It is the maximum absolute value of negative resistance  $|R_{n0}|_{max}$  that can be obtained.

The locus of  $-Z_m(p)$  given by (2.8) is plotted in dotted line in the same figure. It is a vertical strait line at distance  $-R_m$  of the imaginary axis.

According to (3.8), the critical condition for oscillation is reached at the intersection of the two loci. For the particular case depicted in Fig. 4.4, there are two solutions labelled A and B. We will show later that solution B is unstable, because it does not fulfill the condition (1.2) for phase stability.



**Figure 4.4** Loci of  $Z_c(G_m)$  and  $-Z_m(p)$  in the complex plane.

The only stable solution is at intersection A, for the particular value  $G_{mcrit}$  of  $G_m$  called *critical transconductance* for oscillation.

If  $G_m$  is increased beyond  $G_{mcrit}$ , the oscillation will start up and grow exponentially with time constant  $\tau_0$  given by (3.15) (as long as the circuit remains linear). A maximum amount of net negative resistance  $R_{n0} + R_m$  is obtained for  $G_m = G_{mopt}$ , corresponding to a minimum value of time constant  $\tau_0$ . If  $G_m$  is increased beyond  $G_{mcrit}$ ,  $\tau_0$  starts increasing again, until it becomes infinite at point B, for  $G_m = G_{mmax}$ .

If the quality factor  $Q$  given by (2.3) decreases, then  $R_m$  increases and the intersection points A and B move to the left. They approach each other, until they merge into a single point, when  $-Z_m(p)$  becomes tangent to  $Z_c(G_m)$ . No solution exists for  $R_m > |R_{n0}|_{max}$ ; no oscillation is then possible, whatever the value of transconductance  $G_m$ .

For the critical condition, the frequency pulling  $p$  takes the value  $p_c$  obtained by equating the imaginary part of  $Z_c$  at point A with that of  $-Z_m$  given by (2.8). This yields

$$p_c = -\frac{\omega C_m}{2} \operatorname{Im}(Z_c|_A). \quad (4.3)$$

Now, it is important to notice that the variation of  $R_m$  due to a variation of quality factor  $Q$  moves the point A not only horizontally, but also *vertically*, proportionally to the slope  $d\operatorname{Im}(Z_c)/d\operatorname{Re}(Z_c)$  at point A. Hence, according to (4.3):

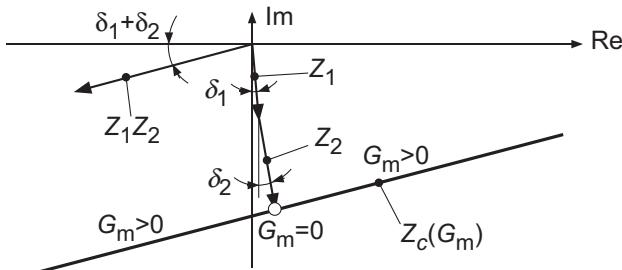
$$\frac{dp_c}{dQ/Q} = -\frac{dp_c}{dR_m/R_m} = -\frac{\omega C_m R_m}{2} \frac{d\text{Im}(Z_c)}{d\text{Re}(Z_c)}|_A = -\frac{1}{2Q} \frac{d\text{Im}(Z_c)}{d\text{Re}(Z_c)}|_A. \quad (4.4)$$

Since, even in good resonators, the quality factor can change by a large amount with temperature variations, this sensitivity to the quality factor should be minimized to avoid a degradation of the frequency stability. This can be obtained by pushing the point A as close as possible to the top of the circle, where the sensitivity is zero (horizontal tangent). Notice that this sensitivity tends to infinity when  $R_m$  approaches  $|R_{n0}|_{max}$ .

The radius of the circle increases with the value of  $Z_3$ . If  $Z_3$  is infinite, then

$$Z_c = Z_1 + Z_2 + G_m Z_1 Z_2 \quad \text{for } Z_3 = \infty \quad (4.5)$$

becomes a *linear function* of  $G_m$ . As illustrated in Fig. 4.5, this corresponds to a circle of infinite radius. The maximum value of  $|R_{n0}|$  is no longer limited,



**Figure 4.5** Locus of  $Z_c(G_m)$  for infinite  $Z_3$ .

and the slope of this strait-line locus would be zero if  $Z_1$  and  $Z_2$  would be purely capacitive. However, if the capacitors have losses represented by their loss angles  $\delta_1$  and  $\delta_2$  as shown in the figure, the locus of  $Z_c(G_m)$  has a slope characterized by an angle  $\delta_1 + \delta_2$ , and some sensitivity of  $p_c$  to  $Q$  remains.

Notice that an infinite value of  $Z_3$  cannot be obtained with an electromechanical resonator. Indeed, since the figure of merit  $M_0$  defined by (2.10) is never infinite, the electrical capacitance  $C_{12}$  always remains as a component of  $Z_3$ . The situation of Fig. 4.5 can be approached by using large values of  $C_1$  and  $C_2$ , in order to obtain  $Z_1 + Z_2 \ll Z_3$  for  $G_m \ll G_{mopt}$ .

### 4.2.2 Lossless Circuit

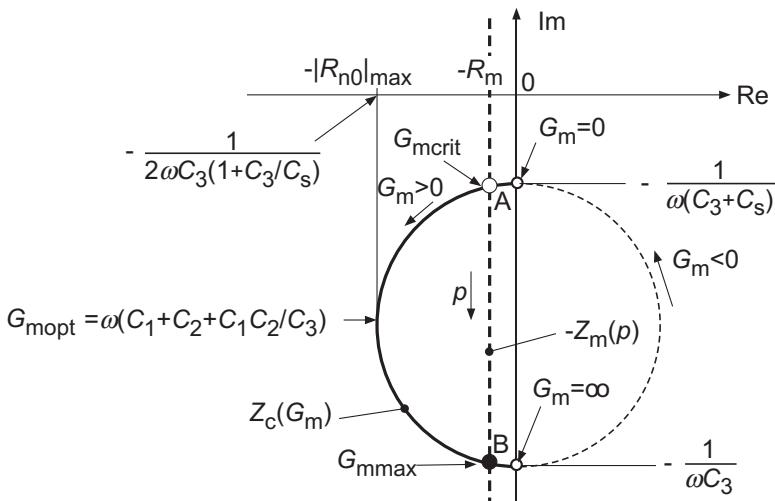
To obtain a maximum activity and a minimum sensitivity of the frequency to the quality factor, the circuit should be made of lossless capacitors, thus

$$Z_i = \frac{1}{j\omega C_i} \quad (4.6)$$

The expression (4.2) of the circuit impedance then becomes

$$Z_c = \frac{-G_m C_1 C_2 - j[\omega(C_1 + C_2)(C_1 C_2 + C_2 C_3 + C_3 C_1) + G_m^2 C_3 / \omega]}{\omega^2 (C_1 C_2 + C_2 C_3 + C_3 C_1)^2 + (G_m C_3)^2}. \quad (4.7)$$

The locus  $Z_c(G_m)$  of Fig. 4.4 is now centered on the imaginary axis, as shown in Fig. 4.6. The right half of the circle corresponding to negative values of transconductance is of no practical interest. For  $G_m = 0$  the circuit impedance



**Figure 4.6** Loci of  $Z_c(G_m)$  and  $-Z_m(p)$  in the complex plane for a lossless circuit.

is imaginary and has the value

$$Z_c = \frac{-j}{\omega(C_3 + C_s)} \quad \text{for } G_m = 0, \quad (4.8)$$

where  $C_s$  is the series combination of  $C_1$  and  $C_2$ :

$$C_s = \frac{C_1 C_2}{C_1 + C_2} \quad (4.9)$$

It is also imaginary for  $G_m = \infty$  where it has the value

$$Z_c = \frac{-j}{\omega C_3} \quad \text{for } G_m = \infty. \quad (4.10)$$

Some negative resistance is produced for  $0 < G_m < \infty$ , with a maximum given by the radius of the circle. Hence, from (4.8) and (4.10):

$$|R_{n0}|_{max} = \frac{1}{2\omega C_3(1 + C_3/C_s)}. \quad (4.11)$$

The minimum possible value of the start-up time constant  $\tau_0$  can be obtained by introducing this expression in (3.15):

$$\frac{1}{\tau_{0min}} = \omega \left( \frac{C_m}{4C_3(1 + C_3/C_s)} - \frac{1}{2Q} \right) = \frac{\omega}{2Q} \left( \frac{M}{2(1 + C_3/C_s)} - 1 \right), \quad (4.12)$$

where the figure of merit  $M$  is defined by (2.9).

The value of transconductance producing this maximum can be obtained by equating to zero the first derivative of the real part of  $Z_c$  in (4.7). This gives

$$G_{mopt} = \omega \left( C_1 + C_2 + \frac{C_1 C_2}{C_3} \right). \quad (4.13)$$

By using the fact that the locus of  $Z_c(G_m)$  is a centered circle of radius  $|R_{n0}|_{max}$ , and remembering that  $\text{Re}(Z_c) = R_{n0}$ , the imaginary part of the circuit impedance can be expressed as

$$\text{Im}(Z_c) = -\frac{1}{\omega(C_s + C_3)} - |R_{n0}|_{max} \left[ 1 \pm \sqrt{1 - \left( \frac{|R_{n0}|}{|R_{n0}|_{max}} \right)^2} \right], \quad (4.14)$$

whereas the slope of the locus is given by

$$\frac{d\text{Im}(Z_c)}{d\text{Re}(Z_c)} = \frac{\pm 1}{\sqrt{\left( \frac{|R_{n0}|_{max}}{|R_{n0}|} \right)^2 - 1}}. \quad (4.15)$$

It is zero on the imaginary axis ( $|R_{n0}| = 0$ ) and infinite for  $|R_{n0}| = |R_{n0}|_{max}$ .

The locus of  $-Z_m(p)$  is also reported in Fig. 4.6, for a particular value of motional resistance  $R_m$ . A necessary condition for oscillation is that  $R_m = |R_{n0}| < |R_{n0}|_{max}$ . By introducing (4.11), (2.3) and (2.9), this condition can be expressed as

$$M = \frac{QC_m}{C_3} > 2(1 + C_3/C_s) > 2. \quad (4.16)$$

Hence *no oscillation is possible* with the Pierce oscillator if the factor of merit  $M$  of the resonator (and *a fortiori* its intrinsic value  $M_0$ ) is smaller than two. This is because the lumped impedance between the drain and the gate in Fig. 4.1 must become inductive.

Moreover, the condition (4.16) must be fulfilled with a large margin, in order to limit the sensitivity the oscillator frequency to variations of  $Q$ . Thus we shall impose a margin factor

$$K_m \triangleq \frac{|R_{n0}|_{max}}{R_m} = \frac{M}{2(1+C_3/C_s)} \gg 1. \quad (4.17)$$

Then, according to (4.4) and (4.15) the sensitivity at of the frequency at the stable solution A is given

$$\frac{dp_c}{dQ/Q} = \frac{-1}{2Q\sqrt{K_m^2 - 1}}. \quad (4.18)$$

It is drastically degraded when  $K_m$  approaches 1.

The exact amount of frequency pulling at the stable point A is obtained by introducing (4.14) (with the minus sign in the parenthesis) and (4.17) into (4.3), giving

$$p_c = \frac{C_m}{2(C_s + C_3)} + \frac{C_m}{4C_3(1+C_3/C_s)} \left( 1 - \sqrt{1 - \frac{1}{K_m^2}} \right). \quad (4.19)$$

If  $K_m^2 \gg 1$ , this expression can be approximated by

$$p_c \cong \frac{C_m}{2(C_s + C_3)} + \frac{1}{2QM} \left( 1 + \frac{C_3}{C_s} \right). \quad (4.20)$$

Now, since usually  $QM \gg (C_s + C_3)/C_m$ , this result can be further simplified by neglecting the second term:

$$p_c \cong \frac{C_m}{2(C_s + C_3)}. \quad (4.21)$$

The amount of frequency pulling is then independent of the quality factor. The capacitance that is responsible for the frequency pulling, in this case  $C_s + C_3$ , is usually called (in quartz data sheets) the *load capacitance* of the resonator.

The value of transconductance at solutions A and B in Fig. 4.6 is obtained by equating the real part of  $Z_c$  in (4.7) with  $-R_m$  and solving for  $G_m$ . This yields

$$G_m = \frac{C_1 C_2}{2 R_m C_3^2} \left[ 1 \pm \sqrt{1 - \left[ \frac{2}{M} \left( 1 + \frac{C_3}{C_s} \right) \right]^2} \right], \quad (4.22)$$

where the positive sign gives the maximum value (at point B) and the negative sign gives the critical value. According to (4.17) the squared term in the square root is  $1/K_m^2$ . If  $K_m^2 \gg 1$ , this result can be approximated to give the maximum transconductance

$$G_{mmax} \cong \frac{C_1 C_2}{R_m C_3^2} = \frac{\omega C_m C_1 C_2 Q}{C_3^2} = M \frac{\omega C_1 C_2}{C_3}, \quad (4.23)$$

and the critical transconductance (for the lossless circuit)

$$G_{mcrit0} \cong \omega^2 R_m C_1 C_2 (1 + C_3/C_s)^2 = \frac{\omega}{Q C_m} C_1 C_2 (1 + C_3/C_s)^2. \quad (4.24)$$

It is worth noticing that the ratio

$$\frac{G_{mmax}}{G_{mcrit0}} \cong \frac{M^2}{(1 + C_3/C_s)^2} \underset{\text{for } C_3 \ll C_s}{\cong} M^2 \quad (4.25)$$

is essentially dependent on the figure of merit  $M$ .

It is interesting to replace the squared parenthesis in (4.24) by its value obtained from (4.21). The critical transconductance can then be expressed as

$$G_{mcrit0} \cong \frac{\omega C_m}{Q p_c^2} \frac{(C_1 + C_2)^2}{4 C_1 C_2} \underset{\text{for } C_2 = C_1}{=} \frac{\omega C_m}{Q p_c^2}. \quad (4.26)$$

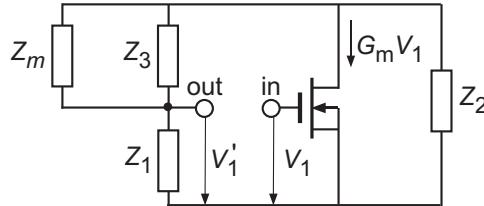
For a given quartz resonator, the critical transconductance is thus inversely proportional to the square of the frequency pulling  $p_c$  and is minimum for  $C_1 = C_2$ . Hence, decreasing the sensitivity of the frequency of oscillation to circuit parameters by decreasing  $p_c$  requires a large increase of bias current. This is especially true if the device is a MOS transistor operated in strong inversion: indeed, the transconductance is then only proportional to the square root of the bias current; decreasing  $p_c$  by a factor 10 would then require 10'000 more current!

For  $C_1 = C_2$  (4.24) becomes

$$G_{mcrit0} \cong \omega^2 R_m (C_1 + 2C_3)^2 = \frac{\omega}{Q C_m} (C_1 + 2C_3)^2. \quad (4.27)$$

### 4.2.3 Phase Stability

In order to verify the phase stability condition (1.2), the overall oscillator can be opened at the gate of the transistor, as illustrated in Fig. 4.7.



**Figure 4.7** Open-loop oscillator for calculation of gain  $G$ .

The open-loop gain  $G$  is then easily calculated to be

$$G = \frac{V'_1}{V_1} = \frac{-G_m Z_1 Z_2}{Z_1 + Z_2 + \frac{Z_3 Z_m}{Z_3 + Z_m}}, \quad (4.28)$$

where  $Z_m$  is given by (2.8) and  $Z_1$  to  $Z_3$  by (4.6) for a lossless oscillator. To simplify the analysis, let us assume that  $|Z_1 + Z_2| \ll |Z_3 Z_m (Z_3 + Z_m)|$  (very large values of  $C_1$  and  $C_2$ ), which should have no effect on the phase stability. The tangent of the argument of  $G$  is then obtained as

$$\tan(\arg G) = \frac{4C_3}{\omega C_m^2 R_m} p^2 - \frac{2p}{\omega C_m R_m} + \omega C_3 R_m, \quad (4.29)$$

the derivative of which is

$$\frac{d(\tan(\arg G))}{dp} = \frac{2}{\omega C_3 R_m} \left( \frac{4pC_3}{C_m} - 1 \right). \quad (4.30)$$

Now, since the sign of  $d(\arg G)/d\omega$  is the same as that of  $d(\tan(\arg G))/dp$ , condition (1.2) becomes

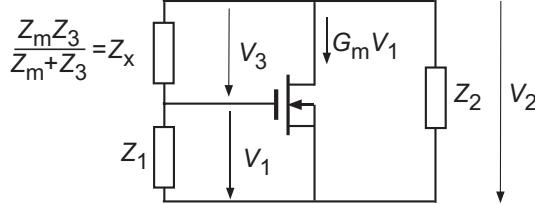
$$\text{stable phase for } p < \frac{C_m}{4C_3} \quad (\text{point A}) \quad (4.31)$$

$$\text{unstable phase for } p > \frac{C_m}{4C_3} \quad (\text{point B}). \quad (4.32)$$

Thus, point A of figures 4.4 and 4.6 is indeed stable, whereas point B is unstable.

#### 4.2.4 Relative Oscillator Voltages

By lumping the parallel impedances  $Z_m$  and  $Z_3$  in to a single impedance  $Z_x$ , the overall oscillator at small signals can be redrawn as shown in Fig. 4.8.



**Figure 4.8** Calculation of voltage ratios.

Now, since  $Z_3$  is already included in  $Z_x$ , at the critical condition (3.8) for oscillation, according to (4.5)

$$Z_x = -Z_c|_{Z_3=\infty} = -(Z_1 + Z_2 + G_{mcrit}Z_1Z_2). \quad (4.33)$$

Voltage ratios can then easily be calculated by means of Fig. 4.8:

$$\frac{V_2}{V_1} = 1 + \frac{Z_x}{Z_1} = -Z_2 \left( \frac{1}{Z_1} + G_{mcrit} \right), \quad (4.34)$$

with a modulus

$$\frac{|V_2|}{|V_1|} = \sqrt{\frac{(G_1 + G_{mcrit})^2 + (\omega C_1)^2}{G_2^2 + (\omega C_2)^2}}, \quad (4.35)$$

and

$$\frac{V_3}{V_1} = \frac{Z_x}{Z_1} = \frac{V_2}{V_1} - 1. \quad (4.36)$$

with a modulus

$$\frac{|V_3|}{|V_1|} = \sqrt{\frac{(G_1 + G_2 + G_{mcrit})^2 + \omega^2(C_1 + C_2)^2}{G_2^2 + (\omega C_2)^2}}. \quad (4.37)$$

For a lossless circuit with a large margin factor  $K_m$ , the critical transconductance is given by (4.24), and the voltage ratio becomes

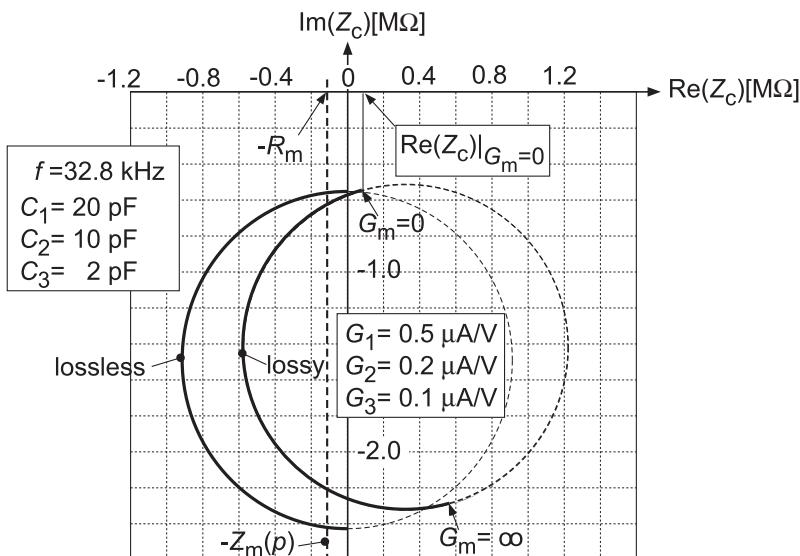
$$\frac{V_2}{V_1} = -\frac{C_1}{C_2} + j \frac{C_1}{QC_m} \left( 1 + \frac{C_3}{C_1} + \frac{C_3}{C_2} \right)^2. \quad (4.38)$$

If  $C_2$  is not too large, the imaginary part of this expression is usually smaller or much smaller than  $C_1/C_2$ . Then, for  $C_1 = C_2$ ,  $V_2 \cong -V_1$  and  $V_3 \cong -2V_1$ .

### 4.2.5 Effect of Losses

#### 4.2.5.1 Numerical Example

The effect of losses on the locus of  $Z_c(G_m)$  is obtained by introducing the full expression of  $Z_1$ ,  $Z_2$  and  $Z_3$  given by (4.1) in the equation (4.2) of  $Z_c$ , which gives a very complicated analytical result. A numerical example is shown in Fig. 4.9 with particular values corresponding to a realistic case of a 32 kHz oscillator with large losses.

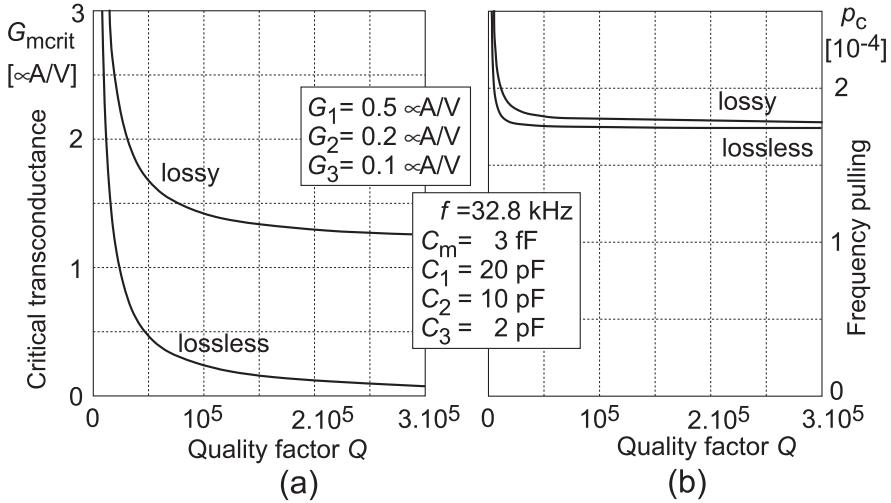


**Figure 4.9** Example of the effect of loss conductance  $G_1$ ,  $G_2$  and  $G_3$  on the locus of  $Z_c(G_m)$ .

As can be seen, the circle is moved to the right of the complex plane, thereby reducing the amount of negative resistance. The corresponding effects on the critical transconductance can be obtained by equating the real part of  $-Z_c(G_m)$  to the motional resistance  $R_m = 1/(\omega C_m Q)$ , thereby providing  $Q(G_m)$ . The result obtained with the same numerical values is shown in Fig. 4.10(a).

Losses result in an increase of the critical transconductance

$$G_{mcrit} = G_{mcrit0} + \Delta G_{mcrit} \quad (4.39)$$



**Figure 4.10** Example of the effect of loss conductance  $G_1, G_2$  and  $G_3$ ; (a) on the critical transconductance; (b) on the amount of frequency pulling.

where  $\Delta G_{m\text{crit}}$  is approximately independent of the quality factor. In this example,  $G_{m\text{crit}}$  is increased by a factor 6 for  $Q = 10^5$ .

The effect of losses on the frequency pulling  $p_c$  calculated by (4.3) is shown in Fig. 4.10(b) for the same numerical values. It is smaller than  $10^{-5}$  for  $Q = 10^5$ . This figure also shows the dependency of  $p_c$  on  $Q$  that was discussed in Section 4.2.1.

#### 4.2.5.2 Approximative Expression for the Increase of $G_m$

An inspection of Fig. 4.9 shows that if the shift of the circle is small with respect to its radius, then the effect of losses is approximately equivalent to an increase  $\Delta R_m$  of the motional resistance given by

$$\Delta R_m = \text{Re}(Z_c)|_{G_m=0}. \quad (4.40)$$

Then, according to (4.24)

$$\Delta G_{m\text{crit}} \cong \omega^2 C_1 C_2 (1 + C_3/C_s)^2 \Delta R_m. \quad (4.41)$$

For  $G_m = 0$ , the expression (4.2) of  $Z_c$  is reduced to

$$|Z_c|_{G_m=0} = \frac{1}{1/(Z_1 + Z_2) + 1/Z_3}. \quad (4.42)$$

If the losses are small with

$$G_i^2 \ll (\omega C_i)^2, \quad (4.43)$$

then

$$\text{Re}(Z_c)|_{G_m=0} = \frac{G_1 C_2^2 + G_2 C_1^2 + G_3 (C_1 + C_2)^2}{\omega^2 (C_1 C_2 + C_2 C_3 + C_3 C_1)^2} \quad (4.44)$$

By introducing (4.40) and (4.44) in (4.41), the increase of critical transconductance due to losses can be approximated by

$$\Delta G_{mcrit} \cong \frac{G_1 C_2^2 + G_2 C_1^2 + G_3 (C_1 + C_2)^2}{C_1 C_2}. \quad (4.45)$$

Notice that this approximation is independent of  $C_3$ . For  $C_1 = C_2$ , it becomes

$$\Delta G_{mcrit} \cong G_1 + G_2 + 4G_3, \quad (4.46)$$

showing the larger effect of the drain-gate conductance  $G_3$ .

#### 4.2.6 Frequency Adjustment

The mechanical resonant frequency  $\omega_m$  of the resonator cannot be adjusted with a precision better than about 10 ppm. It is therefore usually necessary to fine tune the frequency of oscillation by electrically adjusting the amount of frequency pulling  $p$ , given in a good approximation by (4.21).

One possibility would be to adjust capacitor  $C_3$ . However, this is not a good solution, since  $C_3$  should remain as small as possible to maximize the radius of the circular locus of  $Z_c(G_m)$ .

Best would be to adjust  $C_1$  and  $C_2$  while maintaining  $C_1 = C_2$ , since it ensures a minimum of critical transconductance for a given amount of frequency pulling, as expressed by (4.26). It is usually more convenient to adjust only one capacitor.

Now the relative range of frequency adjustment can be expressed as

$$\frac{\omega_{max} - \omega_{min}}{\omega} = p_{max} - p_{min}. \quad (4.47)$$

To increase  $p_{max}$ ,  $C_1$  and/or  $C_2$  must be reduced. This increases the relative importance of parasitic capacitors (usually voltage-dependent) and reduces the radius of the circular locus of  $Z_c(G_m)$ . The frequency stability is therefore degraded. The absolute maximum of  $p$  for stable oscillation is reached at the

point corresponding to  $G_{mopt}$  in Fig. 4.4. Calculation for a lossless circuit (Fig. 4.6) yields

$$p_{maxmax} = \frac{C_m}{2C_3} \left( 1 - \frac{1}{M} \right), \quad (4.48)$$

which is lower than the pulling  $p_{pa}$  at parallel resonance given by (2.15).

According to (4.26), a reduction of  $p_{min}$  increases the critical transconductance and therefore the power consumption of the oscillator. The absolute minimum of  $p$  would be reached for infinite values of  $C_1$  and  $C_2$  (hence infinite critical transconductance) and is equal to its value at series resonance given by (2.14).

The maximum possible range of frequency adjustment is thus limited by considerations on frequency stability and power consumption. In practice, it is never more than a small fraction of  $C_m/(2C_3)$ .

In some applications like time-keeping, the precise adjustment of the oscillator can be replaced by adjusting the ratio of the following frequency division chain. The amount of pulling can then be kept at an optimal value with respect to power consumption and frequency stability.

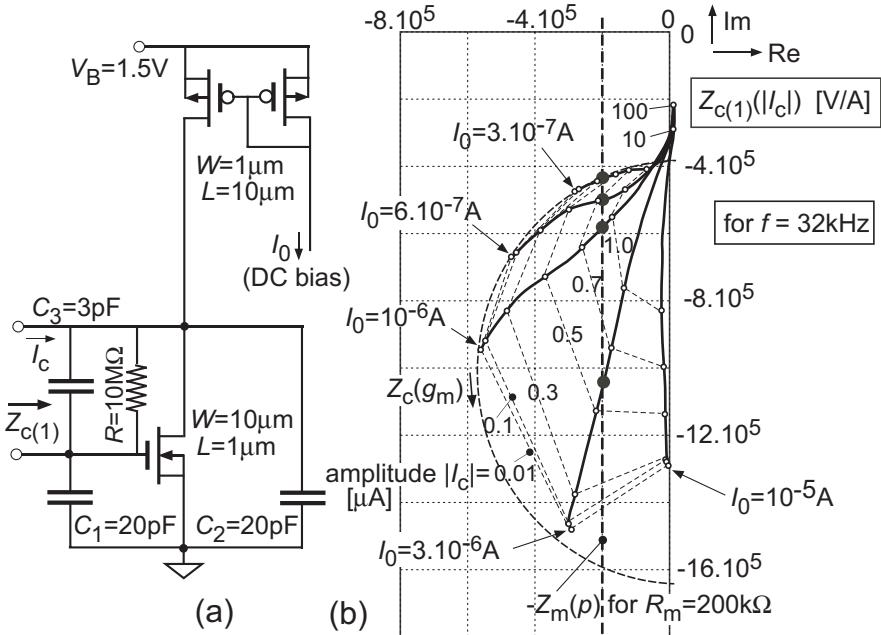
## 4.3 Nonlinear Analysis

### 4.3.1 Numerical Example

As soon as the critical transconductance is exceeded, the amplitude of oscillation increases until it is limited by nonlinear effects. As explained in Section 3.1, these nonlinear effects can be analyzed by computing the circuit impedance for the fundamental frequency  $Z_{c(1)}$  defined by (3.1).

As an example, consider the simple Pierce oscillator circuit shown in Fig. 4.11(a). The active N-channel transistor is biased by means of the current  $I_0$  (mirrored by the P-channel transistors) and the resistor  $R$  connected between drain and gate. The locus of  $Z_{c(1)}(I_c)$  has been calculated according to the procedure introduced in Section 3.1, by using the EKV model [18] of MOS transistors for a standard a  $0.18\mu\text{m}$  process. The extraction of the fundamental component  $V_{(1)}$  of the voltage resulting from the sinusoidal current  $I_c$  forced into the circuit was obtained by simulating an  $LC$  filter tuned at exactly the same frequency.

The results at a frequency of  $32\text{kHz}$  are depicted in Fig. 4.11(b) for several values of bias current  $I_0$ .



**Figure 4.11** Example of nonlinear effects in a Pierce oscillator: (a) Circuit schematic with numerical values; (b) Loci of  $Z_{c(1)}(I_c)$  for several values of bias  $I_0$  at 32 kHz.

The circle in dotted line is the theoretical locus of  $Z_c(G_m)$  for the linear circuit. It includes the losses due to bias resistor  $R$ , but not those due to the output conductance of the transistors.

For a bias current  $I_0 = 0.6\mu\text{A}$ , these additional losses are negligible and the locus of  $Z_{c(1)}(I_c)$  starts on the circle. It remains on the circle ( $Z_{c(1)} = Z_c$ ) as long as the amplitude  $|I_c| \leq 10\text{nA}$ . Indeed, assuming that all the AC current flows through  $C_1$ , 10nA flowing in 20pF produce a voltage of about 5mV, for which the circuit remains linear. For  $|I_c| = 100\text{nA}$ , the circuit is already nonlinear: the locus leaves the circle and the negative resistance is reduced. It is further reduced when the amplitude increases. For  $10\mu\text{A}$  and above, the losses are so high that the real part of  $Z_{c(1)}$  becomes positive (no negative resistance produced by the circuit).

For a bias current  $I_0 = 1\mu\text{A}$ , more negative resistance is produced (close to the maximum possible), but the losses due to the output conductance of the active transistor are no longer negligible: the locus of  $Z_{c(1)}(I_c)$  does not start exactly on the circle.

For  $I_0 = 3\mu\text{A}$ , the linear solution is unstable as established in Section 4.2.3. As a consequence, the slope of the locus starts by being negative before becoming positive but very large. The imaginary part of  $Z_{c(1)}$ , which is proportional to the amount of frequency pulling according to (3.7), becomes very sensitive to the amplitude.

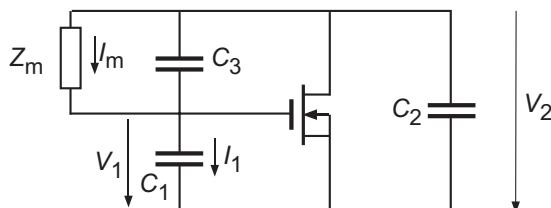
For the extreme case with  $I_0 = 10\mu\text{A}$ , almost no negative resistance is produced and the slope of the locus is almost infinite. The very large losses at low amplitude are due to a lack of saturation of the mirror output (these losses are reduced if the supply voltage is increased).

Now, let us assume that the motional resistance of the resonator  $R_m = 200\text{k}\Omega$ . According to Fig. 3.3(b), the locus of  $Z_m(p)$  is then the vertical line at  $\text{Re}(Z_{c(1)}) = -2 \cdot 10^5 \text{ V/A}$  also shown in Fig. 4.11(b). Stable oscillation is obtained at the intersection of this locus with that of  $Z_{c(1)}(I_c)$  (large black dots). As can be seen in the figure, the imaginary part of  $Z_{c(1)}$  at this intersection, and thus the amount of frequency pulling  $p_s$  at stable oscillation, is very dependent on the bias current  $I_0$ . Furthermore, for large values of  $I_0$  ( $1\mu\text{A}$  and  $3\mu\text{A}$ ), it is also very sensitive to the value of motional resistance  $R_m$  and therefore to the quality factor  $Q$  of the resonator.

This example illustrates the importance of avoiding excessive values of bias current.

### 4.3.2 Distortion of the Gate Voltage

Consider the lossless oscillator circuits for AC components of Fig. 4.12. As



**Figure 4.12** Equivalent circuit of the lossless oscillator for AC components.

derived in Section 4.2.4, the ratio of gate to drain voltages for components at the oscillation frequency is approximately given by

$$V_1/V_2|_F \cong -C_2/C_1. \quad (4.49)$$

But for harmonic components of the drain voltage, the motional impedance  $Z_m$  is almost infinite, therefore the drain to gate voltage ratio is simply given by the capacitive divider  $C_1 - C_3$ :

$$V_1/V_2|_H = \frac{C_3}{C_1 + C_3}. \quad (4.50)$$

The relative attenuation of harmonics is thus

$$\frac{V_1/V_2|_H}{V_1/V_2|_F} \approx \frac{C_3 C_1}{(C_1 + C_3) C_2}. \quad (4.51)$$

Therefore, even if the drain voltage is strongly distorted, the gate voltage can remain sinusoidal if  $C_3 = 0$  (or more generally if  $Z_3 = \infty$ ). Practically, it remains almost sinusoidal if  $C_3 \ll C_2$ .

It must be pointed-out that it is very important to limit the amount of distortion of the gate voltage. Indeed, harmonic components can be intermodulated by the nonlinear transfer function of the transistor, thereby producing an additional fundamental component of drain current. Since the phase of this additional component will be different from that of the main component, the frequency of oscillation will be shifted by nonlinear effects.

For  $Z_3 = \infty$ , the gate signal would remain perfectly sinusoidal, hence the nonlinear transfer function would have no effect on the frequency. Referring to Fig. 3.3(b), this means that the locus of  $Z_{c(1)}(|I_c|)$  would be an horizontal straight line.

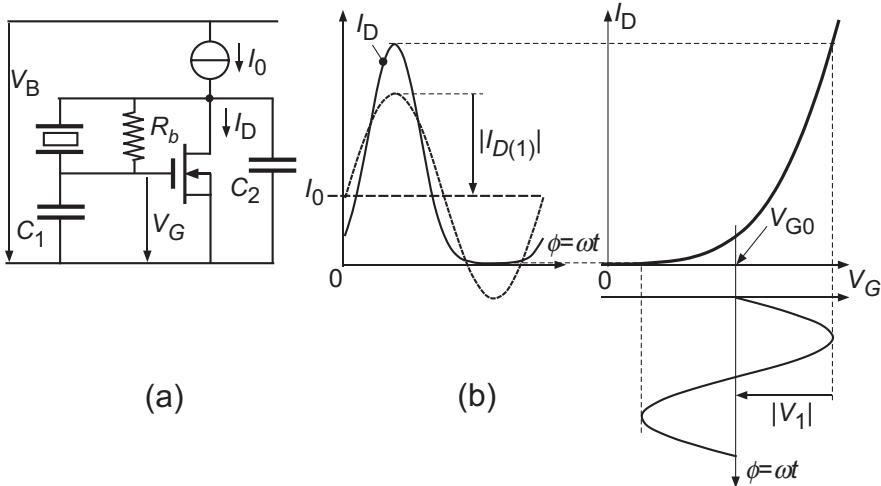
### 4.3.3 Amplitude Limitation by the Transistor Transfer Function

#### 4.3.3.1 Introduction

When the oscillation grows up, it is usually first limited by the nonlinear transfer function of the active device, as illustrated in Fig. 4.13. Part (a) of the figure shows the oscillator circuit with its bias current  $I_0$ . A resistive path  $R_b$  is provided between drain and gate so that, at equilibrium, the DC component of the drain current  $I_D$  can reach the imposed value  $I_0$ . The supply voltage  $V_B$  must be large enough in order to maintain  $I_0$  constant even during the positive peaks of drain voltage.

As was discussed in Section 4.3.2, the gate voltage of amplitude  $|V_1|$  remains approximately sinusoidal, with

$$V_G(t) = V_{G0} + |V_1| \sin \omega t, \quad (4.52)$$



**Figure 4.13** Amplitude limitation by the nonlinear transfer function of a transistor; (a) basic circuit; (b) mechanism of limitation.

But when its amplitude grows, the drain current  $I_D$  is distorted by the nonlinearity of  $I_D(V_G)$ , as shown in part (b) of the figure, and

$$I_D(t) = I_0 + |I_{D(1)}| \sin \omega t + \text{harmonic components}. \quad (4.53)$$

The harmonic components cannot flow through the motional impedance, and therefore flow mainly through capacitor  $C_2$ . The only useful component of  $I_D$  is the fundamental component of amplitude  $|I_{D(1)}|$ . Hence the relevant transconductance is that for the fundamental frequency, defined by

$$G_{m(1)} \triangleq \frac{|I_{D(1)}|}{|V_1|} = \frac{I_{D(1)}}{V_1}. \quad (4.54)$$

It is a real value as long as no phase shift exists in the transistor itself.

Now, because of the creation of harmonics,  $|I_{D(1)}|$  grows less than linearly with  $|V_1|$  and therefore  $G_{m(1)}$  decreases when  $|V_1|$  increases. The latter stops increasing when the condition for stable oscillation is reached for

$$G_{m(1)} = G_{mcrit}, \quad (4.55)$$

where  $G_{mcrit}$  is given by (4.39), (4.24) and (4.45). The amplitude obtained for a given current depends on the critical transconductance and on the width-to-length ratio of the transistor, which affects the specific current  $I_{spec}$  defined by (3.41).

### 4.3.3.2 Transistor in Weak Inversion

Let us assume that the transistor remains in weak inversion even for the peak value of drain current. In order to avoid losses, it should also remain saturated (fulfilling condition (3.46)), even for the minimum value of drain voltage. Thus  $I_D = I_F$  and weak inversion is ensured if  $I_{spec} \gg I_{Dmax}$ . Since the source voltage  $V_S = 0$ , the drain current given by the model described in Section 3.8 is

$$\frac{I_D}{I_{spec}} = \exp \frac{V_G - V_{T0}}{nU_T} = \exp \frac{V_{G0} - V_{T0} + |V_1| \sin \phi}{nU_T} = e^{v_e + v_1 \sin \phi}, \quad (4.56)$$

where  $\phi = \omega t$  and

$$v_e = \frac{V_{G0} - V_{T0}}{nU_T} \text{ and } v_1 = \frac{|V_1|}{nU_T} \quad (4.57)$$

are normalized variables.

Notice that saturation may be difficult to ensure with a large drain voltage amplitude if  $V_{T0}$  is too small. This problem will be discussed in Section 5.1.6.

The DC component of drain current is obtained by averaging (4.56) over one period:

$$\frac{I_0}{I_{spec}} = e^{v_e} \cdot \frac{1}{2\pi} \int_0^{2\pi} e^{v_1 \sin \phi} d\phi = e^{v_e} \cdot I_{B0}(v_1), \quad (4.58)$$

where

$$I_{B0}(v_1) = 1 + \frac{v_1^2}{2^2} + \frac{v_1^4}{2^2 \cdot 4^2} + \frac{v_1^6}{2^2 \cdot 4^2 \cdot 6^2} + \dots \quad (4.59)$$

is the modified Bessel function of order 0.

The fundamental component of drain current is given by

$$\frac{|I_{D(1)}|}{I_{spec}} = e^{v_e} \cdot \frac{1}{\pi} \int_0^{2\pi} e^{v_1 \sin \phi} \sin \phi d\phi = e^{v_e} \cdot 2I_{B1}(v_1), \quad (4.60)$$

where

$$I_{B1}(v_1) = \frac{v_1}{2} + \frac{v_1^3}{2^2 \cdot 4} + \frac{v_1^5}{2^2 \cdot 4^2 \cdot 6} + \frac{v_1^7}{2^2 \cdot 4^2 \cdot 6^2 \cdot 8} + \dots \quad (4.61)$$

is the modified Bessel function of order 1.

The transconductance for the fundamental frequency can then be expressed as a function of the bias current  $I_0$  and of the normalized gate voltage amplitude  $v_1$  by introducing (4.57), (4.58) and (4.60) into (4.54), which gives

$$G_{m(1)} = \frac{I_0}{nU_T} \cdot \frac{2I_{B1}(v_1)}{v_1 I_{B0}(v_1)} = G_m \frac{2I_{B1}(v_1)}{v_1 I_{B0}(v_1)}, \quad (4.62)$$

where, according to (3.54)

$$G_m = \frac{I_0}{nU_T} \quad (4.63)$$

is the small-signal transconductance (in weak inversion) at bias current  $I_D = I_0$ . Therefore, at the critical condition for oscillation (where  $v_1 = 0$ )

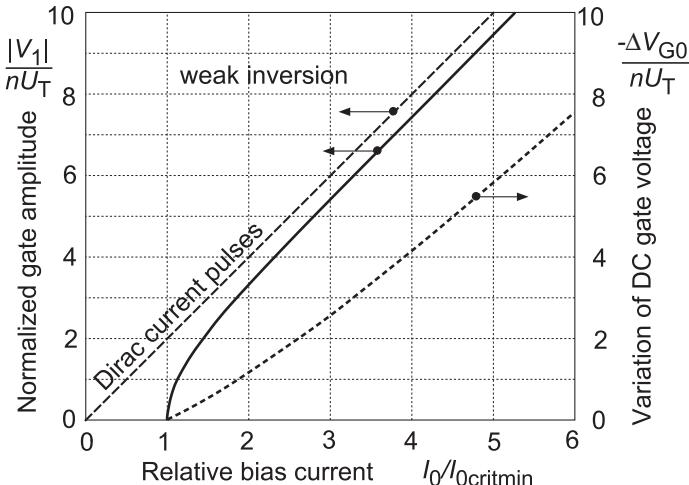
$$G_m = G_{mcrit} = \frac{I_{0critmin}}{nU_T}, \quad (4.64)$$

where  $I_{0critmin}$  is the critical current for oscillation in weak inversion. It is the minimum possible value of  $I_{0crit}$  since weak inversion provides the maximum possible transconductance for a given bias current  $I_0$ .

Introducing (4.62) and (4.64) into (4.55) gives

$$\frac{I_0}{I_{0critmin}} = \frac{I_{B0}(v_1)}{2I_{B1}(v_1)} v_1. \quad (4.65)$$

This relation between the bias current and the amplitude is plotted in Fig. 4.14. As soon as the critical current is reached, the amplitude grows abruptly until



**Figure 4.14** Normalized gate voltage amplitude as a function of bias current for a transistor operated in weak inversion.

it is limited by the nonlinearity at some fraction of  $nU_T$ . More current is then needed to increase the amplitude.

As the amplitude increases, the duration of the peaks of drain current is progressively reduced. If these peaks of current would be Dirac functions (zero duration and infinite amplitude), then  $|I_{D(1)}|/I_0 = 2$ . Introducing (4.62) and (4.64) into (4.55) would then give

$$v_1 = \frac{|V_1|}{nU_T} = 2 \frac{I_0}{I_{0critmin}}. \quad (4.66)$$

This asymptotic linear behavior is also represented in Fig. 4.14. It is a reasonable approximation of weak inversion for  $|V_1| \gg nU_T$ .

What is the variation of  $v_e$  (and thus of the DC gate voltage  $V_{G0}$ ) when the amplitude increases? For stable oscillation, (4.55) and (4.60) give

$$G_{mcrit} = G_{m(1)} = \frac{|I_{D(1)}|}{|V_1|} = \frac{|I_{D(1)}|}{v_1 n U_T} = \frac{I_{spec}}{n U_T} \cdot \frac{e^{v_e} \cdot 2 I_{B1}(v_1)}{v_1}. \quad (4.67)$$

Solving for  $v_e$  results in

$$v_e = \frac{V_{G0} - V_{T0}}{nU_T} = \ln \frac{I_{0critmin}}{I_{spec}} - \underbrace{\ln \frac{2I_{B1}(v_1)}{v_1}}_{\Delta V_{G0}/(nU_T)}. \quad (4.68)$$

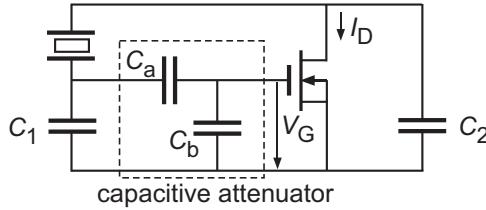
The normalized value of DC gate voltage variation  $\Delta V_{G0}$  is also represented (in dotted line) in Fig. 4.14.

### 4.3.3.3 Larger Amplitude by Capacitive Attenuator

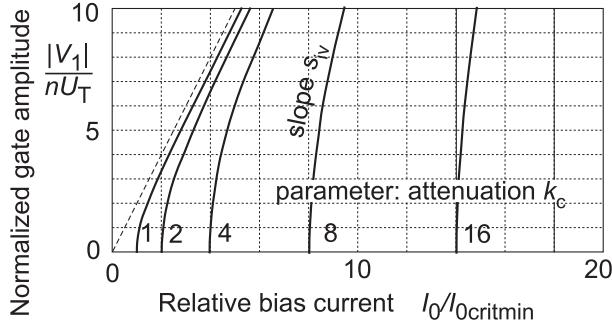
As shown by Fig. 4.14, to obtain a gate voltage amplitude larger than a few  $nU_T$  in weak inversion, a bias current  $I_0$  much larger than its critical value is needed. As a consequence, the drain current will be strongly distorted. One possibility to alleviate this problem is to introduce a capacitive attenuator at the gate, as depicted by Fig. 4.15. The AC component of gate voltage is then attenuated by a factor

$$k_c = (C_a + C_b)/C_a, \quad (4.69)$$

where  $C_b$  includes the gate capacitance of the transistor. For the AC component, this is equivalent to a transistor in weak inversion with  $U_T$  replaced by  $k_c U_T$ , thereby producing an equivalent transconductance  $I_0/(k_c n U_T)$ . Hence, the current axis and the voltage axis of Fig. 4.14 are both expanded by factor  $k_c$ . The result is shown in Fig. 4.16 for several values of attenuation  $k_c$ .



**Figure 4.15** Capacitive attenuator of the AC component of gate voltage (biasing not shown).



**Figure 4.16** Normalized gate voltage amplitude for a transistor operated in weak inversion with a capacitive attenuator.

#### 4.3.3.4 Transistor in Moderate or Strong Inversion

Another way to increase the amplitude while maintaining an acceptable amount of distortion is to operate the transistor in strong inversion.

Using the full model (3.40) of the transistor in saturation ( $I_D = I_F = I(V_S, V_G)$ ) and the normalized voltages  $v_e$  and  $v_1$  defined by (4.57), the DC and fundamental components of drain current can be expressed as

$$\frac{I_0}{I_{spec}} = \frac{1}{2\pi} \int_0^{2\pi} \left[ \ln \left( 1 + e^{(v_e + v_1 \sin \phi)/2} \right) \right]^2 d\phi, \quad (4.70)$$

$$\frac{|I_{D(1)}|}{I_{spec}} = \frac{1}{\pi} \int_0^{2\pi} \left[ \ln \left( 1 + e^{(v_e + v_1 \sin \phi)/2} \right) \right]^2 \sin \phi d\phi. \quad (4.71)$$

Compared to weak inversion (equations (4.58) and (4.60)), the calculation is more complicated since the normalized DC gate voltage  $v_e$  remains inside the integral.

Let us define the inversion coefficient at the critical current for oscillation (hence for  $|V_1| = 0$ ) as

$$IC_0 \triangleq I_{0crit}/I_{spec}. \quad (4.72)$$

The critical transconductance can then be calculated by applying (3.55) with  $I_D = I_{0crit}$ :

$$G_{mcrit} = \frac{I_{0crit}}{nU_T} \cdot \frac{1 - e^{-\sqrt{IC_0}}}{\sqrt{IC_0}}. \quad (4.73)$$

According to (4.54) and (4.55), the condition for stable oscillation can be expressed as

$$\frac{|I_{D(1)}|}{|V_1|} = \frac{|I_{D(1)}|}{v_1 n U_T} = G_{mcrit}. \quad (4.74)$$

Using (4.64), (4.73) and (4.72), we obtain the ratio

$$\frac{I_{0critmin}}{I_{spec}} = \frac{nU_T G_{mcrit}}{I_{spec}} = \frac{I_{0crit}}{I_{spec}} \cdot \frac{1 - e^{-\sqrt{IC_0}}}{\sqrt{IC_0}} = \sqrt{IC_0} (1 - e^{-\sqrt{IC_0}}), \quad (4.75)$$

which only depends on  $IC_0$ . The same ratio can be obtained from (4.74):

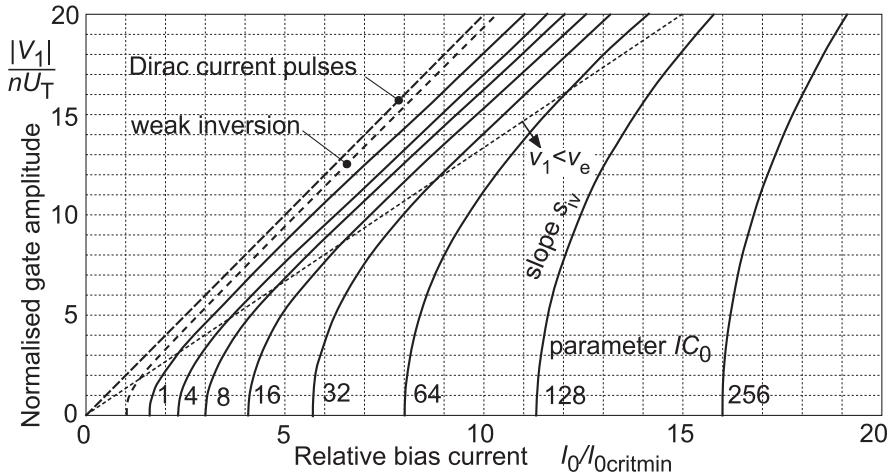
$$\frac{I_{0critmin}}{I_{spec}} = \frac{nU_T G_{mcrit}}{I_{spec}} = \frac{|I_{D(1)}|}{v_1 I_{spec}}. \quad (4.76)$$

The required current  $I_0$  can then be related to the critical current in weak inversion  $I_{0critmin}$  (minimum critical current) by

$$\frac{I_0}{I_{0critmin}} = \frac{I_0}{I_{spec}} \cdot \frac{I_{spec}}{I_{0critmin}}. \quad (4.77)$$

The calculation of the current required for a given amplitude can thus be carried out in the following manner:

1. Select a value of  $IC_0$ .
2. Calculate the corresponding value of  $I_{0critmin}/I_{spec}$  by (4.75)
3. Select a value of normalized DC gate voltage  $v_e$ .
4. Compute  $|I_{D(1)}|(v_1)/I_{spec}$  for the selected value of  $v_e$ , using (4.71).
5. Choose the value of  $v_1$  giving the required value of  $I_{0critmin}/I_{spec}$ , using (4.76).
6. Compute the value of  $I_0/I_{spec}(v_e, v_1)$  by (4.70)
7. Apply (4.77) to obtain  $I_0/I_{0critmin}(v_1)$ ; this gives one point of the curve.
8. Go back to step 3 to calculate a new point.



**Figure 4.17** Normalized gate voltage amplitude as a function of bias current for several values of  $IC_0$ , the inversion coefficient at the critical condition for oscillation. It is assumed that the transistor remains saturated all along the oscillation cycle. The limit of validity of the strong inversion model (4.86) is indicated by the thin dotted line.

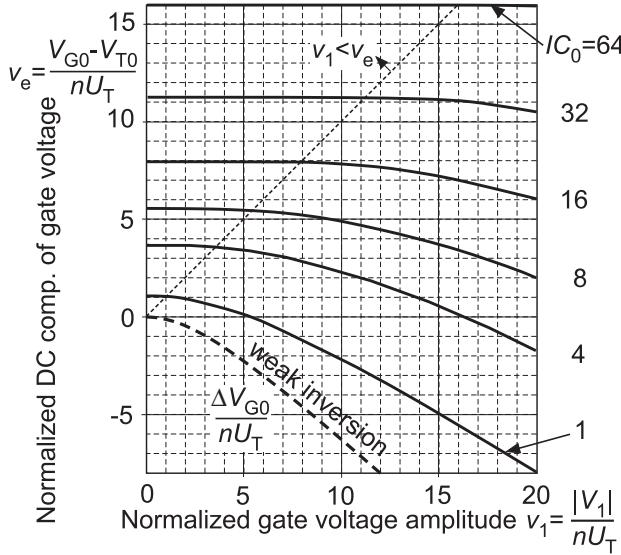
The result of this procedure applied for several values of  $IC_0$  is presented in Fig. 4.17. It must be remembered that this result is only valid if the active transistor and the transistor providing the bias current  $I_0$  remain saturated during the whole cycle of oscillation. If one of these transistors leaves saturation, the resulting increase of losses will reduce the amplitude.

A comparison with Fig. 4.16 shows that these results are comparable to those obtained with a capacitive attenuator (compare for example  $k_c = 8$  in Fig. 4.16 with  $IC_0 = 64$  in Fig. 4.17). In both cases, a large amplitude can be obtained with a bias current not much higher than its critical value (for example, with  $IC_0 = 64$ ,  $|V_1| = 11nU_T$  for  $I_0/I_{0\text{crit}} = 1.25$ ).

However, this increase of linearity is obtained at the price of a larger current for a given amplitude (all the curves are at the right side of that for weak inversion).

The variation of the normalized DC gate voltage  $v_e$  with the normalized amplitude  $v_1$  obtained with the above calculations is shown in Fig. 4.18. The shift of DC gate voltage in weak inversion given by (4.68) is also reported on this figure. It will be needed later for properly designing the bias circuitry.

The nonlinear effects due to the transfer function are essentially equivalent to a reduction of the small-signal transconductance  $G_m$  (this is exactly true if  $Z_3$  is very large, so that  $V_1$  remains perfectly sinusoidal). Thus the locus of



**Figure 4.18** Variation of the DC component  $V_{G0}$  of gate voltage with the gate voltage amplitude  $|V_1|$  at stable oscillation. The shift  $\Delta V_{G0}$  in weak inversion is shown in dotted line.

$Z_{c(1)}(I_c)$  follows the circular locus of  $Z_c(G_m)$ . For a given value of  $R_m$ , the value of  $p_c$  is therefore independent of the amplitude.

As illustrated in the example of Fig. 4.11, this is not the case for stronger nonlinear effects such as those due to the desaturation of the active transistor, or of the transistor delivering the bias current. In order to avoid those effects, the amplitude should be limited. This is best obtained by using an amplitude control loop as will be described in Section 5.2.

#### 4.3.3.5 Transistor Strictly in Strong Inversion

If the transistor is in strong inversion at the critical current for oscillation ( $I_{spec} \ll I_{0crit}$ ) then from (3.56):

$$I_{0crit} = nU_T \sqrt{IC_0} G_{mcrit} = \sqrt{IC_0} I_{0critmin}. \quad (4.78)$$

If the transistor remains strictly in strong inversion as the oscillation grows up, its drain current in saturation  $I_D = I_F$  can be expressed from (3.43) by

$$I_D = \frac{I_{spec}}{4} (v_e + v_1 \sin \phi)^2, \quad (4.79)$$

where  $v_e$  and  $v_1$  are the normalized voltages defined by (4.57). The fundamental component of  $I_D$  is then given by

$$\frac{|I_{D(1)}|}{I_{spec}} = \frac{1}{4\pi} \int_0^{2\pi} (v_e + v_1 \sin \phi)^2 \sin \phi d\phi = \frac{v_e v_1}{2}. \quad (4.80)$$

The transconductance for the fundamental frequency, equal to the critical transconductance at stable oscillation according to (4.55), becomes

$$G_{m(1)} = \frac{|I_{D(1)}|}{|V_1|} = \frac{v_e I_{spec}}{2nU_T} = G_{mcrit}. \quad (4.81)$$

Solving for  $v_e$  gives

$$v_e = \frac{2nU_T G_{mcrit}}{I_{spec}} = \frac{2I_{0critmin}}{I_{spec}} = 2\sqrt{IC_0} \quad (4.82)$$

where the last expression comes from the fact that, using (4.78):

$$\frac{I_{0critmin}}{I_{spec}} = \frac{I_{0crit}}{I_{spec}} \cdot \frac{I_{0critmin}}{I_{0crit}} = \frac{IC_0}{\sqrt{IC_0}} = \sqrt{IC_0}. \quad (4.83)$$

The normalized effective DC gate voltage  $v_e$  is thus constant. But this is true only for

$$v_1 < v_e = 2\sqrt{IC_0} \quad (4.84)$$

otherwise the transistor enters weak inversion in the negative half periods of gate voltage and (4.79) is no longer valid. This limit is shown by the dotted strait line in Fig. 4.18. Notice that  $v_e$  is already slightly descending below this limit, since the full model used for the calculation includes moderate inversion.

Returning to strict strong inversion, the DC component of drain current, that is the bias current  $I_0$  is given by

$$\frac{I_0}{I_{spec}} = \frac{1}{8\pi} \int_0^{2\pi} (v_e + v_1 \sin \phi)^2 d\phi = \frac{1}{4} \left( v_e^2 + \frac{v_1^2}{2} \right) = IC_0 + \frac{v_1^2}{8}. \quad (4.85)$$

Hence

$$\frac{I_0}{I_{0critmin}} = \frac{I_0}{I_{spec}} \cdot \frac{I_{spec}}{I_{0critmin}} = \sqrt{IC_0} + \frac{v_1^2}{8\sqrt{IC_0}}. \quad (4.86)$$

By introducing the condition (4.84), the limit of validity becomes

$$v_1 < \frac{3}{4} \frac{I_0}{I_{0critmin}}. \quad (4.87)$$

It is reported as a thin dotted line in Fig. 4.17.

#### 4.3.4 Energy and Power of Mechanical Oscillation

As explained in Section 2.4, the energy of mechanical oscillation is directly related to the amplitude of motional current  $I_m$  flowing in the motional impedance  $Z_m$ . Considering the lossless case of Fig. 4.12, this current is related to the current  $I_1$  flowing through capacitor  $C_1$  by

$$I_1 = (1 + j\omega C_3 Z_m) I_m. \quad (4.88)$$

The real part of  $Z_m$  is  $R_m$ , whereas at stable oscillation its imaginary part compensates that of the circuit:

$$\text{Im}(Z_m) = -\text{Im}(Z_{c(1)}). \quad (4.89)$$

If the circuit is not strongly nonlinear,  $Z_{c(1)}$  may be replaced by  $Z_c$ , the circular locus of which is represented in Fig. 4.6. Now if  $R_m \ll |R_{n0}|_{max}$  ( $K_m \gg 1$ ), this figure shows that  $\text{Im}(Z_c) = 1/j\omega(C_s + C_3)$ . Thus, at stable oscillation:

$$Z_m = R_m - \frac{1}{j\omega(C_s + C_3)}, \quad (4.90)$$

which, introduced in (4.88) yields

$$\frac{I_1}{I_m} = \left( 1 - \frac{C_3}{C_s + C_3} + j\omega C_3 R_m \right) = \left( \frac{C_s}{C_s + C_3} + \frac{j}{M} \right), \quad (4.91)$$

or, for the amplitudes:

$$\frac{|I_1|}{|I_m|} = \sqrt{\left( \frac{C_s}{C_s + C_3} \right)^2 + \frac{1}{M^2}}. \quad (4.92)$$

Now the second term may usually be neglected since  $M \gg 2$ , hence

$$|I_m| \cong \left( 1 + \frac{C_3}{C_s} \right) |I_1| = \left( 1 + \frac{C_3}{C_s} \right) \omega C_1 |V_1|. \quad (4.93)$$

The amplitude of motional current depends on the gate voltage amplitude  $|V_1|$  calculated in Section 4.3.3. The energy of mechanical oscillation is then obtained by introducing this result in (2.23):

$$E_m \cong \left( 1 + \frac{C_3}{C_s} \right)^2 \frac{C_1^2}{2C_m} |V_1|^2. \quad (4.94)$$

It is proportional to the maximum energy stored in capacitor  $C_1$  and to the ratio  $C_1/C_m$ . The power dissipated in the resonator can be obtained by applying (2.24), which gives

$$P_m = \frac{\omega}{Q} E_m \cong \left( 1 + \frac{C_3}{C_s} \right)^2 \frac{\omega C_1^2}{2QC_m} |V_1|^2 = \left( 1 + \frac{C_3}{C_s} \right)^2 \frac{\omega^2 C_1^2 R_m}{2} |V_1|^2. \quad (4.95)$$

### 4.3.5 Frequency Stability

#### 4.3.5.1 Introduction

The main feature to be optimized in a crystal oscillator, especially for time-keeping applications, is its frequency stability. Separated in three groups, the causes of degradation of this stability will be discussed in what follows, together with possible cures.

#### 4.3.5.2 Resonator

The resonant frequency  $\omega_m$  of the resonator itself is not perfectly constant:

- a. Some variation with temperature is always present. As discussed in Section 2.5, this variation depends on the type of resonator, which must be selected in accordance with the specifications of the oscillator.
- b. There is no way to avoid some aging of the resonator after fabrication. Since the rate of aging usually decreases with time, it is possible to carry out some pre-aging on the resonator before using it.

#### 4.3.5.3 Nonlinear Effects in the Circuit

The amount of frequency pulling  $p_s$  at stable oscillation was discussed in Section 3.2. As explained by Fig. 3.3, it is proportional to the imaginary part of  $Z_{c(1)}$  (the circuit impedance for the fundamental frequency) at the stable point S.

Now, as illustrated by the example of Fig. 4.11(b), this imaginary part may be strongly dependent on nonlinear effects. The nonlinear effects are themselves dependent on various variables, including the supply voltage of the circuits, the threshold voltage of the transistor and the ambient temperature. They must therefore be minimized to improve the frequency stability.

- a. The nonlinear transfer function  $I_D(V_G)$  of the active transistor are the first to intervene when the amplitude increases. They limit the amplitude  $|V_1|$  at the gate as illustrated in Fig. 4.17. To limit the resulting nonlinear effects, the bias current should not be much higher than its critical value, typically no more than 10 or 20% above. The inversion coefficient  $IC_0$  of the transistor should be selected in order to obtain the desired amplitude. Now, precise values of currents are hard to obtain in integrated circuits, and the critical current itself depends on many possibly variable parameters. Thus, the only

possibility to control the amount of overdrive is to implement some kind of voltage amplitude regulation, as will be discussed in Section 5.2.

As was already explained in Section 4.3.2, the change of frequency due to the nonlinear  $I_D(V_G)$  function is caused by intermodulation between harmonic components of the gate voltage. These are produced by harmonic components of current flowing through the drain-to-gate impedance  $Z_3$ , which can be reduced by increasing  $|Z_3|$  (in particular by decreasing  $C_3$ ).

- b. Nonlinearities in  $Z_1$  are due to the nonlinear dependency of the gate capacitance on the gate voltage. Their effect can be reduced by implementing a sufficiently large value of  $C_1$  by means of a linear capacitor.
- c. An important nonlinearity in  $Z_2$  occurs when the amplitude is so large that the active transistor and/or the transistor delivering the bias current  $I_0$  leave saturation in the peaks of drain voltage. Both transistors should be kept saturated all along the oscillation cycle.
- d. If  $|Z_3|$  is large, as it should be, its possible nonlinearity should have negligible effect on the frequency.

#### 4.3.5.4 Variation of Linear Effects

If nonlinear effect on the frequency are made negligible, the amount of frequency pulling is equal to its value  $p_c$  at the critical condition for oscillation. As illustrated by Fig. 4.4,  $p_c$  is proportional to the imaginary part of the circuit impedance  $Z_c$  at the solution point A, where the real part of  $Z_c$  compensates the motional resistance of the resonator ( $\text{Re}(Z_c) = -R_m$ ). Hence, any vertical displacement of A results in a variation of  $p_c$ . Such a displacement may be due to several causes:

a. Even if the resonator has a very constant motional frequency, its quality factor may change, resulting in a change of motional resistance  $R_m$ . The effect of a variation of  $R_m$  is proportional to the slope of  $Z_c$  at point A. This slope can be minimized by

- reducing  $C_3$  to increase the radius of the circle,
  - reducing the losses, in order to have the circular locus better centered on the imaginary axis, and/or
  - reducing  $R_m$  (increasing  $Q$ ).
- b. Variation of the losses, that should therefore be
- as small as possible
  - as constant as possible.

c. Variations of  $C_1$ ,  $C_2$  and/or  $C_3$ , with an effect on  $p_c$  given by (4.21). These 3 capacitors should therefore be kept as constant as possible. The voltage dependency of  $C_1$  due to the voltage dependent gate capacitance of the transistor can be minimized by implementing a sufficiently large value of  $C_1$  by means of a linear capacitor. The same can be done to reduce the voltage dependency of  $C_2$  due to the voltage dependent junction capacitance at the drain node of the circuit.

Some capacitance variation may be due to mechanically unstable connections between the circuit and the resonator.

The sensitivity of  $p_c$  to capacitance variations can be obtained by differentiating (4.21). For  $C_s$  (series connection of  $C_1$  and  $C_2$ ) much larger than  $C_3$ , this gives

$$dp_c = -p_c \left( \frac{C_2}{C_1(C_1+C_2)} dC_1 + \frac{C_1}{C_2(C_1+C_2)} dC_2 + \frac{1}{C_s} dC_3 \right). \quad (4.96)$$

Thus, the effect of capacitance variations on the frequency of oscillation can be reduced by reducing  $p_c$ . But, as already explained in Section 4.2.2, this may require a large increase of bias current, according to (4.26).

### 4.3.6 Elimination of Unwanted Modes

#### 4.3.6.1 Introduction

As was explained in Section 2.2, all electromechanical resonators, in particular the quartz resonator, have several possible modes of oscillation. Each of them corresponds to a series resonant circuit in the complete equivalent circuit of Fig. 2.2(a). We have explained in the same section that, once oscillation was obtained on one of these modes, no coupling could be produced by the circuit to the other modes.

Now, in all previous analyses, we have assumed that oscillation was obtained at the “wanted” mode and not at any other “unwanted” mode. Let us now examine how this can be ensured.

Assuming that the circuit is designed to provide, for the desired mode, a large margin factor  $K_m$  (defined by (4.17)) and that losses are negligible, the critical transconductance is given by (4.24) repeated here for convenience:

$$G_{mcrit0} \cong \omega^2 R_m \cdot C_1 C_2 (1 + C_3/C_s)^2. \quad (4.97)$$

Now, the part after the dot is given by the circuit, and is at least the *same for all the other modes* (it could be larger for some modes if the corresponding

value of  $K_m$  would not be large, and (4.22) would have to be used instead of (4.24)).

On the contrary, the term  $\omega^2 R_m$  ( $=\omega/(QC_m)$ ) is *specific to each mode*. Hence  $(\omega^2 R_m)_w$  can be used to distinguish the wanted mode from all other unwanted modes, each of them being characterized by their value of  $(\omega^2 R_m)_u$ . Let us define

$$\alpha \triangleq \frac{(G_{mcrit})_u}{(G_{mcrit})_w}. \quad (4.98)$$

For the lossless case, according to (4.97):

$$\alpha = \alpha_0 \triangleq \frac{(G_{mcrit0})_u}{(G_{mcrit0})_w} = \frac{(\omega^2 R_m)_u}{(\omega^2 R_m)_w}. \quad (4.99)$$

The wanted mode will be said to be *more active* than the unwanted mode if  $\alpha > 1$  and less active if  $\alpha < 1$ .

According to (3.55), the transconductance is proportional to the current if the transistor is in weak inversion ( $IC_0 \ll 1$ ), but only to the square root of the current if the transistor is in strong inversion ( $IC_0 \gg 1$ ). Hence:

$$(I_{0crit})_u = \alpha(I_{0crit})_w \quad \text{in weak inversion} \quad (4.100)$$

$$(I_{0crit})_u = \alpha^2(I_{0crit})_w \quad \text{in strong inversion.} \quad (4.101)$$

#### 4.3.6.2 Wanted Mode More Active Than Unwanted Modes ( $\alpha > 1$ )

The wanted mode of oscillation is frequently the most active one. A safe procedure is then to impose a fixed bias current  $I_0$  in the range

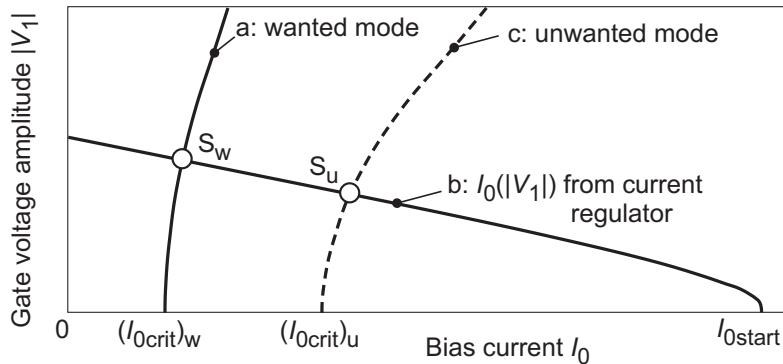
$$(I_{0crit})_w < I_0 < (I_{0crit})_u. \quad (4.102)$$

In practice however, this is only possible if  $\alpha \gg 1$ . Indeed, a small range of possible current would require a precise value of current that is not available in an integrated circuit environment. Even if such a precise current would be possible, its value would depend on  $G_{mcrit}$  and therefore on the value of quality factor  $Q$  and on that of the various capacitors. Moreover, a small ratio  $I_0/I_{0crit}$  would provide only a small excess of negative resistance, resulting in a large start-up time constant  $\tau_0$  given by (3.15), and thus in a very long start-up time.

If the range of possible current is limited ( $\alpha$  not much larger than 1), the best solution is to generate the bias current by means of an amplitude

regulator, as was explained in Section 3.4. Such a regulator provides a large initial bias current, which ensures a short start-up time. This bias current decreases when the amplitude increases, until equilibrium is reached.

Instead of regulating the current  $|I_{cs}| = |I_m|$  in the motional branch as in Fig. 3.4, it is preferable to limit the voltage  $|V_1|$  at the gate, which is related to  $|I_m|$  by (4.93). This type of regulation is illustrated by Fig. 4.19 and will be detailed in Section 5.2.

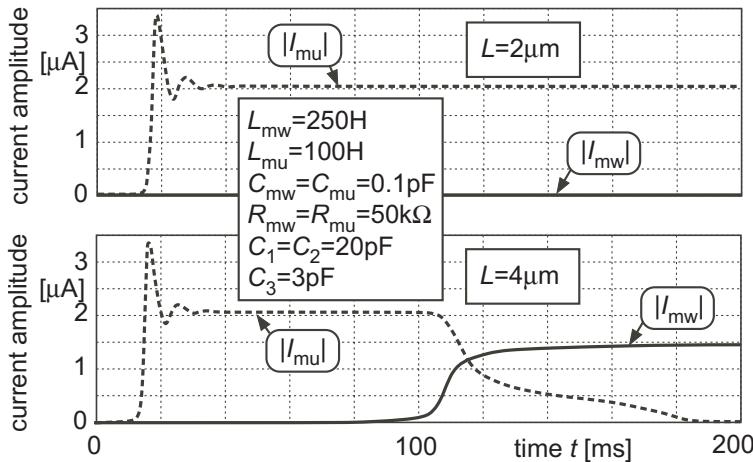


**Figure 4.19** Regulation of the gate voltage amplitude.

In this example, Curve a represents the amplitude of oscillation  $|V_1|$  at the gate as a function of the bias current  $I_0$  for the wanted mode, as given by Fig. 4.16 or 4.17. Curve b represents the bias current  $I_0(|V_1|)$  delivered by the amplitude detector. When the loop is closed, the system is expected to reach the stable point  $S_w$ , with a bias current only slightly larger than its critical value  $(I_{0\text{crit}})_w$ . For the unwanted mode, the  $|V_1|(I_0)$  relationship is given by Curve c.

Let us assume that the start-up time constant of the unwanted mode is shorter than that for the wanted mode. Oscillation will start at this unwanted mode, and possibly reach the corresponding equilibrium point  $S_u$ , with a value of bias current just slightly larger than  $(I_{0\text{crit}})_u$ . The transconductance of the transistor is thus practically not affected by this oscillation, and remains larger than its critical value for the wanted mode. The amplitude of the wanted mode can therefore still grow up, thereby reducing  $I_0$  until the stable point  $S_w$  is reached. The bias current is then below its critical value for the unwanted mode, that can no longer be sustained. Oscillation at the wanted mode only is thus ensured.

It is important to point out such a behavior is *not ensured* if  $I_0$  at point  $S_u$  is much larger than  $(I_{0crit})_u$ , resulting in a strongly nonlinear behavior of the transistor. As a consequence, the remaining transconductance may not be sufficient for starting up oscillation at the wanted mode. This is illustrated by the results of simulations depicted in Fig. 4.20.



**Figure 4.20** Possible dominance of the less active of two possible modes; in these simulation of start-up in a  $0.18\mu\text{m}$  process, the channel width is  $W = 50\mu\text{m}$  whereas the channel length  $L$  is changed from  $2$  to  $4\mu\text{m}$ . Notice that low values of quality factors ( $Q_u < Q_w = 1000$ ) are used to facilitate the simulation.

In this example, the resonator has two possible modes (two series branches in parallel). The wanted mode w has a resonant angular frequency  $\omega_w = 2 \cdot 10^5 \text{ s}^{-1}$  with a motional inductance  $L_{mw}=250\text{H}$ , whereas  $L_{mu}=100\text{H}$  for the unwanted mode u, giving  $\omega_u = 3.16 \cdot 10^5 \text{ s}^{-1}$ . It is therefore less active than mode w, in a ratio  $\alpha = 2.5$ . The upper part of the figure shows that, for a channel length  $L = 2\mu\text{m}$  of the active transistor, the motional current  $|I_{mw}|$  of mode w remains zero (no oscillation at the wanted mode) whereas  $|I_{mu}|$  stabilizes at about  $2\mu\text{A}$ . If  $L$  is increased to  $4\mu\text{m}$ , the circuit become slightly less nonlinear because the inversion coefficient in the peaks of drain current is increased (from 0.26 to 0.49). As a result, oscillation at mode u does not prevent mode w to grow and to finally stay alone.

### 4.3.6.3 Effect of Losses

As discussed in Section 4.2.5, the main effect of losses is to increase the critical transconductance  $G_{mcrit}$ . At a given frequency, these losses may always be represented by an additional component of conductance  $G_1$ ,  $G_2$  and/or  $G_3$  in parallel with the capacitors. As long as they are not too large, the resulting increase of  $G_{mcrit}$  is given by (4.45).

If the  $G_i$  remain independent of the frequency (as is the case if they are due to real conductances in parallel), the critical transconductance is increased by the same amount for all possible modes of oscillation. The relative difference of critical transconductances is reduced and, according to (4.98), the value of  $\alpha$  becomes closer to unity. The potential problem illustrated by Fig. 4.20 is worsened, and this kind of losses cannot help separating the wanted mode from the unwanted one.

But each of the  $G_i$  can possibly be frequency dependent. The most simple case is a resistance  $R_i$  in series with capacitance  $C_i$ . If  $(\omega C_i R_i)^2 \ll 1$ , then

$$G_i \cong \omega^2 C_i^2 R_i. \quad (4.103)$$

The loss conductance is then increasing with the frequency, which may help eliminating an unwanted mode, as discussed below.

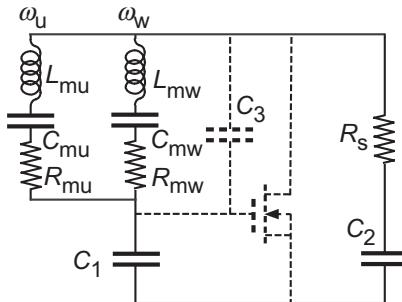
### 4.3.6.4 Wanted Mode Less Active Than Unwanted Modes ( $\alpha < 1$ )

This is a difficult situation. If the unwanted mode has a *higher* frequency than the wanted mode, its overall activity may be reduced by introducing a resistance in series with  $C_1$  and/or  $C_2$ . As given by (4.103), this will produce an additional component of  $G_1$  and/or  $G_2$  that is proportional to  $\omega^2$ . This component is therefore larger for the unwanted mode, which may push the value of  $\alpha$  above unity.

An other way to analyze this solution is to consider the path of the motional current for each mode as illustrated in Fig. 4.21. If  $C_3$  is sufficiently small to be negligible, most of the motional current of each resonator branch flows in the loop closed by capacitors  $C_1$  and  $C_2$ . Hence, a resistor  $R_s$  inserted in this loop is approximately added to the motional resistors  $R_{mw}$  and  $R_{mu}$ . The effective activity ratio can therefore be approximated by

$$\alpha \cong \frac{\omega_u^2 (R_{mu} + R_s)}{\omega_w^2 (R_{mw} + R_s)}, \quad (4.104)$$

which is assumed to be smaller than unity for  $R_s = 0$  (more active unwanted mode at higher frequency). This ratio will become larger than unity for



**Figure 4.21** Loss resistor  $R_s$  is the main loop of oscillation current.

$$R_s > \frac{\omega_w^2 R_{mw} - \omega_u^2 R_{mu}}{\omega_u^2 - \omega_w^2} = \frac{1 - \alpha_0}{(\omega_u/\omega_w)^2 - 1} R_{mw}. \quad (4.105)$$

If  $\alpha_0$  is close to unity or if the frequency ratio is large, then  $R_s \ll R_{mw}$  and the unwanted mode can be eliminated without too much effect on the wanted mode.

The situation is even more difficult if the unwanted mode is more active and has a *lower* frequency than the wanted mode. This is the case if the wanted mode is an overtone.

One possible solution would be to exploit the nonlinear effects illustrated by Fig. 4.20. Indeed, in the upper part of the figure, the less active higher frequency mode dominates because it has a shorter start-up time constant. However, this solution is *not recommended* because two possible stable modes of oscillation exist, and which one dominates depends on the initial conditions. For example, simulations show that, in the example of the figure with  $L = 2\mu\text{m}$ , the more active low-frequency mode still dominates if the supply voltage of the circuit is raised very slowly instead of being switched on abruptly.

There is no simple way to produce losses that increase when the frequency decreases, but the unwanted mode can be avoided by inserting a parallel resonant circuit tuned to its frequency in series with the source of the transistor. The unwanted mode will then be prevented if the (real) impedance at the resonance is larger than  $1/G_{mcritu}$  (where  $G_{mcritu}$  is the critical transconductance for the unwanted mode). Furthermore, the capacitance of the resonant circuit should be large enough to prevent source degeneration for the wanted mode. For the example of Fig. 4.20, this solution would require a capacitance of 1 nF, an inductance of 25 mH and parallel resistance of 1 MΩ, corresponding to a quality factor of 200, which is not realistic. In an integrated circuit en-

vironment, this solution is thus only applicable at high frequencies, and for a large ratio  $\omega_w/\omega_u$ .

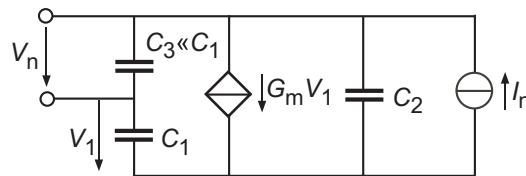
## 4.4 Phase Noise

### 4.4.1 Linear Effects on Phase Noise

#### 4.4.1.1 General Case

According to (3.30), the phase noise of the oscillator depends on the energy of oscillation  $E_m$ , the quality factor  $Q$  of the resonator, and the frequency of oscillation  $\omega$ . It also depends on the noise excess factor  $\gamma$  of the circuit.

As defined by (3.23), this noise excess factor is the ratio between the spectrum  $S_{V_n^2}$  of the noise voltage  $V_n$  produced by the circuit to that of the thermal noise of the motional resistance  $4kTR_m$ . If  $G_i \ll \omega C_i$ , losses can be neglected and this noise voltage can be calculated from the equivalent circuit of Fig. 4.22. The source of noise  $I_n$  is the channel noise of the transistor plus



**Figure 4.22** Equivalent circuit of the Pierce oscillator for the calculation of the noise voltage  $V_n$ .

additional noise delivered by the biasing current source. Assuming  $C_3 \ll C_1$  and  $C_2$ , the noise voltage can be expressed as

$$V_n = \frac{I_n}{j\omega_n C_2 + G_m C_3 / C_1}, \quad (4.106)$$

where  $\omega_n$  is the frequency at which noise is considered.

At frequencies close to the oscillation frequency  $\omega$ , the spectral densities are thus related by

$$S_{V_n^2} = \frac{S_{I_n^2}}{(\omega C_2)^2 + (G_m C_3/C_1)^2} = \frac{S_{I_n^2}}{(\omega C_2)^2 \left[ 1 + \left( \frac{G_m}{M G_{mcrit0}} \right)^2 \right]} \cong \frac{S_{I_n^2}}{(\omega C_2)^2}, \quad (4.107)$$

where the second expression has been obtained by introducing the factor of merit  $M$  defined by (2.9) through the relationship (4.24) between  $R_m$  and  $G_{mcrit0}$ . Since  $M \gg 1$ , the term between brackets is usually close to unity, thus the noise excess factor for very small amplitudes is

$$\gamma_0 \triangleq \frac{S_{V_n^2}}{4kTR_m} \cong \frac{S_{I_n^2}}{4kTR_m(\omega C_2)^2} \quad (4.108)$$

#### 4.4.1.2 Channel Noise of the Active Transistor

If the bias current were free of noise, the only source of  $I_n$  would be the channel noise of the active transistor. Its spectral density given by (3.60) can be introduced into (4.108). The noise excess factor is then given by

$$\gamma_0 \cong \frac{\gamma n G_{mcrit}}{(\omega C_2)^2 R_m}. \quad (4.109)$$

Using again (4.24) to replace  $R_m$  by  $G_{mcrit0}$ , it becomes

$$\gamma_0 \cong \gamma n \cdot \frac{C_1}{C_2} \cdot \frac{G_{mcrit}}{G_{mcrit0}}. \quad (4.110)$$

#### 4.4.2 Phase Noise in the Nonlinear Time Variant Circuit

##### 4.4.2.1 Introduction

As discussed in Section 3.7.2, the results obtained in the previous section are no longer valid when the amplitude increases, since the circuit becomes nonlinear and the noise becomes cyclostationary.

Neglecting the parallel capacitor  $C_3$ , the phase noise can be analyzed by means of the equivalent circuit of Fig. 3.9 with  $C_i = C_2$ . The cyclostationary noise sources are functions of  $\sin(\phi + \Delta\phi)$ , where  $\phi = \omega t$  and  $\Delta\phi$  is the phase shift between the sinusoidal voltages  $V_2$  and  $V_1$ .

An approximation of this phase shift can be calculated at the critical condition for oscillation from (4.34) and (4.45). As long as the condition (4.43) is fulfilled (small losses):

$$\tan \Delta\phi \cong \frac{1}{\omega C_1} \left[ G_{mcrit0} + G_1 \left( 1 + \frac{C_2}{C_1} \right) + G_3 \frac{C_1 + C_2}{C_s} \right]. \quad (4.111)$$

It is independent of a possible loss conductance  $G_2$ .

Now, because of the presence of  $C_3$  (or more generally  $Z_3$ ) between drain and gate, some noise fed back through the transistor is added to the noise current  $I_n$  of Fig. 4.22. This effect will be *neglected*, as was done in the linear analysis.

#### 4.4.2.2 Effect of the White Channel Noise in Weak Inversion

In weak inversion, the variation of drain current during each cycle of stable oscillation can be expressed by introducing (4.58) and (4.65) in (4.56). With the phase shift  $\Delta\phi$ , this yields

$$I_D = I_{0critmin} \frac{v_1}{2I_{B1}(v_1)} e^{v_1 \sin(\phi + \Delta\phi)}. \quad (4.112)$$

Thus, from (3.61) and (3.54), the cyclostationary drain noise current spectrum is

$$\underbrace{\alpha_i^2 S_{I_n^2}}_{S_{I_n^2}} = \underbrace{2nkTG_{mcrit}}_{\alpha_i^2} \underbrace{\frac{v_1}{2I_{B1}(v_1)}}_{\alpha_i^2} e^{\underbrace{v_1 \sin(\phi + \Delta\phi)}_{\alpha_i^2}}, \quad (4.113)$$

where the first part is the spectrum  $S_{I_n^2}$  of a fictitious white noise current modulated by  $\alpha_i$ . According to (3.34), the squared RMS value of the effective impulse sensitivity function (ISF) is then

$$\overline{I_i^2(v_1)} = \overline{\cos^2 \phi \alpha_i^2} = \frac{1}{2\pi} \int_0^{2\pi} \cos^2 \phi \cdot e^{v_1 \sin(\phi + \Delta\phi)} d\phi \quad (\text{weak inversion}). \quad (4.114)$$

The phase noise spectrum is then obtained by introducing the above values of  $S_{I_n^2}$  and  $\overline{I_i^2}$  in (3.33), which results in

$$S_{\phi_n^2} = S_{\phi_n^{20}} \frac{v_1}{I_{B1}(v_1)} \overline{I_i^2(v_1)}, \quad (4.115)$$

where

$$S_{\phi_n^2 0} = \frac{n k T G_{mcrit}}{2(C_2 |V_2| \Delta \omega)^2} \cdot \frac{C_m^2}{C_2^2}. \quad (4.116)$$

is the phase noise spectrum for very small amplitudes. Referring to Fig. 3.9,  $C_2 |V_2|$  may be replaced by  $|I_m|/\omega$  (even with a small phase shift, the amplitude of the current is only very slightly affected). Thus, by introducing the expression (4.24) of the lossless critical transconductance  $G_{mcrit0}$  (with  $C_3$  neglected):

$$S_{\phi_n^2 0} = \frac{n C_1}{2 C_2} \cdot \frac{G_{mcrit}}{G_{mcrit0}} \cdot \frac{kT}{Q^2 |I_m|^2 R_m} \cdot \frac{\omega^2}{\Delta \omega^2}. \quad (4.117)$$

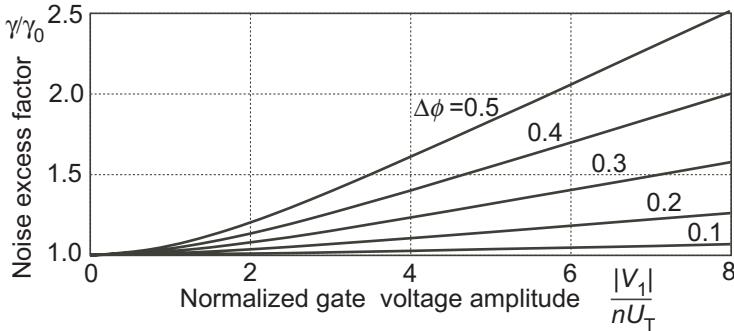
According to (3.29), this corresponds to an noise excess factor

$$\gamma_0 = \frac{n C_1}{2 C_2} \cdot \frac{G_{mcrit}}{G_{mcrit0}}, \quad (4.118)$$

which is identical to the value given by (4.110) and obtained by the linear analysis, since  $\gamma_t = 1/2$  in weak inversion. For larger amplitudes,  $\gamma$  grows proportionally to the noise spectrum contribution:

$$\gamma = \gamma_0 \frac{v_1}{I_{B1}(v_1)} \overline{I_i^2(v_1)}. \quad (4.119)$$

This variation is plotted in Fig. 4.23 for several values of phase shift  $\Delta\phi$ .



**Figure 4.23** Phase noise excess factor in weak inversion.

The increase of  $\gamma$  with the amplitude depends on the phase shift  $\Delta\phi$ . There would be no increase with  $\Delta\phi = 0$ .

#### 4.4.2.3 Effect of the White Channel Noise in Strong Inversion

The variation of the transconductance in strong inversion can be expressed by introducing in (3.56) the normalized variables  $v_e$  and  $v_1$  defined by (4.57):

$$G_m = \beta U_T (v_e + v_1 \sin(\phi + \Delta\phi)). \quad (4.120)$$

In stable oscillation, the value of  $v_e$  is independent of the amplitude, as indicated by (4.82). Hence  $\beta U_T v_e = G_{mcrit}$ , giving

$$G_m = G_{mcrit} (1 + m_v \sin(\phi + \Delta\phi)), \quad (4.121)$$

where

$$m_v = \frac{v_1}{v_e} = \frac{|V_1|}{2nU_T \sqrt{IC_0}} \leq 1 \quad (4.122)$$

is the gate voltage modulation index. Thus, from (3.60), the spectrum of the cyclostationary drain current noise is

$$\alpha_i^2 S_{I_n^2} = \underbrace{4\gamma k T n G_{mcrit}}_{S_{I_n^2}} \underbrace{(1 + m_v \sin(\phi + \Delta\phi))}_{\alpha_i^2}. \quad (4.123)$$

The squared RMS value of the effective ISF is thus

$$\overline{I_i^2(v_1)} = \frac{1}{2\pi} \int_0^{2\pi} \cos^2 \phi \cdot (1 + m_v \sin(\phi + \Delta\phi)) d\phi = \frac{1}{2}. \quad (4.124)$$

It is constant, hence the phase noise spectrum is independent of the phase shift  $\Delta\phi$  and of the amplitude of oscillation. This is true as long as the transistor remains strictly in strong inversion (i.e with  $m_v \leq 1$ ). It can easily be shown that the corresponding noise excess factor is  $\gamma = \gamma_0$  given by (4.110).

#### 4.4.2.4 Effect of the Flicker Noise in Weak Inversion

Using the approximation (3.62) of a noise voltage at the gate independent of the current, the resulting drain current noise spectrum is

$$\alpha_i^2 S_{I_n^2} = \frac{K_f G_m^2}{\omega_n} = \underbrace{\frac{K_f G_{mcrit}^2}{\omega_n}}_{K_{fi}/\omega_n} \left( \frac{v_1}{2I_{B1}(v_1)} \right)^2 \underbrace{\left( e^{v_1 \sin(\phi + \Delta\phi)} \right)^2}_{\alpha_i^2}, \quad (4.125)$$

since the transconductance is proportional to the drain current given by (4.112). The first part is the spectrum density  $K_{fi}/\omega_n$  of a fictitious stationary flicker current noise source modulated by  $\alpha_i$ .

According to (3.34), the average value of the effective ISF is then

$$\overline{I_i} = \overline{\cos \phi \cdot \alpha_i} = \frac{1}{2\pi} \int_0^{2\pi} \cos \phi \cdot e^{v_1 \sin(\phi + \Delta\phi)} d\phi. \quad (4.126)$$

Now

$$\int_0^{2\pi} \cos \phi \cdot e^{v_1 \sin(\phi + \Delta\phi)} d\phi = \sin(\Delta\phi) \int_0^{2\pi} \sin \phi \cdot e^{v_1 \sin \phi} d\phi. \quad (4.127)$$

Thus:

$$\bar{I}_i = \sin(\Delta\phi) \cdot I_{B1}(v_1). \quad (4.128)$$

The phase noise spectrum is obtained by introducing the above values of  $K_{fi}$  and  $\bar{I}_i$  in (3.36), which yields

$$S_{\phi_n^2} = \left( \frac{G_{mcrit} C_m v_1}{2C_2^2 |V_2|} \right)^2 \cdot \frac{K_f}{\Delta\omega^3} \cdot \sin^2(\Delta\phi). \quad (4.129)$$

By introducing again the expression (4.24) of the lossless transconductance  $G_{mcrit0}$  ( $C_3$  neglected) and using the good approximation  $C_2|V_2| = C_1|V_1|$ , this results becomes

$$S_{\phi_n^2} = \left( \frac{G_{mcrit}}{G_{mcrit0}} \right)^2 \left( \frac{\omega}{2QnU_T} \right)^2 \cdot \frac{K_f}{\Delta\omega^3} \cdot \sin^2(\Delta\phi), \quad (4.130)$$

which is *independent of the amplitude*. Thus the flicker noise contribution to the phase noise is independent of the amplitude, but depends on the phase shift  $\Delta\phi$ . Remember that this results is obtained with the hypotheses of a sinusoidal drain voltage and the noise model (3.62).

#### 4.4.2.5 Effect of the Flicker Noise in Strong Inversion

Using the expression (4.121) of the transconductance, the noise current drain spectrum is

$$\alpha_i^2 S_{I_n^2} = \frac{K_f G_m^2}{\omega_n} = \underbrace{\frac{K_f G_{mcrit}^2}{\omega_n}}_{K_{fi}/\omega_n} \underbrace{(1 + m_v \sin(\phi + \Delta\phi))^2}_{\alpha_i^2}. \quad (4.131)$$

The average value of the effective ISF is thus

$$\bar{I}_i = \overline{\cos \phi \cdot \alpha_i} = \frac{1}{2\pi} \int_0^{2\pi} \cos \phi \cdot (1 + m_v \sin(\phi + \Delta\phi)) d\phi = \frac{m_v}{2} \sin(\Delta\phi). \quad (4.132)$$

The phase noise spectrum is obtained by introducing the above values of  $K_{fi}$  and  $\bar{I}_i$  in (3.36):

$$S_{\phi_n^2} = \left( \frac{m_v G_{mcrit} C_m}{2C_2^2 |V_2|} \right)^2 \cdot \frac{K_f}{\Delta\omega^3} \cdot \sin^2(\Delta\phi). \quad (4.133)$$

This result is identical to (4.129), except that the normalized voltage  $v_1$  is replaced by the modulation index  $m_v = v_1/(2\sqrt{IC_0})$  (as defined by (4.122)). For strong inversion, the result (4.130) is thus changed to

$$S_{\phi_n^2} = \left( \frac{G_{mcrit}}{G_{mcrit0}} \right)^2 \left( \frac{\omega}{4QnU_T} \right)^2 \cdot \frac{1}{IC_0} \cdot \frac{K_f}{\Delta\omega^3} \cdot \sin^2(\Delta\phi). \quad (4.134)$$

For the same value of phase shift  $\Delta\phi$ , the noise spectrum is reduced by a factor  $4IC_0$  compared to weak inversion.

#### 4.4.2.6 Effect of the Noise in the Bias Current

The noise density associated with the bias current  $I_0$  is constant along the oscillation cycle, thus  $\alpha_i = 1$ . As long as the hypothesis of a sinusoidal voltage  $V_2$  is valid, the effective ISF  $\Gamma_i$  is given by (3.34).

Hence, the average value of the effective ISF is zero and no flicker noise (or other low frequency noise) is transposed around the oscillation frequency.

Still according to (3.34),  $\overline{\Gamma_i^2} = 1/2$ . The phase noise produced by the white noise content of the bias current of density  $S_{I_{nb}^2}$  is thus, from (3.33)

$$S_{\phi_n^2} = \frac{S_{I_{nb}^2}}{4(C_2|V_2|)^2 \Delta\omega^2} \cdot \frac{C_m^2}{C_2^2}. \quad (4.135)$$

Or, after replacing again  $C_2|V_2|$  by  $|I_m|/\omega$  and using (2.3) to replace  $C_m$ :

$$S_{\phi_n^2} = \frac{S_{I_{nb}^2}}{(2|I_m|C_2QR_m\Delta\omega)^2}. \quad (4.136)$$

According to (3.29), the phase noise excess factor due to bias noise is thus

$$\gamma_b = \frac{S_{I_{nb}^2}}{4kTR_m(\omega C_2)^2}. \quad (4.137)$$

The comparison with (4.108) shows that, with the hypothesis of a sinusoidal drain voltage  $V_2$ , the circuit behaves linearly with respect to the noise of the bias current  $I_0$  (as could be expected).

Now if the saturated transistor delivering the bias current is controlled by a gate voltage that is free of noise at frequencies around the oscillation

frequency, then  $S_{f_{nb}^2}$  is given by (3.60). Using the expression of the critical transconductance  $G_{mcrit0}$  of the lossless circuit and neglecting  $C_3$ , (4.137) becomes

$$\gamma_b = \gamma_t n \frac{C_1}{C_2} \cdot \frac{G_{mb}}{G_{mcrit0}}, \quad (4.138)$$

where  $G_{mb}$  is the transconductance of the biasing transistor.

This contribution to phase noise can thus be made negligible by having this transconductance much lower than  $G_{mcrit}$ , by operating the biasing transistor in strong inversion at an inversion coefficient much larger than  $IC_0$ , and by filtering out the noise at its gate for frequencies around the oscillation frequency.

## 4.5 Design Process

### 4.5.1 Design Steps

On the basis of what has been explained so far, the design of the core of a Pierce oscillator should be done according to the following steps.

#### 4.5.1.1 Selection of a Quartz Crystal or MEM Resonator

Several criteria should be considered, most of them imposed by the system. Most important are the desired frequency of oscillation and its acceptable dependency on temperature. Both have an impact on the type of resonator. For example, very low frequency is only possible with resonators oscillating in flexural mode (possibly in the form of a tuning fork), but their temperature dependency is quadratic, with a coefficient of about  $-4 \cdot 10^{-8}/^\circ\text{C}^2$ . For very high frequencies, a thickness mode is necessary, either shearing or expansion. Other criteria are cost, size, and aging properties. The quality factor  $Q$  should be as high as possible, especially to ensure a low phase noise. A good circuit design can always take advantage of its high value.

Technical data published by commercial quartz crystal vendors always include the frequency of oscillation  $\omega$  and the motional resistor  $R_m$  (or at least its maximum value). They do not always publish the third parameter needed to characterize the series resonant circuit of Fig. 2.2, namely  $Q$  or  $C_m$ . But they usually give the value of the “static capacitor”  $C_0$  across the

resonator measured as a dipole, defined by (2.1). The value of  $C_{12}$  can thus be obtained since the values of  $C_{10}$  and  $C_{20}$  are known, measurable or negligible.

Knowing  $C_{12}$ , the value of  $C_m$  is always smaller than  $C_{12}/100$  (because of the limited piezoelectric coupling coefficient of quartz). It is usually ranging between 0.1 and 0.25 this limit. Practical numerical values range from 0.5 to 5 fF for quartz resonators.

The value of  $C_m$  might be smaller for MEM resonators, due to the small value of the electrical capacitance given by (2.27). The motional resistance  $R_m$  would then be higher and the parallel capacitance  $C_3$  would be dominated by parasitic capacitances, thereby reducing the margin factor  $K_m$  defined by (4.17). In the extreme case, oscillation might not be possible with the Pierce oscillator, and alternative architectures like those discussed in Chapter 6 might be needed.

#### 4.5.1.2 Choice of Circuit Capacitances $C_1$ and $C_2$ and Estimation of $C_3$

As given by (4.21), the values of  $C_1$  and  $C_2$  essentially control the amount of frequency pulling  $p_c$  by the circuit. If  $p_c$  is increased, the frequency of oscillation moves away from the intrinsic mechanical resonant frequency of the resonator and becomes more dependent on the sustaining circuit. Frequency stability is then degraded. If  $p_c$  is reduced, (4.26) shows that the critical transconductance  $G_{mcrit}$  is increased, resulting in an increase of power consumption. The same formula shows that for a given amount of pulling,  $G_{mcrit}$  is minimum for  $C_1 = C_2$ .

As explained in Section 4.2.2,  $C_1$  and  $C_2$  must be large enough with respect to  $C_3$  to ensure a maximum value of negative resistance much larger than the motional resistance  $R_m$  ( $K_m \gg 1$ ). This is to minimize the effect of variations of  $R_m$  on the frequency of oscillation.

If the source of the transistor is grounded,  $C_3$  is usually dominated by the intrinsic parallel capacitance  $C_{12}$  of the resonator plus the drain-to-source capacitance of the transistor (that must be pre-estimated). If the drain is grounded,  $C_{10}$  (or  $C_{20}$ ) is added (see Fig. 2.2) and  $C_3$  may become much larger.

It should be pointed out that many crystal vendors do not provide the value of motional capacitor  $C_m$ , but specify instead the value of load capacitance for the specified frequency of oscillation (thereby imposing the value of  $p_c$ ). This load capacitance is the total equivalent capacitance connected in parallel with the physical resonator. Thus, for the Pierce oscillator:

$$C_{Load} \triangleq C_3 + C_s - C_0, \quad (4.139)$$

If frequency adjustment is obtained by adjusting the value of  $C_s$ , best would be to maintain  $C_1 = C_2$ . In practice, only  $C_1$  or  $C_2$  is adjusted, depending on which of the 3 nodes in grounded in the final implementation.

#### 4.5.1.3 Calculation of Pulling and Series Resonant Frequency

Knowing  $C_m$ ,  $C_1$ ,  $C_2$  and  $C_3$ , the frequency pulling  $p_c$  at the critical condition for oscillation can be calculated by (4.21), assuming a negligible effect of losses. In a good design, this effect as well as that of nonlinearities should be kept negligible. Hence the pulling  $p_s$  at stable oscillation will be very close to this value. Knowing the specified frequency of stable oscillation  $f_s$ , the exact (series) resonant frequency  $f_m$  to be specified for the resonator is given by

$$f_m \triangleq \frac{\omega_m}{2\pi} = f_s(1 - p_c). \quad (4.140)$$

#### 4.5.1.4 Calculation of the Minimum Start-up Time Constant and of the Corresponding Transconductance

The maximum possible negative resistance  $|R_{n0}|_{max}$  is given by (4.11). The minimum start-up time constant is then calculated by (3.15), and (4.13) gives the value  $G_{mopt}$  of the transconductance for which it is obtained.

#### 4.5.1.5 Calculation of the Critical Transconductance and Minimum Critical Bias Current

Assuming that  $K_m^2$  is duly much larger than unity, the lossless critical transconductance  $G_{mcrit0}$  is given by (4.24) (since the values of  $\omega$  and  $R_m$  are always available from the resonator data sheet).

After verification of the condition (4.43) with the expected values of loss conductances, the increase of critical transconductance  $\Delta G_{mcrit}$  due to theses losses can be calculated by (4.45) and added to its lossless value  $G_{mcrit0}$ .

The minimum value of critical current  $I_{critmin}$ , which would be obtained with the transistor operated in weak inversion, can be calculated by (4.64).

#### 4.5.1.6 Choice of the Amplitude of Oscillation $|V_1|$ at the Gate

If the amplitude of oscillation is too small, the output signal has to be amplified to be used in the system. As will be shown later, the input admittance of the amplifier may have a real part proportional to its voltage gain, which adds losses in the oscillator. Moreover, the input referred noise of the amplifier is transformed into a component of phase noise. Furthermore, according to (4.94), the energy of oscillation is proportional to  $|V_1^2|$ . Thus, according to (3.30), a too small value of  $|V_1|$  may result in an unacceptable level of phase noise around the frequency of oscillation.

If the amplitude of oscillation is too large, the power dissipated in the resonator ( given by (4.95)) can exceed the acceptable limit, resulting in excessive aging or even breaking of the resonator. Moreover, a large amplitude of oscillation requires a large value of supply voltage to maintain the active transistor in saturation, in order to avoid additional losses and a degradation of frequency stability.

#### 4.5.1.7 Calculation of Power

The power dissipated in the resonator is obtained by (4.95). This is always possible since  $\omega$  and  $R_m$  are always known. The result must then be compared with the maximum acceptable value, as given by the vendor.

#### 4.5.1.8 Choice of the Amount of Overdrive

As illustrated by Fig. 4.17 (or by Fig. 4.16), the overdrive current ratio  $I_0/I_{0crit}$  necessary to obtain a given amplitude can be controlled by  $IC_0$ , the inversion coefficient of the transistor at  $I_{0crit}$  (or by  $k_c$ , the attenuation of the capacitive divider of Fig. 4.16).

A small amount of overdrive should be chosen to minimize the nonlinear effects. This is needed to reduce the risk of oscillation on an unwanted mode, as discussed in Section 4.3.6. It is also needed for a good frequency stability, as explained in Section 4.3.5.3a.

But Fig. 4.17 also shows that the larger the overdrive, the smaller the bias current necessary to obtain a given amplitude. Indeed, the absolute minimum is obtained when the transistor is weak inversion.

#### 4.5.1.9 Calculation of Critical Current, Bias Current and Specific Current of the Transistor

Once the choice of  $IC_0$  has been made, the critical current of oscillation (bias current for zero amplitude) is obtained from (4.73) and (4.64):

$$I_{0crit} = I_{0critmin} \frac{\sqrt{IC_0}}{1 - e^{-\sqrt{IC_0}}}. \quad (4.141)$$

It is simply  $k_c \cdot I_{0critmin}$  in weak inversion with a capacitive attenuator as in Fig. 4.15.

The bias current needed to obtain the expected amplitude is then be obtained by inspecting Fig. 4.17 (or Fig. 4.16).

Knowing  $I_{0crit}$  and  $IC_0$ , the specific current of the transistor is obtained from the definition (4.72) of  $IC_0$ :

$$I_{spec} = I_{0crit}/IC_0. \quad (4.142)$$

#### 4.5.1.10 Calculation of the Active Transistor

The width-to-length ratio of the active transistor  $W/L$  is obtained from the definition (3.41) of  $I_{spec}$ .

To avoid additional losses due to the output conductance  $G_{ds}$ , the intrinsic voltage gain of the transistor given by (3.58) should be much larger than unity. Thus, the channel length  $L$  should be more than the minimum possible, to ensure an acceptable value of  $V_M$ .

Knowing the values of  $L$  and  $W$ , the gate capacitance can be calculated to verify that it is only a small fraction of  $C_1$ , since it is voltage dependent.

The voltage-dependent drain capacitance is proportional to  $W$ , and should only be a small fraction of  $C_2$ .

The drain to gate capacitance is also proportional to  $W$ . It must be included in the value of  $C_3$ .

#### 4.5.1.11 Calculation of Energy and Phase Noise

The energy of oscillation in the resonator is given by 4.94. Its calculation requires the value of  $C_m$  or an approximation of it.

The phase shift  $\Delta\phi$  is obtained from the approximation (4.111).

In strict strong inversion, the noise excess factor due to the active transistor alone is just the small amplitude value given by (4.110). In weak inversion, it increases with the amplitude as expressed by (4.119). It should be augmented to include the noise component of the bias current as discussed in Section (4.4.2.6). The phase noise spectrum due white noise sources can then be calculated by (3.30).

The component of phase noise due to the flicker noise of the active transistor is calculated by (4.130) in weak inversion, and by (4.134) in strong inversion.

Overall, and due to the very large values of quality factor  $Q$ , the phase noise of the quartz oscillator itself is negligible in many applications.

#### 4.5.1.12 Final Complete Design

The next design steps will be to select which of the three points of the basic circuit is grounded, to define a bias scheme (including the very important amplitude limitation) and to design the output circuitry that is usually an amplifying stage. These steps will be discussed in Chapter 5.

#### 4.5.2 Design Examples

The design process summarized in the previous section will now be illustrated by two examples with two different quartz resonators. Their characteristics are given in Table 4.1.

The quartz of Example 1 is a typical miniaturized wristwatch tuning fork. Its flexural mode in X+5 cut gives a quadratic temperature behavior ( $3.5 \cdot 10^{-8}/^{\circ}\text{C}^2$ , with a maximum around  $25^{\circ}\text{C}$ ). The quartz of Example 2 is a high frequency AT cut inverted mesa, with a cubical temperature behavior. It has a lower minimum value of quality factor  $Q$  and oscillates in fundamental mode.

Table 4.2 gives the main data of the process to be used in these examples. It is a typical  $0.18\mu\text{m}$  process. Note that, except for the threshold  $V_{T0}$ , only the nominal values are given; the final design should be checked for the worst case by computer simulation.

The successive design steps of Section 4.5.1 are presented in Table 4.3.

The quartz data do not provide the value of  $C_{12}$  defined in Fig. 2.2(a). Instead, they only give the lumped parallel capacitance  $C_0$  defined by (2.1) (quartz considered as a dipole). To consider the worst case in Step 2, we

	Param.	Example 1	Example 2	Unit
exact osc.frequency	$f_s$	32768.00	$50.00000 \cdot 10^6$	Hz
approximation	$\omega$	$2.06 \cdot 10^5$	$3.14 \cdot 10^8$	1/s
max. resistance	$R_m$	$42 \cdot 10^3$	100	$\Omega$
motional capacitance	$C_m$	$2.1 \cdot 10^{-15}$	$2.7 \cdot 10^{-15}$	F
min. quality factor	$Q$	55100	11800	
parallel capacitance	$C_0$	$0.9 \cdot 10^{-12}$	$2.4 \cdot 10^{-12}$	F
max. power	$P_{max}$	$10^{-6}$	$10^{-4}$	W

**Table 4.1** Quartz crystal data.

parameter	N-channel	P-channel	unit
$kT$	$4.16 \cdot 10^{-21}$	$4.16 \cdot 10^{-21}$	J
$U_T$	$26 \cdot 10^{-3}$	$26 \cdot 10^{-3}$	V
$n$	1.30	1.35	
$I_{spec}$ (for $L = W$ )	$0.50 \cdot 10^{-6}$	$0.20 \cdot 10^{-6}$	A
$V_{T0}$	$0.45 \pm 0.1$	$0.45 \pm 0.1$	V
$C_{ox}$	$8.50 \cdot 10^{-3}$	$8.50 \cdot 10^{-3}$	$F/m^2$
$C_d/W$	$0.90 \cdot 10^{-9}$	$1.05 \cdot 10^{-9}$	$F/m$
$C_{gd}/W$	$0.36 \cdot 10^{-9}$	$0.33 \cdot 10^{-9}$	$F/m$
$V_M/L$	$30 \cdot 10^6$	$40 \cdot 10^6$	$V/m$
$WLK_f$	$2 \cdot 10^{-22}$		$m^2V^2$

**Table 4.2** Process data.

assume that  $C_{12} = C_0$  to evaluate the value of  $C_3$ . Only a very small additional capacitor due to interconnects is assumed for the more critical high frequency quartz.

Step 3 assumes that the amount of pulling  $p_s$  in stable oscillation is not modified by losses or by nonlinear effects, hence  $p_s = p_c$ . It provides the exact value of the resonant frequency  $f_m$ .

The maximum negative resistance obtained in Step 4 is much larger than  $R_m$  for Example 1. It is sufficiently larger ( $K_m^2 = 20.7 \gg 1$ ) for Example 2 to validate the approximations of  $p_c$  by (4.21) and of  $G_{mcrit0}$  by (4.24). From the values obtained for  $\tau_{0min}$ , the minimum start-up times (ranging between  $7\tau_{0min}$  and  $15\tau_{0min}$ ) are 0.16 to 0.35 s and 0.15 to 0.32 ms. These values will be larger if the transconductance at start-up is smaller (or larger) than the calculated value of  $G_{mopt}$ .

In Step 5, estimated values of loss conductances are introduced.  $G_1$  accounts for the load by the output amplifier.  $G_2$  is essentially the output conductance of the saturated transistor and that of the driving current source.  $G_3$  will be mainly due to the device biasing the gate. All these value will have

to be verified during the final design stage, and corrected if necessary. The increase of critical transconductance  $\Delta G_{mcrit}$  is calculated by the approximation (4.45) after verification of the condition (4.43).

In Step 6, the amplitude of oscillation is chosen sufficiently low to be compatible with a supply voltage below 1.5V. For Example 2, it is also limited to maintain the power  $P_m$  dissipated in the resonator (Step 7) below its maximum acceptable value  $P_{max}$ . The drain voltage amplitude  $|V_2|$  is obtained by (4.35).

The choice of the inversion coefficient  $IC_0$  is made in Step 8. In Example 1, the noise is not critical and the risk of exciting unwanted overtones is small. Hence, a reasonably large overdrive is acceptable, and  $IC_0 = 1$  is chosen to achieve the minimum possible bias current. The transistor is thus approximately in weak inversion.

Nonlinear effects must be limited in Example 2, essentially to minimize the phase noise. The choice is then  $IC_0 = 64$ , resulting in an overdrive  $I_0/I_{0crit} = 1.078$ , as calculated in Step 9.

In Step 9, the critical current  $I_{0crit}$  is calculated by (4.141) and the bias current  $I_0$  is obtained from Fig. 4.17 (or calculated by (4.86) for Example 2).

In Step 10, a long channel length  $L$  is chosen for Example 1, to render the output conductance  $G_{ds}$  totally negligible. The length is reduced in Example 2 to avoid a too large width  $W$ . As a consequence, the value of  $G_{ds}$  is the main part of  $G_2$ . Calculation of the various (voltage-dependent) capacitors of the transistor show that they are all negligible with respect to  $C_1$ ,  $C_2$  and  $C_3$ .

In Step 11, the noise excess factor  $\gamma$  is equal to its small amplitude value  $\gamma_0$  in strong inversion (Example 2). It does not include the noise contribution of the current source  $I_0$ . But even if  $\gamma$  is increased by a factor 10, thereby increasing the noise by about 10dB, the phase noise remains very low.

The noise included in  $I_0$  is not modulated by the active transistor. Hence its low-frequency noise content is not shifted around  $f_s$ .

Notice that the resulting phase noise is expressed in dBc/Hz (decibel relative to the carrier) for  $\Delta f = 1\text{kHz}$ . With negligible amplitude noise, this is about equivalent to radian<sup>2</sup>/Hz.

step	variable	Example 1	Example 2	unit	ref.
2	$C_1$	$20 \cdot 10^{-12}$	$15 \cdot 10^{-12}$	F	
	$C_2$	$20 \cdot 10^{-12}$	$15 \cdot 10^{-12}$	F	
	$C_3$	$2.0 \cdot 10^{-12}$	$2.6 \cdot 10^{-12}$	F	
	$C_s$	$10 \cdot 10^{-12}$	$7.5 \cdot 10^{-12}$	F	(4.9)
3	$p_c$	$87.5 \cdot 10^{-6}$	$134 \cdot 10^{-6}$		(4.21)
	$f_m$	32765.13	$49.99332 \cdot 10^6$	Hz	(4.140)
4	$ R_{n0} _{max}$	$1.01 \cdot 10^6$	455	$\Omega$	(4.11)
	$K_m$	24.1	4.55		(4.17)
	$\tau_{0min}$	$23.2 \cdot 10^{-3}$	$21.2 \cdot 10^{-6}$	s	(3.15)
	$G_{mopt}$	$49.4 \cdot 10^{-6}$	$36.6 \cdot 10^{-3}$	A/V	(4.13)
5	$G_{mcrit0}$	$1.03 \cdot 10^{-6}$	$4.03 \cdot 10^{-3}$	A/V	(4.24)
	$G_1$	$0.10 \cdot 10^{-6}$	$0.20 \cdot 10^{-3}$	A/V	
	$G_2$	$0.01 \cdot 10^{-6}$	$0.20 \cdot 10^{-3}$	A/V	
	$G_3$	$0.10 \cdot 10^{-6}$	$0.20 \cdot 10^{-3}$	A/V	
	$\Delta G_{mcrit}$	$0.51 \cdot 10^{-6}$	$1.20 \cdot 10^{-3}$	A/V	(4.45)
	$G_{mcrit}$	$1.54 \cdot 10^{-6}$	$5.23 \cdot 10^{-3}$	A/V	(4.39)
	$I_{0critmin}$	$51.9 \cdot 10^{-9}$	$0.177 \cdot 10^{-3}$	A	(4.64)
6	$ V_1 /nU_T$	4.00	6.00		
	$ V_1 $	$135 \cdot 10^{-3}$	$203 \cdot 10^{-3}$	V	
	$ V_2 $	$145 \cdot 10^{-3}$	$309 \cdot 10^{-3}$	V	(4.35)
	$ V_3 $	$276 \cdot 10^{-3}$	$472 \cdot 10^{-3}$	V	(4.37)
7	$E_m$	$2.51 \cdot 10^{-9}$	$3.11 \cdot 10^{-9}$	J	(4.94)
	$P_m$	$9.37 \cdot 10^{-9}$	$82.8 \cdot 10^{-6}$	W	(4.95)
8	$IC_0$	1	64		
	$I_0/I_{0critmin}$	2.70	8.6		Fig. 4.17
9	$I_{0crit}$	$82.1 \cdot 10^{-9}$	$1.41 \cdot 10^{-3}$	A	(4.141)
	$I_0$	$140 \cdot 10^{-9}$	$1.52 \cdot 10^{-3}$	A	
	$I_{spec}$	$82.1 \cdot 10^{-9}$	$22.1 \cdot 10^{-6}$	A	(4.142)
10	$W/L$	0.164	44.2		(3.41)
	$L$	$6.00 \cdot 10^{-6}$	$1.00 \cdot 10^{-6}$	m	
	$W$	$0.985 \cdot 10^{-6}$	$44.2 \cdot 10^{-6}$	m	
	$V_M$	180	30	V	
	$G_{ds}$	$0.78 \cdot 10^{-9}$	$50.6 \cdot 10^{-6}$	A/V	(3.57)
	$C_g$	$50 \cdot 10^{-15}$	$376 \cdot 10^{-15}$	F	
	$C_d$	$0.88 \cdot 10^{-15}$	$39.8 \cdot 10^{-15}$	F	
	$C_{gd}$	$0.36 \cdot 10^{-15}$	$15.9 \cdot 10^{-15}$	F	
11	$\Delta\phi$	0.376	0.837	rad	(4.111)
	$\gamma_0$	0.973	1.12		(4.110)
	$\gamma$	1.31			Fig.4.23
	$S_{\Phi_n^2/f^2}$ at 1k	-187	-150	dBc/Hz	(3.30)
	$S_{\Phi_n^2/f^3}$ at 1k	-189		dBc/Hz	(4.130)
	$S_{\Phi_n^2/f^3}$ at 1k		-140	dBc/Hz	(4.134)

Table 4.3 Design calculations.

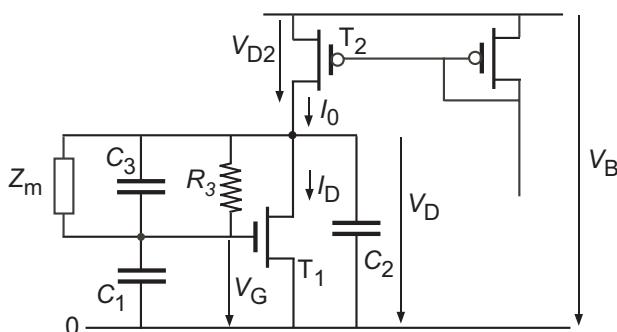
# Chapter 5

## Implementations of the Pierce Oscillator

### 5.1 Grounded-Source Oscillator

#### 5.1.1 Basic Circuit

Grounding the source of the active transistor results in the basic oscillator circuit depicted in Fig. 5.1. Transistor  $T_2$  is part of a current mirror that delivers the bias current  $I_0$  to the active transistor  $T_1$ . The latter is maintained in active mode by a resistor  $R_3$  that forces the DC component  $V_{D0}$  of the drain voltage  $V_D$  to be equal to the DC component  $V_{G0}$  of the gate voltage  $V_G$  (since no current is flowing through  $R_3$ ).



**Figure 5.1** Basic grounded source oscillator.

To avoid unnecessary losses, both transistor must remain saturated all along the oscillation cycle.

If  $T_1$  is in *weak inversion*, it remains saturated as long as  $V_D > 5U_T$ , according to (3.46). Since  $V_{Dmin} = V_{D0} - |V_2|$ , the minimum acceptable value of threshold voltage can be expressed as

$$V_{T0} > 5U_T + |V_2| - (V_{D0} - V_{T0}), \quad (5.1)$$

where  $(V_{D0} - V_{T0})$  is given by (4.68) for  $V_{D0} = V_{G0}$ . The drain amplitude  $|V_2|$  is related to the gate amplitude  $|V_1|$  by (4.35). Some additional margin should be provided to account for nonlinear effects that result in slightly larger negative half periods of drain voltage.

For  $T_1$  is in *strong inversion*, the minimum value of drain voltage ensuring saturation is given by (3.47). By introducing the DC components  $V_{G0}$  and  $V_{D0}$  and the complex voltages  $V_1$  and  $V_2$  at the gate and at the drain, this condition becomes

$$V_{T0} > |V_1 - nV_2| + V_{G0} - nV_{D0}. \quad (5.2)$$

For  $V_{D0} = V_{G0}$ , it may be rewritten to express the minimum acceptable threshold voltage:

$$V_{T0} > \frac{1}{n} [|V_1 - nV_2| - (n-1)(V_{G0} - V_{T0})]. \quad (5.3)$$

The first term in the square parenthesis can be related to  $|V_1|$  by using (4.35):

$$|V_1 - nV_2| = |V_1| \sqrt{\frac{(nG_1 + G_2 + nG_{mcrit})^2 + \omega^2(nC_1 + C_2)^2}{G_2^2 + (\omega C_2)^2}}. \quad (5.4)$$

The value  $V_{G0} - V_{T0}$  for a given value of AC amplitude  $|V_1|$  can be obtained from Fig. 4.18 or from (4.82) for strict strong inversion. To ensure that the active transistor remains saturated along the whole oscillation cycle, the minimum threshold guaranteed for the process should fulfill condition (5.3). If this condition is not fulfilled, the circuit should be modified to obtain a DC component of drain voltage larger than  $V_{G0}$ , as will be discussed in Section 5.1.6.

For a given amplitude of oscillation  $|V_2|$ , the minimum value of supply voltage  $V_B$  is limited by the need to maintain the P-channel biasing transistor  $T_2$  in saturation:

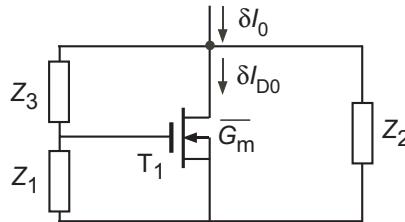
$$V_B > V_{D0} + |V_2| + V_{D2sat}, \quad (5.5)$$

where  $V_{D2sat}$  is the saturation drain voltage of  $T_2$  given by (3.47) (with  $V_S = 0$ ) if it is in strong inversion. It has a minimum value given by (3.46)

obtained in weak inversion. Hence, if its width does not become too large, this transistor should have a specific current larger than the bias current  $I_0$  to reduce the minimum value of  $V_B$ . But, according to (4.138), the noise contribution of  $T_2$  is then no longer negligible. The drain amplitude  $|V_2|$  is related to the gate amplitude by (4.35) and the DC component of drain voltage  $V_{D0} = V_{G0}$  can be found in Fig. 4.18, using the maximum value of  $V_{T0}$  for the process considered.

### 5.1.2 Dynamic Behavior of Bias

If the bias current  $I_0$  is constant, then the DC component of drain current  $I_{D0}$  has the same value. But if there are variations of  $I_0$ , they are not followed immediately by  $I_{D0}$ . Let us consider the equivalent circuit the oscillator driven by small variations of the bias current, as shown in Fig. 5.2.  $\delta I_0$  and  $\delta I_{D0}$



**Figure 5.2** Calculation of the bias transfer function.

are now complex variables representing small variations of  $I_0$  and  $I_{D0}$ . The (angular) frequency  $\Omega$  of these variations is supposed to be much smaller than  $\omega_m$ , hence the motional impedance can be neglected (since  $C_m \ll C_1$ ). It can easily be shown that

$$\frac{\delta I_{D0}}{\delta I_0} = \frac{G_m Z_1 Z_2}{Z_1 + Z_2 + Z_3 + \overline{G_m} Z_1 Z_2}, \quad (5.6)$$

where  $\overline{G_m}$  is the average value of transconductance along each oscillatory cycle. It has the value

$$\overline{G_m} = \frac{I_0}{nU_T} \text{ (in weak inv.)} \quad \text{and} \quad \overline{G_m} = G_{mcrit} \text{ (in strict strong inv.)}, \quad (5.7)$$

since it is proportional to the drain current in weak inversion and varies linearly with the gate voltage in strong inversion.

Calculating (5.6) for the general case with real and imaginary parts of the impedances would result in a complicated expression, so it should be computed numerically. But let us consider lossless capacitive impedances  $Z_1, Z_2$  (as in the example of Fig. 5.1), and neglect  $C_3$ , thus  $Z_3 = R_3$ . This expression becomes, in the s-domain

$$\frac{\delta I_{D0}}{\delta I_0} = \frac{\overline{G_m}}{s^2 C_1 C_2 R + s(C_1 + C_2) + \overline{G_m}}. \quad (5.8)$$

For  $G_m R_3 \gg (C_1 + C_2)^2 / (C_1 C_2)$ , the roots of the denominator are conjugate complex, thus this expression can be rewritten as

$$\frac{\delta I_{D0}}{\delta I_0} = \frac{\Omega_0^2}{s^2 + s\Omega_0/Q_b + \Omega_0^2}. \quad (5.9)$$

This transfer function has a resonant peak at frequency

$$\Omega_0 = \sqrt{\frac{\overline{G_m}}{R_3 C_1 C_2}} \quad (5.10)$$

In stable oscillation,  $\overline{G_m} \geq G_{mcrit0}$ , hence by introducing the expression (4.24) of  $G_{mcrit0}$  (and neglecting  $C_3$ ), (5.10) becomes

$$\Omega_0 \geq \omega_m \sqrt{\frac{R_m}{R_3}}, \quad (5.11)$$

showing that the bias resistance  $R_3$  must be much larger than the motional resistance  $R_m$  to obtain a resonant frequency of the bias circuit much lower than the frequency of oscillation.

The quality factor of this resonant circuit is

$$Q_b = \sqrt{\frac{\overline{G_m} R_3 C_1 C_2}{(C_1 + C_2)^2}} = \underbrace{\sqrt{\overline{G_m} R_3 / 4}}_{\text{for } C_1 = C_2}. \quad (5.12)$$

So, without  $C_3$  the resonant peak could be very large, since  $R_3 \gg 1/G_m$  to limit the loss conductance  $G_3$ . However,  $C_3$  strongly attenuates this peak as soon as its impedance at  $\Omega_0$  is comparable to  $R_3$ , which occurs if

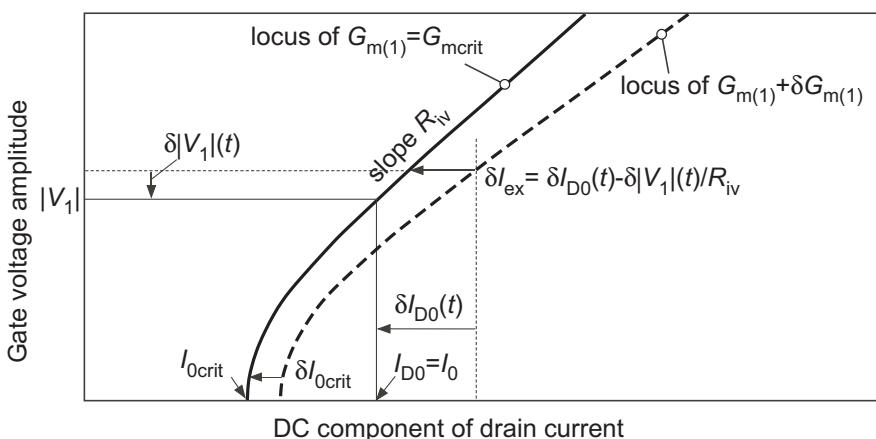
$$C_3 \cong \sqrt{\frac{C_1 C_2}{\overline{G_m} R_3}} = \frac{C_s}{Q_b}. \quad (5.13)$$

so the higher the peak without  $C_3$ , the more it is attenuated by  $C_3$ . For example, with  $C_1 = C_2$  and  $C_3 = C_1/10$ , the maximum peak is only 1.43 and occurs for  $G_m R_3 \cong 30$  (where it would be 2.74 with  $C_3 = 0$  according to (5.12)). For  $C_3 = C_1/100$ , the maximum peak is 3.62 and occurs for  $G_m R_3 \cong 200$  (where it would be 7.07 with  $C_3 = 0$ ). Thus, with usual values of  $C_3/C_1$ , the peak is never very large. However, just above the peak frequency, the phase always reaches at least 90 degrees, which may have consequences on the stability of an amplitude regulating loop, as will be seen further.

### 5.1.3 Dynamic Behavior of Oscillation Amplitude

For a constant DC component of drain current  $I_{D0} = I_0$ , stable oscillation is reached with a gate amplitude  $|V_1|$  as plotted in Fig. 4.17 (or Fig. 4.16). At this point the negative resistance  $R_n$  produced by the circuit compensates exactly the motional resistance  $R_m$  of the resonator, and the time constant of growth (or decay)  $\tau$  defined by (3.3) is infinite.

Now, if at some time  $I_{D0}$  differs from this stable point by an amount  $\delta I_{D0}(t)$ , the instantaneous value of amplitude will depart by an amount  $\delta|V_1|(t)$  from its stable value, as illustrated by Fig. 5.3.



**Figure 5.3** Calculation of the dynamic behavior of the oscillation amplitude.

As shown by the figure, this produces an instantaneous excess of current  $\delta I_{ex}$  (that would tend to zero if  $\delta I_{D0}(t)$  would remain constant). Since all these variables are time dependent, we can express them in the s-domain as:

$$\delta I_{ex} = \delta I_0 - \delta |V_1| / R_{iv} \quad (5.14)$$

where resistance  $R_{iv}$  is the slope of the  $|V_1|/I_0$  curve corresponding to stable oscillation. According to (4.55), this curve is the locus of  $G_{m(1)} = G_{mcrit}$ , where  $G_{m(1)}$  is the effective transconductance including the effect of nonlinearity of the transistor. The small excess current  $\delta I_{ex}$  produces an increase of transconductance  $\delta G_{m(1)}$ , thus in the s-domain:

$$\delta G_{m(1)} = k_1 \delta I_{ex}, \quad (5.15)$$

where

$$k_1 \triangleq \frac{dG_{m(1)}}{dI_{ex}} \quad (5.16)$$

This increase of  $G_{m(1)}$  is the same as what would be obtained by an increase  $\delta I_{0crit}$  of the critical transconductance, as illustrated by the curve in interrupted line. Since  $G_{m(1)} = G_m$  at  $I_{0crit}$ , the coefficient  $k_1$  can therefore be expressed as

$$k_1 = \frac{dI_{0crit}}{dI_{ex}} \cdot \frac{dG_m}{dI_D} \Big|_{I_D=I_{0crit}} = \frac{I_{0crit}}{I_0} \cdot \frac{1}{2nU_T} \left( \frac{1 - e^{-\sqrt{IC_0}}}{\sqrt{IC_0}} + e^{-\sqrt{IC_0}} \right) \quad (5.17)$$

by using expression (3.55) of the transconductance  $G_m$ . In weak inversion,  $I_0/I_{0crit}$  is given by (4.65) and  $IC_0 \ll 1$ ; (5.17) then becomes

$$k_1 = \frac{2I_{B1}(v_1)}{|V_1|I_{B0}(v_1)} \quad (\text{weak inversion}) \quad (5.18)$$

It must be remembered that  $G_{m(1)} = G_{mcrit} = G_{mcrit0} + \Delta G_{mcrit}$  is the value of transconductance needed to produce a negative resistance  $R_n$  equal the motional resistance  $-R_m$ . Then, if the increase of critical transconductance  $\Delta G_{mcrit}$  due to losses is constant, from (4.24):

$$k_2 \triangleq -\frac{dR_n}{dG_{m(1)}} = \frac{R_m}{G_{mcrit0}} = \frac{1}{\omega^2 C_1 C_2 (1 + C_3/C_s)^2}. \quad (5.19)$$

Thus, the excess current  $\delta I_{ex}$  produces a net excess of negative resistance given by

$$\delta R_n = \frac{dR_n}{dG_{m(1)}} \cdot \frac{dG_{m(1)}}{dI_{ex}} \delta I_{ex} = -k_1 k_2 \delta I_{ex} \quad (5.20)$$

The time constant  $\tau$  given by (3.3) is then no longer infinite but, by introducing (5.20) and (5.14)

$$\frac{1}{\tau(s)} = \frac{\delta R_n}{-2L_m} = \frac{k_1 k_2}{2L_m} \left( \delta I_0 - \frac{\delta |V_1|}{R_{iv}} \right), \quad (5.21)$$

where all variables are in the s-domain. The exponential growth of gate voltage amplitude can be expressed in the time domain as

$$\frac{d(\delta |V_1|)}{dt} = \frac{|V_1|}{\tau}, \quad (5.22)$$

which becomes, in the s-domain

$$s \delta |V_1| = \frac{|V_1|}{\tau(s)} = K_{iv} \left( \delta I_0 - \frac{\delta |V_1|}{R_{iv}} \right), \quad (5.23)$$

where

$$K_{iv} = \frac{k_1 k_2 |V_1|}{2L_m} = \frac{k_1 k_2 \omega^2 C_m |V_1|}{2}. \quad (5.24)$$

Solving (5.23) for  $\delta |V_1|$  gives low-pass the transfer function for the amplitude of oscillation

$$\frac{\delta |V_1|}{\delta I_{D0}} = \frac{K_{iv}}{s + \Omega_{civ}}, \quad (5.25)$$

where

$$\Omega_{civ} = K_{iv}/R_{iv} \quad (5.26)$$

is the cut-off frequency. The differential resistance  $R_{iv}$  is related to the slope  $s_{iv}$  of the normalized function of Fig. 4.17 (or Fig. 4.16) by

$$R_{iv} = s_{iv}/G_{mcrit}. \quad (5.27)$$

The expressions (5.17) of  $k_1$  and (5.19) of  $k_2$  can be introduced in (5.24), which gives

$$K_{iv} = \frac{|V_1|}{4nU_T} \cdot \frac{I_{0crit}}{I_0} \cdot \frac{C_m}{C_1 C_2 (1 + C_3/C_s)^2} \cdot \left( \frac{1 - e^{-\sqrt{IC_0}}}{\sqrt{IC_0}} + e^{-\sqrt{IC_0}} \right), \quad (5.28)$$

where the term in parenthesis changes from 2 in weak inversion to  $1/\sqrt{IC_0}$  in strong inversion. For the lossless case,  $G_{mcrit} = G_{mcrit0} = R_m/k_2$  according to (5.19). The cut-off frequency can then be expressed from (5.26) as

$$\Omega_{civ} = \frac{\omega}{4Qs_{iv}} \cdot \frac{|V_1|}{nU_T} \cdot \frac{I_{0crit}}{I_0} \cdot \left( \frac{1 - e^{-\sqrt{IC_0}}}{\sqrt{IC_0}} + e^{-\sqrt{IC_0}} \right) \quad (\text{lossless case}). \quad (5.29)$$

It is proportional to the frequency of oscillation and inversely proportional to the quality factor  $Q$  of the resonator. The amplitude of oscillation follows the variations of the drain current for frequencies lower than  $\Omega_{civ}$ , with the transresistance  $R_{iv}$ . Beyond this frequency, the transfer function is that of an integrator  $K_{iv}/s$  and the variations are attenuated. However, they are shifted by 90 degrees, which may endanger the stability of an amplitude regulating loop. As can be seen in (5.28), this integrating behavior does not depend on the frequency of oscillation nor on the quality factor of the resonator.

### 5.1.4 Design Examples

Table 5.1 shows the values obtained for the implementation of the two examples introduced in Section 4.5.2 (Tables 4.1 and 4.2), using the results of Table 4.3. For the calculation of the minimum value of the N-channel threshold ensuring saturation of the active transistor, weak inversion has been assumed for Example 1 with  $V_{Dsat} = 5U_T$ , and strong inversion for Example 2. Both results are lower than the minimum value of 0.35 V guaranteed for the process.

To minimize the value of supply voltage  $V_B$  in Example 1, the bias transistor  $T_2$  is operated at an inversion coefficient  $IC_2 = 1$  for which a value of  $V_{Dsat} = 150 \text{ mV}$  is assumed. The minimum supply voltage is then only 0.86 V in the worst case of maximum threshold. Such a low value of  $IC_2$  would have required an excessively large transistor ( $W=2.3 \text{ mm}$ ) in Example 2. Therefore, the inversion coefficient has been increased to 10, with the result of an increase of saturation voltage. Combined with the large inversion coefficient of the active transistor and with the larger amplitude of oscillation, it increases the minimum value of  $V_B$  to 1.62 V in the worst case. Of course, the oscillator would still work under this limit, but the amplitude of oscillation would be limited by losses due to the output conductance of  $T_2$ , with the negative consequences discussed in Section 4.3.5.

Even if the gate voltage of the biasing transistor  $T_2$  is free of noise, the contribution  $\gamma_b$  of the bias current noise is not negligible. It increases the phase noise by 2 dB in Example 1 and 4 dB in Example 2.

Sizing the bias transistor is easy in Example 1. In Example 2, the channel length  $L$  has been selected as short as possible while keeping a value of output conductance  $G_{ds}$  smaller than the estimated value of  $G_3$ . Because of the large current, a very wide transistor is however needed to limit the inversion coefficient at a large value of current. For both examples, the added

variable	Example 1	Example 2	unit	ref.
$ V_1 - nV_2 $	$319 \cdot 10^{-3}$	$561 \cdot 10^{-3}$	V	(5.4)
$V_{T0min}$	$321 \cdot 10^{-3}$	$307 \cdot 10^{-3}$	V	(5.1),(5.3)
$IC_2$	1.00	10.0	V	choice
$V_{D2sat}$	$150 \cdot 10^{-3}$	$200 \cdot 10^{-3}$	V	(3.46),(3.47)
$V_{Bmin}$	0.86	1.62	V	(5.5)
$G_{mb} = G_{m2}$	$2.52 \cdot 10^{-6}$	$13.1 \cdot 10^{-3}$	A/V	(3.55)
$\gamma_b$	1.66	2.93		(4.138)
$\gamma_0 + \gamma_b$	2.97	4.05		
$S_{\Phi_n^2/f^2}$ at 1kHz	-185	-146	dBc/Hz	(3.30)
$I_{spec2}$	$1.40 \cdot 10^{-7}$	$1.52 \cdot 10^{-4}$	A	(3.45)
$W_2/L_2$	0.7	760		(3.41)
$L_2$	$4 \cdot 10^{-6}$	$3 \cdot 10^{-7}$	m	choice
$W_2$	$2.8 \cdot 10^{-6}$	$228 \cdot 10^{-6}$	m	
$V_{M2}$	160	$12 \cdot 10^{-6}$	V	
$G_{ds2}$	$0.88 \cdot 10^{-9}$	$0.13 \cdot 10^{-3}$	A/V	(3.57)
$C_{d2}$	$2.94 \cdot 10^{-15}$	$239 \cdot 10^{-15}$	F	
$C_{gd2}$	$0.92 \cdot 10^{-15}$	$75.2 \cdot 10^{-15}$	F	
$R_3$	$1.00 \cdot 10^7$	$5.00 \cdot 10^3$	V/A	choice
$G_m$	$4.14 \cdot 10^{-6}$	$5.23 \cdot 10^{-3}$	A/V	(5.7)
$\Omega_0$	$32.0 \cdot 10^3$	$68.2 \cdot 10^6$	1/s	(5.10)
$\Omega_b$	3.22	2.55		(5.12)
$s_{iv}$	2.05	5.33		Fig. 4.17
$R_{iv}$	$1.34 \cdot 10^6$	$1.02 \cdot 10^3$	V/A	(5.27)
$K_{iv}$	$2.14 \cdot 10^6$	$1.16 \cdot 10^6$	V/As	(5.28)
$\Omega_{civ}$	1.60	$1.13 \cdot 10^3$	1/s	(5.26)

**Table 5.1** Examples of practical implementations of the basic grounded source oscillator.

parasitic capacitors (drain and drain-to-gate) can be considered negligible with respect to  $C_2$ .

The only component of loss conductance  $G_3$  is the drain-to-gate bias resistor, so  $R_3 = 1/G_3$ . The resulting resonance of the bias circuit occurs at a frequency sufficiently lower than the oscillation frequency.

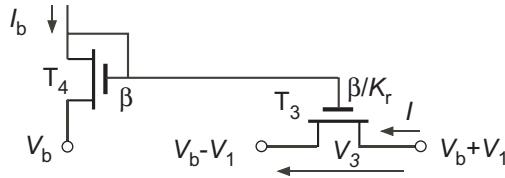
The maximum frequency for which the amplitude of oscillation follows the variations of drain current ( $\Omega_{civ}$ ) is very low. Hence, these variations are strongly attenuated at frequencies for which the phase is increased beyond 180 degrees by the other poles in a amplitude regulation loop. This will be needed to ensure the stability of this loop.

### 5.1.5 Implementation of the Drain-to-Gate Resistor

The drain-to-gate resistor  $R_3$  in the basic grounded-source oscillator of Fig. 5.1 is needed to bias the active transistor  $T_1$  in saturation. Its value must be sufficiently large to limit the loss conductance  $G_3$  (but not too large, in order to keep  $\Omega_0 \gg \Omega_{civ}$ ).

Many processes do not provide any possibility to implement a real resistor. When they do, the sheet resistivity is usually high enough to implement the few kilohms needed in Example 2 above. But it is usually much to small to implement the  $10\text{M}\Omega$  resistors of Example 1 on a acceptable area.

A possibility to replace a linear resistor by a transistor is illustrated in Fig. 5.4. It is applicable when the imaginary part of (4.38) relating the AC drain voltage  $V_2$  to the AC gate voltage  $V_1$  is much smaller than unity. Then  $V_2 = -V_1$  if  $C_2 = C_1$ .



**Figure 5.4** Implementation of a linear resistive element by a transistor.

The voltage  $V_3 = 2V_1$  across transistor  $T_3$  varies symmetrically with respect to some constant voltage  $V_b$ . This voltage is applied at the source of the associated transistor  $T_4$ , with a bias current  $I_b$ .

Assuming that both transistors are in strong inversion ( $I_b \gg I_{spec4}$ ), the application of (3.39) and (3.43) to the saturated  $T_4$  ( $I_{D4} = I_{F4} = I_b$ ) and to the non-saturated  $T_3$  ( $I_{D3} = I_{F3} - I_{R3} = I$ ) that share the same constant gate voltage  $V_G$  yields

$$I = \frac{\beta}{K_r}(V_G - V_{T0} - nV_b)V_3 = \frac{1}{K_r}\sqrt{2n\beta I_b} \cdot V_3, \quad (5.30)$$

corresponding to a resistor of value

$$R = K_r / \sqrt{2n\beta I_b} = \frac{K_r U_T}{I_{spec} \sqrt{IC}} \quad (\text{in strong inversion}). \quad (5.31)$$

where  $I_{spec}$  and  $IC$  are the specific current and the inversion coefficient of transistor  $T_4$ . This linearity is maintained as long as  $T_3$  is not saturated, hence for value of voltage limited by

$$|V_3| < \frac{2}{n}(V_G - V_{T0} - nV_b) = 2\sqrt{2I_b/\beta n} = 4U_T\sqrt{IC}. \quad (5.32)$$

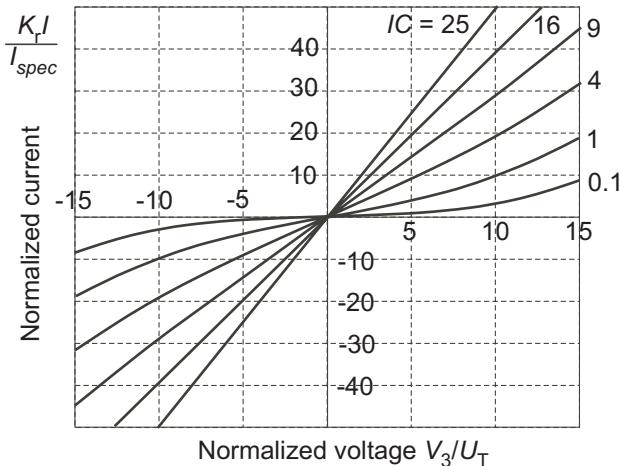
Once the value of  $IC$  has been selected to fulfill (5.32), the specific current  $I_{spec}/K_r$  of transistor  $T_3$  needed for the desired value of  $R$  can be calculated from (5.31).

If  $R$  is very large as in our Example 1, the corresponding value of  $I_{spec}/K_r$  becomes very low, requiring a very large value of channel length  $L$ . But there are limits to  $L$ . One limit is the area occupied by the device. Another limit is the channel-to-substrate leakage current due to carrier generation in the space charge region underneath the channel. Therefore, there is a limit to the minimum possible value of  $I_{spec}/K_r$ . Below this limit, the only possibility to further increase  $R$  given by (5.31) is to reduce the inversion coefficient, thereby reducing the range of linearity given by (5.32).

The behavior of the circuit at low values of  $IC$  can be obtained by using the full model (3.40) instead of (3.43) in the calculation of  $I(V_3)$ . This yields

$$\frac{K_r I}{I_{spec}} = \left[ \ln \left( 1 + e^{V_3/4U_T} (e^{\sqrt{IC}} - 1) \right) \right]^2 - \left[ \ln \left( 1 + e^{-V_3/4U_T} (e^{\sqrt{IC}} - 1) \right) \right]^2. \quad (5.33)$$

This equation is plotted in Fig. 5.5 for several values of inversion coefficient  $IC$ . As can be seen, this  $I(V_3)$  function is linear within the voltage range rep-



**Figure 5.5** Current-voltage relationship in moderate and weak inversion.

resented for  $IC = 16$  and  $25$ , the slope corresponding to the value of  $R$  given by (5.31). For  $IC = 9$ , the function is already slightly nonlinear; according

to (5.32), it leaves the linear range for  $V_3 > 12U_T$ ). For lower values of  $IC$ , the transistors are no longer truly in strong inversion, and the nonlinearity increases. The limit case of weak inversion can be calculated either by the limit of (5.33) for  $IC \rightarrow 0$  or by using (3.42) in the calculation of  $I(V_3)$ . The result is then

$$I = \frac{2I_b}{K_r} \sinh \frac{V_3}{2U_T} = \frac{I_b}{K_r} \left( e^{V_1/U_T} - e^{-V_1/U_T} \right) \quad (\text{weak inversion}) \quad (5.34)$$

The slope of this function at  $V_3 = 0$  is the small signal equivalent conductance  $G_0$  given by

$$G_0 = \frac{I_b}{K_r U_T} \quad (\text{weak inversion}). \quad (5.35)$$

For amplitudes larger than  $U_T$ , this function becomes nonlinear. Assuming that the gate voltage  $V_1$  remains sinusoidal in spite of this small additional nonlinearity, the equivalent conductance contributing to the loss conductance  $G_3$  is the conductance for the fundamental frequency component:

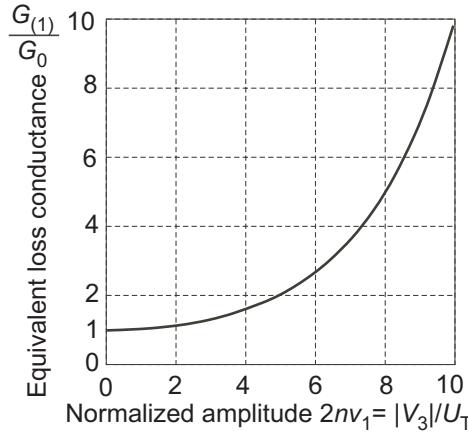
$$G_{(1)} \triangleq \frac{I_{(1)}}{|V_3|} = \frac{I_{(1)}}{2|V_1|} = \frac{I_b}{K_r} \cdot \frac{1}{\pi} \int_0^{2\pi} \sin \phi \left( e^{nv_1 \sin \phi} - e^{-nv_1 \sin \phi} \right) d\phi \quad (5.36)$$

where  $v_1 = |V_1|/(nU_T)$  as defined previously. By introducing (5.35) we obtain finally

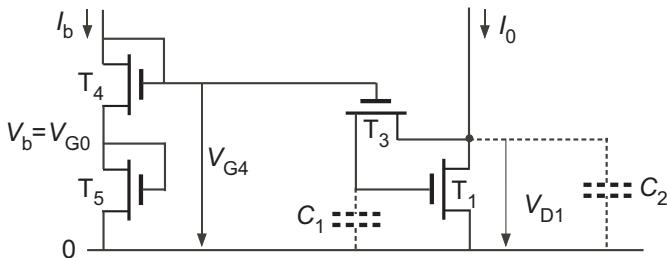
$$G_{(1)} = G_0 \cdot \frac{2I_{B1}(nv_1)}{nv_1} \quad (5.37)$$

This result is plotted in Fig. 5.6. As can be seen,  $G_{(1)} = G_0$  for very small values of  $|V|$ , but it increases rapidly for  $|V_3| = 2|V_1| > U_T$  due to the strong nonlinearity of equation (5.34). In Example 1 of Table 4.3,  $V_3 \cong 10U_T$ . Thus  $G_{(1)} \cong 10G_0$  and a value of  $G_0 = 10^{-8}$  A/V would have to be realized to obtain  $G_3 = 10^{-7}$  A/V as intended. According to (5.35), the saturation current of  $T_3$  would then be  $I_b/K_r = 0.25$  nA.

Now, to implement the drain-to-gate bias resistor by means of the scheme of Fig. 5.4, the bias voltage  $V_b$  must be equal to the DC component of gate voltage  $V_{G0}$  of the active transistor  $T_1$ . As illustrated in Fig. 5.7, this can be done by means of an additional transistor  $T_5$  matched to  $T_1$ . Indeed, if the two transistors have the same inversion coefficient ( $I_b/I_{spec5} = I_0/I_{spec1}$ ), then  $V_b = V_{G0}$  in absence of oscillation ( $|V_1| = 0$ ). But when  $|V_1|$  increases,  $V_{G0}$  is reduced as illustrated by Fig. 4.18. This variation  $\Delta V_{G0}$  is negligible if  $|V_1|$  remains small or if  $IC_0$  is large. Otherwise  $V_b$  must be reduced by the same amount by reducing the inversion coefficient of  $T_5$ .



**Figure 5.6** Equivalent loss conductance of the nonlinear resistor implemented by transistors in weak inversion (for a *symmetrical* sinusoidal signal of total amplitude  $|V_3|$ ).



**Figure 5.7** Implementation of the drain-to-source bias resistor  $R_3$  by transistor  $T_3$  (all transistors are in the same substrate).

If all transistors are in weak inversion,  $\Delta V_{G0}$  is given by (4.68) (or by Fig. 4.18) and is usually not negligible. But it can be compensated by choosing

$$\ln \frac{IC_5}{IC_0} = \frac{\Delta V_{G0}}{nU_T} \quad \text{or} \quad \frac{IC_5}{IC_0} = \frac{|V_1|/nU_T}{2I_{B1}(|V_1|/nU_T)}, \quad (5.38)$$

where  $IC_0$  is, as before, the inversion coefficient of  $T_1$  at the critical condition of oscillation, and  $I_{B1}$  the modified Bessel function first order.

The implementation of  $R_3$  by this scheme increases the minimum value of supply voltage  $V_B$  of Fig. 5.4, because of the stack of transistors  $T_5$  and  $T_4$ . Indeed, to obtain the linearity provided by strong inversion, (5.32) implies

$$V_{G4} = V_{T0} + nV_{G0} + n|V_3|/2 > V_{D1max} = V_{G0} + |V_2|. \quad (5.39)$$

This problem may be alleviated by reducing the inversion coefficient  $T_4$  below the limit given by (5.32). As shown by Fig. 5.5, the resulting nonlinearity remains acceptable even for an inversion coefficient as low as 1.

### 5.1.6 Increasing the Maximum Amplitude

Even with a large supply voltage, the maximum of  $|V_2|$  is limited by the fact that the active transistor leaves saturation in the negative peaks of drain voltage. This limitation is especially important when the threshold  $V_{T0}$  is low. In order to increase  $|V_2|$ , some scheme must be implemented to raise the DC component of drain voltage  $V_{D0}$  by  $\Delta V_{D0}$  above the DC component of gate voltage  $V_{G0}$ . According to (5.2), the minimum possible value of  $V_{T0}$  in strong inversion is then decreased by  $n\Delta V_{D0}$  (but only by  $\Delta V_{D0}$  in weak inversion, according to (5.1)).

In the basic circuit of Fig. 5.1,  $V_{D0}$  and  $V_{G0}$  are forced to be equal by the linear resistor  $R_3$ . This situation is not changed if  $R_3$  is implemented by a transistor as in Fig. 5.7 (because of the transistor is also a symmetrical device), provided  $V_2 = -V_1$ . But the symmetry is lost if  $|V_2| > |V_1|$ , and  $V_{D0}$  is pushed above  $V_{G0}$ . The amount of increase  $\Delta V_{D0}$  can be calculated by stating that the average current through transistor  $T_3$  is zero, or that the average forward component of current compensates the average reverse component (according to the definition introduced in Section 3.8). If the transistor  $T_3$  remains in weak inversion during the whole oscillation cycle, this is expressed by means of (3.39) and (3.42) as

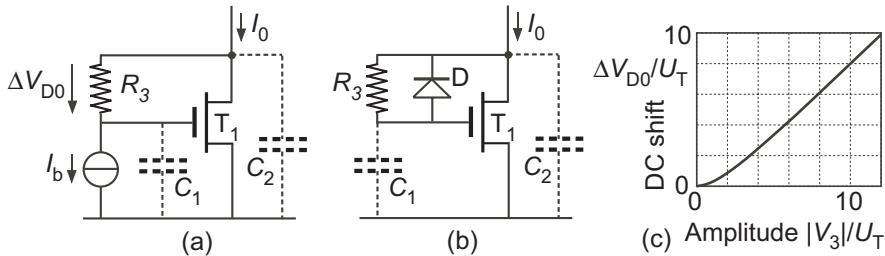
$$e^{-\frac{V_{G0}}{U_T}} \int_0^{2\pi} e^{-\frac{|V_1|}{U_T} \sin \phi} d\phi = e^{-\frac{V_{D0}}{U_T}} \int_0^{2\pi} e^{-\frac{|V_2|}{U_T} \sin \phi} d\phi, \quad (5.40)$$

which yields finally

$$\Delta V_{D0} = V_{D0} - V_{G0} = U_T \ln \frac{I_{B0}(|V_2|/U_T)}{I_{B0}(|V_1|/U_T)}. \quad (5.41)$$

Notice that  $\Delta V_{D0}$  becomes negative (reduction of  $V_{D0}$ ) if  $|V_2|/|V_1| < 1$ .

In the case of a linear biasing resistor  $R_3$ , a voltage shift  $\Delta V_{D0} = R_3 I_b$  can be created by flowing a current  $I_b \ll I_0$  through this resistor, as shown in Fig. 5.8(a). If floating diodes are available in the process, a diode D can be placed between gate and drain, as illustrated in Fig. 5.8(b). For an ideal diode and an infinite resistance  $R_3$ , the shift of drain voltage would depend on the amplitude  $|V_3|$  across the diode according to



**Figure 5.8** Ways to increase the maximum possible amplitude of oscillation; (a) by flowing a DC current  $I_b$  through resistor  $R_3$ ; (b) by adding a floating diode  $D$ ; (c) shift  $\Delta V_{D0}$  produced by an ideal diode  $D$  for  $R_3$  infinite.

$$\Delta V_{D0} = U_T \ln[I_{B0}(|V_3|/U_T)]. \quad (5.42)$$

The plot of Fig. 5.8(c) shows that this shift would be just slightly smaller than the amplitude. But an integrated diode is never ideal, which reduces the shift. Furthermore, a resistance  $R_3$  is usually still needed to ensure a sufficient settling speed of the bias circuitry, according to (5.10), which further reduces the shift.

If the polarity of the diode is inverted, then  $V_{D0} < V_{G0}$ . This may be useful to reduce the minimum of supply voltage  $V_B$  when desaturation of the active transistor is not a problem (small amplitude and/or high threshold  $V_{T0}$ ).

## 5.2 Amplitude Regulation

### 5.2.1 Introduction

We know that an oscillator must be somewhat nonlinear in order to fix the amplitude of oscillation. We have seen in Section 4.3.3 that the first nonlinearity that plays a role when the oscillation grows up is that of the transfer function of the active transistor (this will no longer be true for the inverter-oscillator that will be discussed in Section 5.4.1). We have also pointed out that this nonlinearity has only a small effect on the frequency of oscillation (none at all if  $|Z_3|$  is infinite). On the contrary, as illustrated by the example of Section 4.3.1, other nonlinear effects (in particular the desaturation of transistors) may have a dramatic impact on the frequency, while dissipating power uselessly. It is therefore very important to avoid these effects by limiting the bias current  $I_0$  of the active transistor.

Best is to limit  $I_0$  just above its critical value  $I_{0crit}$  as in our examples of Section 4.5.2. But this requires a very precise value of bias current. Moreover,  $I_{0crit}$  depends not only on the precise value of capacitors, but also on the quality factor of the resonator and on the amount of losses that are neither predictable nor constant.

Therefore, the only realistic way is to implement a control loop that regulates the voltage amplitude  $|V_1|$  at the gate. Some kind of voltage reference is needed, but it should not depend on process parameters or on the supply voltage.

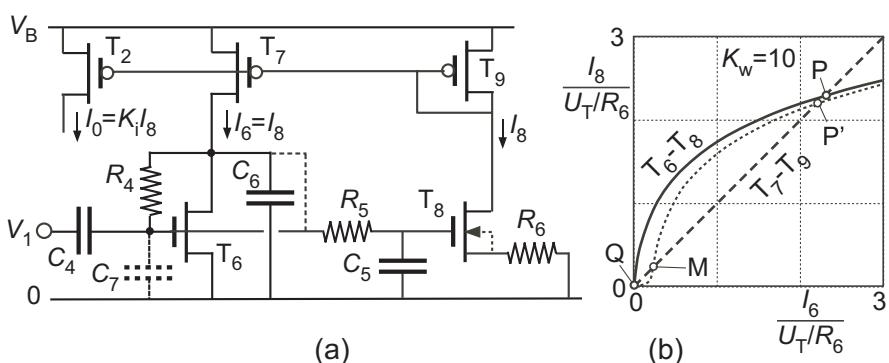
The next section describes an amplitude regulator that has become a standard in low-power oscillators for time-keeping. It uses  $U_T$  as an internal voltage reference.

### 5.2.2 Basic Regulator

The basic circuit of the regulator is shown in Fig. 5.9(a). It is driven by the voltage  $V_1$  produced at the gate of the oscillator, and delivers the bias current  $I_0$  of the oscillator. Transistors  $T_6$  and  $T_8$  are designed to operate in *weak inversion*. They have the same channel length, but their channel widths are in the ratio

$$K_w \triangleq W_8/W_6 > 1. \quad (5.43)$$

They are in the same substrate but the source of  $T_8$  is degenerated by a resistor  $R_6$ .



**Figure 5.9** (a) Basic amplitude regulator; (b) DC solutions.

In absence of oscillation ( $V_1 = 0$ ), the circuit settles to DC values. Resistors  $R_4$  and  $R_5$  can be considered as short circuits since there are no gate currents. The two N-channel transistors are saturated so the expressions (3.39) and (3.42) of the drain currents for  $I_R$  negligible give

$$I_8 = I_6 \cdot K_w e^{-R_6 I_8 / U_T}, \quad (5.44)$$

which is represented in a normalized form in Fig. 5.9(b) for  $K_w = 10$ .

The one-to-one complementary mirror  $T_9 - T_7$  forces the two branch currents to be equal with  $I_6 = I_8$ . This is represented by the interrupted line in the same figure.

Two solutions are possible corresponding to point P and Q. It can be shown that P is stable, hence Q is unstable. The circuit is self-starting (from noise). The current at stable point P is obtained by equating  $I_6$  and  $I_8$  in (5.44); it is multiplied by the gain  $K_i$  of the current mirror  $T_9 - T_2$  to produce the start-up value of  $I_0$ :

$$I_{0start} = \frac{K_i U_T}{R_6} \ln K_w. \quad (5.45)$$

It should be pointed out that if the transistor  $T_8$  is placed inside a separate well connected to its source (as shown in dotted line in Fig. 5.9(a), then  $U_T$  is replaced by  $nU_T$  in (5.45).

Although this circuit is in principle self-starting, this might no longer be true if some leakage currents are present (e.g. currents of reverse-biased drain-substrate junctions). Fig. 5.9(b) shows in dotted line the case of a dominant leakage current flowing across  $T_6$  and/or  $T_9$ . If this current is small, the new stable solution P' remains very close to P, but a third solution appears at point M, between P' and Q. This solution is unstable, therefore Q becomes stable. This does not occur in the opposite case of a leakage current across  $T_7$  and/or  $T_8$ . It is therefore very important to implement the ratio  $K_w$  by  $W_8 = K_w W_6$  and *not* by  $L_6 = K_w L_8$ . The dominant drain leakage of the wider  $T_8$  then ensures that the circuit is self-starting.

If  $I_{0start}$  is larger than  $I_{crit}$  of the oscillator, the oscillation grows up and  $V_1$  is superimposed on the DC component of gate voltage for  $T_6$ , but not for  $T_8$ , since  $V_1$  is blocked by the low-pass filter of time constant  $R_5 C_5$ . The two transistors still have the same DC component of gate voltage but the average drain current of  $T_6$  is amplified by  $I_{BO}(v_1)$  (with  $v_1 = |V_1|/(nU_T)$  as previously), as is shown by (4.58). Thus, from (5.44):

$$I_6 = \frac{I_{BO}(v_1)}{K_w} I_8 e^{R_6 I_8 / U_T}. \quad (5.46)$$

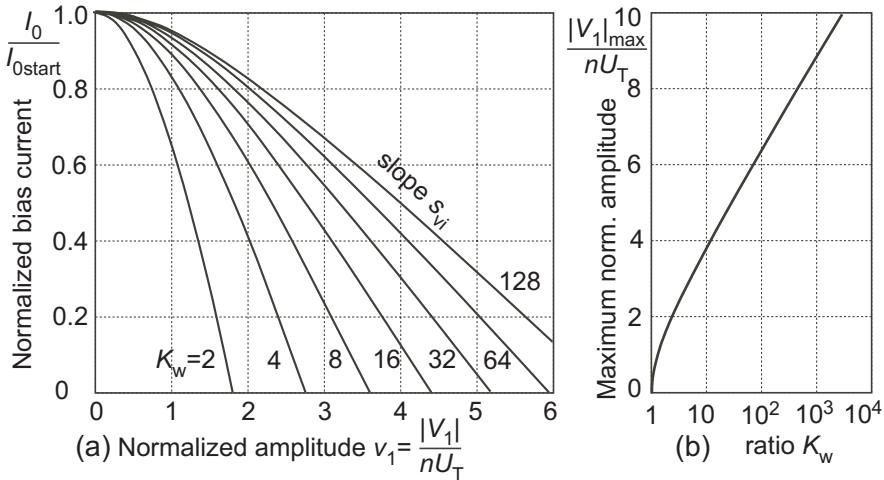
Again, equating the two currents provides their value, which is then multiplied by  $K_i$  to obtain the current delivered to the oscillator:

$$I_0 = \frac{K_i U_T}{R_6} \ln \frac{K_w}{I_{B0}(v_1)}, \quad (5.47)$$

or, by introducing (5.45):

$$\frac{I_0}{I_{0start}} = \frac{\ln [K_w / I_{B0}(v_1)]}{\ln K_w} = 1 - \frac{\ln [I_{B0}(v_1)]}{\ln K_w}. \quad (5.48)$$

This result is plotted in Fig. 5.10(a) for several values of  $K_w$ . The limit of the



**Figure 5.10** (a) Regulation curve; (b) maximum regulated amplitude.

regulated amplitude for  $I_0 \ll I_{0start}$  is obtained by nulling the left hand side of (5.48), giving

$$I_{B0}(v_{1max}) = K_w, \quad (5.49)$$

which is plotted in Fig. 5.10(b). For amplitudes larger than  $v_{1max}$ , the regulator delivers just a very small current essentially due to the drain to substrate leakage of  $T_8$ .

It should be noticed that, according to (4.58), the shift  $\Delta V_{G06}$  of the DC gate voltage component of  $T_6$  due to the AC amplitude  $|V_1|$  at a fixed bias current  $I_6$  is

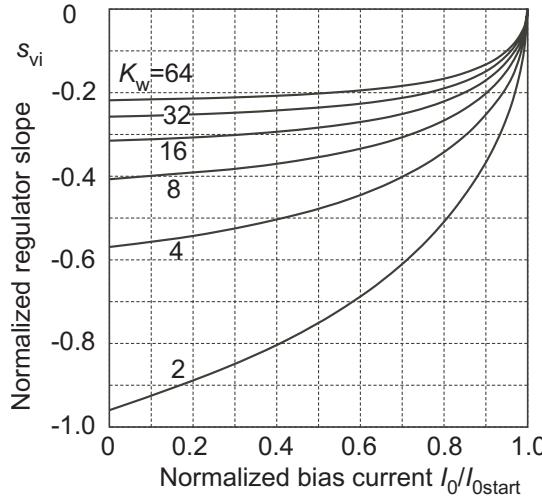
$$\Delta V_{G06} = -nU_T \ln [I_{B0}(v_1)]. \quad (5.50)$$

It is different from the shift  $\Delta V_{G0}$  at *constant*  $G_{m(1)} = G_{mcrit}$  expressed in (4.68).

The slope  $s_{vi}$  of the regulator's normalized transfer function is obtained by differentiating (5.48):

$$s_{vi} = -\frac{1}{\ln K_w} \cdot \frac{I_{B1}(v_1)}{I_{B0}(v_1)}, \quad (5.51)$$

since the derivative of  $I_{B0}(v_1)$  is  $I_{B1}(v_1)$ . The variation of this slope with the normalized current can be calculated by using (5.51) and (5.48) as parametric equations,  $v_1$  being the parameter. It is plotted in Fig. 5.11 for several values of  $K_w$ . After de-normalization, this slope is the transconductance of



**Figure 5.11** Normalized transconductance of the regulator.

the regulator

$$G_{vi} \triangleq \frac{\delta I_0}{\delta |V_1|} = \frac{I_{0start}}{nU_T} s_{vi} = -\frac{I_{0start}}{nU_T \ln K_w} \cdot \frac{I_{B1}(v_1)}{I_{B0}(v_1)} = -\frac{K_i}{nR_6} \cdot \frac{I_{B1}(v_1)}{I_{B0}(v_1)}, \quad (5.52)$$

where the last form has been obtained by introducing (5.45). Now for  $|V_1| > nU_T$  ( $v_1 > 1$ ), the ratio  $I_{B1}(v_1)/I_{B0}(v_1)$  is comprised between 0.5 and 1. Hence,  $G_{vi}$  is approximately equal to  $K_i/(nR_6)$ .

The previous results are only valid if transistor  $T_6$  remains in weak inversion, even in the peaks of drain current. Its maximum inversion coefficient can be expressed from (4.56) as

$$IC_{6max} = e^{v_e} \cdot e^{v_1}, \quad (5.53)$$

with  $v_1$  and  $v_e$  defined by (4.57) applied to  $T_6$  and  $T_8$ . Now, the DC current  $I_6$  obtained from (4.58) is

$$I_6 = I_{spec6} I_{B0}(v_1) e^{v_e}, \quad (5.54)$$

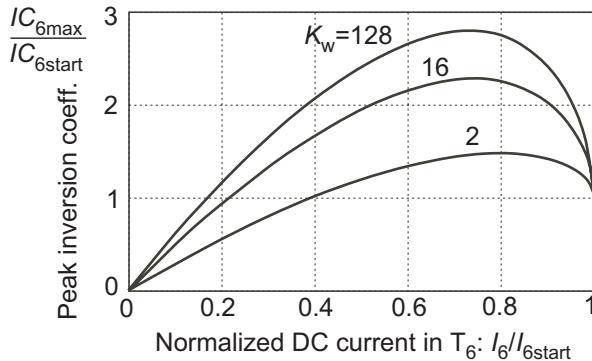
but it can also be expressed from (5.48) as

$$I_6 = I_{6start} \frac{\ln(K_w/I_{B0}(v_1))}{\ln K_w}. \quad (5.55)$$

The value of  $v_e$  can be obtained by equating these two expressions. It can then be introduced in (5.53), which yields

$$\frac{IC_{6max}}{IC_{6start}} = \frac{\ln(K_w/I_{B0}(v_1))}{\ln K_w} \frac{e^{v_1}}{I_{B0}(v_1)}, \quad (5.56)$$

where  $IC_{6max}$  is the inversion coefficient of  $T_6$  for  $I_6 = I_{6start}$ . Combined with (5.48) (applied to  $I_6/I_{6start}$ ) and using  $v_1$  as a parameter, this equation gives the variation of  $IC_6/IC_{6start}$  in the whole possible range of  $I_6$ . It is plotted in Fig. 5.12 for several values of  $K_w$ .



**Figure 5.12** Peak inversion coefficient of transistor  $T_6$ .

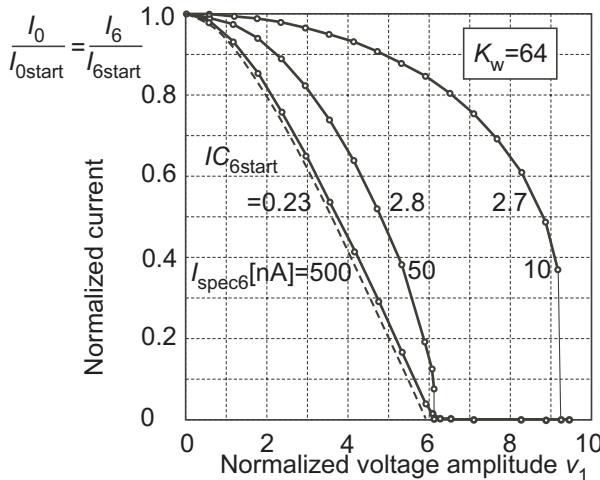
It can be seen that the maximum value of  $IC_6$  is 1.5 to  $3IC_{6start}$ . Thus, to ensure weak inversion with  $IC_6 < 0.1$ ,  $IC_{6start}$  should be smaller than 0.03 to 0.06. As shown by the simulations reported in Fig. 5.13, this requirement is exaggerated and a value

$$IC_{6start} < 0.2 \quad (5.57)$$

is sufficient to remain very close to the theoretical result for weak inversion (shown in dotted line).

But if  $I_{spec6}$  is reduced further, the voltage scale is expanded at high current because of strong inversion, but unchanged at low current. As a consequence, the slope  $s_{vi}$  increases at intermediate current levels, and finally becomes negative. The overall loop will then be unstable.

The inversion coefficient of  $T_8$  is always smaller, since this transistor is  $K_w$ -times wider as does not receive the AC voltage.



**Figure 5.13** Effect of strong inversion on the regulator characteristics. The theoretical curve for weak inversion is shown in dotted line.

Capacitor  $C_6$  is needed in Fig. 5.9(a) to limit the AC drain variation of transistor  $T_6$ , thereby keeping it in saturation. For the fundamental component, the AC amplitude  $|V_{D6}|$  at the drain is

$$|V_{D6}| = \frac{1 - G_{m6(1)}R_4}{\sqrt{1 + (\omega R_4 C_6)^2}} V_1, \quad (5.58)$$

with, according to (4.62)

$$G_{m6(1)} = \frac{I_6}{|V_1|} \cdot \frac{2I_{B1}(v_1)}{I_{B0}(v_1)} = G_{m6} \cdot \frac{2I_{B1(v_1)}}{v_1 I_{B0(v_1)}}. \quad (5.59)$$

It could in principle be cancelled by choosing  $G_{m6(1)}R_4 = 1$ , but the harmonic components would remain. An upper bound of  $|V_{D6}|$  including all components may be estimated by assuming that the drain current is a very large spike

of negligible length with respect to the period of oscillation  $2\pi/\omega$ . The drain voltage would then be a triangular wave of amplitude

$$|V_{D6}|_{max} \cong \frac{\pi I_6}{\omega C_6}. \quad (5.60)$$

The DC component of gate voltage is obtained by applying (4.58) to transistor  $T_6$ :

$$V_{G06} = V_{T0} + nU_T \ln \frac{I_6}{I_{spec6} \cdot I_{B0}(v_1)}. \quad (5.61)$$

In order to maintain  $T_6$  in saturation,  $C_6$  should be sufficiently large to ensure

$$V_{G06} - |V_{D6}| > 5U_T \quad (5.62)$$

for the largest value  $I_6 = I_{6start}$ .

The values of  $R_4$  and  $R_5$  should be sufficiently large to limit the loss conductance  $G_1$  of the oscillator.

The regulator of Fig. 5.9 is a positive feedback loop. At equilibrium, its open-loop low-frequency gain for *constant input voltage*  $|V_1|$  can be calculated to be

$$G_{R0(ol)} = \frac{1}{1+\alpha} \leq 1, \quad (5.63)$$

with

$$\alpha \triangleq \frac{V_{R6}}{nU_T} = \frac{I_0}{I_{0start}} \ln K_w, \quad (5.64)$$

where  $V_{R6}$  is the voltage across resistor  $R_6$ . This gain is always smaller than unity, but it approaches unity if the bias current becomes much smaller than the start-up current.

If the output noise current spectral density (noise content of current  $I_0$ ) in open-loop is  $S_{i_{n0}^2(ol)}$ , when the loop is closed it becomes

$$S_{i_n^2} = \left( \frac{1}{1-G_0} \right)^2 S_{i_{n0}^2(ol)} = \left( 1 + \frac{1}{\alpha} \right)^2 S_{i_{n0}^2(ol)}, \quad (5.65)$$

showing that the noise content of the output current  $I_0$  increases with  $I_{0max}/I_0$ . This noise may be reduced by an RC filter before it reaches the gate of  $T_2$ , but care must be taken to maintain the stability of the overall amplitude regulating loop discussed in Section 5.2.3.

For a frequency  $\Omega$  much lower than the frequency  $\Omega_{ci}$  of each of the  $N$  poles inside the regulator loop, the phase of the open-loop gain can be approximated by

$$\Phi_{R(ol)} = - \sum_1^N \frac{\Omega}{\Omega_{ci}}. \quad (5.66)$$

Hence, the closed-loop gain  $G_R$  (for constant  $|V_1|$ ) is given by

$$\frac{1}{G_R} = \frac{1}{G_{R0(ol)}(1 + j\Phi_{R(ol)})} - 1 = \frac{\alpha - j\Phi_{R(ol)}}{1 + \Phi_{R(ol)}}. \quad (5.67)$$

For  $\Phi_{R(ol)} \ll 1$ , it becomes

$$G_R = \frac{1 + j\Phi_R}{\alpha}, \quad (5.68)$$

with

$$\Phi_R = \Phi_{R(ol)}(1 + 1/\alpha). \quad (5.69)$$

Thus, reducing the value of  $\alpha$  also results in an increase of the phase shift in the regulator, which may endanger the stability of the regulation loop. According to (5.64), the ratio  $I_{0start}/I_0$  must therefore be limited.

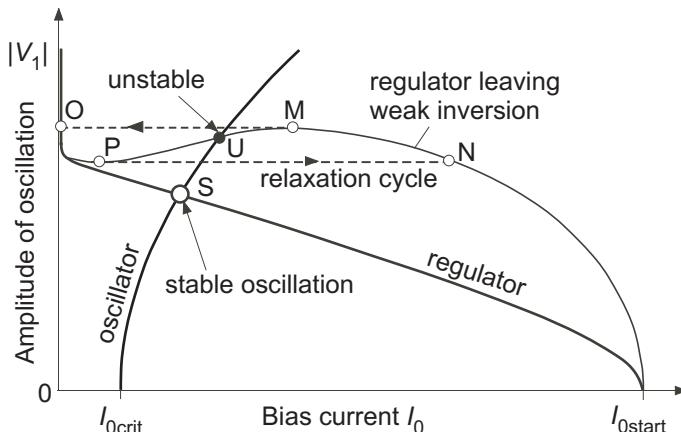
If  $R_4$  is a perfectly linear resistor, the DC voltage component at the drain of  $T_6$  is equal to that at its gate. Thus, the resistor  $R_5$  of the low-pass filter can be connected to the drain instead of the gate, as illustrated in dotted line in the figure. This variant offers the advantage of reducing the load on the oscillator. Furthermore, it improves the attenuation of the residual AC component that reaches the gate of  $T_8$ .

A very large value of ratio  $K_w$  is required to reach an amplitude larger than  $4U_T$ , as can be seen in Fig. 5.10(a). Instead, the regulated amplitude can be increased by attenuating the input voltage of the regulator. This can be done by adding a capacitor  $C_7$  shown in dotted line in Fig. 5.9(a). A part of  $C_7$  can be the gate capacitance of transistor  $T_6$ . It can be shown that, since this transistor is in weak inversion, its gate capacitor is the oxide capacitor multiplied by  $(n - 1)/n < 1$ .

### 5.2.3 Amplitude Regulating Loop

The amplitude regulating loop is realized by combining the oscillator of Fig. 5.1 with the regulator of Fig. 5.9(a). The input of the regulator is connected to the gate of  $T_1$ , since it is the gate voltage amplitude that needs to be regulated.

As illustrated in Fig. 5.14, a stable amplitude is reached at the intersection S of the  $|V_1|(I_0)$  function of the oscillator with the  $I_0(|V_1|)$  function of the



**Figure 5.14** Amplitude regulating loop; a stable amplitude is reached at point S if the regulator has the monotonic descending transfer function obtained in weak inversion. If it leaves weak inversion, monotonicity is lost and a relaxation cycle may occur.

regulator. But this is true only if the current delivered by the regulator is descending monotonically when the amplitude increases, as obtained when the transistor  $T_6$  is maintained in weak inversion by observing the condition (5.57).

This monotonicity is lost if the transistor leaves weak inversion during the peaks of AC current. If the intersection with the  $|V_1|(I_0)$  function of the oscillator occurs in a region of positive slope (point U), the loop is no longer stable. Instead, a relaxation cycle takes place, as shown in interrupted line in the figure. At start-up, the amplitude  $|V_1|$  increases and the current  $I_0$  decreases down to point M where the slope becomes positive. The current jumps abruptly to a very low value (point O) where the amplitude starts decreasing, until point P is reached. The current then jumps to a high value at point N and the cycle is repeated.

A negative slope of the regulator is thus a necessary condition for a stable loop, but this condition is not sufficient. Indeed, the loop must also satisfy the Nyquist criterion of stability.

Neglecting all other poles than the dominant pole  $\Omega_{civ}$  of the oscillator amplitude, the gain of the open loop is obtained by combining (5.25), (5.26) and (5.52):

$$G_{ol} \triangleq \frac{\delta V_1}{\delta I_{D0}} \cdot \frac{\delta I_0}{\delta |V_1|} = \frac{K_{iv} G_{vi}}{s + K_{iv}/R_{iv}}, \quad (5.70)$$

variable	Example 1	Example 2	unit	reference
$C_7/C_4$	0	1		choice
$K_w$	16	8		choice
$I_0/I_{start}$	0.12	0.21		Fig. 5.10a
$I_{0start}$	$1.17 \cdot 10^{-6}$	$7.24 \cdot 10^{-3}$	A	from $I_0$
$K_i$	10	100		choice
$I_{6start}$	$0.117 \cdot 10^{-6}$	$72.4 \cdot 10^{-6}$	A	from $I_{0start}$
$R_6$	$0.617 \cdot 10^6$	$74.7 \cdot 10^3$	V/A	(5.45)
$I_{spec6}$	$584 \cdot 10^{-9}$	$362 \cdot 10^{-6}$	A	(5.57)
$W_6/L_6$	1.17	724		
$L_6 = L_8$	$2 \cdot 10^{-6}$	$0.5 \cdot 10^{-6}$	m	choice
$W_6$	$2.34 \cdot 10^{-6}$	$362 \cdot 10^{-6}$	m	
$W_8 = K_w W_6$	$37.4 \cdot 10^{-6}$	$2.89 \cdot 10^{-3}$	m	
$v_1 C_4 / (C_4 + C_7)$	4	3		
$-s_{vi}$	0.31	0.39		(5.51)
$-G_{vi}$	$10.8 \cdot 10^{-6}$	$83.4 \cdot 10^{-3}$	A/V	(5.52)
$\Omega_1$	23	$96.5 \cdot 10^3$	1/s	(5.71)
$\Omega_0/\Omega_1$	1400	706		

**Table 5.2** Examples of practical implementations of the amplitude regulator.

where  $K_{iv}$  and  $R_{iv}$  and  $G_{vi}$  are given by (5.28), (5.27) and (5.52) respectively. For very low frequencies including DC, it has the absolute value  $R_{iv} G_{vi}$  that should be sufficiently higher than unity to obtain a good regulation. But for frequencies higher than  $\Omega_{civ} = K_{iv}/R_{iv}$ , it behaves as an integrator with a unity gain frequency (or gain-bandwidth product) simply given by

$$\Omega_1 = K_{iv} |G_{vi}|. \quad (5.71)$$

There are several other poles in the loop. Indeed, we have seen that the dynamic behavior of the oscillator bias has a resonant frequency with two poles at  $\Omega_0$ . Moreover, the basic regulator of Fig. 5.9(a) may introduce three more poles. For loop stability, each of these poles should be at frequency much higher than  $\Omega_1$ . If this condition is verified, the phase margin at  $\Omega_1$  can be approximated by using (5.69) and (5.66):

$$\Delta\Phi = \frac{\Pi}{2} - 2 \frac{\Omega_1}{\Omega_0} - (1 + 1/\alpha) \sum_{i=1}^N \frac{\Omega_1}{\Omega_{ci}}, \quad (5.72)$$

where  $N$  is the number of poles in the regulator and  $\Omega_{ci}$  the frequency of pole  $i$ .

Examples of implementation of regulators adapted to the two examples of oscillators described in the previous sections (Tables 4.1, 4.2, 4.3 and 5.1) are given in Table 5.2.

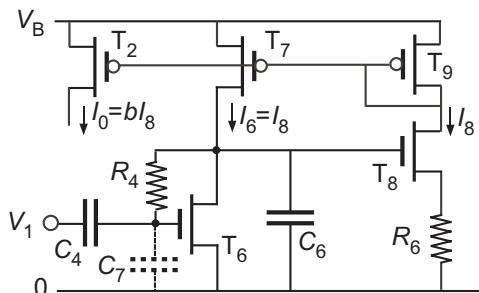
To avoid a too large value of  $K_w$  in Example 2, the input voltage of the regulator is divided by two by introducing  $C_7 = C_4$ . The regulator is then designed for  $v_1 = 3$  instead of 6.

In this example, in spite of a large current ratio  $K_i$ , a very large width of transistors  $T_6$  and  $T_8$  is needed to maintain them in weak inversion.

For both examples, the unity gain frequency  $\Omega_1$  is, as it should, much lower than the resonant frequency  $\Omega_0$  of the biasing circuit. The loop will be stable if the additional poles due to the regulator itself are also at a much higher frequency. Their number and their values depend on the specific implementation of the regulator. Several possibilities will be discussed in the following sections.

### 5.2.4 Simplified Regulator Using Linear Resistors

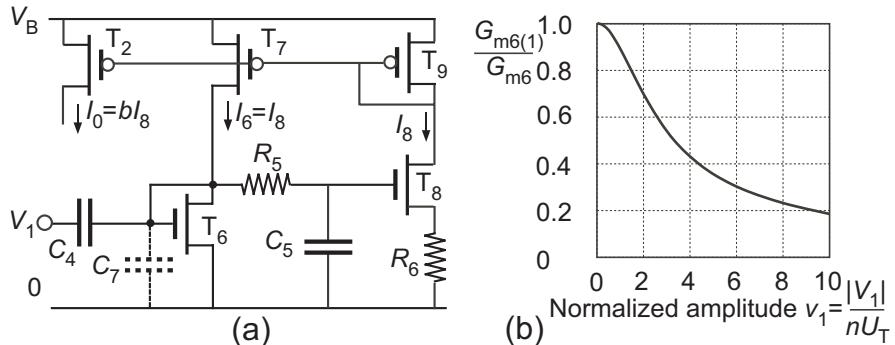
If  $R_4$  is a linear resistor, the DC component  $V_{D0}$  of drain voltage remains equal to  $V_{G0}$  at the gate. If  $C_6$  is sufficiently large, it will limit the amplitude of drain voltage  $|V_{D6}|$  evaluated by (5.58) to a very low value, so that the low-pass filter  $R_5C_5$  can be removed, as shown in Fig. 5.15. For a correct



**Figure 5.15** Simplified form of the regulator; the low-pass filter  $R_5C_5$  is suppressed and  $T_8$  is driven directly by the DC component of drain voltage  $V_{D06}$  that follows  $V_{G06}$ .

operation of the regulator, the residual AC amplitude  $|V_{D6}|$  should be smaller than about  $0.3nU_T$ . If the required value of  $C_6$  is too large, it might be better to keep the additional low-pass filter  $R_5C_5$ .

Another simplified version of the regulator is depicted in Fig. 5.16(a). Here, the low-pass filter  $R_5C_5$  is maintained, but the drain of  $T_6$  is directly connected to the gate. This transistor is therefore a nonlinear load for the

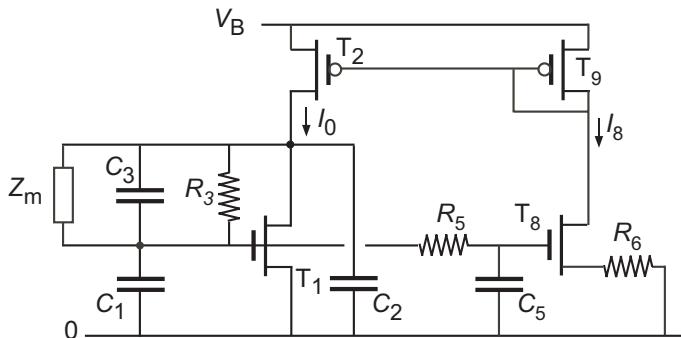


**Figure 5.16** (a) Simplified form of the regulator; the drain of  $T_6$  is directly connected to the gate. (b) The equivalent conductance loading the oscillator is smaller than the small-signal transconductance  $G_{m6}$ .

oscillator, which should be made negligible. The contribution to  $G_1$  is the transconductance for the fundamental component  $G_{m6(1)}$  given by (5.59) and plotted in Fig. 5.16(b).

Thanks to the DC shift, it is always smaller than the small-signal conductance  $G_{m6}$  for  $I_{D6} = I_6$ . To avoid a too large loss conductance  $G_1$ , the branch current  $I_6$  should be much smaller than the bias current  $I_0$  of the oscillator.

The most compact solution is obtained by merging the regulator with the oscillator as illustrated in Fig. 5.17 [21]. Transistors  $T_6$  and  $T_7$  of the reg-



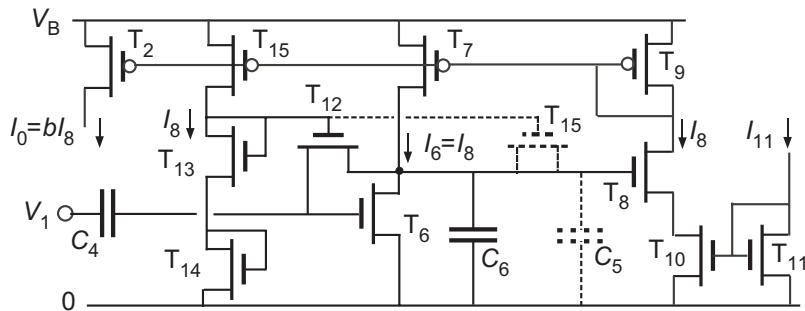
**Figure 5.17** Compact regulating loop by merging the oscillator with the regulator.

ulator are merged with  $T_1$  and  $T_2$  of the oscillator, so that  $T_1$  and  $T_8$  have the same DC gate voltage. Since transistor  $T_6$  must be in weak inversion,

this solution is only possible if the oscillator is designed with  $T_2$  in weak inversion, with  $I_{spec1} > 5I_{0start}$  according to (5.57).

### 5.2.5 Elimination of Resistors

A possible implementation of the regulator without any resistor is depicted in Fig. 5.18.



**Figure 5.18** Possible implementation of the amplitude regulator without resistors. Resistor  $R_4$  of Fig. 5.15 is replaced by transistor  $T_{12}$ ; this modifies the characteristics of the regulator. Resistor  $R_6$  is replaced by transistor  $T_{10}$ .

The role of resistor  $R_6$  of the original circuit (Fig. 5.9) is to define the value of start-up current. It is here replaced by transistor  $T_{10}$  operating in strong inversion with  $V_D \ll V_{Dsat}$  (or  $I_F - I_R \ll I_F$ ). The corresponding resistance is the inverse of the source transconductance of  $T_{10}$  given by (3.50). If transistors  $T_{10}$  and  $T_{11}$  are identical, the equivalent resistance is then

$$R_6 = \frac{U_T}{\sqrt{I_{F10} I_{spec10}}} = \frac{U_T}{\sqrt{I_{11} I_{spec10}}}. \quad (5.73)$$

The bias current  $I_{11}$  must be provided by some external current reference. This could be avoided by suppressing  $T_{11}$  and connecting the gate of  $T_{10}$  to some bias voltage  $V_b$ . From (3.50), the equivalent resistance would then be

$$R_6 = \frac{1}{\beta_{10}(V_b - V_{T0})}. \quad (5.74)$$

A simple possibility is to use the supply voltage  $V_B$  as bias voltage  $V_b$ , with the risk of perturbing the oscillator by the noise content of  $V_B$ .

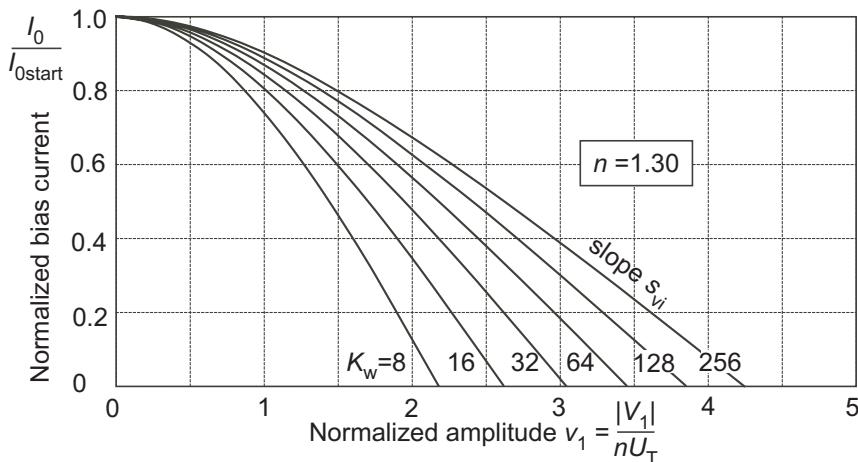
The linear resistor  $R_4$  of Fig. 5.15 is replaced by transistor  $T_{12}$ , according to the scheme described in Fig. 5.4 (with  $T_3, T_4$  becoming  $T_{12}, T_{13}$ ). However, to obtain a linear element, this scheme required symmetrical voltage variations at the two ends of the device. It is therefore not applicable to eliminate the AC component without producing an additional shift of the DC component. Since the AC component of voltage is filtered out at the drain, this voltage shift for weak inversion can be obtained by applying (5.41) with  $|V_2| = 0$ :

$$\Delta V_{D06} = V_{D06} - V_{G06} = -U_T \ln (I_{B0}(nv_1)). \quad (5.75)$$

This shift must be added to  $\Delta V_{G06}$  (given by (5.50)) in the calculation of the regulator transfer function. The result (5.48) is modified to

$$\frac{I_0}{I_{0start}} = 1 - \frac{\ln [I_{B0}(v_1)] + \ln [I_{B0}(nv_1)]/n}{\ln K_w}, \quad (5.76)$$

which becomes dependent on the value of  $n$ . It is plotted in Fig. 5.19 for  $n = 1.30$ . Compared to those of Fig. 5.10, these regulation curves have a



**Figure 5.19** Regulation curve for the circuit of Fig. 5.18 with  $T_{12}$  in weak inversion.

reduced voltage scale, thereby requiring a larger value of the ratio  $K_w$  to achieve a given amplitude.

The contribution of the regulator to the loss conductance  $G_1$  of the oscillator is the conductance  $G_{(1)}$  of transistor  $T_{12}$  for the fundamental frequency component (at the gate node of  $T_6$ ). Assuming that all N-channel transistors are in weak inversion, this conductance can be calculated to be :

$$G_{(1)} = G_0 \cdot \frac{2I_{B1}(nv_1)}{nv_1}. \quad (5.77)$$

This result is identical to (5.37) plotted in Fig. 5.6, but the small signal value  $G_0$  is

$$G_0 = e^{(V_{G14} - V_{G06})/U_T} \frac{I_8}{K_r U_T} \quad (5.78)$$

with  $K_r = \beta_{13}/\beta_{12}$ . The voltage difference  $(V_{G14} - V_{G06})$  depends on the relative size of transistors  $T_6$  and  $T_{14}$  and on the shift of DC gate voltage of  $T_6$  given by (5.50):

$$V_{G14} - V_{G06} = nU_T \cdot \ln \left[ \frac{\beta_6}{\beta_{14}} I_{B0}(v_1) \right], \quad (5.79)$$

thus (5.78) becomes

$$G_0 = \left[ \frac{\beta_6}{\beta_{14}} I_{B0}(v_1) \right]^n \frac{I_8}{K_r U_T}, \quad (5.80)$$

which is can be made independent of  $n$  by choosing  $\beta_{14}/\beta_6 = I_{B0}(v_1)$ .

To improve the amount of filtering, the low-pass filter  $R_5 C_5$  of Fig. 5.9(a) can be implemented by means of an additional transistor  $T_{15}$  (shown in dotted line in Fig. 5.18) with the same gate voltage as  $T_{12}$ . This transistor does not produce any voltage shift since it only receives the very small residual AC voltage, but it should have a smaller value of specific current to compensate for the additional voltage shift given by (5.75). To obtain the same small signal conductance  $G_0$  as  $T_{12}$ :

$$\beta_{15} = \beta_{12}/I_{B0}(nv_1). \quad (5.81)$$

Now, even if  $T_{12}$  and  $T_{13}$  are in strong inversion, with inversion coefficients  $IC_{12} = IC_{13}$  much larger than unity,  $T_{12}$  cannot behave as a linear resistor, since there is no AC voltage at the drain of  $T_6$ . The voltage shift can be calculated to be

$$\Delta V_{D06} = V_{D06} - V_{G06} = 2U_T \sqrt{IC_{13}} \left[ 1 - \sqrt{1 - \frac{|V_1|^2}{8U_T^2 IC_{13}}} \right], \quad (5.82)$$

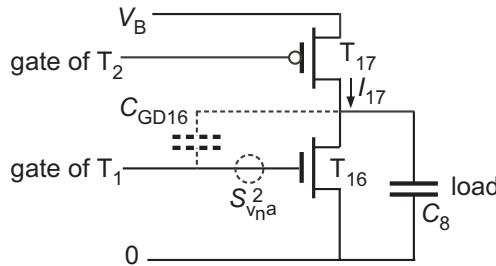
which is only valid if the peaks of  $V_1$  do not saturate  $T_{12}$ , i.e. for

$$|V_1| < 2U_T \sqrt{IC_{13}}. \quad (5.83)$$

This shift can be made negligible with respect to  $\Delta V_{G06}$  expressed by (5.50) by choosing a large value of inversion coefficient  $IC_{13}$ . The basic regulation curves of Fig. 5.10(a) will then remain valid.

### 5.3 Extraction of the Oscillatory Signal

The amplitude  $|V_1|$  of the signal produced by the oscillator is usually not sufficient for the intended application and must therefore be amplified. The most simple amplifier is shown in Fig. 5.20. The complementary transistors  $T_{16}$  and  $T_{17}$  replicate  $T_1$  and  $T_2$  of the oscillator with a ratio  $K_a$  in specific current, current and transconductance (e.g.  $I_{spec16} = K_a I_{spec1}$ ). Their capacitive load  $C_8$  is usually much smaller than the functional capacitance  $C_2$  of the oscillator. Since the gate of  $T_{16}$  is connected to that of  $T_1$ , the transconduct-



**Figure 5.20** Buffer amplifier for signal extraction.

ance for the fundamental is proportional to the critical transconductance of the oscillator:  $G_{m16(1)} = K_a G_{mcrit}$ . The voltage gain is the given by

$$A_v = \frac{K_a G_{mcrit}}{\omega C_8}. \quad (5.84)$$

The input capacitance of this amplifier can be included in the functional capacitor  $C_1$  of the oscillator. But the unavoidable drain-to-gate capacitance produces an increase of the loss conductance  $G_1$ . Indeed, as long as the two transistors remain saturated, a fraction  $C_{GD16}/(C_8 + C_{GD16})$  of the drain current variations is feed back to the input, which corresponds to an input conductance for the fundamental

$$G_{in(1)} = K_a G_{mcrit} \frac{C_{GD16}}{C_8 + C_{GD16}}. \quad (5.85)$$

The noise of this amplifier can be characterized by its input-referred noise voltage spectral density  $S_{v_{na}^2}$ . The white noise component of this spectrum can be expressed as

$$S_{v_{na}^2} = \frac{4\gamma_a kT}{K_a G_{mcrit}}, \quad (5.86)$$

where  $\gamma_a$  is the noise excess factor of the amplifier. This factor is always larger than 1/2, but it may be much larger than unity if  $T_{16}$  is in strong inversion with an inversion coefficient much larger than that of  $T_{17}$ .

This voltage noise results in a component of phase noise, with a spectrum given by given by

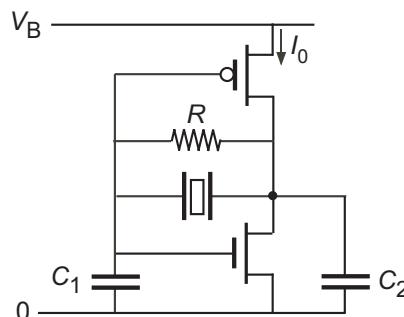
$$S_{\phi_n^2 a} = S_{v_n^2 a} / |V_1^2|. \quad (5.87)$$

This noise is added to the phase noise of the oscillator (given by (3.29) or (3.30)) and dominates at frequencies distant from the frequency of oscillation.

## 5.4 CMOS-Inverter Oscillator

### 5.4.1 Direct Implementation

One of the earliest implementations of a CMOS oscillator is illustrated by Fig. 5.21. It is a simple CMOS inverter biased in active mode by a resistor



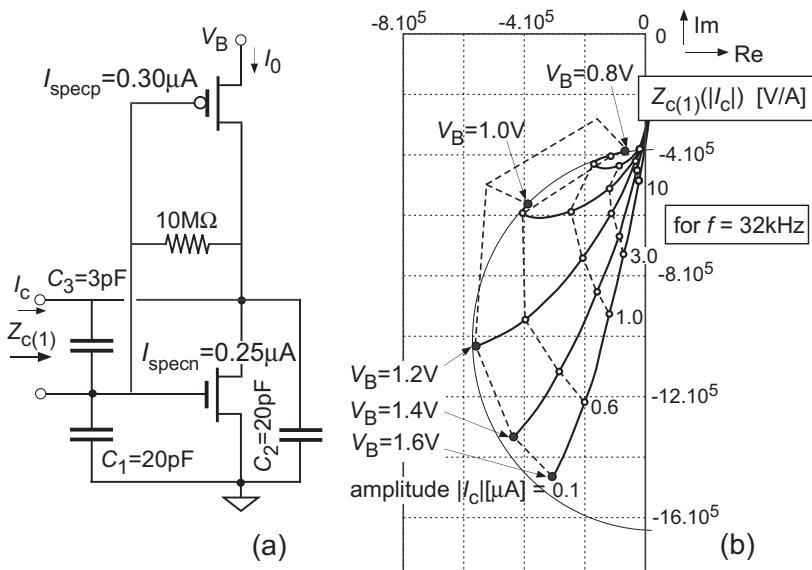
**Figure 5.21** Direct implementation of a CMOS inverter as an oscillator.

$R$ , to which the two functional capacitors of the Pierce circuit are added. It is still a grounded-source configuration, since both sources are grounded with respect to AC signals. The transconductances of the two transistors are added, but they are produced by the same current  $I_0$ . If the transistors are designed to have the same specific current, the combined transconductance is doubled. According to (3.55), the critical current is thus reduced by a factor 2 for any given value of inversion coefficient  $IC_0$ .

However, this simple circuit suffers from two major drawbacks.

First, the current drawn from the supply voltage is not constant and its average value  $I_0$  depends on the supply voltage and on the threshold voltage of the two transistors. This dependency increases when the inversion factor is decreased and is maximum in weak inversion.

The second drawback is that, at low values of the inversion coefficient, the nonlinearity of the transfer function of the inverter results in an *increase* of the transconductance for the fundamental frequency  $G_{m(1)}$  with the amplitude of oscillation. Thus, as soon as the critical transconductance is reached (for a critical value of  $V_B$ ), the amplitude increases abruptly, until it is limited by the loss conductance of the transistors leaving saturation in the peaks of oscillation. The corresponding variation of  $Z_{c(1)}(|I_c|)$  simulated in an example is shown in Fig. 5.22. The simulated circuit is depicted in part (a) of



**Figure 5.22** Simulation of the circuit impedance for the fundamental frequency  $Z_{c(1)}$  of a CMOS-inverter oscillator.

the figure. The two complementary transistors have approximately identical specific currents and the loss due to the biasing resistor is practically negligible.

Part (b) of the figure shows the loci of  $Z_{c(1)}(|I_c|)$  calculated from simulations with several values of supply voltage  $V_B$ . As long as the amplitude  $|I_c|$  of the sinusoidal current injected in the circuit is smaller than 100 nA, the cir-

cuit remains linear and its small-signal transconductance  $G_m$  increases with  $V_B$ . The corresponding values of the linear circuit impedance  $Z_c$  are located approximately on the expected circular locus (shown in thin line). The small departure for large values of  $V_B$  is caused by the output conductance  $G_{ds}$  of the transistors. Indeed, this conductance is not constant but increases with the current, thereby progressively shifting the circle.

For larger values of  $|I_c|$ , the circuit becomes nonlinear. Its impedance  $Z_{c(1)}$  for the fundamental frequency starts changing with the amplitude.

For  $V_B \leq 1\text{ V}$ , the bias current is small and the transistors are in weak or moderate inversion. The negative resistance first *increases* with the amplitude as a result of the increase of  $G_{m(1)}$ . It only starts decreasing when the amplitude is so large as to push the transistors out of saturation, which creates a large equivalent loss conductance  $G_2$ . The current drain  $I_0$  is always much larger than its critical value and the excess of power is dissipated in losses.

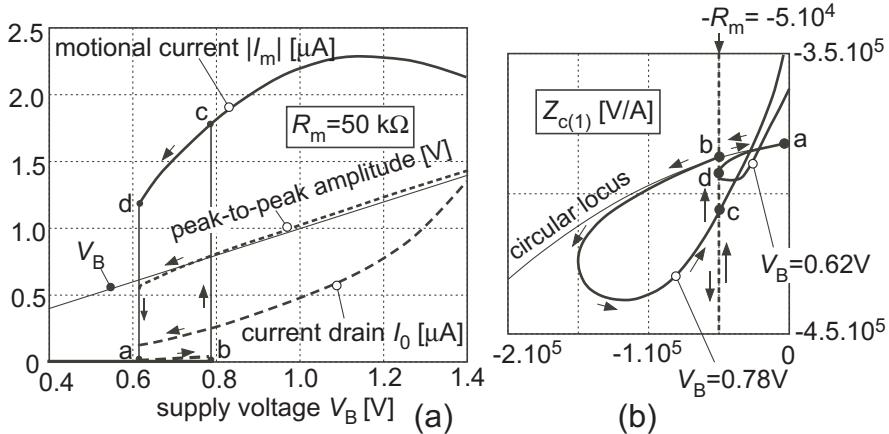
For  $V_B \geq 1.2\text{ V}$ , the transistors are in strong inversion and the voltage-to-current transfer function of the inverter are approximately linear (difference of two approximately identical shifted square laws). Thus, as soon as the critical transconductance is reached, the amplitude grows until the transistors leave saturation, thereby reducing the negative resistance.

With the values selected, this circuit provides a maximum negative resistance of about  $580\text{k}\Omega$  at  $V_B=1.2\text{ V}$ . Simulation results obtained with a motional resistance  $R_m=50\text{k}\Omega$  are illustrated in Fig. 5.23(a).

Starting from low values of  $V_B$ , the critical value of the current  $I_0$  flowing through the transistors is reached for  $V_B=0.78\text{ V}$  (point b). At this point, the amplitude of oscillation grows until the peak-to-peak value of the voltage at the drains reaches approximately  $V_B$  (point c). The current is then much larger than its critical value, and the drain voltage is strongly distorted. A further increase of  $V_B$  is followed by the drain amplitude, and results in a further increase of  $I_0$ . The motional current  $I_m$  also increases first, but then decreases. This is because the increase of losses produced by desaturated transistors overcomes the increase of bias current.

Starting from high values of  $V_B$ , the oscillation is sustained down to  $V_B = 0.62\text{ V}$  (point d). At this point, it decreases to zero and  $I_0$  falls down much lower than its critical value

The explanation of this hysteresis loop can be found in part (b) of the figure. To each value of supply voltage  $V_B$  corresponds one locus of the fundamental impedance  $Z_{c(1)}(|I_c|)$ . The figure shows only the loci simulated for the two critical values of  $V_B$ . With the amplitude  $|I_c|$  increasing, these loci first follow the circular locus of the linear circuit (corresponding to an in-



**Figure 5.23** Simulation of the CMOS inverter-oscillator of Fig. 5.22(a) with  $R_m = 50 \text{ k}\Omega$ ; (a) variation of motional current, current drain and peak-to-peak drain amplitude; (b) partial  $Z_{c(1)}$  complex plane explaining the hysteresis loop.

crease of the negative resistance  $|R_n|$ ). This is because  $G_{m(1)}$  increases with the amplitude, as explained above. When the losses at the drain becomes too important, the loci loop back and the negative resistance decreases as normally.

The locus of the motional impedance  $-Z_m(p)$  for  $R_m=50\text{k}\Omega$  is represented in dotted line in the same figure. As explained in Chapter 3, stable oscillation can be reached for  $Z_{c(1)} = Z_m$ .

Starting from low values of  $V_B$ , the first solution is found at point b (origin of the  $Z_{c(1)}$  locus for  $V_B = 0.78 \text{ V}$ ). But this solution is unstable since the amplitude stability criterion (1.3) is not met. At this value of  $V_B$ , the amplitude first increases and then decreases until the stable point c is reached. Larger values of  $V_B$  correspond to lower positions of this stable solution.

When  $V_B$  is reduced below 0.78 V, the stable solution will move on intermediate loci, until point d is reached for  $V_B=0.62 \text{ V}$ . But this point is metastable since for any small change of amplitude the negative resistance becomes smaller than  $R_m$ . At this value of  $V_B$ , the amplitude decreases until point a is reached.

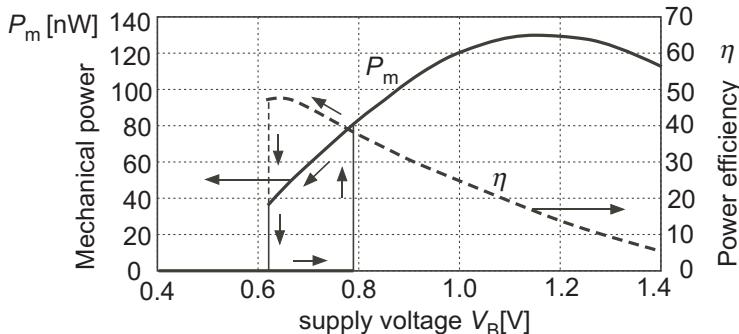
This hysteresis loop can disappear if the transistors are both in strong inversion at the critical value of  $V_B$ . But this requires a higher value of  $V_B$  and the critical current is increased, thus the advantage of minimizing the current is lost. It is very difficult in practice to avoid dissipating much more power than the minimum needed for a given amplitude of oscillation.

The current (and thus the excess of negative resistance) is strongly dependent on the supply voltage and on the gate threshold voltage of the transistors. Since the amplitude limitation is achieved by increasing the losses, the amount of frequency pulling depends also strongly on these voltages and thus on the temperature. Furthermore, because of this strong possible overdrive, this circuit is prone to parasitic oscillation on unwanted modes of the resonator.

Its only advantages are a possible rail-to-rail output (peak-to-peak drain voltage close to  $V_B$ ) and a large power efficiency

$$\eta = \frac{P_m}{V_B I_0}. \quad (5.88)$$

The mechanical power  $P_m$  and the efficiency  $\eta$  calculated from the simulation of the circuit of Fig. 5.22 are plotted in Fig. 5.24. The power efficiency



**Figure 5.24** Mechanical power and power efficiency of the CMOS inverter-oscillator of Fig. 5.22(a) with  $R_m = 50 \text{ k}\Omega$ .

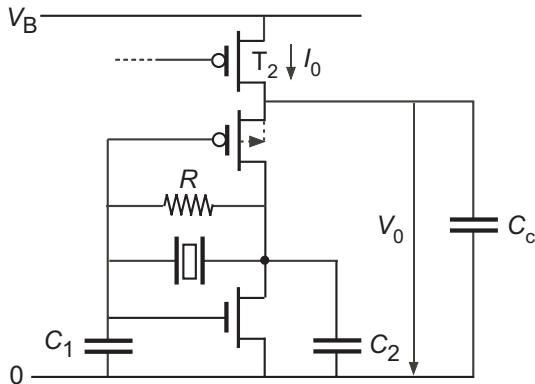
reaches a maximum close to 50% at the minimum value of  $V_B$  but decreases for higher values with the increase of losses.

Compared to the current-biased Pierce oscillator, the high value of  $P_m$  (and thus of  $E_m$  for a given value of  $Q$ ) might be an advantage to reduce the phase noise, according to (3.30). However, the noise excess factor  $\gamma$  is increased by a higher current due to losses, which compensates this higher energy of oscillation. Moreover, for high frequency resonators,  $P_m$  might largely exceed the acceptable value (it was close to the limit in Example 2 of Tables 4.1 to 4.3).

In spite of its apparent simplicity the direct implementation of a CMOS inverter-oscillator illustrated in Fig. 5.21 is not recommended because of its many pitfalls.

### 5.4.2 Current-controlled CMOS-inverter oscillator

The best way of exploiting the increased transconductance provided by a complementary inverter is to impose its bias current as illustrated by Fig. 5.25 [22].



**Figure 5.25** CMOS-inverter oscillator biased by current  $I_0$ . The coupling capacitor  $C_c$  is necessary to activate the P-channel transistor.

As for the basic grounded source circuit of Fig. 5.1 and all its variants and extensions, the bias current  $I_0$  is imposed by transistor  $T_2$ . A coupling capacitor  $C_c$  must be added to ensure the activity of the P-channel part of the inverter. Its impedance must be much lower than the source transconductance of the transistor. Assuming that the two complementary transistors have about the same transconductance (otherwise the complementary scheme is useless):

$$\omega C_c \gg nG_{mcrit}/2 \quad (5.89)$$

For the Example 1 of Section 4.5.2, this gives  $C_c \gg 4.9\text{ pF}$ , thus a large capacitance of at least  $50\text{ pF}$  is needed.

The large signal behavior of this complementary circuit is exactly the same as that of the basic circuit. When the amplitude grows, the DC component  $V_{G0}$  of the N-channel transistors decreases by  $\Delta V_{G0}$  according to Fig. 4.18 to keep  $I_0$  constant. For the P-channel transistor, the current is kept constant by a decrease  $\Delta V_0$  of the voltage  $V_0$  at its source. According to (3.40), the saturated drain current is controlled by  $V_G - nV_S$ . Hence, for symmetrical transistors ( $I_{specp} = I_{specn}$ ):

$$\Delta V_0 = 2\Delta V_{G0}/n. \quad (5.90)$$

To minimize losses, the two transistors should remain saturated in the peaks of drain amplitude:

$$V_{DS0n} + |V_2| < V_{DSsatn} \quad \text{and} \quad V_{DS0p} + |V_2| < V_{DSsatp}, \quad (5.91)$$

where  $V_{DS0n}$  and  $V_{DS0p}$  are the DC component of the voltage across the transistors, and  $|V_2|$  is, as before, the amplitude of oscillation at the drain.

Considering the case of *weak inversion*, (4.58),  $V_{DS0n}$  is obtained directly from (4.68):

$$V_{DS0n} = V_{G0n} = V_{T0n} - nU_T \ln \left[ \frac{I_{spec}}{I_{0critmin}} \cdot \frac{2I_{B1}(v_1)}{v_1} \right] \quad (5.92)$$

The same DC current  $I_0$  flows through the two complementary transistors. It is given by (4.58) with

$$v_e = v_{en} = \frac{V_{G0n} - V_{T0n}}{n_n U_T} \quad (5.93)$$

for the N-channel transistor and

$$v_e = v_{ep} = \frac{V_{G0p} - V_{T0p} - nV_{Sp}}{n_p U_T} \quad (5.94)$$

for the P-channel device (with the definitions of Fig. 3.10 for voltages). If the transistors are symmetrical ( $I_{specp} = I_{specn}$  and  $n_p = n_n$ ), equating the two expressions of  $I_0$  yields

$$V_{Sp} = (V_{G0p} - V_{T0p} - V_{G0n} + V_{T0n})/n, \quad (5.95)$$

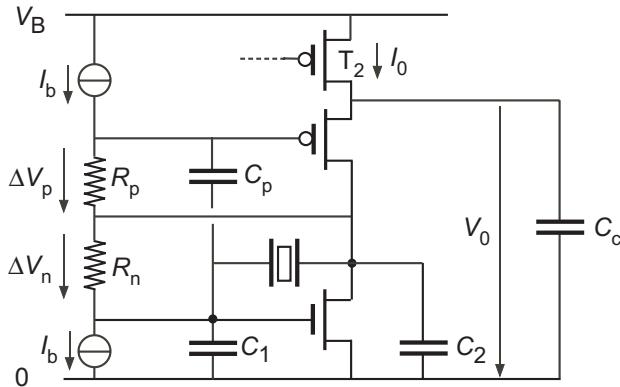
where  $V_{T0n}$  and  $V_{T0p}$  are the values of threshold  $V_{T0}$  for the two types of transistors. Now  $V_{G0p} = V_B - V_{G0n}$ , thus

$$V_{DS0p} = V_{G0p} - V_{Sp} = V_B \left( 1 - \frac{1}{n} \right) + V_{G0n} \left( \frac{2}{n} - 1 \right) + \frac{V_{T0p} - V_{T0n}}{n}, \quad (5.96)$$

or, by introducing (5.92)

$$V_{DS0p} = \frac{V_{T0p}}{n} + \frac{n-1}{n} (V_B - V_{T0n}) - (2-n)U_T \ln \left[ \frac{I_{spec}}{I_{0critmin}} \cdot \frac{2I_{B1}(v_1)}{v_1} \right]. \quad (5.97)$$

The drain amplitude  $|V_2|$  must then be limited to fulfill the two conditions of (5.91) with  $V_{DSsatn} = V_{DSsatp} \cong 5U_T$ . If needed, the DC voltage  $V_{DS0n}$



**Figure 5.26** CMOS-inverter oscillator modified to allow an increase of drain amplitude.

across the N-channel transistor can be increased by one of the schemes discussed in Section 5.1.6.

If the DC voltages across both transistors must be increased, the solution depicted in Fig. 5.26 can be implemented. Two separate resistors  $R_n$  and  $R_p$  are used to bias the gates of the two transistors, and a small current  $I_b$  is flown through them. The voltage drops  $\Delta V_n$  and  $\Delta V_p$  across them are equivalent to an increase of  $V_{Tn}$  and  $V_{Tp}$  in equations (5.92) and (5.96). The gate of the P-channel transistor is coupled by means of capacitor  $C_p$ .

If transistors must be used to implement resistors, the floating resistor  $R_p$  is hard to realize. It is then better to bias the gate of the P-channel transistor from a separate voltage source of adequate value.

As shown by (5.96),  $V_{DS0p}$  increases with  $V_B$ . This would not be the case if the P-channel transistor were put in a separate well connected to its source (as indicated in dotted line in Fig. 5.25). The DC voltage across the transistor would then be symmetrical to that of the N-channel device:

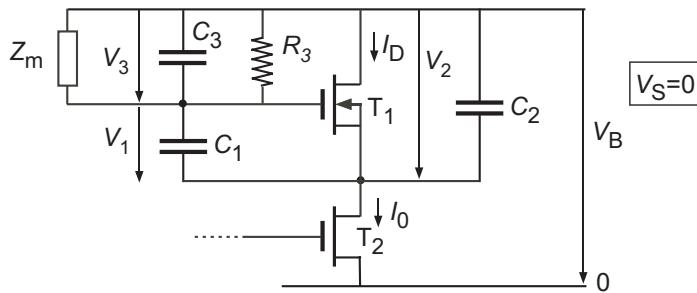
$$V_{DS0p} = V_{G0p} = V_{T0p} - nU_T \ln \left[ \frac{I_{spec}}{I_{0critmin}} \cdot \frac{2I_{B1}(V_1)}{v_1} \right], \quad (5.98)$$

which is always smaller than the value given by (5.96). The advantage would be a reduction of the minimum value of supply voltage  $V_B$ .

## 5.5 Grounded-Drain Oscillator

### 5.5.1 Basic Implementation

The basic grounded-drain version of the Pierce oscillator is shown in Fig. 5.27. To avoid modulation by the source, the active transistor  $T_1$  is put in a sep-



**Figure 5.27** Basic grounded-drain version of the 3-point Pierce oscillator.

arate well connected to its source. In this N-channel implementation, the drain of  $T_1$  is connected to the positive rail of the power supply (which is the ground of the AC signal), and a bias current  $I_0$  is delivered by a current source  $T_2$  (also N-channel). As in the grounded-source version,  $T_1$  is biased in saturation by means of resistor  $R_3$ .

All the results obtained in Chapter 4 for the Pierce oscillator are applicable to this circuit. But there are some notable differences with respect to the grounded-source implementation of Section 5.1.

One side of the resonator is grounded. Therefore, only one additional pin is needed, hence its appellation “single pin oscillator” [23]. But this advantage also turns out to be a drawback, since  $C_3$  now includes parasitic capacitors to ground (connecting pad, package feedthrough, external connections). Even if these are minimized, it includes  $C_{10}$  or  $C_{20}$  of the resonator itself. As a result,  $C_3$  becomes much larger than its minimum value  $C_{12}$  due to the resonator. The radius of the circular locus of Fig. 4.6 and the margin factor  $K_m$  defined by (4.17) are thus drastically reduced, with the various negative consequences discussed in Chapter 4.

One potential advantage of this implementation is that the voltage  $V_3$  across the resonator can be used as the output signal. As expressed by (4.37) this voltage is larger than  $V_1$ . However, this will further increase the over-

all value of  $C_3$ . It might also increase the loss conductance  $G_3$ , which has a strong effect on the critical transconductance, according to (4.45).

Another negative point is the fact that the relatively large capacitance to ground of the separate well is now part of  $C_2$ . Since this capacitance is voltage dependent, the frequency stability is degraded.

As for the grounded-source realization, even with a large value of supply voltage, the maximum amplitude is limited by the desaturation of the active transistor in the peak of oscillation. This limit can be pushed by flowing some current through the bias resistor  $R_3$ , thereby lowering the DC voltages at the gate and at the source and substrate node.

The resistor can be implemented by means of a P-channel transistor  $T_3$  biased in the linear region of strong inversion. Then, according to (3.50):

$$R_3 = \frac{1}{G_{ms3}} = \frac{U_T}{\sqrt{I_{F3} I_{spec3}}}. \quad (5.99)$$

The circuit of Fig. 5.27 assumes that a the N-channel active transistor can be put in a separate P-type well. If only N-type wells are available, P-channel devices must be used.

The amplitude of oscillation can be controlled by the regulator discussed in Section 5.2 (or by its P-channel version). This circuit can be capacitively coupled to the gate of  $T_1$  to control  $|V_3|$ , or to its drain to control  $|V_2|$ . It delivers the bias current  $I_0$ .

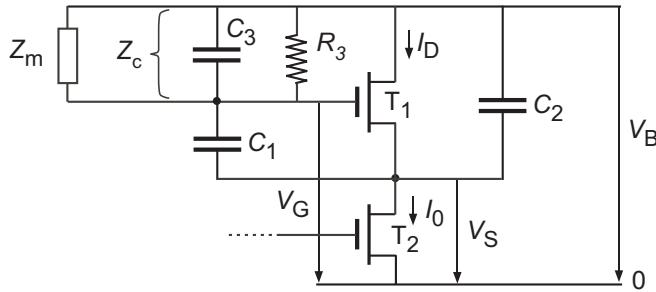
### 5.5.2 Single-Substrate Implementation

It might be tempting to avoid a separate well for the active transistor  $T_1$  and to realize the circuit as shown in Fig. 5.28. This was the only possibility for the first implementation of this oscillator in a P-MOS process [24]. The common substrate of the N-channel devices is now the negative rail of the power supply (reference 0). The source voltage  $V_S$  and drain voltage  $V_G$  are both changing with the oscillatory signal, whereas the drain voltage is constant and equal to  $V_B$ .

The general expression of the circuit impedance  $Z_c$  is now

$$Z_c = \frac{Z_1 Z_3 + Z_2 Z_3 + n G_m Z_1 Z_2 Z_3}{Z_1 + Z_2 + Z_3 + G_m Z_2 [n Z_1 + (n - 1) Z_3]}, \quad (5.100)$$

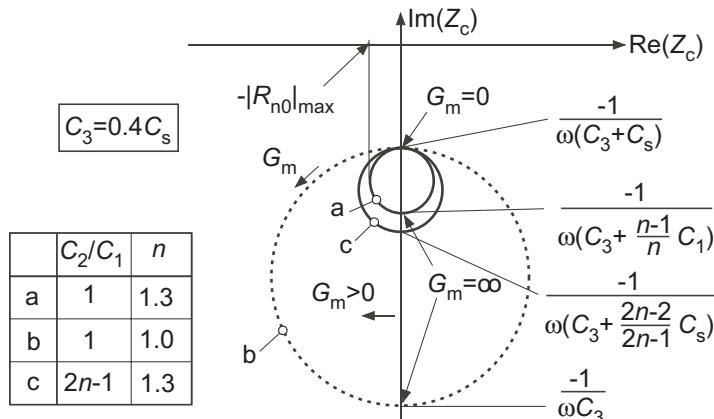
where each impedance  $Z_i$  is defined by (4.1). It would be reduced to (4.2) (impedance of the basic circuit) for  $n = 1$ . The circuit impedance is still a



**Figure 5.28** Grounded-drain 3-point Pierce oscillator without separate well.

bilinear function of the gate transconductance  $G_m$ , hence the locus of  $Z_c(G_m)$  is still a circle.

For the lossless circuit ( $Z_i = 1/j\omega C_i$ ), this circle is centered on the imaginary axis, as illustrated in Fig. 5.29.



**Figure 5.29** Loci of  $Z_c(G_m)$ : a: Single-substrate with  $C_1 = C_2$ ; b: separate well with  $C_1 = C_2$  (optimum ratio); c: single-substrate with  $C_2/C_1 = 2n-1$  (optimum ratio). All three loci have the same value of  $C_s + C_3$ , thus same frequency pulling for  $R_m \ll |R_{n0}|_{max}$ . The radius of the loci for the single-substrate is dramatically reduced.

Compared to the basic implementation of Fig. 5.27 (corresponding to  $n = 1$ ), the upper point of the circle ( $G_m = 0$ ) is not changed, but the lower point ( $G_m = \infty$ ) is much higher, due to the term  $C_1(n-1)/n$  added to  $C_3$ . The radius of the circle is therefore drastically reduced. The maximum value of negative resistance (radius of the circle) is reduced to

$$|R_{n0}|_{max} = \frac{n - (n-1)C_1/C_s}{2\omega C_3(1+C_3/C_s)(n+(n-1)C_1/C_3)}, \quad (5.101)$$

where  $C_s$  is the series combination of  $C_1$  and  $C_2$ .

For  $R_m \ll |R_{n0}|_{max}$  (which is much more difficult to satisfy), the critical transconductance for the lossless case is

$$G_{mcrit0} \cong \frac{\omega^2 R_m (C_1 C_2 + C_2 C_3 + C_3 C_1)^2}{C_1 [C_2 - (n-1)C_1]}, \quad (5.102)$$

or, by combination with (4.21) (which is not modified):

$$G_{mcrit0} \cong \frac{\omega C_m}{Q p_c^2} \cdot \frac{(C_1 + C_2)^2}{4C_1 [C_2 - (n-1)C_1]}, \quad (5.103)$$

which reduces to (4.26) for  $n = 1$ . The optimum is no longer for  $C_1 = C_2$ , but for

$$C_2 = (2n-1)C_1 \quad \text{giving} \quad G_{mcrit0} \cong n \frac{\omega C_m}{Q p_c^2}. \quad (5.104)$$

Thus, even with the optimum capacitance ratio, the critical transconductance for a given value of frequency pulling is increased by factor  $n$ . As shown in Fig. 5.28 (curve c), the radius of the locus is slightly larger than for  $C_1 = C_2$  (curve a), but still much smaller than for the optimum implementation with a separate well (curve b).

In summary, the implementation of the grounded-drain Pierce oscillator in a single substrate (with no separate well) strongly reduces the radius of the circular locus, thereby reducing the margin factor  $K_m$  defined by (4.17). The minimum critical transconductance is increased and is obtained with  $C_1 < C_2$  (and thus  $|V_1| > |V_2|$  according to (4.38)). In view of these many drawbacks, this solution should be avoided.

# Chapter 6

## Alternative Architectures

### 6.1 Introduction

The basic 3-point Pierce oscillator of Fig. 4.1 is the only possible configuration of a quartz (or MEMS) oscillator using a single active transistor. As soon as two or more active transistors are considered, many configurations become possible. Three of them will be discussed in this last Chapter.

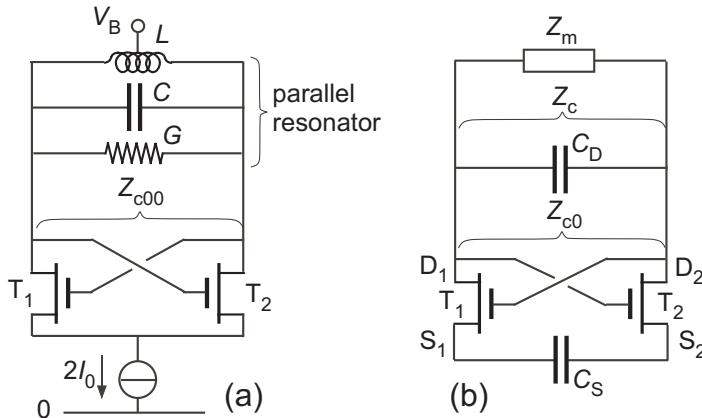
Two-transistors symmetrical circuits for parallel and series resonance will be analyzed in Sections 6.2 and 6.3. An example of more complicated architecture using an operational transconductance amplifier (OTA) will be presented more briefly in Section 6.4. These three circuits will be compared with the Pierce oscillator in Section 6.5.

### 6.2 Symmetrical Oscillator for Parallel Resonance

#### 6.2.1 Basic Structure

The standard circuit used for a symmetrical parallel resonance oscillator is illustrated in Fig. 6.1(a). It is based on a known circuit using vacuum tubes (figure 68b, page 82 of [15]). The negative resistance produced by the cross-coupled differential pair is simply

$$Z_{c00} = -2/G_m, \quad (6.1)$$



**Figure 6.1** Basic parallel resonance oscillator; (a) standard circuit for a  $R, L, G$  resonator; (b) modified circuit adapted to the absence of a DC path in the resonator (without bias circuitry).

where  $G_m$  is the transconductance of each transistor. The critical condition for oscillation is thus

$$G_m = 2G, \quad (6.2)$$

and oscillation will take place exactly at the resonant frequency of the resonator, since the circuit admittance is real (except for the effect of parasitic capacitors).

This circuit produces a *voltage stable* negative resistance compatible with parallel resonance. It would not provide a stable oscillatory solution with a plain series resonator. One obvious reason is that a DC path is needed across the resonator, otherwise the circuit becomes bistable. But even if bistability is avoided by some means, no stable oscillation would be possible, because the basic condition (1.2) for phase stability would not be fulfilled. Therefore, if this circuit is associated with a quartz resonator, it must exploit the parallel resonance discussed in Chapter 2. For this parallel resonance, the parallel capacitance  $C_P$  is part of the resonator. If necessary, this capacitance may be increased to a value  $C_D > C_P$  to reduce the amount of frequency pulling.

To eliminate the DC bistable solution, the DC coupling between the sources of the transistors must be replaced by a capacitive coupling  $C_S$  as illustrated in Fig. 6.1(b). The circuit impedance (without parallel capacitance) becomes

$$Z_{c0} = -\frac{2}{G_m} + j \frac{n}{\omega C_S}. \quad (6.3)$$

Away from the resonant frequencies of the quartz, the drains are simply connected by a parallel capacitance  $C_D$  and a parasitic oscillation may occur at the frequency  $\omega_p$  that cancels the imaginary part of the total admittance:

$$\text{Im} \left[ \frac{1}{Z_{c0}(\omega_p)} \right] + \omega_p C_D = 0, \quad (6.4)$$

which results in

$$\omega_p^2 = \frac{nG_m^2}{4C_D C_S} \left( 1 - \frac{nC_D}{C_S} \right). \quad (6.5)$$

Thus if

$$C_S < nC_D, \quad (6.6)$$

this frequency does not exist and no parasitic oscillation can occur.

### 6.2.2 Linear Analysis with the Parallel Resonator

The variation of the parallel impedance  $Z_p$  of the resonator (i.e with the parallel capacitance  $C_p$  across the motional impedance  $Z_m$ ) was discussed in Chapter 2, with the locus of  $Z_p(Qp)$  illustrated in Fig. 2.3. This circular locus is reproduced in Fig. 6.2, with the figure of merit  $M$  replaced by its value for the loaded dipole resonator defined by

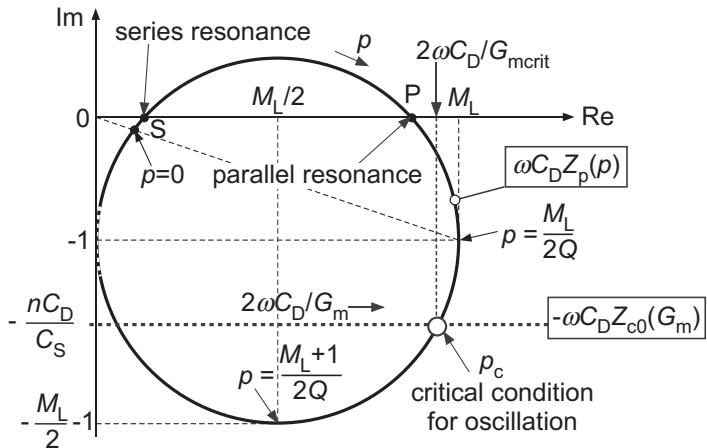
$$M_L \triangleq \frac{QC_m}{C_D} \leq M_D < M_0. \quad (6.7)$$

The circuit impedance  $Z_{c0}$  given by (6.3) (without the parallel capacitance  $C_D$  that is now part of the parallel resonator) is a linear function of  $2/G_m$  with a constant imaginary part. The locus of  $-\omega C_D Z_{c0}$  is plotted in dotted line in Fig. 6.2. It is an horizontal strait line that is below -1 in order to fulfill condition (6.6). One of its two intersections with  $\omega C_D Z_p(p)$  corresponds to the critical condition for oscillation (the other can be shown to be unstable).

As can be seen, the oscillation frequency is always *above* the parallel resonance frequency. By introducing the definition (6.7) of  $M_L$ , the range of possible pulling can be expressed as

$$\frac{C_m}{2C_D} \leq p_c \leq \frac{C_m}{2C_D} + \frac{1}{2Q}, \quad (6.8)$$

whereas the range of critical transconductance for the lossless circuit is



**Figure 6.2** Normalized loci of  $Z_p(p)$  and  $-Z_{c0}(G_m)$ . Their intersection defines the critical condition for oscillation.

$$\frac{2\omega C_D}{M_L} \leq G_{mcrit0} \leq \frac{4\omega C_D}{M_L}. \quad (6.9)$$

In normal cases,  $M_L \gg 1$  (very large circle) whereas  $nC_D/C_s$  is not much larger than unity. Then  $G_{mcrit0}$  has the lowest value of this range:

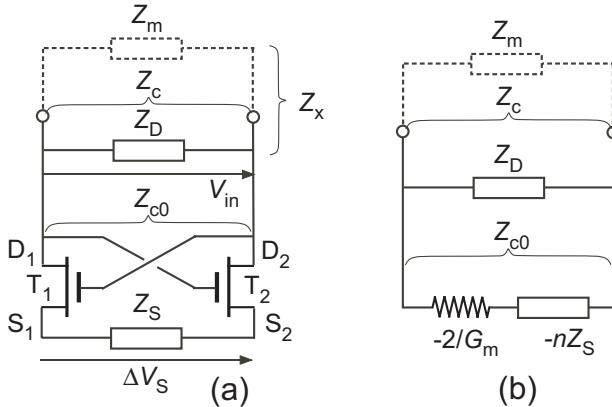
$$G_{mcrit0} = \frac{2\omega C_D}{M_L} = \frac{2\omega C_D^2}{QC_m} = 2\omega^2 C_D^2 R_m. \quad (6.10)$$

### 6.2.3 Linear Analysis with the Series Motional Resonator

Although it is basically a parallel resonance oscillator, this circuit can be analyzed as was done for the previous circuit, by separating the motional impedance  $Z_m$  of the resonator from the overall circuit impedance  $Z_c$  (that includes the parallel capacitance  $C_D$ ). Both approaches are equivalent for the small-signal linear analysis, but the splitting  $(Z_m, Z_{c(1)})$  is needed to consider nonlinear effects, as explained in Chapter 3. Indeed, the current flowing through  $Z_p$  is no longer sinusoidal when the voltage across it is distorted.

The impedance of the whole circuit shown in Fig. 6.3(a) in the general case with losses is

$$Z_c = \frac{Z_D Z_{c0}}{Z_D + Z_{c0}} = \frac{Z_D (2 + nG_m Z_S)}{2 + nG_m Z_S - G_m Z_D}, \quad (6.11)$$



**Figure 6.3** Parallel resonance oscillator with lossy impedances  $Z_S$  and  $Z_D$ ; (a) full circuit without bias; (b) small-signal equivalent circuit.

It corresponds to the small-signal equivalent circuit of Fig. 6.3(b).

The values of  $Z_c$  for the extremes of  $G_m$  are

$$Z_c = Z_D \quad \text{for } G_m = 0 \quad \text{and} \quad \frac{nZ_D Z_S}{nZ_S - Z_D} \quad \text{for } G_m = \infty. \quad (6.12)$$

If the two impedances are simply capacitors (lossless circuit), these limits become  $-j/\omega C_D$  and  $-j/\omega(C_D - C_S/n)$ , and the circular locus of  $Z_c$  is centered on the imaginary axis, as illustrated in Fig. 6.4.

The stable locus with  $C_S < C_D$  looks similar to the locus of  $Z_c(G_m)$  for the Pierce lossless oscillator, represented in Fig. 4.6. However, there is a major difference due to the fact that  $C_D$  plays the role of  $C_3 + C_s$ , but can be much smaller. The amount of pulling can therefore be larger than for the Pierce circuit, with the advantage of a smaller value of critical transconductance (given by (6.10)), and the drawback of a larger dependency on  $C_D$ .

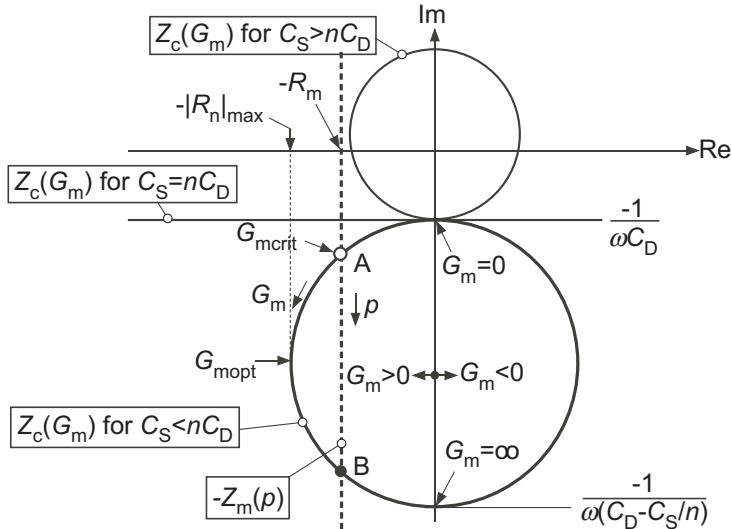
As for the Pierce circuit, the locus of  $-Z_m(p)$  is also represented in Fig. 6.4. The critical condition for oscillation is at its intersection A with  $Z_c(G_m)$ .

The maximum value of negative resistance is easily obtained by inspection, since it is the radius of the circle:

$$|R_{n0}|_{max} = \frac{1}{2\omega C_D(nC_D/C_S - 1)}. \quad (6.13)$$

It is reached for  $G_m = G_{mopt}$  given by

$$G_{mopt} = \frac{2\omega C_D}{nC_D/C_S - 1}. \quad (6.14)$$



**Figure 6.4** Loci of  $Z_c(G_m)$  and  $-Z_m(p)$  for the circuit of Fig. 6.1(b); the limit case for  $nC_S = C_D$  and the unstable case for  $nC_S > C_D$  are represented in thinner lines.

The maximum negative resistance increases to infinity for the limit case  $C_S = nC_D$ . In practice, it is limited by the need to ensure some margin of security. This margin depends on the worst mismatch expected between  $C_D$  and  $C_S/n$ . This mismatch can be large, since the two capacitors do not have the same structure.

Let us define the maximum relative mismatch

$$\varepsilon_{max} \triangleq \frac{(nC_D/C_S)_{max} - (nC_D/C_S)_{min}}{(nC_D/C_S)_{max} + (nC_D/C_S)_{min}}. \quad (6.15)$$

Since the minimum value of  $nC_D/C_S$  must be larger or equal to unity, its nominal value must be at least  $1/(1 - \varepsilon_{max})$  and its maximum value will be  $(1 + \varepsilon_{max})/(1 - \varepsilon_{max})$ . The maximum value of negative resistance will be in the range

$$\frac{1 - \varepsilon_{max}}{4\omega C_D \cdot \varepsilon_{max}} \leq |R_{n0}|_{max} \leq \infty, \quad (6.16)$$

with  $C_D \geq C_P$ .

Now, as was discussed for the Pierce circuit, the motional resistance  $R_m$  should be much smaller than the maximum negative resistance  $|R_n|_{max}$ , so that the point A corresponding to stable oscillation remains located at the top of the circle. The imaginary part is then  $-1/\omega C_D$ , which introduced in (3.10) gives

$$p_c = \frac{C_m}{2C_D}, \quad (6.17)$$

the minimum of the range defined by (6.8).

By introducing this result in (6.10), the critical transconductance can be expressed as

$$G_{mcrit0} = \frac{\omega C_m}{2Q p_c^2}. \quad (6.18)$$

An inspection of Fig. 6.3 shows that the amplitudes at the gates and at the sources are simply related by  $V_{in}/\Delta V_S = -Z_x/Z_S$ , where  $Z_x$  is the parallel combination of  $Z_m$  and  $Z_D$  ( $Z_x = Z_p$  if  $Z_D$  is just the lossless parallel capacitance  $C_D$ ).

Now, at the critical condition for oscillation,  $Z_x = Z_{c0}$ . In the lossless case,  $Z_{c0}$  is given by (6.3). Hence, with  $G_{mcrit}$  given by (6.10):

$$\frac{V_{in}}{\Delta V_S} = -\frac{Z_{c0}}{Z_S} = n + j \frac{2\omega C_S}{G_{mcrit}} = n + j \frac{C_S}{C_D} \cdot \frac{QC_m}{C_D} = n + j \frac{C_S}{C_D} \cdot M_L. \quad (6.19)$$

If  $C_D$  is not too large, the figure of merit  $M_L$  defined by (6.7) remains much larger than unity. Moreover,  $C_S/C_D$  is close to  $n$ . Hence, the voltage ratio  $V_{in}/\Delta V_S$  is essentially imaginary and much larger than unity. But this is no longer true if  $C_D$  is made much larger than  $C_p$  to reduce the frequency pulling given by (6.17).

#### 6.2.4 Effect of Losses

The lossy impedance at the drain can be expressed as

$$Z_D = \frac{1}{G_D + j\omega C_D}. \quad (6.20)$$

Its real part is then

$$\text{Re}(Z_D) = \frac{G_D}{G_D^2 + (\omega C_D)^2} \underbrace{\simeq \frac{G_D}{(\omega C_D)^2}}_{\text{for } G_D^2 \ll (\omega C_D)^2}. \quad (6.21)$$

Since most of the oscillatory current flows around the loop  $Z_m Z_D$ , this resistance comes in series with the motional resistance  $R_m$  (thereby reducing the quality factor Q). According to (6.10), this increases the critical transconductance by

$$\Delta G_{mcrit} = 2\omega^2 C_D^2 \operatorname{Re}(Z_D) \cong 2G_D. \quad (6.22)$$

With losses, the imaginary part of  $Z_D$  is

$$\operatorname{Im}(Z_D) = \frac{-1}{\omega C_D \left[ 1 + \left( \frac{G_D}{\omega C_D} \right)^2 \right]}. \quad (6.23)$$

The effective value of  $C_D$  is thus increased, which increases the margin of stability imposed by (6.6). But it also has an effect of the frequency of oscillation, according to (6.17).

Losses associated with  $C_S$  at the oscillation frequency are best characterized by a series resistance  $R_S$ :

$$Z_S = R_S + \frac{1}{j\omega C_S}. \quad (6.24)$$

This resistance has no effect on the pulling, but half of it degenerates the transconductance of each transistor. Introducing (6.22), the critical transconductance with losses becomes

$$G_{mcrit} = \frac{G_{mcrit0}}{1 - nR_S G_{mcrit0}/2} + 2G_D. \quad (6.25)$$

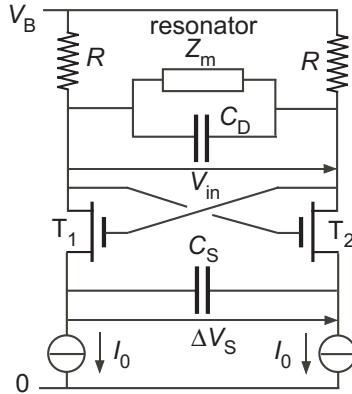
### 6.2.5 Nonlinear Analysis

The most immediate way of biasing the active transistors is shown in Fig. 6.5 [25]. The two transistors are biased by separate current sources  $I_0$ , and load resistors  $R$  fix the common mode drain voltage at  $V_B - RI_0$ . The value of these resistors should be high enough to limit the drain loss conductance  $G_D = 1/2R$ . Indeed, according to (6.22) they cause an increase of critical transconductance  $\Delta G_{mcrit} = 1/R$ .

Now, the AC drain voltage is produced by the drain current flowing through the parallel resonant circuit of impedance  $Z_p$ . At the frequency of oscillation Fig. 6.2 shows that for the usual case of  $M_L \gg 1$

$$\omega C_D Z_p = M_L - jnC_D/C_S. \quad (6.26)$$

Hence,  $|Z_p|$  is much larger than the impedance of  $C_D$  alone. Since the latter is further reduced for harmonic components of current produced by the



**Figure 6.5** parallel resonance oscillator biased by current sources  $I_0$  and resistors  $R$ .

transistors, these are virtually short-circuited, and the voltage  $V_{in}$  across it remains approximately sinusoidal.

The active part of the circuit can be seen as a differential pair with the source transconductance of each transistor degenerated by a series capacitance  $2C_S$ . The degeneration can be neglected if

$$G_{ms} = nG_m \ll 2\omega C_S. \quad (6.27)$$

By introducing the expression (6.10) of  $G_{mcrit0}$ , this condition becomes

$$\frac{G_m}{G_{mcrit0}} \cdot \frac{nC_D}{C_S} \ll M_L. \quad (6.28)$$

Thus, as long as the figure of merit  $M_L$  of the loaded resonator is sufficiently large, a *good approximation* is obtained by considering the circuit as a differential amplifier biased by a current source  $2I_0$ , and driven by the differential sinusoidal gate voltage  $V_{in}$ .

When the bias current  $I_0$  exceeds a critical value  $I_{0crit}$ , the amplitude  $|V_{in}|$  increases until it is limited by the nonlinear transfer function of this differential pair. A small values of  $V_{in}$  produces a small difference of drain currents  $\Delta I_D = G_m V_{in}$  that mainly flows through the parallel resonator. Indeed, the small-signal transconductance of the differential pair is equal to the transconductance  $G_m$  of one of the transistors alone, and the critical condition of oscillation is obtained for  $G_m = G_{mcrit}$ .

When  $|V_{in}|$  increases  $\Delta I_D$  is distorted, and its fundamental component  $\Delta I_{D(1)}$  is reduced. Stable oscillation is reached when  $G_{m(1)} = G_{mcrit}$ , where

$G_{m(1)}$  is the transconductance of the differential pair for the fundamental frequency defined by

$$G_{m(1)} \triangleq |\Delta I_{D(1)}| / |V_{in}|. \quad (6.29)$$

If the transistors are in *weak inversion*, the transfer function of the differential pair is a hyperbolic tangent and the fundamental component of output current is given by

$$\Delta I_{D(1)} = 2I_0 \cdot \underbrace{\frac{1}{\pi} \int_0^{2\pi} \tanh\left(\frac{v_{in}}{2} \sin \phi\right) \sin \phi \cdot d\phi}_{f_w(v_{in})}, \quad (6.30)$$

where  $v_{in}$  is the normalized value of the amplitude  $|V_{in}|$  defined by

$$v_{in} \triangleq \frac{|V_{in}|}{nU_T}. \quad (6.31)$$

Introducing (6.30) in (6.29) gives at stable oscillation

$$G_{m(1)} = \frac{2I_0}{nU_T} \cdot \frac{f_w(v_{in})}{v_{in}} \equiv G_{mcrit} = \frac{I_{0critmin}}{nU_T}, \quad (6.32)$$

or finally

$$\frac{I_0}{I_{0critmin}} = \frac{v_{in}}{2f_w(v_{in})}. \quad (6.33)$$

This result is plotted in Fig. 6.6.

If the transistors are in *strict strong inversion*, the transfer function of the differential pair biased by  $2I_0$  can be calculated from (3.43). The dependency of the two drain currents on the differential input voltage  $V_{in}$  obtained from this calculation is

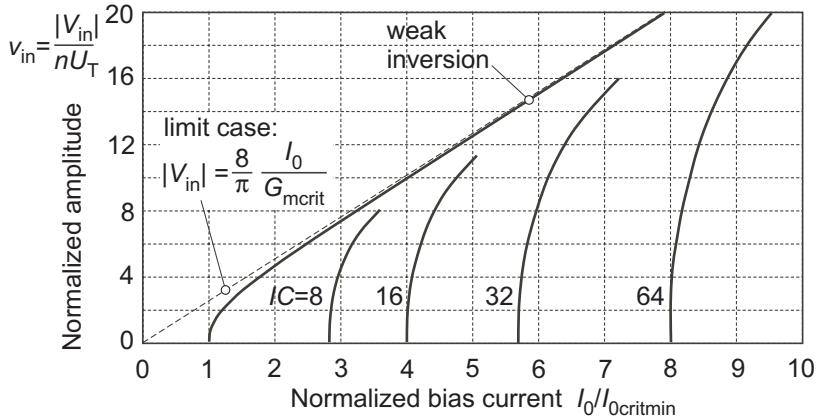
$$I_{D1} = I_0(1 - m_{vd}\sqrt{2 - m_{vd}^2}) \text{ and } I_{D2} = I_0(1 + m_{vd}\sqrt{2 - m_{vd}^2}), \quad (6.34)$$

where

$$m_{vd} \triangleq \frac{|V|_{in}}{2nU_T\sqrt{2IC}} = \frac{v_{in}}{2\sqrt{2IC}}, \leq 1, \quad (6.35)$$

is the index of voltage modulation of the differential pair and  $IC = I_0/I_{spec}$  is the inversion coefficient of the transistors at current  $I_0$ . Notice that this inversion coefficient is *different* from its value  $IC_0 = I_{0crit}/I_{spec}$  as soon as the amplitude is increased. But introducing  $IC_0$  instead of  $IC$  does not result in a closed form solution.

The difference of drain currents is then



**Figure 6.6** Amplitude limitation by a differential pair. These results are applicable to the parallel resonance oscillator if  $|V_{in}| \gg |\Delta V_S|$  according to (6.19). Here, the curves for strong inversion correspond to a constant value of inversion coefficient  $IC$ , and not to a constant  $I_{spec}$  of the transistors.

$$\frac{\Delta I_D}{2I_0} = m_{vd} \sqrt{2 - m_{vd}^2}. \quad (6.36)$$

The fundamental component of output current is given by

$$\Delta I_{D(1)} = 2I_0 \cdot \underbrace{\frac{1}{\pi} \int_0^{2\pi} m_{vd} \sin^2 \phi \sqrt{2 - (m_{vd} \sin \phi)^2} \cdot d\phi}_{f_s(m_{vd})}. \quad (6.37)$$

Introducing again this result in (6.29) gives at stable oscillation

$$G_{m(1)} = \frac{2I_0}{nU_T} \cdot \frac{f_s(m_{vd})}{v_{in}} \equiv G_{mcrit} = \frac{I_{0critmin}}{nU_T}, \quad (6.38)$$

where  $I_{0critmin}$  is the minimum critical current (that would be reached in weak inversion). Finally, knowing that  $I_{0crit} = \sqrt{IC_0} \cdot I_{0critmin}$ :

$$I_0 = \frac{v_{in}}{2f_s(\frac{v_{in}}{2\sqrt{2IC}})} I_{0critmin} = \frac{\sqrt{2}m_{vd}}{f_s(m_{vd})} \cdot \sqrt{\frac{IC}{IC_0}} I_{0crit}. \quad (6.39)$$

This result is also plotted in Fig. 6.6 for several values of inversion coefficient  $IC$ . Now, the parameter  $IC = I_0/I_{spec}$  is *not constant* if the bias current  $I_0$  is increased to increase the amplitude. Thus, the curves for strong inversion *do not* represent the variation of amplitude for a given value of  $I_{spec}$ . The design process should therefore be the following:

- select an amplitude  $v_i$
- select an inversion coefficient  $IC$
- obtain the value of  $I_0$  from the graph and from  $I_{0critmin} = nU_T G_{mcrit}$ .
- calculate the required value of  $I_{spec} = I_0/IC$ .

Part of the curves are missing in the calculation due to the limit of validity of (6.36), but all curves finally merge at the limit value

$$|V_{in}|_{lim} = \frac{8nU_T I_0}{\pi I_{0critmin}} = \frac{8}{\pi} \cdot \frac{I_0}{G_{mcrit}} \quad (6.40)$$

corresponding to a square waveform of the drain currents.

Knowing the voltage amplitude  $|V_{in}|$  across the resonator, the motional current can be calculated. For  $R_m \ll 1/(\omega C_D)$  (hence for  $M_L \gg 1$ ),  $1/Z_m = -1/Z_c \cong -j\omega C_D$ . The motional current is then

$$I_m = V_{in}/Z_m = -j\omega C_D V_{in}. \quad (6.41)$$

This result can be introduced in (2.23) and (2.24) to obtain the energy of mechanical oscillation and the power dissipated in the resonator:

$$E_m = \frac{C_D^2 |V_{in}|^2}{2C_m} \quad \text{and} \quad P_m = \frac{\omega C_D^2 |V_{in}|^2}{2QC_m}. \quad (6.42)$$

In order to avoid clipping the sinusoidal drain voltage, the voltage drop  $RI_0$  across the resistors should be larger than half the amplitude  $|V_{in}| = k|V_{in}|_{lim}$ , with  $k \leq 1$  and  $|V_{in}|_{lim}$  given by (6.40). The resistance produces a loss conductance  $2G_D = 1/R$ , which must be added to the lossless transconductance  $G_{mcrit0}$  according to (6.22). This gives the condition

$$R \geq \frac{1}{G_{mcrit0}} \left( \frac{4k}{\pi} - 1 \right), \quad (6.43)$$

which is easily fulfilled, even with the maximum value of  $k = 1$  (or  $|V_{in}| = |V_{in}|_{lim}$ ). However, at this limit, the critical transconductance is increased by a factor close to 5 by the losses due to the resistor. To reduce these losses, the value of  $R$  must be increased much above this limit, at the cost of an increase of supply voltage  $V_B$ . In order to limit the excess of transconductance  $\Delta G_{mcrit}$  to a small value  $\alpha \cdot G_{mcrit0}$ , the voltage drop across  $R$  must be increased to

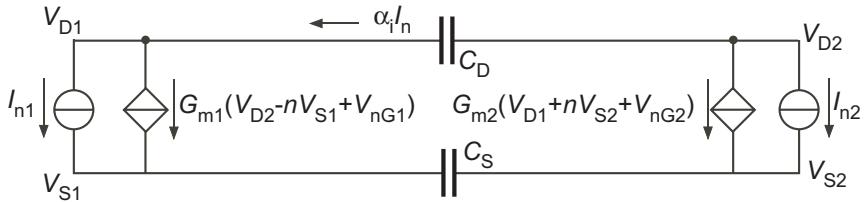
$$RI_0 = \frac{\pi(1+\alpha)}{4\alpha} \cdot \frac{|V_{in}|_{lim}}{2}. \quad (6.44)$$

For example, for  $\alpha = 0.1$ , the voltage drop must be increased to 8.6 times the maximum amplitude  $|V_{in}|_{lim}/2$ , which requires a large value of supply voltage  $V_B$ . This can be avoided by using the practical implementations discussed in Section 6.2.7.

### 6.2.6 Phase Noise

#### 6.2.6.1 Noise Current

The noise analysis of the basic lossless circuit of Fig. 6.1(b) can be carried out with the equivalent circuit of Fig. 6.7.



**Figure 6.7** Equivalent circuit for the calculation of noise.

Although the circuit is physically symmetrical, the transconductance  $G_{m1}$  and  $G_{m2}$  of the transistors vary in opposite phase along each cycle of oscillation. Therefore, their values are not equal. Furthermore, the noise sources  $I_{n1}$ ,  $I_{n2}$ ,  $V_{nG1}$  and  $V_{nG2}$  are not correlated. Calculations with this circuit give the cyclostationary noise current flowing through  $C_D$ :

$$\alpha_i I_n = \frac{G_{m2}I_{n1} - G_{m1}I_{n2} + G_{m1}G_{m2}(V_{nG1} - V_{nG2})}{(G_{m1} + G_{m2}) + G_{m1}G_{m2}(n/C_S - 1/C_D)/j\omega_n}. \quad (6.45)$$

According to (6.6), the equivalent capacitance

$$C_{eq} \triangleq \frac{1}{n/C_S - 1/C_D} = \frac{C_D}{nC_D/C_S - 1} \quad (6.46)$$

is always positive for the stable circuit. The corresponding imaginary part in (6.45) is negligible if

$$\omega_n C_{eq} \gg G_{meq} = \frac{G_{m1}G_{m2}}{G_{m1} + G_{m2}}. \quad (6.47)$$

or, by using (6.46), (6.10) and (6.7)

$$\frac{\omega_n C_D}{nC_D/C_S - 1} \gg G_{meq} = \frac{G_{meq}}{G_{mcrit0}} \cdot \frac{2\omega C_D^2}{QC_m} = \frac{G_{meq}}{G_{mcrit0}} \cdot \frac{2\omega C_D}{M_L}. \quad (6.48)$$

Hence, the imaginary part in (6.45) can be neglected for

$$\frac{\omega_n}{\omega} \gg \left( \frac{nC_D}{C_S} - 1 \right) \cdot \frac{G_{meq}}{G_{mcrit0}} \cdot \frac{2}{M_L}. \quad (6.49)$$

The right hand term is normally much smaller than unity, therefore this condition is fulfilled even for noise frequencies  $\omega_n$  much lower than the oscillation frequency  $\omega$ . The expression (6.45) can then be approximated by

$$\alpha_i I_n = \frac{G_{m2}I_{n1} - G_{m1}I_{n2} + G_{m1}G_{m2}(V_{nG1} - V_{nG2})}{G_{m1} + G_{m2}}. \quad (6.50)$$

This approximation corresponds to a worst case, since the imaginary term would reduce the value of  $\alpha_i I_n$ .

Because of the capacitance  $C_S$  between the two sources, the transconductance of the differential amplifier is slightly reduced. Although this effect can be (and has been) neglected in the calculation of the amplitude, it creates a phase shift  $\Delta\phi$  between the gate voltages and the drain currents. This phase shift is given by

$$\tan \Delta\phi = \frac{nG_{m1}G_{m2}}{\omega C_S(G_{m1} + G_{m2})}. \quad (6.51)$$

For small amplitudes,  $G_{m1} = G_{m2} = G_{mcrit}$ , thus

$$\tan \Delta\phi = \frac{nG_{mcrit}}{2\omega C_S} = \frac{nC_D}{C_S} \cdot \frac{1}{M_L} \cdot \frac{G_{mcrit}}{G_{mcrit0}}, \quad (6.52)$$

where the last form has been obtained by introducing the expression (6.10) of  $G_{mcrit0}$ . This phase shift has a minimum value  $\Delta\phi = \arctan(1/M_L)$  for  $C_S = nC_D$  and  $G_{mcrit} = G_{mcrit0}$  (no loss in the circuit).

For large amplitudes,  $\Delta\phi$  is variable along each cycle (which means that it participates to the distortion of the drain currents), but we will use the *approximation of a constant phase shift* given by (6.52), which is the maximum value of (6.51).

### 6.2.6.2 Phase Noise of the Linear Circuit

If the amplitude is very small, the circuit remains linear, and the phase noise can be calculated as explained in Section (3.7.1). The noise voltage  $V_n$  across  $C_D$  is obtained from (6.50) with  $\alpha_i = 1$  (stationary noise),  $V_{G1} = V_{G2} = 0$  (since the 1/f gate noise voltage cannot be transposed around the oscillation frequency) and  $G_{m1} = G_{m2} = G_{mcrit}$ :

$$V_n = \frac{I_{n1} - I_{n2}}{2j\omega C_D}. \quad (6.53)$$

If the noise currents are solely the channel noise of the transistors, their spectra are given by (3.60). The noise spectrum of  $V_n$  can then be expressed as

$$S_{V_n^2} = 2kTn\gamma_t \frac{G_{mcrit}}{(\omega C_D)^2} = 4kTn\gamma_t R_m \cdot \frac{G_{mcrit}}{G_{mcrit0}}, \quad (6.54)$$

where the second form has been obtained by introducing the expression (6.10) of the critical transconductance for the lossless circuit.

The small-amplitude noise excess factor due to the channel noise of the active transistors is then obtained by inspection of Fig. 3.7:

$$\gamma_0 = \frac{S_{V_n^2}}{4kTR_m} = n\gamma_t \frac{G_{mcrit}}{G_{mcrit0}}, \quad (6.55)$$

where  $G_{mcrit}/G_{mcrit0}$  is the increase of critical transconductance due to possible losses.

### 6.2.6.3 Phase Noise due to White Channel Noise in the Nonlinear Time Variant Circuit

For a large amplitude of oscillation, the voltage  $V_{in}$  across  $C_D$  remains approximately sinusoidal but the drain currents are distorted. From (6.50) and (3.60), the spectrum of the cyclostationary noise current injected in  $C_D$  is then

$$\alpha_i^2 S_{I_n^2} = \frac{G_{m2}^2 S_{I_{nD1}^2} + G_{m1}^2 S_{I_{nD2}^2}}{(G_{m1} + G_{m2})^2} = 4kTn\gamma_t \frac{G_{m1}G_{m2}}{G_{m1} + G_{m2}}. \quad (6.56)$$

Notice that the simplification in the second form is made possible by the introduction of the channel noise sources of the two transistors. This is possible since the values of  $\alpha_i^2$  corresponding to each source will be simply added in the calculation of  $\overline{I_i^2}$ .

Neglecting the effect of  $C_S$ , the drain currents in *weak inversion* can be expressed as

$$I_{D1} = \frac{2I_0}{1 + e^{v_{in}\sin\phi}} \quad \text{and} \quad I_{D2} = \frac{2I_0}{1 + e^{-v_{in}\sin\phi}}, \quad (6.57)$$

where  $v_{in}$  is the normalized voltage amplitude defined by (6.31) and  $\phi = \omega t$ . The corresponding transconductances in saturation are thus given by (3.54):

$$G_{m1} = \frac{2I_0}{nU_T(1 + e^{v_{in}\sin\phi})} \quad \text{and} \quad G_{m2} = \frac{2I_0}{nU_T(1 + e^{-v_{in}\sin\phi})}, \quad (6.58)$$

Using (6.33) to replace  $I_0$  by  $I_{0critmin}$ , these expressions can be introduced in (6.56), which gives

$$\alpha_i^2 S_{I_n^2} = \underbrace{2\gamma q I_{0critmin} \cdot \frac{v_{in}}{2f_w(v_{in})}}_{S_{I_n^2}} \cdot \underbrace{\frac{4}{2 + e^{v_{in}\sin\phi} + e^{-v_{in}\sin\phi}}}_{\alpha_i^2}. \quad (6.59)$$

According to (3.34), the mean squared RMS value of the effective impulse sensitivity function (ISF) is thus, for *weak inversion*

$$\overline{I_i^2} = \overline{\cos^2(\phi + \Delta\phi)\alpha_i^2} = \frac{1}{2\pi} \int_0^{2\pi} \frac{4\cos^2(\phi + \Delta\phi)}{2 + e^{v_{in}\sin\phi} + e^{-v_{in}\sin\phi}} d\phi, \quad (6.60)$$

where  $\Delta\phi$  is the phase shift approximated by (6.52). The phase noise spectrum is then obtained by introducing the above values of  $S_{I_n^2}$  and  $\overline{I_i^2}$  in (3.33), which results in

$$S_{\phi_n^2} = S_{\phi_n^2 0} \cdot \frac{v_{in}}{f_w(v_{in})} \cdot \overline{I_i^2}, \quad (6.61)$$

where

$$S_{\phi_n^2 0} = \frac{\gamma_t q I_{0critmin}}{2(C_D |V_{in}|)^2 \Delta\omega^2} \cdot \left( \frac{C_m}{C_D} \right)^2, \quad (6.62)$$

or, by introducing (3.54), (6.10) and (2.3), and knowing that  $C_D V_{in} = I_m / \omega$ :

$$S_{\phi_n^2 0} = \frac{\gamma_t n k T \omega^2}{|I_m|^2 Q^2 R_m \Delta\omega^2} \cdot \frac{G_{mcrit}}{G_{mcrit0}}. \quad (6.63)$$

Comparing this result with (3.29) gives the expression (6.55) of the noise excess factor  $\gamma_0$  for small amplitudes, which was obtained from the linear model.

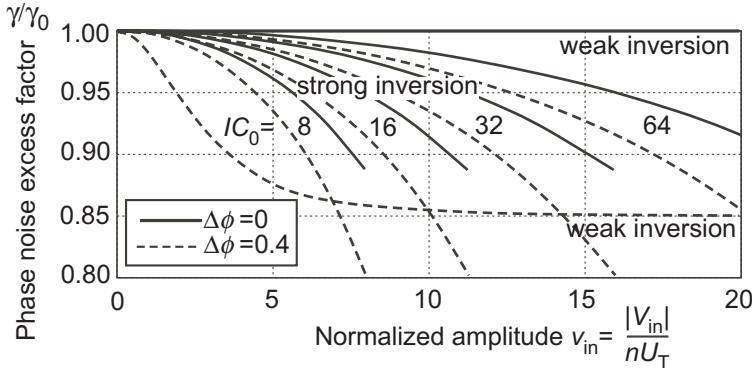
For larger amplitudes, according to (6.61), the noise excess factor is

$$\gamma = \gamma_0 \cdot \frac{v_{in}}{f_w(v_{in})} \cdot \overline{I_i^2}. \quad (6.64)$$

This result is plotted in Fig. 6.8 for  $\Delta\phi = 0$  and  $\Delta\phi = 0.4$ .

As can be seen, in weak inversion  $\gamma$  remains constant with the amplitude if  $\Delta\phi = 0$ . If  $\Delta\phi \neq 0$ , it decreases when the amplitude increases, but only slightly even for a large phase shift  $\Delta\phi = 0.4$ .

In *strict strong inversion* the two drain currents are given by (6.34). The transconductance variations can thus be obtained by introducing these currents in (3.56), which gives



**Figure 6.8** Variation of the noise excess factor with the drain-to-drain amplitude. The results for strong inversion are based on the approximation  $IC = IC_0$ .

$$G_{m1(2)} = \frac{\sqrt{I_0 I_{spec}}}{n U_T} \sqrt{1 \mp m_{vd} \sin \phi \sqrt{2 - (m_{vd} \sin \phi)^2}}. \quad (6.65)$$

Thus, from (6.56):

$$\alpha_i^2 S_{I_n^2} = 2n\gamma_t kT \cdot \frac{\sqrt{I_0 I_{spec}}}{n U_T} \cdot \alpha_i^2, \quad (6.66)$$

with

$$\alpha_i^2 = \frac{2}{\frac{1}{\sqrt{1+m_{vd} \sin \phi \sqrt{2-(m_{vd} \sin \phi)^2}}} + \frac{1}{\sqrt{1-m_{vd} \sin \phi \sqrt{2-(m_{vd} \sin \phi)^2}}}}. \quad (6.67)$$

We do not have a closed form expression for the variation of  $I_0$  with the amplitude of oscillation. Indeed, both  $m_{vd}$  and  $IC$  depend on  $I_0$  in (6.39). We shall neglect these dependencies, and approximate  $IC$  by  $IC_0$ .

By using (6.39) to replace  $I_0$  by  $I_{0crit}$  and (3.56) to express  $G_{mcrit}$  from  $I_{0crit}$ , (6.66) becomes

$$\alpha_i^2 S_{I_n^2} = \underbrace{2nkT \gamma_t G_{mcrit}}_{S_{I_n^2}} \sqrt{\frac{\sqrt{2}m_{vd}}{f_s(m_{vd})}} \alpha_i^2, \quad (6.68)$$

According to (3.34), the squared RMS value of the effective impulse sensitivity function (ISF) is

$$\overline{I_i^2} = \frac{1}{2\pi} \int_0^{2\pi} \cos^2(\phi + \Delta\phi) \alpha_i^2 d\phi, \quad (6.69)$$

where  $\Delta\phi$  is the phase shift between gate voltage and drain current approximated by (6.52).

For small amplitudes,  $S_{I_n^2} = S_{I_{n0}^2}$ ,  $\alpha_i^2 = 1$  and therefore  $\overline{I_i^2} = 0.5$ . Introducing these values in (3.33) gives, as could be expected, the phase noise spectrum  $S_{\phi_n^2 0}$  obtained for weak inversion and by given (6.63), and the noise excess factor  $\gamma_0$  given by (6.55).

For large amplitudes:

$$\gamma = \gamma_0 \cdot 2 \sqrt{\frac{\sqrt{2}m_{vd}}{f_s(m_{vd})} \cdot \overline{I_i^2}}. \quad (6.70)$$

This variation of  $\gamma$  is also plotted in Fig. 6.8 for various values of  $IC_0$ , using the definition (6.35) of  $m_{vd}$  (with the approximation  $IC = IC_0$ ).

These results do not include the additional noise due to the biasing circuitry and to losses. But they already include in  $\gamma_0$  the increase of transconductance  $G_{mcrit}/G_{mcrit0}$  due to losses.

#### 6.2.6.4 Phase Noise Due to 1/f Flicker Noise

According to the simple model introduced in Section (3.8), the flicker noise of each of the two transistors can be modelled by a noise voltage  $V_{nG}$ , with a spectral density given by (3.62).

The expression (6.45) of the noise current flowing through  $C_D$  shows that the function weighting the noise voltages  $V_{nG1}$  and  $V_{nG2}$  is symmetrical with respect to  $G_{m1}$  and  $G_{m2}$ . For this reason the mean value of the ISF given by (3.34) is zero. Hence, no 1/f noise is transferred around the oscillation frequency if the noise source is a bias independent noise voltage at the gates (which corresponds to a drain current noise spectral density proportional to the square of the transconductance).

But this model is an approximation. Let us introduce a more general model by defining a drain current noise spectral density

$$S_{I_{nd}^2 1/f} = \frac{F_a}{\omega_n} \left( \frac{G_m}{G_a} \right)^a, \quad (6.71)$$

where  $G_a$  is the value of  $G_m$  for which the spectrum density has the value  $F_a/\omega_n$ . Considering the noise of transistor  $T_1$  only, the resulting cyclostationary noise spectrum is then, from (6.50):

$$\alpha^2 S_{I_n^2} = \left( \frac{G_{m2}}{G_{m1} + G_{m2}} \right)^2 \frac{F_a}{\omega_n} \left( \frac{G_{m1}}{G_a} \right)^a. \quad (6.72)$$

In *weak inversion*, the transconductance is given by (6.58) or, by using (6.33) to replace  $I_0$  by its critical value  $I_{0critmin} = nU_T G_{mcrit}$ :

$$G_{m1} = \frac{2G_{mcrit}}{1 + e^{v_{in}\sin\phi}} \cdot \frac{v_{in}}{2f_w(v_{in})} \quad \text{and} \quad G_{m2} = \frac{2G_{mcrit}}{1 + e^{-v_{in}\sin\phi}} \cdot \frac{v_{in}}{2f_w(v_{in})}. \quad (6.73)$$

Introducing these expressions in (6.72) yields

$$\alpha^2 S_{I_n^2} = \underbrace{\frac{F_a}{\omega_n} \left( \frac{2G_{mcrit}}{G_a} \right)^a \left( \frac{v_{in}}{2f_w(v_{in})} \right)^a}_{K_{fi}/\omega_n} \underbrace{\frac{(1 + e^{v_{in}\sin\phi})^{2-a}}{(2 + e^{v_{in}\sin\phi} + e^{-v_{in}\sin\phi})^2}}_{\alpha_i^2}, \quad (6.74)$$

where  $K_{fi}/\omega_n$  is the power spectrum of a fictitious source of stationary flicker noise current.

The average value of the effective ISF is thus

$$\bar{\Gamma}_i = \overline{\alpha_i \cos(\phi + \Delta\phi)} = \frac{1}{2\pi} \int_0^{2\pi} \frac{(1 + e^{v_{in}\sin\phi})^{1-a/2} \cos(\phi + \Delta\phi)}{2 + e^{v_{in}\sin\phi} + e^{-v_{in}\sin\phi}} d\phi. \quad (6.75)$$

which is equal to zero for  $\Delta\phi = 0$ . Using the decomposition  $\cos(\phi + \Delta\phi) = \cos\phi \cos\Delta\phi - \sin\phi \sin\Delta\phi$ , the dependency on  $\Delta\phi$  can be made more explicit:

$$\bar{\Gamma}_i = \frac{-\sin\Delta\phi}{2\pi} \int_0^{2\pi} \frac{(1 + e^{v_{in}\sin\phi})^{1-a/2} \sin\phi}{2 + e^{v_{in}\sin\phi} + e^{-v_{in}\sin\phi}} d\phi. \quad (6.76)$$

For a very small amplitude  $v_{in} \ll 1$ , this ISF becomes

$$\bar{\Gamma}_{i0} = -\frac{1-a/2}{2^{3+a/2}} v_{in} \sin\Delta\phi. \quad (6.77)$$

Furthermore, for very small amplitudes  $2f_w(v_{in}) = v_{in}$ , thus from (6.74):

$$K_{fi0} = F_a \left( \frac{2G_{mcrit}}{G_a} \right)^a. \quad (6.78)$$

The phase noise spectrum for very small amplitude is then obtained by introducing (6.77) and (6.78) in (3.36) with  $C_i = C_D$  and  $V_i = V_{in}$ , which gives

$$S_{\phi_n^2 0} = 2 \left( \frac{(1-a/2)C_m \sin\Delta\phi}{8nU_T C_D^2} \right)^2 \frac{(G_{mcrit}/G_a)^a F_a}{\Delta\omega^3}, \quad (6.79)$$

where a factor 2 has been introduced to include the noise of the second transistor  $T_2$ . This result can be further simplified by using the expression (6.10) of the lossless critical transconductance  $G_{mcrit0} = I_{0crit0}/(nU_T)$ , which yields:

$$S_{\phi_n^2 0} = \left( \frac{(1 - a/2)\omega \sin \Delta\phi}{QI_{0critmin0}} \right)^2 \frac{(G_{mcrit}/G_a)^a F_a}{8\Delta\omega^3}, \quad (6.80)$$

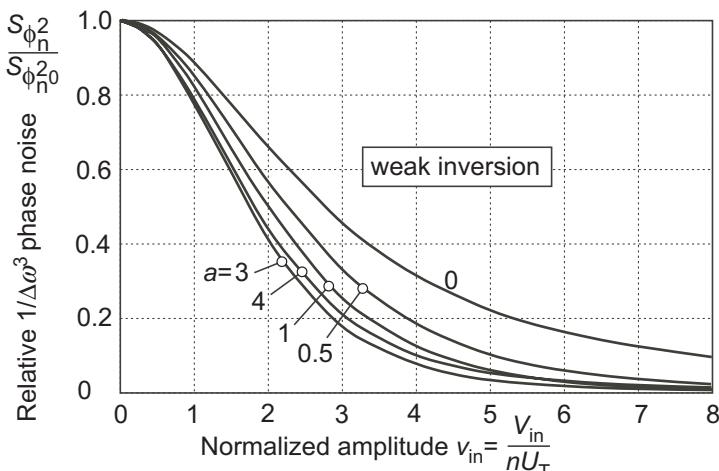
where  $I_{0critmin0}$  is the critical bias current for the lossless circuit. Notice that if the flicker noise of the transistor is characterized at the critical transconductance, then  $G_a = G_{mcrit}$  and the expression is further simplified.

As could be expected, the phase noise cancels for  $a = 2$ , which corresponds to the model (3.62) that assumes a bias-independent noise voltage at the gate. This situation is approached when the transistors operate at the upper limit of weak inversion [18].

For large amplitudes,  $K_{fi0}$  is multiplied by  $[v_{in}/(2f_w)]^a$  according to (6.74) and  $\bar{I}_{i0}$  is replaced by  $\bar{I}_i$  given by (6.76). Thus:

$$S_{\phi_n^2} = S_{\phi_n^2 0} \left( \frac{\bar{I}_i}{\bar{I}_{i0}} \right)^2 \left( \frac{v_{in}}{2f_w(v_{in})} \right)^a. \quad (6.81)$$

This variation is represented in Fig. 6.9 for several values of  $a$ .

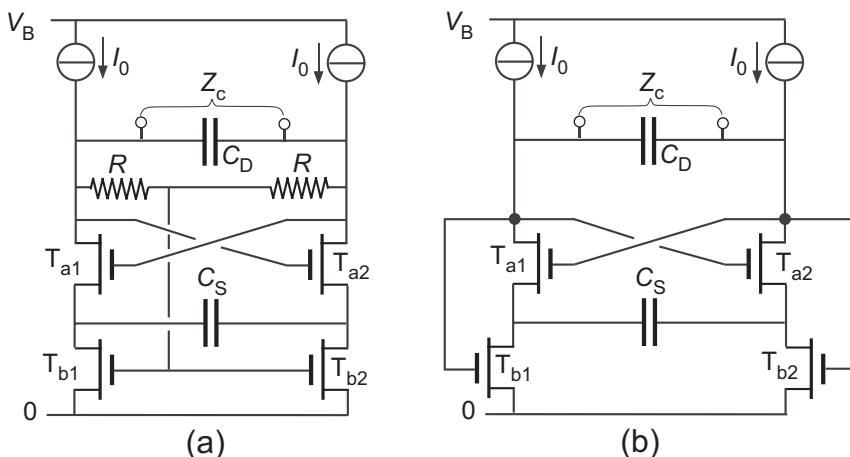


**Figure 6.9** Variation of the  $1/\Delta\omega^3$  noise due to flicker noise with the amplitude (transistors in weak inversion). The noise spectrum for very small amplitudes  $S_{\phi_n^2 0}$  is given by (6.80). The parameter  $a$  defined in (6.71) represents the dependency of the drain current flicker noise on the transconductance.

Now, it should be remembered that these results for flicker noise are based on the expression (6.50) of the cyclostationary noise, in which the imaginary part of the full expression (6.45) has been neglected. For frequencies  $\omega_n$  that are too small to fulfill condition (6.49), the noise is reduced, thus the phase noise spectrum stops increasing with  $1/\Delta\omega^3$ .

### 6.2.7 Practical Implementations

To avoid the need to increase the supply voltage in order to reduce the losses, the parallel resonance oscillator can be biased as illustrated in Fig. 6.10(a). The biasing resistors are replaced by current sources  $I_0$  and the common-



**Figure 6.10** Practical biasing of the parallel resonance oscillator.

mode drain voltage of the active transistors  $T_a$  is controlled by a feedback loop through the biasing transistors  $T_b$ . The role of the resistors is to extract this common-mode voltage, hence their value can be very large without increasing the minimum supply voltage. At the DC bias point, the two transistors  $T_a$  and  $T_b$  in series are equivalent (by symmetry) to a single transistor having its gate connected to its drain. Hence, the common mode voltage is the gate voltage corresponding to a drain current equal to  $I_0$ .

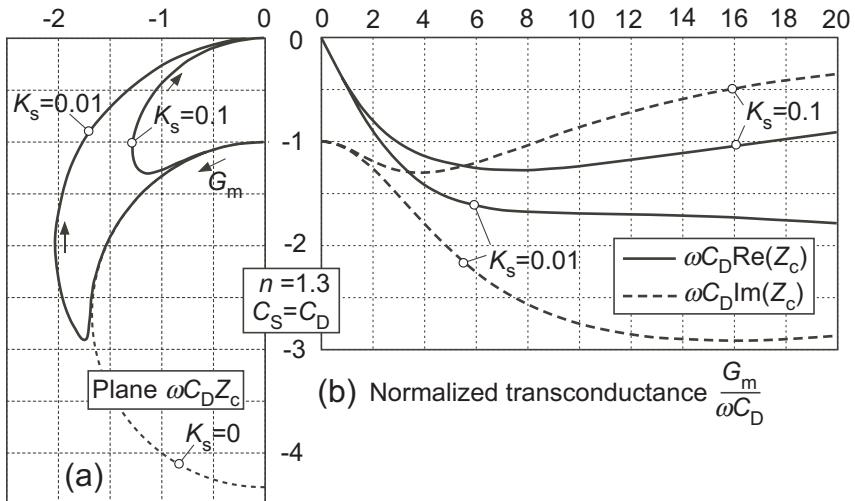
Now, transistors  $T_b$  are not saturated since they have the same gate voltage as  $T_a$ . According to (3.50) and (3.40), their drain (trans)conductance is proportional to the source transconductance of the active transistors:

$$G_{mdb} = K_s \cdot G_{msa} \quad \text{with} \quad K_s \triangleq \frac{I_{specb}}{I_{speca}}, \quad (6.82)$$

since the drain voltage of  $T_b$  is the source voltage of  $T_a$ . This drain conductance corresponds to a loss conductance  $G_S = G_{mdb}/2$  in parallel with  $C_S$ . But this loss conductance is now proportional to the transconductance  $G_m = G_{msa}/n$  of the active transistors, with the consequence that the locus of  $Z_c(G_m)$  is no longer a circle. This locus can be computed by introducing

$$1/Z_S = j\omega C_S + K_s n G_m / 2 \quad (6.83)$$

in the expression (6.11) of the circuit impedance. The result is illustrated in Fig. 6.11 for two values of the ratio  $K_s$  of specific currents. As can be seen,



**Figure 6.11** Normalized locus of circuit impedance  $Z_c(G_m)$  for the oscillator of Fig. 6.10(a), with negligible losses due to resistors  $R$ . The locus for the lossless circuit is shown in dotted line.

the losses due the biasing transistors  $T_b$  are negligible for small values of the transconductance  $G_m$ , but the loci depart from the lossless case when  $G_m$  increases. For this particular (but typical) case with  $n = 1.3$  and  $C_S = C_D$ , the maximum value of negative resistance is not reduced for  $K_s = 0.01$ , but it is reduced by about 50% for  $K_s = 0.1$ .

Now, for the calculation of the loci shown in Fig. 6.11 the value of resistor  $R$  was assumed to be very large. But to maintain a stable bias point this value has an upper limit. Indeed, because of the DC path provided by transistors

$T_b$ , the circuit can become bistable. The active transistor  $T_a$  has its source degenerated by the drain (trans)conductance of  $T_b$  given by (6.82), hence its equivalent gate transconductance at low frequencies is

$$G_{mequ} = \frac{G_{msa}G_{mdb}}{n(G_{msa} + G_{mdb})} = \frac{G_m}{1 + 1/K_s}. \quad (6.84)$$

Bistability is avoided if the voltage gain  $G_{mequ}R$  of each branch is smaller than unity, which results in the following condition for stability of the bias point:

$$R < \frac{1 + 1/K_s}{G_{mmax}}, \quad (6.85)$$

where  $G_{mmax}$  is gate transconductance of  $T_a$  alone obtained at the maximum value of bias current  $I_0$ . Hence,  $K_s$  must be very small to limit the losses due to  $R$ , especially if  $I_0 \gg I_{0crit}$  at start-up.

To avoid using resistors, the gates of the biasing transistors  $T_b$  can be connected as shown in Fig. 6.10(b) [25]. The DC bias point remains the same, since by symmetry the two drains are at the same (common mode) potential. But the transistors  $T_b$  are now active, with a gate transconductance  $G_{mb}$ . The circuit impedance *without* the parallel capacitance  $C_D$  becomes

$$Z_{c0} = \frac{1 + K_s + \frac{2}{nG_m Z_S}}{\frac{G_{mb}}{2} - \frac{1}{nZ_S} - \frac{K_s G_m}{2}}. \quad (6.86)$$

Now, the relationship between  $G_{mb}$  and the gate transconductance  $G_m$  of the main active transistors depends on their mode of operation. Knowing that  $T_a$  and  $T_b$  have the same gate voltage with  $T_a$  saturated, their components of drain current can be expressed as

$$I_{Rb} = K_s I_{Fa} = K_s I_0 \quad \text{and} \quad I_{Fb} = I_0 + I_{Rb} = (1 + K_s) I_0. \quad (6.87)$$

If both transistors are in strong inversion, the corresponding values of gate transconductance are obtained from (3.53) and (3.51):

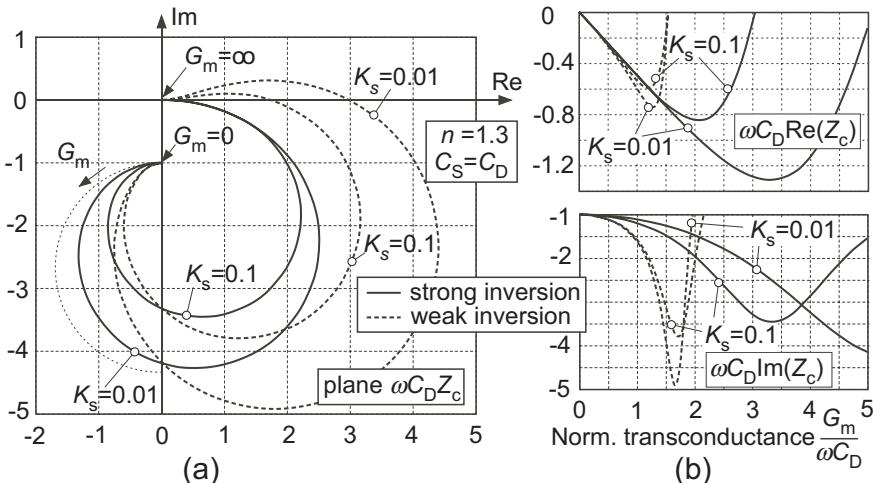
$$G_m = \frac{\sqrt{I_0 I_{speca}}}{nU_T} \quad \text{and} \quad G_{mb} = \frac{\sqrt{I_0 I_{specb}} (\sqrt{1 + K_s} - \sqrt{K_s})}{nU_T}, \quad (6.88)$$

and their ratio is

$$\frac{G_{mb}}{G_m} = \sqrt{K_s(1 + K_s)} - K_s \quad (\text{in strong inversion}). \quad (6.89)$$

This ratio tends to  $\sqrt{K_s}$  for  $K_s \ll 1$  and never exceeds 0.5.

The introduction of (6.89) in (6.86) gives  $Z_{c0}(G_m)$ , which can be combined with  $Z_D$  according to (6.11) to obtain the full circuit impedance  $Z_c(G_m)$ . The analytical result is too complicated to be expressed, but the numerical calculation can be carried out step by step. The result for the lossless case ( $G_D = G_S = 0$ ) is plotted in full lines in Fig. 6.12(a) for two values of the ratio  $K_s$  of specific currents.



**Figure 6.12** (a) Normalized locus of circuit impedance  $Z_c(G_m \geq 0)$  for the oscillator of Fig. 6.10(b); full lines: for all transistors always in strong inversion; dotted lines: for all transistors always in weak inversion. The circular lossless locus for the basic circuit of Fig. 6.1(b) is shown in fine dotted line for comparison. (b) Variation of the real and imaginary parts with the normalized transconductance.

Compared to the circular locus of the basic circuit (shown in fine dotted line), the maximum negative resistance is reduced by the activity of the biasing transistors.

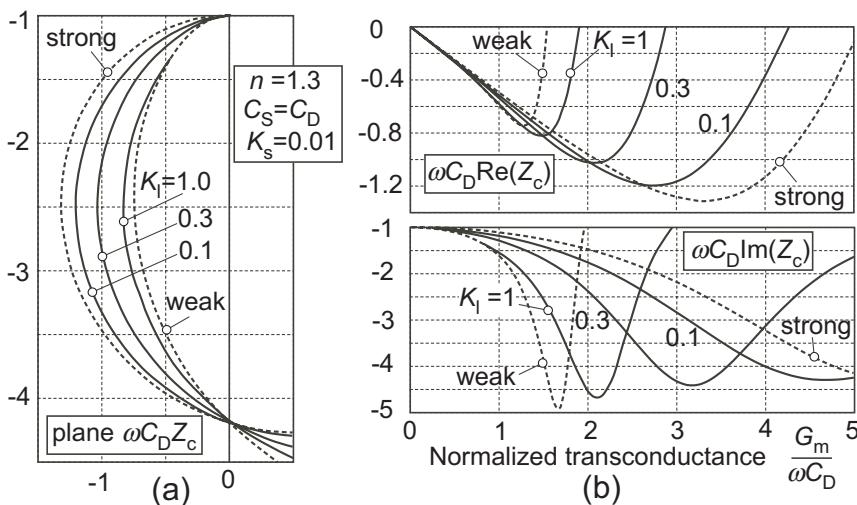
If the transistors are in weak inversion, the gate transconductance only depends on the total drain current that is the same for the two transistors, hence  $G_{mb} \equiv G_m$ . The degradation is increased due to the larger  $G_{mb}$ , as shown by the corresponding results in dotted lines. However, as can be seen in part (b) of the figure, as long as the negative resistance  $R_n = -\text{Re}(Z_c)$  is much smaller than its maximum value, it always depends linearly on the transconductance with

$$R_n = -\frac{G_m}{2(\omega C_D)^2}, \quad (6.90)$$

thereby resulting in the critical condition for oscillation  $G_{mcrit}$  for the lossless circuit given by (6.10).

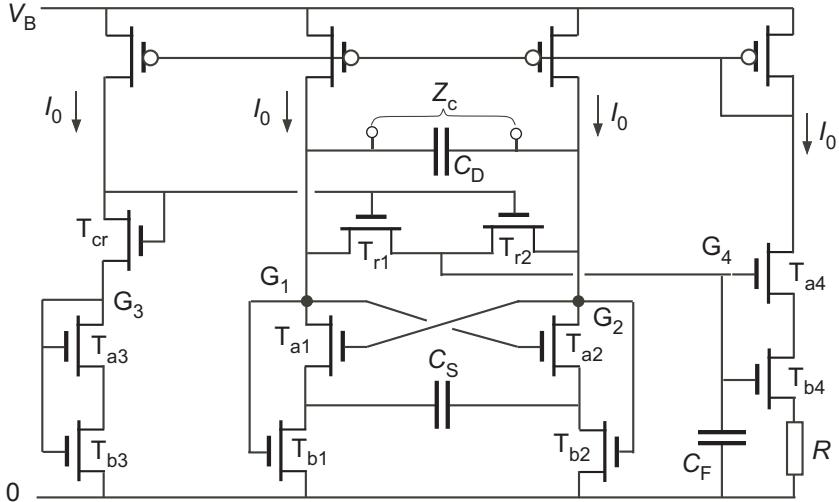
Furthermore, for  $|R_n| \ll |R_n|_{max}$ , the imaginary part remains close to -1, thus the expression (6.17) of the frequency pulling is not affected.

Now, the plots of Fig. 6.12 have been obtained by assuming the all transistors are always in weak or in strong inversion. In reality, all transistors are in weak inversion at very low currents (i.e. for very low values of the transconductance), and all transistors are in strong inversion for very high currents. The transition occurs at a level of current that depends on the specific currents  $I_{speca}$  and  $I_{specb}$ , according to the general equation (3.50) for the transconductance. No analytical expression of  $Z_c(G_m)$  can be found in the general case.



**Figure 6.13** (a) Normalized locus of circuit impedance  $Z_c(G_m \geq 0)$  for the oscillator of Fig. 6.10(b) with transistors  $T_a$  in weak inversion and  $T_b$  in strong inversion characterized by parameter  $K_l$  (defined by (6.92)). Curves in dotted lines are for the asymptotic cases of all transistor in weak and in strong inversion. (b) Variation of the real and imaginary parts with the normalized transconductance.

To minimize the value of the critical bias current  $I_{0crit}$ , the active transistors  $T_a$  must be operated in weak inversion, whereas the biasing transistors  $T_b$  should be in strong inversion to reduce their transconductance. Their transconductance given by (6.88) can then be expressed as a function of the main transconductance  $G_m = I_0/(nU_T)$ :



**Figure 6.14** Parallel resonance oscillator with amplitude regulation.

$$\frac{G_{mb}}{\omega C_D} = \sqrt{K_l} \cdot \sqrt{\frac{G_m}{\omega C_D}} (\sqrt{1+K_s} - \sqrt{K_s}), \quad (6.91)$$

where  $K_l$  is a parameter defined by

$$K_l \triangleq \frac{I_{specb}}{\omega C_D n U_T} \quad (6.92)$$

that characterizes the level of the specific current.

This new expression of  $G_{mb}$  can again be combined with (6.86) and (6.11) to obtain  $Z_c(G_m)$ . An example with  $K_s = 0.01$  and several values of  $K_l$  is illustrated in Fig. 6.13. The results are between the extreme cases of weak and strong inversion for both transistors.

The amplitude of oscillation can be regulated by delivering the bias current from the regulator discussed in Section (5.2). A more compact solution is depicted in Fig. 6.14 [25].

Two pairs of transistors matched to the main pairs  $T_a - T_b$  have been added. The same current  $I_0$  flows through all four branches. The common mode voltage of the main pairs is extracted by transistors  $T_{r1}$  and  $T_{r2}$  matched to their biasing transistor  $T_{cr}$ .

The pair  $T_{a3} - T_{b3}$  is identical to the main pair. Hence, in absence of oscillation, all four gates nodes  $G_1$  to  $G_4$  are at the same potential. But the specific currents of the transistors of the fourth pair are  $K_w$  times larger than

those of the main pair, which must be compensated by a voltage drop  $RI_0$  across resistor  $R$ .

If all pairs are in *weak inversion*, a stable solution without oscillation is reached as in the regulator of Section (5.2) for

$$I_0 = I_{0start} = \frac{U_T}{R} \ln K_w. \quad (6.93)$$

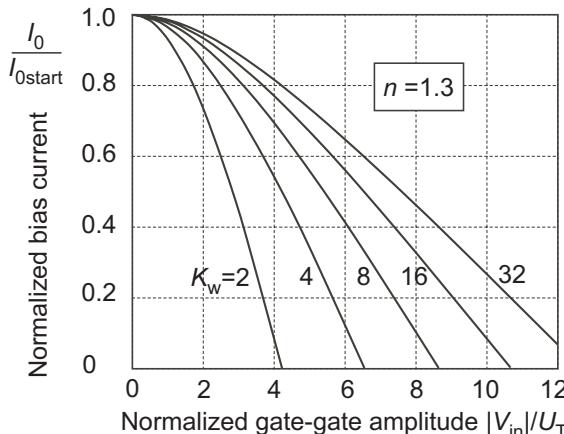
If this current is larger than the critical current, the oscillation starts growing, but unlike for the single transistor of the Pierce oscillator, the common mode voltage remains essentially constant at constant  $I_0$ . Hence no amplitude regulation would occur if the common mode would be extracted by linear resistors instead of transistors. But the nonlinearity of the transistor produces a voltage drop at the node  $G_4$  given by (5.41) with  $|V_2| = 0$  and  $|V_1|$  replaced by  $|V_{in}|/2$ :

$$\Delta V_{G0} = -U_T \ln [I_{B0}(|V_{in}|/2U_T)]. \quad (6.94)$$

The transfer function of the regulator is then obtained by adding  $\Delta V_{G0}/n$  to  $U_T \ln K_w$  in the expression (6.93) of the current, which yields:

$$\frac{I_0}{I_{0start}} = 1 - \frac{\ln [I_{B0}(|V_{in}|/2U_T)]}{n \ln K_w}, \quad (6.95)$$

where  $|V_{in}|$  is the gate to gate amplitude of oscillation. This function is plotted in Fig. 6.15 for several values of ratio  $K_w$ .



**Figure 6.15** Regulation curves for the circuit of Fig. 6.14 with all transistors operated in weak inversion. The small drain voltage shift due to the distortion of drain current is neglected.

The loss conductance due to transistors  $T_r$  (for the fundamental frequency) can be obtained as discussed in Section 5.1.5, with  $V_{in}/2$  across each transistor:

$$G_1 \equiv G_{(1)} = G_0 \frac{2I_{B1}(|V_{in}|/2U_T)}{|V_{in}|/2U_T}. \quad (6.96)$$

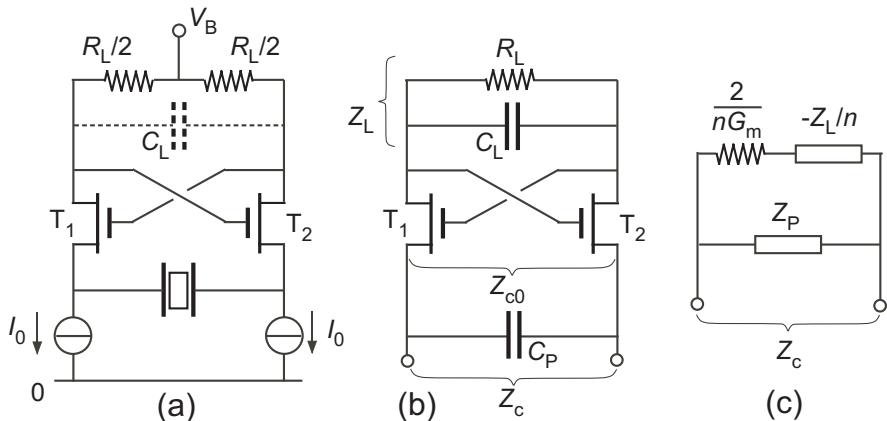
With the specific current of the biasing transistor  $T_{cr}$   $K_r$ -times larger than that of one of the transistors  $T_r$ , the small-signal value  $G_0$  of this loss conductance is now

$$G_0 = \frac{I_0}{2K_r U_T}. \quad (6.97)$$

## 6.3 Symmetrical Oscillator for Series Resonance

### 6.3.1 Basic Structure

The basic symmetrical oscillator circuit intended for series resonators is shown in Fig. 6.16(a). It is based on a *current stable* negative resistance circuit developed for vacuum tubes (Fig. 69e, page 82 of [15]). A version with bipolar transistors was used in early developments of electronic watches [26]. Each of the two cross-coupled transistors is biased by a cur-



**Figure 6.16** Symmetrical oscillator for series resonator; (a) complete oscillator; (b) negative resistance circuit without bias sources; (c) small-signal general equivalent circuit.

rent source  $I_0$  and is loaded by a resistor of value  $R_L/2$ . As long as the circuit remains symmetrical, the effect of all capacitors at the drains can be represented by a single load capacitance  $C_L$  between the two drains. The resonator connects the sources of the two transistors. The transistors are assumed to be in the same local substrate.

### 6.3.2 Linear Analysis

#### 6.3.2.1 Circuit Impedance in the General Case

To calculate the small-signal circuit impedance  $Z_c$ , the circuit may be represented as in Fig. 6.16(b), after removing the biasing elements. Capacitance  $C_P$  is the capacitance  $C_0$  of the quartz resonator considered as a dipole defined by (2.1), augmented by the parasitic capacitors in the circuit.

At frequencies for which the capacitors can be neglected, the circuit impedance is easily calculated to be

$$Z_c|_{\omega=0} = \frac{2 - G_m R_L}{G_{ms}} = \frac{1}{n}(2/G_m - R_L), \quad (6.98)$$

where  $G_{ms}$  is the source transconductance, which is  $n$  times larger than the gate transconductance  $G_m$ , according to (3.55). Hence, unlike the Pierce oscillator, this circuit provides a DC negative resistance. It becomes DC unstable, that is bi-stable, when it is connected to a resistor of value smaller than this negative resistance.

But it can also become AC unstable, i.e. an oscillator, when it is connected to the sole capacitance  $C_P$ . The AC circuit impedance  $Z_{c0}$  without  $C_P$  is given by

$$Z_{c0} = \frac{2 - G_m Z_L}{G_{ms}} = \frac{1}{n}(2/G_m - Z_L), \quad (6.99)$$

where the load impedance  $Z_L$  including  $C_L$  can be expressed as

$$Z_L = \frac{R_L - j\omega C_L R_L^2}{1 + (\omega C_L R_L)^2}. \quad (6.100)$$

Thus

$$Z_{c0} = \frac{2}{nG_m} - \frac{R_L/n}{1 + (\omega C_L R_L)^2} + j \frac{\omega C_L R_L^2/n}{1 + (\omega C_L R_L)^2}. \quad (6.101)$$

When  $C_P$  is connected, an oscillation can occur at the frequency for which  $\text{Im}(Z_{c0}) = 1/(\omega C_P)$ , that is for

$$\omega^2 = \frac{1}{C_L R_L^2 (C_P/n - C_L)}. \quad (6.102)$$

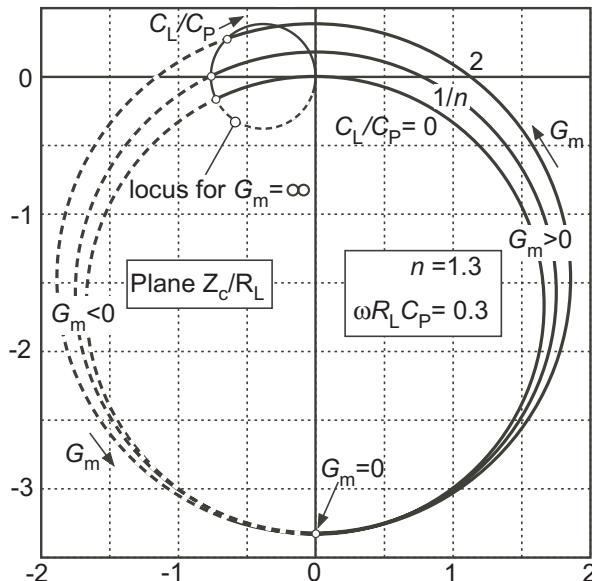
this frequency does not exist if

$$C_L > C_P/n, \quad (6.103)$$

which is a *sufficient* condition to avoid this parasitic oscillation. But this condition is not absolutely necessary, since the real part of  $Z_{c0}$  in (6.101) must be negative at the frequency given by (6.102). This requirement gives the following *necessary* condition for no parasitic oscillation:

$$C_L > \frac{C_P}{n} \left( 1 - \frac{2}{R_L G_m} \right), \quad (6.104)$$

which is reduced to (6.103) for  $R_L G_m \gg 1$ .



**Figure 6.17** Loci of circuit impedance  $Z_c/R_L$  for  $\omega R_L C_P = 0.3$  and  $n = 1.3$ . Notice that  $C_L/C_P = 0$  will produce a parasitic oscillation whereas  $C_L/C_P = 1/n$  corresponds to the sufficient condition (6.103) for no parasitic oscillation.

Adding the impedance  $Z_P$  of the parallel capacitor  $C_P$  (with possible losses) in parallel with  $Z_{c0}$  gives the overall circuit impedance

$$Z_c = \frac{Z_P(2 - G_m Z_L)}{2 + G_m(n Z_P - Z_L)}, \quad (6.105)$$

which corresponds to the equivalent circuit of Fig. 6.16(c). It is a bilinear function of the transconductance  $G_m$ . The corresponding circle in the complex plane is plotted in Fig. 6.17 for particular values of  $\omega R_L C_P$  and slope factor  $n$ , and for various values of the capacitance ratio  $C_L/C_P$ .

### 6.3.2.2 Particular Case with $C_L = C_P/n$

The analytic expressions of the real and imaginary parts of  $Z_c$  are complicated, but they can be simplified for the particular (and realistic) case for which the sufficient condition (6.103) is just fulfilled, i.e. for  $C_L = C_P/n$ . *All the following derivations will be made with this assumption.*

The results are then

$$\operatorname{Re}(Z_c) = \frac{1}{\omega C_P} \cdot \frac{AB(2B + 2/B - A)}{4 + (2B - A)^2} \quad (6.106)$$

$$\operatorname{Im}(Z_c) = \frac{1}{\omega C_P} \cdot \frac{4(AB - B^2 - 1)}{4 + (2B - A)^2}, \quad (6.107)$$

where

$$A \triangleq \frac{G_m}{\omega C_L} = \frac{nG_m}{\omega C_P} \quad \text{and} \quad B \triangleq \omega C_L R_L = \omega C_P R_L / n. \quad (6.108)$$

The locus of the normalized circuit impedance for positive values of transconductance  $G_m$  is plotted in Fig. 6.18 for various values of  $B$  (thus of  $R_L$  for  $\omega C_P/n$  constant). This locus is a circle of radius  $(1 + B^2)/2$  that is always centered on the imaginary axis.

For  $G_m = 0$  the transistors are not active and the impedance is that of the parallel capacitance  $C_P$ .

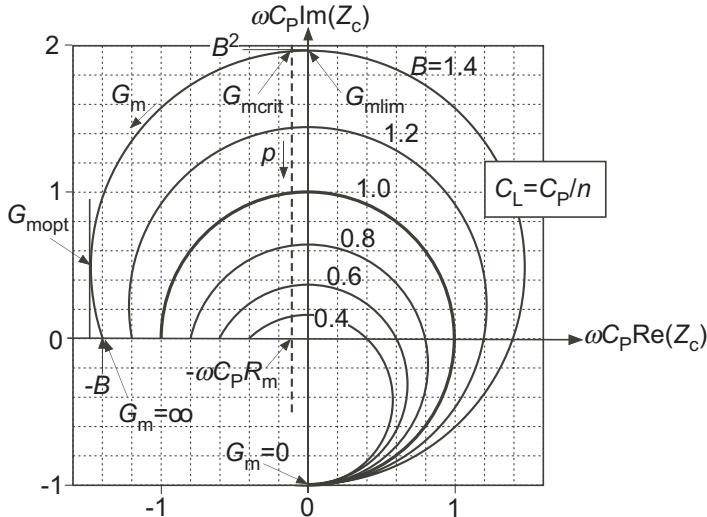
The value of transconductance needed to obtain a negative resistance is obtained from (6.106):

$$G_m > G_{mlim} = \frac{2(1 + B^2)}{R_L} = \frac{2\omega C_P}{n} (B + 1/B). \quad (6.109)$$

The imaginary part of  $Z_c$  at the limit of negative resistance (for  $\operatorname{Re}(Z_c) = 0$ ) is

$$\operatorname{Im}(Z_c)_{lim} = \operatorname{Im}(Z_c)|_{\operatorname{Re}(Z_c)=0} = \frac{B^2}{\omega C_P} = BR_L/n. \quad (6.110)$$

Eliminating  $B$  between these two equations gives



**Figure 6.18** Locus of the normalized circuit impedance  $\omega C_P Z_c$  for several values of  $B = \omega C_P R_L / n$ . The locus of  $-Z_m(p)$  for a particular value of motional resistance  $R_m$  is represented in dotted line.

$$G_{mlim} = \frac{2\omega C_P}{n} \left( \sqrt{\omega C_P \text{Im}(Z_c)_{lim}} + \frac{1}{\sqrt{\omega C_P \text{Im}(Z_c)_{lim}}} \right). \quad (6.111)$$

If the maximum value of negative resistance  $(-R_n)_{max}$  is much larger than the motional resistance  $R_m$  of the resonator (as depicted in dotted line in Fig. 6.18), that is if

$$B \gg \omega C_P R_m = 1/M_D \quad (6.112)$$

(with  $M_D$  defined by (2.22)), then the imaginary part of  $Z_c$  can be approximated by (6.110). According to (4.3), the amount of frequency pulling at the critical condition for oscillation is then

$$p_c \cong -\frac{C_m}{2C_P} B^2. \quad (6.113)$$

The comparison with (4.21) shows that  $C_P/B^2$  plays the same role as  $C_s + C_3$  in the Pierce oscillator. But  $B$  depends on a resistance, which is usually much less precise and stable with the temperature than a capacitor in an integrated circuit. Another important difference is that  $p_c$  is now negative: the frequency of oscillation is *lower* than the mechanical resonant frequency of the resonator.

For  $G_m$  very large, (6.106) gives:

$$Z_c|_{G_m=\infty} = -\frac{B}{\omega C_P} = -R_L/n. \quad (6.114)$$

This is the maximum possible value of negative resistance that can be obtained for  $B \leq 1$ . But for  $B > 1$ , a larger negative resistance can be obtained, corresponding to the radius  $(1+B^2)/2$  of the circle, as can be observed in Fig. 6.18:

$$(-R_n)_{max} = \frac{1+B^2}{2\omega C_P} = \frac{B+1/B}{2n} R_L \quad (\text{for } B > 1) \quad (6.115)$$

for a value  $G_{mopt}$  of the transconductance given by

$$G_{mopt} = \frac{\omega C_P}{n} \cdot \frac{2(B^2 + 1)}{B - 1}. \quad (6.116)$$

For  $G_m > G_{mopt}$ , the slope of the locus becomes negative, and no stable solution exists, as was the case for solution B in Fig. 4.4. Therefore, the only useful range of transconductance for  $B > 1$  is between  $G_{mlim}$  given by (6.109) and  $G_{mopt}$ .

The critical transconductance for oscillation is the value of  $G_m$  for which  $\text{Re}(Z_c) = R_n = -R_m$ . It is obtained by solving (6.106) with respect to  $A = nG_m/(\omega C_P)$ . This gives:

$$G_{mcrit} = \frac{\omega C_P}{n} \cdot \frac{1 + B^2 - 2B\omega C_P R_m + \sqrt{(1+B^2)^2 - (2\omega C_P R_m)^2}}{B - \omega C_P R_m}. \quad (6.117)$$

This critical transconductance can also be expressed as

$$G_{mcrit} = G_{mlim} + \Delta G_m(R_m). \quad (6.118)$$

For  $R_m \ll (-R_n)_{max}$ ,  $\Delta G_m$  can be approximated linearly by

$$\Delta G_m \cong \frac{2\omega^2 C_P^2}{nB^2} R_m = \frac{2nR_m}{R_L^2} = \frac{\omega C_P}{n} \cdot \frac{1}{Q|p_c|}, \quad (6.119)$$

where  $|p_c|$  has been obtained from (6.113). The combination of (6.118), (6.109) and (6.119) gives an approximation of the critical transconductance

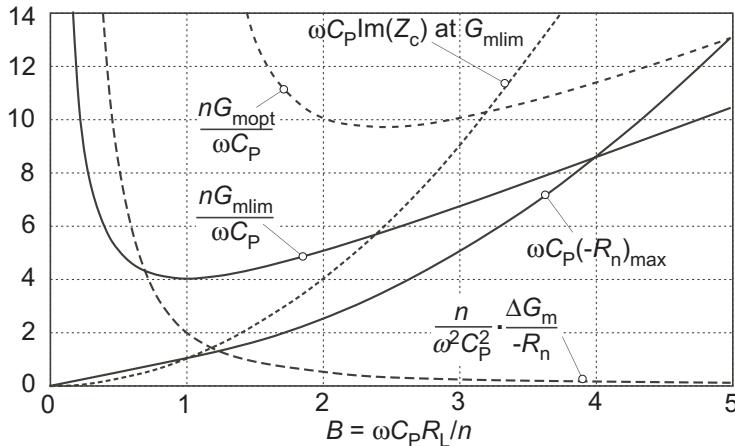
$$G_{mcrit} \cong \frac{2\omega C_P}{n} \left( B + \frac{1}{B} + \frac{1}{2Q|p_c|} \right). \quad (6.120)$$

It is worth noticing that, as long as  $Q|p_c|$  is sufficiently large, it has no effect on the critical transconductance:

$$G_{mcrit} = G_{mlim} = \frac{2\omega C_P}{n}(B + 1/B) \quad \text{for } 2Q|p_c| \gg \frac{B}{1+B^2}. \quad (6.121)$$

Unlike for the Pierce oscillator (see (4.26)), the critical transconductance is not reduced by a large value of quality factor  $Q$ . But it still depends on  $p_c$  through the design parameter  $B$  (i.e. through the choice of load resistance  $R_L$ ).

The dependency of the various important values discussed above on the parameter  $B$  is plotted in Fig. 6.19.



**Figure 6.19** Normalized values of  $G_{mlim}$ ,  $-R_n/\Delta G_m$ ,  $\text{Im}(Z_c)$  at  $G_{mlim}$  (thus for  $R_n = 0$ ),  $(-R_n)_{\max}$  and  $G_{mopt}$  as functions of parameter  $B$ .

For a fixed value of parallel capacitance  $C_P$ , the limit value  $G_{mlim}$  of the transconductance has a minimum for  $B = 1$ :

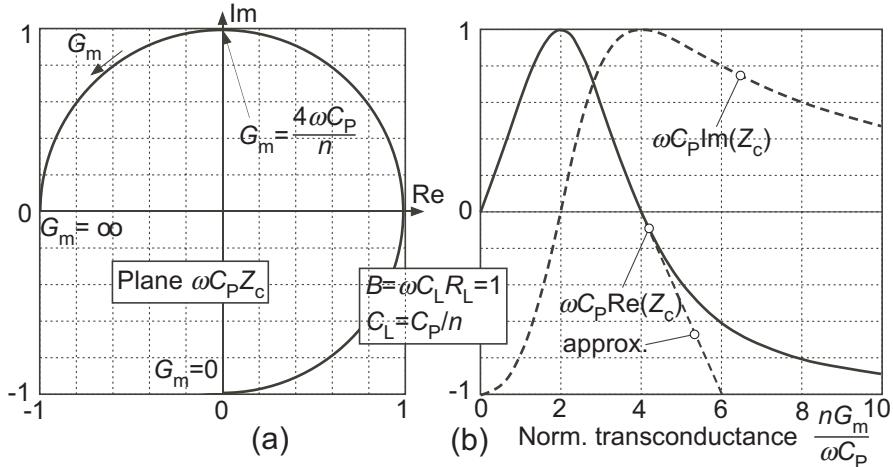
$$G_{mlim_{min}} = 4\omega C_P/n = 4/R_L \quad \text{for } B = 1. \quad (6.122)$$

For  $B > 1$  the imaginary part of  $Z_c$  increases dramatically, thereby increasing the amount of frequency pulling given by (6.113). The only reason to choose  $B > 1$  would thus be to produce a very large value of negative resistance, at the cost of an increase transconductance and an increase of  $p_c$ .

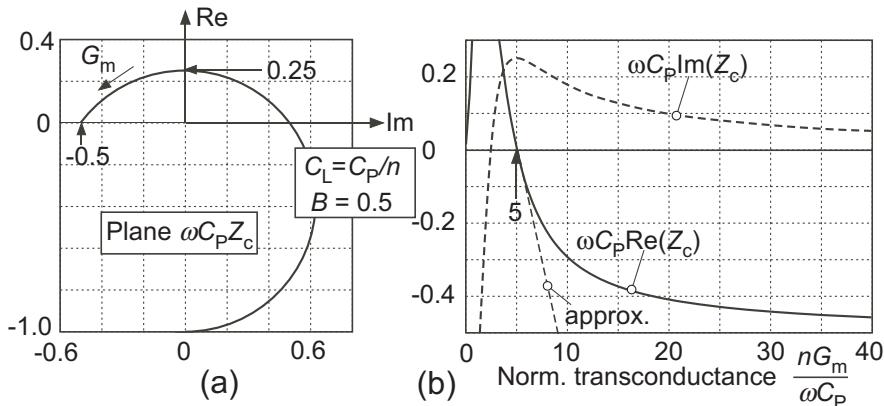
As already pointed out,  $B = 1$  corresponds to a minimum value of limit transconductance  $G_{mlim}$ . The corresponding locus of  $Z_c(G_m)$  is illustrated in Fig. 6.20(a) with the real and imaginary parts in Fig. 6.20(b).

The exact critical transconductance given by (6.117) becomes

$$G_{mcrit}|_{B=1} = \frac{2\omega C_P}{n} \left( 1 + \sqrt{\frac{1 + \omega C_P R_m}{1 - \omega C_P R_m}} \right), \quad (6.123)$$



**Figure 6.20** Normalized circuit impedance  $\omega C_P Z_c$  for  $C_L = C_P/n$  and minimum limit transconductance ( $B = 1$ ). The approximation (6.120) of  $G_{m\text{crit}}(R_n)$  is also shown in dotted line.



**Figure 6.21** Normalized circuit impedance  $\omega C_P Z_c$  for  $C_L = C_P/n$  and  $B = 0.5$ .

and the exact amount of frequency pulling obtained by introducing (6.107) in (4.3) with  $B = 1$  is

$$p_c|_{B=1} = -\frac{C_m}{2C_P} \sqrt{1 - (\omega C_P R_m)^2}. \quad (6.124)$$

For  $B < 1$ , The maximum negative resistance is decreased according to (6.114). The imaginary part of  $Z_c$  decreases rapidly with  $B$  (thereby decreasing the amount of frequency pulling  $p_c$ ), at the cost of an increase of the

necessary value of transconductance. But this increase can be small for a large reduction of  $|p_c|$ . For example, choosing  $B = 0.5$  results in just a 25% increase of  $G_{m\text{lim}}$  whereas  $p_c$  is decreased by a factor 4. This particular case is illustrated in Fig. 6.21.

### 6.3.2.3 Relative Oscillation Currents

At the critical condition for oscillation, the frequency pulling is approximately given by (6.113). Thus the motional impedance expressed by (2.8) becomes

$$Z_m|_{p=p_c} = R_m - j \frac{B^2}{\omega C_P} = R_m(1 - jM_D B^2), \quad (6.125)$$

where  $M_D$  is the factor of merit defined by (2.22).

The AC component of drain current  $I_1$  is split between the motional current  $I_m$  and the current  $I_P$  through the parallel capacitance  $C_P$  according to

$$\frac{I_P}{I_m} = j\omega C_P Z_m = B^2 + \frac{j}{M_D} \cong B^2, \quad (6.126)$$

and the AC component of drain current  $I_1$  is related the motional current  $I_m$  by

$$\frac{I_1}{I_m} = 1 + j\omega C_P Z_m = (1 + B^2) + \frac{j}{M_D} \cong (1 + B^2). \quad (6.127)$$

### 6.3.3 Nonlinear Analysis

As soon as the transconductance  $G_m$  exceeds the critical value given by (6.117) (or by its approximation (6.120)), the amplitude of oscillation grows. The drain current of each transistor can then be expressed as

$$I_D = I_0 + I_1, \quad (6.128)$$

where  $I_0$  is the DC component imposed by the biasing current source, and  $I_1$  is the AC oscillatory current.

According to (6.126), if  $B \ll 1$  and  $M_D \gg 1$  most of the AC current  $I_1$  flowing through the transistors is the motional current of the resonator. Hence  $I_1$  remains *approximately sinusoidal*. Therefore the gate voltage remains also sinusoidal, but the source voltage  $V_S$  is distorted by the nonlinear

transfer function of the transistors. The effective transconductance is reduced and more bias current  $I_0$  is needed to further increase  $I_1$ , until it reaches its maximum value equal to  $I_0$  (100% modulation of bias current  $I_0$ ).

The variation of the amplitude of oscillation with the bias current can be obtained by an approach similar to that used for the Pierce oscillator in Section 4.3.3. However, the source of the transistor is not grounded and the drain current is modulated by gate and source voltage variations. According to (3.40), the drain current in saturation depends on a control voltage

$$V_c \triangleq V_G - V_{T0} - nV_S \quad (6.129)$$

of normalized amplitude

$$\nu_c \triangleq \frac{|V_c|}{nU_T} \quad (6.130)$$

The corresponding transconductance is equal to the gate transconductance at the same value of current:

$$\frac{dI_D}{dV_c} = \frac{dI_D}{dV_G} = G_m \quad (6.131)$$

Let us assume that the AC component of drain current is *perfectly sinusoidal*, with

$$I_D = I_0(1 + m_i \sin \Phi), \quad (6.132)$$

where

$$m_i \triangleq |I_1|/I_0 \quad (6.133)$$

is the index of current modulation.

The value of  $G_m$  for the fundamental frequency can be expressed as

$$G_{m(1)} = \frac{|I_1|}{|V_{c(1)}|} = \frac{m_i I_0}{nU_T \nu_{c(1)}}, \quad (6.134)$$

where  $|V_{c(1)}|$  is the amplitude of the fundamental component of  $V_c$  and  $\nu_{c(1)}$  its value normalized to  $nU_T$ . Stable oscillation is obtained when  $G_{m(1)}$  equals the critical value of  $G_m$

$$G_{mcrit} = \frac{I_{0critmin}}{nU_T}, \quad (6.135)$$

where  $I_{0critmin}$  is the minimum possible value of  $I_0$  needed to produce  $G_{mcrit}$  (that is in weak inversion). Equating (6.134) with (6.135) yields

$$\frac{I_0}{I_{0critmin}} = \frac{\nu_{c(1)}}{m_i}. \quad (6.136)$$

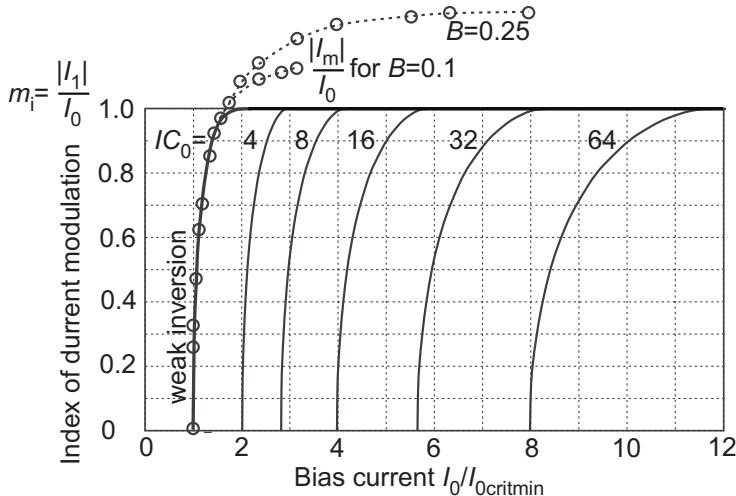
In *weak inversion*, the saturation drain current  $I_D = I_F$  given by (3.42) can be rewritten

$$I_D = I_{spec} \exp(v_c) \quad \text{or} \quad v_c = \ln \frac{I_D}{I_{spec}} = \ln \frac{I_0}{I_{spec}} + \ln(1 + m_i \sin \phi) \quad (6.137)$$

The fundamental component of  $v_c$  is thus given by

$$v_{c(1)} = \frac{1}{\pi} \int_0^{2\pi} \ln(1 + m_i \sin \Phi) \sin \Phi \cdot d\Phi. \quad (6.138)$$

Introducing this result in (6.136) yields the relation between the bias current  $I_0$  in weak inversion and the index of modulation  $m_i$ . It is plotted in Fig. 6.22.



**Figure 6.22** Index of current modulation as a function of the bias current. The parameter  $IC_0$  is the inversion coefficient at the critical bias current  $I_{0crit}$ . Circles are simulation results of  $|I_m|/I_0$  in weak inversion, showing that, except for  $B \ll 1$ , the distortion of the drain current cannot be neglected when saturation is approached.

In *strong inversion*, the saturation drain current  $I_D = I_F$  given by (3.43) can be written

$$I_D = I_{spec} \left( \frac{v_c}{2} \right)^2 \quad \text{or} \quad v_c = 2 \sqrt{\frac{I_D}{I_{spec}}}. \quad (6.139)$$

As for the Pierce circuit, the level of inversion can be characterized by the inversion coefficient at the critical current for oscillation:

$$IC_0 \triangleq \frac{I_{0crit}}{I_{spec}} \quad (6.140)$$

The fundamental component of  $v_c$  can then be expressed as

$$v_{c(1)} = \sqrt{\frac{I_0}{I_{0crit}}} IC_0 \cdot h_s(m_i), \quad (6.141)$$

with

$$h_s(m_i) = \frac{2}{\pi} \int_0^{2\pi} \sqrt{(1 + m_i \sin \Phi)} \cdot \sin \Phi \cdot d\Phi \quad (6.142)$$

According to (3.56), the critical current in strong inversion is related to its minimum value (reached in weak inversion) by

$$I_{0crit} = I_{0critmin} \sqrt{IC_0}, \quad (6.143)$$

therefore (6.141) becomes

$$v_{c(1)} = \sqrt{\frac{I_0}{I_{0critmin}}} \cdot \sqrt[4]{IC_0} \cdot h_s(m_i), \quad (6.144)$$

Introducing this result in (6.136) and solving for  $I_0/I_{0critmin}$  gives finally

$$\frac{I_0}{I_{0critmin}} = \sqrt{IC_0} \cdot \left( \frac{h_s(m_i)}{m_i} \right)^2, \quad (6.145)$$

which is plotted in Fig. 6.22 for several values of  $IC_0$ . As can be seen in this figure,  $|I_1|$  saturates to the value  $I_0$  for  $I_0 > \sqrt{2}I_{0crit}$  (slightly more in weak inversion). But a part of  $I_1$  flows through the load capacitor  $C_L$  and the voltage amplitude at the drain is limited to

$$|V_{D(1)}| = \frac{R_L I_0}{2\sqrt{1+B^2}}. \quad (6.146)$$

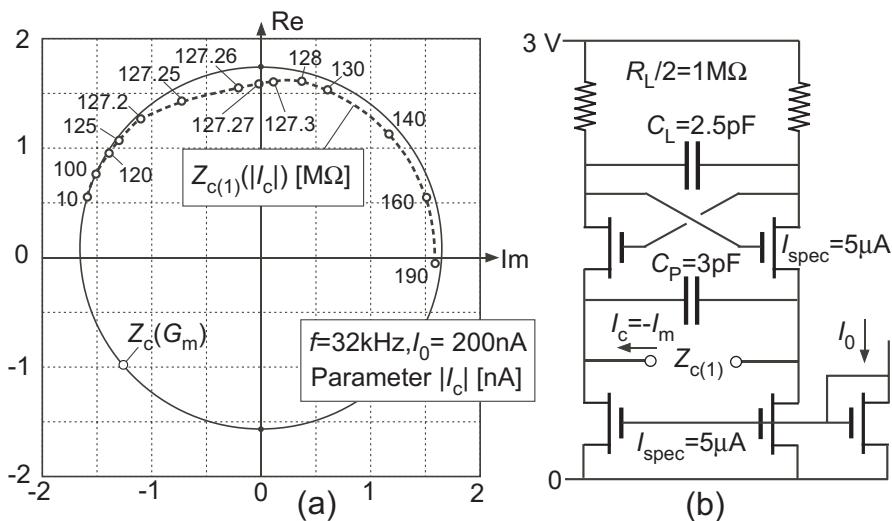
Similarly, a part of  $I_1$  is diverted from the resonator itself to flow through the parallel capacitor  $C_P$ , according to (6.127).

But it must be remembered that this calculation of the amplitude is only an *crude approximation*, since it is based on the assumption that the AC component  $I_1$  of drain current is perfectly sinusoidal. In reality, when the source voltage is distorted, harmonic components of current can flow through the parallel capacitance  $C_P$  and the drain current is distorted.

In practice, except for  $B \ll 1$ , nonlinear effects cannot be neglected when  $|I_1|$  reaches its assumed saturation value  $I_0$ . This is illustrated by the simulation results of  $|I_m|/I_0$  (for  $|R_n| \ll R_L$ ) represented by circles in Fig. 6.22.

According to (6.127),  $|I_m| \cong |I_1|$  for the values of  $B$  used in the simulation (negligible current in  $C_P$ ). It should therefore saturate at  $I_0$ . However, when saturation is approached, the drain current tends to become a square wave of amplitude  $I_0$ , therefore the maximum value of its fundamental components tends to  $4/\pi \cdot I_0$ .

For values of  $B$  approaching unity, nonlinear effects must be analyzed by the general technique introduced in Chapter 3. An example of such an analysis is depicted in Fig. 6.23 for the case of  $B = 1$  (with  $C_L$  slightly larger than  $C_P/n$ ). From (6.109), the minimum transconductance producing a negative

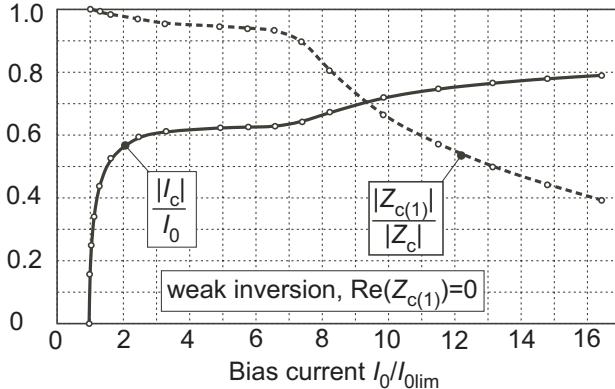


**Figure 6.23** Measurement of  $Z_{c(1)}(|I_c|)$  in a simulated circuit with  $B = 1$ . The bias current  $I_0$  is kept constant at a value much larger than its limit for negative resistance.

resistance is  $2\mu\text{A}/\text{V}$ , which corresponds to a limit bias current  $I_{0lim}=63\text{nA}$ . With  $I_0=200\text{nA}$  applied in this example, the negative resistance is reduced abruptly when the sinusoidal current  $|I_c|$  reaches  $127\text{nA}$ , corresponding to its saturation value. Compared to the linear case, the imaginary part of  $Z_{c(1)}$  is reduced by about 10%.

The variations of  $\text{Im}(Z_{c(1)})$  with the normalized bias current  $I_0/I_{0lim}$  for  $\text{Re}(Z_{c(1)}) \cong 0$  has been simulated for the same circuit, by connecting it to a motional impedance with  $R_m = 0$ . The result is shown in dotted line in Fig. 6.24.

For  $I_0 < 7I_{0lim}$ , the reduction of  $|Z_{c(1)}|$  is smaller than 10%. With the motional capacitance  $C_m = 2.1\text{ fF}$  of Example 1 in Table 4.1, this would cor-



**Figure 6.24** Measurements of  $Z_{c(1)}(I_0)$  and  $|I_c|(I_0)$  in the simulated circuit of Fig. 6.23(b).

respond to a maximum variation of frequency pulling of  $3.5 \cdot 10^{-5}$ . It starts changing more drastically for larger values of  $I_0$ .

The same figure shows the variation of the sinusoidal current  $|I_c| = |I_m|$  with the bias current. The ratio  $|I_c|/I_0$  reaches a first plateau that is about  $4/\pi$  higher than what would be calculated by (6.127) for a sinusoidal drain current of amplitude  $|I_1| = I_0$ , before further increasing.

### 6.3.4 Phase Noise

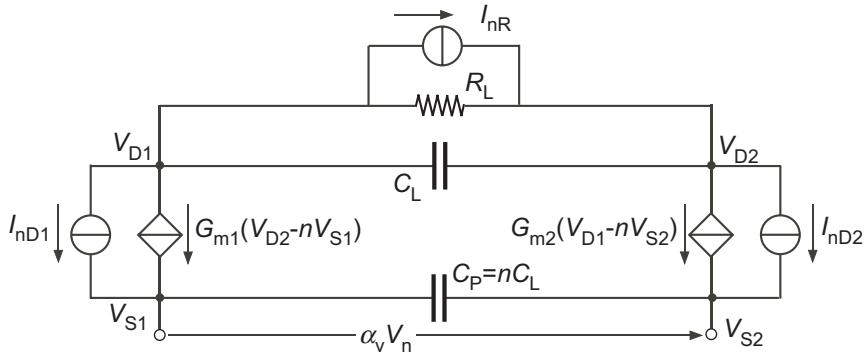
#### 6.3.4.1 Noise Voltage

The effect of the channel noise can be analyzed by means of the equivalent circuit of Fig. 6.25. Besides the channel noise sources  $I_{nD1}$  and  $I_{nD1}$  of the two transistors, the thermal noise current  $I_{nR}$  of the load resistance is included. Calculations on this circuit for the limit case  $C_P = nC_L$  yields the cyclostationary noise voltage across the motional impedance  $Z_m$ :

$$\alpha_v V_n = \frac{1}{n} \cdot \frac{R_L I_{nR} + (1 + jB_n)(I_{nD1}/G_{m1} - I_{nD2}/G_{m2})}{(1 - xB_n^2) + jxB_n}, \quad (6.147)$$

where  $B_n$  is the value of  $B$  defined in (6.108) with  $\omega$  replaced by  $\omega_n$ , the frequency at which the noise is considered. The local variable  $x$  is defined by

$$x \triangleq \frac{1}{R_L} \left( \frac{1}{G_{m1}} + \frac{1}{G_{m2}} \right) \quad (6.148)$$



**Figure 6.25** Equivalent circuit for noise calculation of the series resonance oscillator.

It varies periodically along each cycle of oscillation.

Using the expression (3.60) of the spectrum of  $I_{nD}$ , the spectrum of this cyclostationary voltage is then

$$\alpha_v^2 S_{V_n^2} = \frac{4kTR_L}{n^2} \cdot \frac{1 + (1 + B_n^2)n\gamma_t x}{B_n^2 x^2 + (1 - B_n^2 x)^2}, \quad (6.149)$$

### 6.3.4.2 Phase Noise of the Linear Circuit

For very small amplitudes, the circuit remains linear and only noise frequencies close to the oscillation frequency have to be considered, thus  $\alpha_v = 1$ ,  $G_{m1} = G_{m2} = G_{mcrit}$  and  $B_n = B$ . After approximating  $G_{mcrit}$  by  $G_{mlim}$  given by (6.109), the voltage noise spectral density becomes

$$S_{V_{n0}^2} = 4kTR_L \frac{1 + n\gamma_t}{n^2} (1 + B^2). \quad (6.150)$$

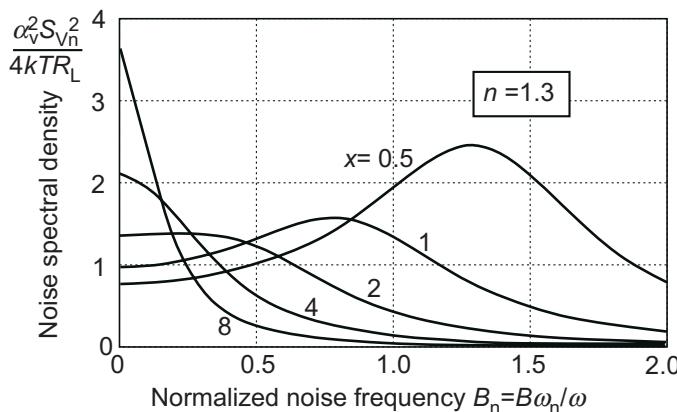
According to Fig. 3.7, the phase noise excess factor at very small amplitudes is obtained after division of the thermal noise spectrum of  $R_m$ :

$$\gamma_0 = \frac{1 + n\gamma_t}{n^2} (1 + B^2) \frac{R_L}{R_m}, \quad (6.151)$$

showing that  $\gamma_0$  is minimum for  $B$  small and for  $R_L$  close to  $R_m$ .

### 6.3.4.3 Phase Noise due to White Noise in the Nonlinear Time Variant Circuit

The calculation of phase noise for large amplitudes is made complicated by the fact that the spectrum of the cyclostationary noise voltage expressed by (6.149) depends on  $B_n$ , i.e. on the frequency  $\omega_n$  at which the noise is considered. Furthermore, this spectrum depends on the value of  $x$  that varies along each cycle with  $G_{m1}$  and  $G_{m2}$ , according to (6.148). This variation is illustrated by Fig. 6.26.



**Figure 6.26** Spectrum of the cyclostationary noise for various values of  $x$ .

To render the problem tractable analytically, we shall assume that the spectrum remains constant at its value at the oscillation frequency by replacing  $B_n$  by  $B$ . As can be seen in the figure, this approximation is only valid for  $\omega_n \ll \omega/B$  and  $x$  not too large. This domain of validity includes noise frequencies above  $\omega$  only if  $B \ll 1$  and  $m_i$  not too close to unity (since the peaks of  $x$  tend to infinity when  $m_i$  approaches unity).

The spectrum (3.60) of the cyclostationary voltage is thus approximated by

$$\alpha_v^2 S_{V_n^2} = \underbrace{\frac{4kTR_L}{n^2}}_{S_{V_n^2}} \cdot \underbrace{\frac{1 + (1 + B^2)n\gamma_i x}{B^2x^2 + (1 - B^2x)^2}}_{\alpha_v^2}, \quad (6.152)$$

where  $S_{V_n^2}$  is the spectrum of a fictitious noise voltage modulated by  $\alpha_v$ .

If the transistors operate in *weak inversion*, the transconductance is given by (3.54) and varies cyclically with the drain current according to (6.132):

$$G_{m1,2} = \frac{I_0}{nU_T} (1 \pm m_i \sin \phi) = G_{mcrit} \cdot \frac{v_{c(1)}}{m_i} (1 \pm m_i \sin \phi), \quad (6.153)$$

where the second form has been obtained by using (6.136) to replace  $I_0$  by its critical value, with  $v_{c(1)}$  given by (6.138).

As done previously, the critical transconductance  $G_{mcrit}$  can be approximated by the limit value  $G_{mlim}$  given by (6.109). The local variable  $x$  defined by (6.148) then becomes

$$x = \frac{1}{1+B^2} \cdot \frac{m_i}{v_{c(1)}} \cdot \frac{1}{1-m_i^2 \sin^2 \phi} \quad (6.154)$$

and can be introduced into (6.152) to obtain  $\alpha_v^2$ . The mean square value of the effective impulse sensitivity function is then given by

$$\overline{\Gamma_v^2} = \overline{\alpha_v^2 \cos^2(\phi + \Delta\phi)} = \frac{1}{2\pi} \int_0^{2\pi} \alpha_v^2 \cos^2(\phi + \Delta\phi) d\phi, \quad (6.155)$$

where  $\Delta\phi$  is the phase shift between the current  $I_1$  through the transistor and the motional current  $I_m$ . Indeed, the peaks of the noise voltage modulation function  $\alpha_v$  coincide with the peaks of current through the transistors. Thus, from (6.127)

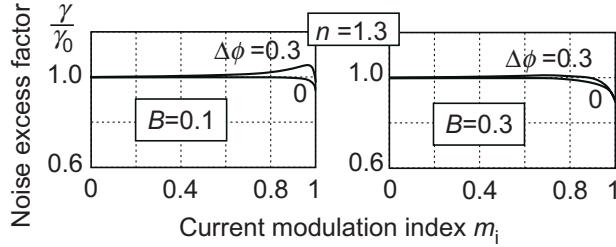
$$\tan \Delta\phi = \frac{1}{M_D(1+B^2)} \quad (6.156)$$

Now,  $S_{V_n^2}$  in (6.152) is independent of the current modulation index  $m_i$ . Therefore, according to (3.31), the spectral density of the phase noise due to the circuit is proportional to  $\overline{\Gamma_v^2}$ . Thus the variation of the phase noise excess factor  $\gamma$  is

$$\frac{\gamma}{\gamma_0} = \frac{\overline{\Gamma_v^2}}{\overline{\Gamma_v^2}|_{m_i=0}}. \quad (6.157)$$

Results obtained by introducing (6.154) and (6.152) in (6.155) are plotted in Fig. 6.27 for two values of the normalized bandwidth  $B$ . They show that the noise excess factor remains approximately constant with the index of modulation.

It must be reminded that the approximation by a white noise voltage spectrum ( $B_n = B$  in (6.149)) is only valid for  $B \ll 1$ . Otherwise, if the modulation factor approaches unity,  $G_{m1}$  or  $G_{m2}$  becomes very small in the peaks of oscillation and  $x$  defined by (6.148) becomes very large. As illustrated by Fig. 6.26, the noise is then no longer white but is concentrated at low frequencies.



**Figure 6.27** Variation of the phase noise excess factor with the amplitude of oscillation, with transistors operated in weak inversion. These results are calculated with the *approximation* of a white noise voltage spectrum across the motional impedance of the resonator.

#### 6.3.4.4 Phase Noise due to the Flicker Noise of the Active Transistors

As for the parallel resonance oscillator, a bias independent voltage source of flicker noise at the gate (as in the simple model defined by (3.62)) produces no phase noise, due to the symmetry of the circuit. Let us use again the more general model (6.71) for a flicker noise drain current. For the noise of transistor  $T_1$  only, the spectral density of cyclostationary noise voltage across the motional impedance given by (6.147) becomes

$$\alpha_v^2 S_{V_n^2} = \frac{(1 + B_n^2)}{(1 - xB_n^2)^2 + x^2 B_n^2} \cdot \frac{F_a (G_{m1}/G_a)^a}{\omega_n n^2 G_{m1}^2}. \quad (6.158)$$

For low-frequency flicker noise,  $B_n = \omega_n/\omega \ll 1$ . Furthermore  $xB_n \ll 1$ , except when  $x$  defined by (6.148) becomes very large in the peaks of oscillation ( $G_{m1}$  or  $G_{m2}$  very small). Therefore, (6.158) can be simplified to

$$\alpha_v^2 S_{V_n^2} = \frac{F_a G_{m1}^{a-2}}{\omega_n n^2 G_a^a}. \quad (6.159)$$

In *weak inversion*, the variation of  $G_{m1}$  along each cycle is given by (6.153), hence

$$\alpha_v^2 S_{V_n^2} = \underbrace{\frac{F_a G_{m1}^{a-2}}{\omega_n n^2 G_a^a} \cdot \left( \frac{v_{c(1)}}{m_i} \right)^{a-2}}_{\frac{1}{2} \cdot \frac{K_{fv}}{\omega_n}} \cdot \underbrace{(1 + m_i \sin \phi)^{a-2}}_{\alpha_v^2}. \quad (6.160)$$

The spectrum of the fictitious flicker noise voltage modulated by  $\alpha_v$  is thus characterized by

$$K_{fv} = 2F_a \cdot \left( \frac{G_{mcrit}}{G_a} \right)^a \cdot \frac{1}{n^2 G_{mcrit}^2} \cdot \left( \frac{v_{c(1)}}{m_i} \right)^{a-2}, \quad (6.161)$$

where a factor 2 has been introduced to account for the noise of the second transistor.

The average value of the effective ISF is

$$\overline{\Gamma_v} = \overline{\alpha_v \cos(\phi + \Delta\phi)} = \frac{1}{2\pi} \int_0^{2\pi} (1 + m_i \sin \phi)^{a/2-1} \cos(\phi + \Delta\phi) d\phi, \quad (6.162)$$

with  $\Delta\phi$  given by (6.156). After decomposing  $\cos(\phi + \Delta\phi)$ , (6.162) becomes

$$\overline{\Gamma_v} = \frac{-\sin \Delta\phi}{2\pi} \int_0^{2\pi} (1 + m_i \sin \phi)^{a/2-1} \sin \phi d\phi. \quad (6.163)$$

Before introducing (6.161) and (6.163) in (3.35) to obtain the phase noise spectrum due to the flicker noise of the transistors, the motional current can be expressed as a function of the current modulation index  $m_i$ . By using (6.127) and (6.136):

$$I_m \cong \frac{I_1}{1+B^2} = \frac{m_i I_0}{1+B^2} = \frac{m_i I_{0critmin}}{1+B^2} \cdot \frac{v_{c(1)}}{m_i}. \quad (6.164)$$

The phase noise spectrum obtained from (3.35) is then

$$S_{\phi_n^2} = \frac{2F_a}{\Delta\omega^3} \left( \frac{G_{mcrit}}{G_a} \right)^a \left( \frac{\omega^2 C_m (1+B^2) \sin \Delta\phi}{n I_{0critmin} G_{mcrit}} \right)^2 \cdot \left( \frac{v_{c(1)}}{m_i} \right)^{a-4} \left[ \frac{\int_0^{2\pi} (1 + m_i \sin \phi)^{a/2-1} \sin \phi d\phi}{2\pi m_i} \right]^2, \quad (6.165)$$

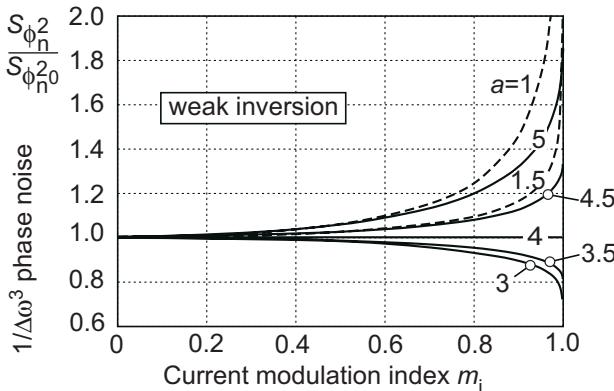
where  $v_{c(1)}$  is given by (6.138).

The first line of this expression is independent of the amplitude, whereas the second line takes the value  $(a-2)^2/16$  for  $m_i = 0$ . The spectral density for very small amplitudes is thus

$$S_{\phi_n^2 0} = \frac{2F_a}{\Delta\omega^3} \left( \frac{G_{mcrit}}{G_a} \right)^a \left( \frac{(a-2)\omega^2 C_m (1+B^2) \sin \Delta\phi}{4n I_{0critmin} G_{mcrit}} \right)^2, \quad (6.166)$$

or after replacing  $I_{0critmin}$  by  $G_{mcrit}$  approximated by  $G_{mlim}$  (given by (6.109)):

$$S_{\phi_n^2 0} \cong \frac{2F_a}{\Delta\omega^3} \left( \frac{G_{mcrit}}{G_a} \right)^a \left( \frac{(a-2)\omega^2 C_m R_L^2 \sin \Delta\phi}{16n^2 U_T (1+B^2)} \right)^2. \quad (6.167)$$



**Figure 6.28** Variation of the  $1/\Delta\omega^3$  phase noise (due to flicker noise) with the index of current modulation  $m_i$ , for various values of the exponent  $a$  of the transistor flicker noise current spectrum described by (6.71).

The variation with  $m_i$  of the  $1/\Delta\omega^3$  noise phase spectrum described by (6.165) is plotted in Fig. 6.28. It must be remembered that these results are calculated for  $xB_n \ll 1$ , i.e. for flicker noise frequencies of the transistors

$$\omega_n \ll \frac{1}{C_L(1/G_{m1} + 1/G_{m2})}. \quad (6.168)$$

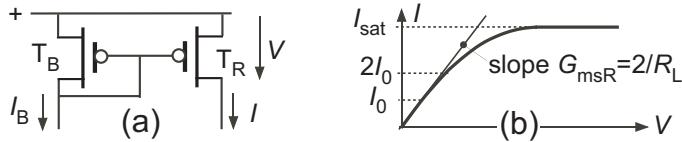
They are therefore not valid for  $m_i$  very close to unity. As can be seen, the  $1/\Delta\omega^3$  noise does not depart significantly from its value for small amplitudes expressed by (6.166) or (6.167).

### 6.3.5 Practical Implementation

Complementary oscillatory signals can be extracted at the drains of the active transistors by simple voltage followers. If no resistors are available, they can be replaced by a non-saturated P-channel transistors  $T_R$  associated with a bias transistor  $T_B$ , as shown in Fig. 6.29, both operated in *strong inversion*. If the maximum current  $I = 2I_0$  is sufficiently smaller than its saturation value  $I_{sat}$  given by

$$I_{sat} = I_B \cdot \frac{I_{specR}}{I_{specB}}, \quad (6.169)$$

then the current  $I$  remains an approximately linear function of the voltage  $V$  across  $T_R$ , with a slope equal to the source transconductance  $G_{msR}$ . Intro-



**Figure 6.29** Implementation of the load resistor  $R_L/2$  by means of transistor  $T_R$ ; (a) circuit; (b)  $I - V$  function.

ducing (6.169) in the expression (3.56) of the source transconductance then yields

$$R_L = 2/G_{msR} = \frac{2U_T}{I_{specR}} \sqrt{\frac{I_{specB}}{I_B}}. \quad (6.170)$$

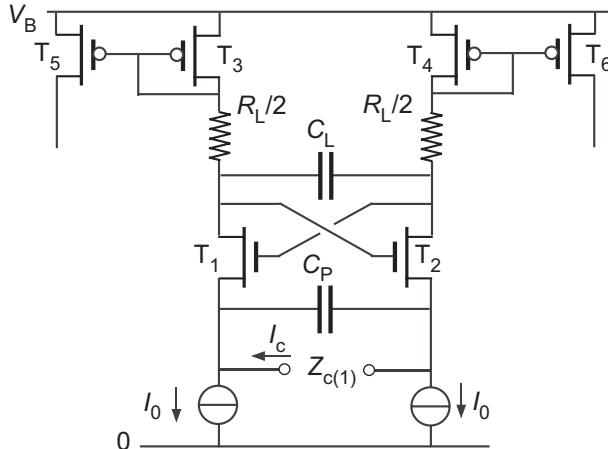
The drain voltage amplitude could be regulated, for example by the scheme developed for the Pierce oscillator and described in Section 5.2. But the simulated example of Fig. 6.23 shows that the nonlinear effects on the imaginary part (and thus on the frequency) are already limited for  $B = 1$ . They are further reduced for lower values of  $B$ , so that amplitude regulation is not really necessary. Anyway, an amplitude regulator would not drastically reduce the current consumption, since the negative resistance increases rapidly with the bias current as soon as the limit transconductance is reached, as can be observed in Fig. 6.20(b).

This circuit is by nature a current-mode oscillator, and the signal is best extracted as a current (or two complementary currents), as depicted in Fig. 6.30. The P-channel transistors  $T_3$  and  $T_4$  of the output mirrors are in series with the load resistors. Thus, in the small-signal analysis, the inverse of the transconductance  $G_{mp}$  of the P-channel transistors must be added to  $R_L/2$ . But this transconductance depends on the bias current  $I_0$  and thus changes with the transconductance  $G_m$  of the N-channel active transistors  $T_1$  and  $T_2$ . The circuit impedance  $Z_c$  is therefore no longer a bilinear function of  $G_m$  and its locus is *no longer a circle*.

Still, the essential characteristics of the basic circuit can be maintained if  $G_{mp} \gg G_m$ . Since the same current flows through both transistors, (3.56) shows that this can only be obtained if the active N-channel transistors operate in strong inversion with specific current much smaller than that of the P-channel input transistors of the mirrors, i.e. if

$$I_{spec1,2} \ll I_0 \text{ and } I_{spec1,2} \ll I_{spec3,4}. \quad (6.171)$$

These conditions can be fulfilled without reducing  $I_{spec1,2}$  too much if the mirrors operate in weak inversion (i.e. with  $I_{spec3,4} > I_0$ ).



**Figure 6.30** Extraction of the oscillatory signals by current mirrors.

If all transistors are in weak inversion, then, according to (3.54), their transconductance are almost equal (with just a small difference due to different values of  $n$  for P-channel and N-channel devices). The transconductance  $G_{mp}$  of the P-channel devices can no longer be neglected.

Let us assume that  $G_{mp} \equiv G_m$ . Since  $1/G_{mp}$  is connected in series with  $R_L/2$ ,  $R_L$  must be replaced by  $R_L + 2/G_m$  in (6.98). Then  $Z_c|_{\omega=0} = -R_L$ . A DC negative resistance would be obtained for an infinitely small value of transconductance. But a finite transconductance is needed to obtain an AC negative resistance. The analysis of Section 6.3.2 can be modified by replacing  $B$  by

$$B \Rightarrow \omega C_L(R_L + 2/G_m) = B + 2/A. \quad (6.172)$$

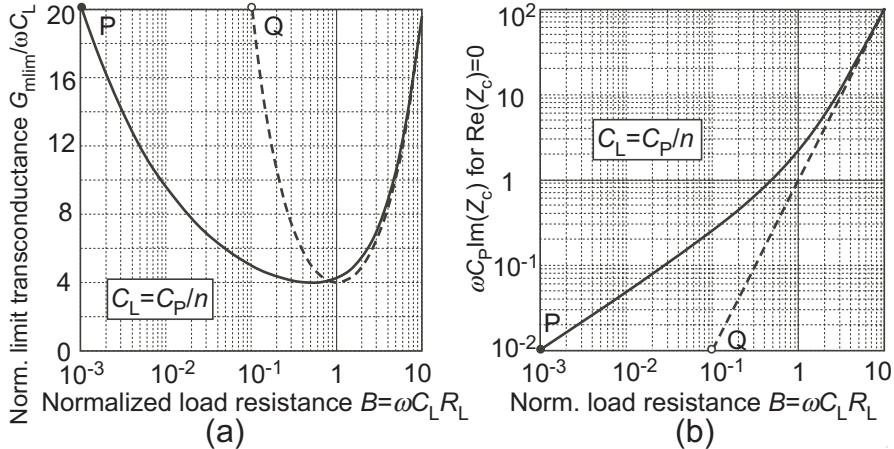
From (6.106), the real part of the impedance  $\text{Re}(Z_c)$  then changes sign for

$$2(B + 2/A) + \frac{2}{(B + 2/A)} - A = 0. \quad (6.173)$$

This is a third order equation in  $A$ , but a second order equation in  $B$ . Solving it for  $B$  gives:

$$B = \frac{1}{4} \left( A - \frac{8}{A} \pm \sqrt{A^2 - 16} \right). \quad (6.174)$$

This result is plotted as  $A(B)$  in Fig. 6.31(a). The minimum transconductance producing a negative resistance is the same as for the basic circuit of Fig. 6.16 ( $G_{m\lim} = 4\omega C_L$ ), but it is reached for  $B = 0.5$  instead of  $B = 1$ . The imaginary part of  $Z_c$  at this limit is obtained by applying the substitution (6.172) in (6.110). The result is plotted in Fig. 6.31(b).



**Figure 6.31** (a) Limit transconductance for negative resistance. (b)  $\text{Im}(Z_c)$  at this limit for the circuit of Fig. 6.30 with  $G_{mp} = G_m$ . The corresponding curves for the basic circuit of Fig. 6.16 (equations (6.106) and (6.110)) are shown in dotted lines.

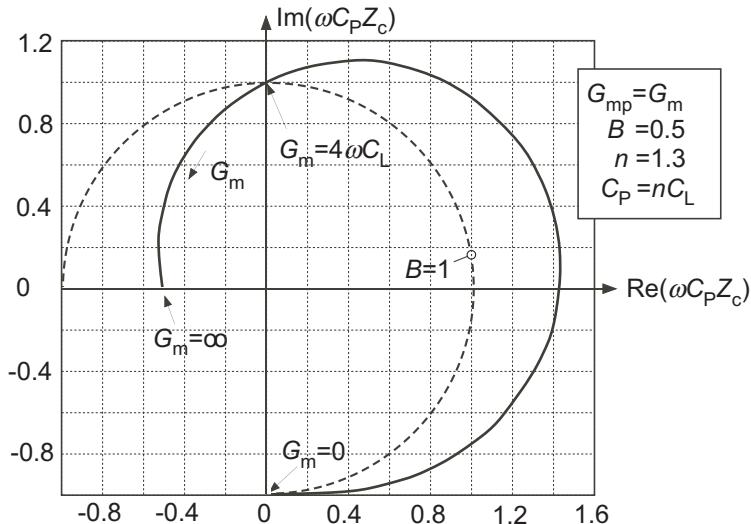
The relation between the limit transconductance for a negative resistance  $G_{m\text{lim}}$  and the imaginary part of the circuit impedance at this limit is given by (6.111). It does not depend on  $B$ . It is thus the same for the modified circuit as for the basic circuit, as illustrated by the example of points P and Q on the curves.

As already pointed out,  $Z_c$  is no longer a bilinear function of  $G_m$ . As an example, the locus of  $Z_c(G_m)$  calculated for  $B = 0.5$  (minimum of  $G_{m\text{lim}}$ ) is plotted in Fig. 6.32. The locus is now a spiral that is decentered with respect to the imaginary axis. Compared to the locus of the basic circuit with  $B = 1$ , the slope is no longer zero on the imaginary axis. This will result in a larger dependency of the frequency pulling on the quality factor and on nonlinear effects.

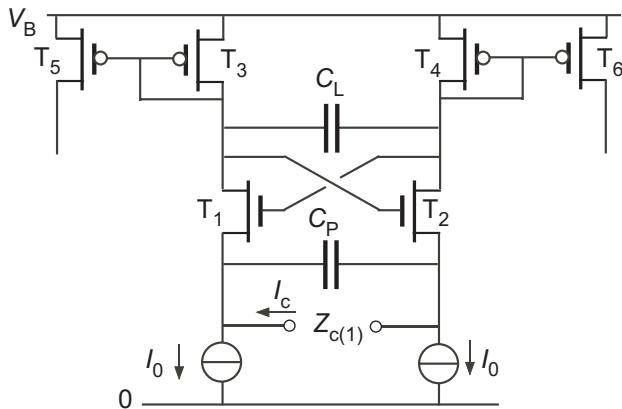
Another variant of the basic circuit is illustrated in Fig. 6.33. The load resistors of Fig. 6.30 have been eliminated and replaced by the transconductance  $G_{mp}$  of the P-channel transistors. The necessary voltage gain is obtained by choosing

$$G_{mp} = G_m/K_t, \quad (6.175)$$

where  $K_t$  is a constant factor sufficiently larger than unity. This is not possible in weak inversion but, according to (3.56), it can be obtained in *strong inversion* by sizing the transistors so that



**Figure 6.32** Locus of  $Z_c(G_m)$  for the circuit of Fig. 6.30 with  $G_{mp} = G_m$  and  $B = 0.5$ . The locus for the basic circuit of Fig. 6.16 with  $B = 1$  is shown in dotted line for comparison.



**Figure 6.33** Implementation without resistors.

$$\frac{I_{spec}}{n^2}|_{P\text{-channel}} = \frac{1}{K_t^2} \cdot \frac{I_{spec}}{n^2}|_{N\text{-channel}} \quad \text{or} \quad \frac{\beta}{n}|_{P\text{-channel}} = \frac{1}{K_t^2} \cdot \frac{\beta}{n}|_{N\text{-channel}}. \quad (6.176)$$

The factor  $K_t$  will not be very precise and will depend on temperature and process variations, since P-channel and N-channel transistors are not well matched. In practice, a value of  $K_t^2$  ranging between 2 and 4 will be obtained

for identical dimensions of N-channel and P-channel devices, due to the difference of mobility between electrons and holes.

With this scheme, the original load resistance  $R_L/2$  is replaced by  $K_t/G_m$  thus, according to (6.108):

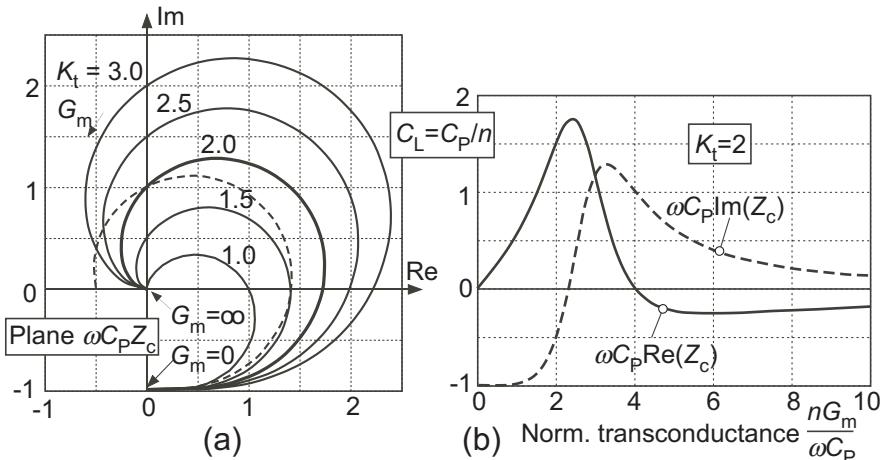
$$B = \frac{2K_t \omega C_L}{G_m} = \frac{2K_t}{A}, \quad (6.177)$$

which, introduced in (6.106) and (6.107) gives

$$\operatorname{Re}(Z_c) = \frac{1}{\omega C_P} \cdot \frac{2K_t(4K_t/A + A/K_t - A)}{4 + (4K_t/A - A)^2} \quad (6.178)$$

$$\operatorname{Im}(Z_c) = \frac{1}{\omega C_P} \cdot \frac{4(2K_t - 4K_t^2/A^2 - 1)}{4 + (4K_t/A - A)^2}, \quad (6.179)$$

with the normalized transconductance  $A$  defined by (6.108). The locus of  $Z_c(G_m)$  is plotted in Fig. 6.34(a) for several values of the transconductance ratio  $K_t$ . It is again a spiral, but  $|Z_c|$  tend to zero when  $G_m$  tends to infinity.



**Figure 6.34** (a) Locus of  $Z_c(G_m)$  for the circuit of Fig. 6.33 for several values of  $K_t = G_m/G_{mp}$ . The locus for the circuit of Fig. 6.30 with  $G_{mp} = G_m$  and  $B = 0.5$  is shown in dotted line for comparison. (b) Real and imaginary parts of  $Z_c$  for  $K_t = 2$ .

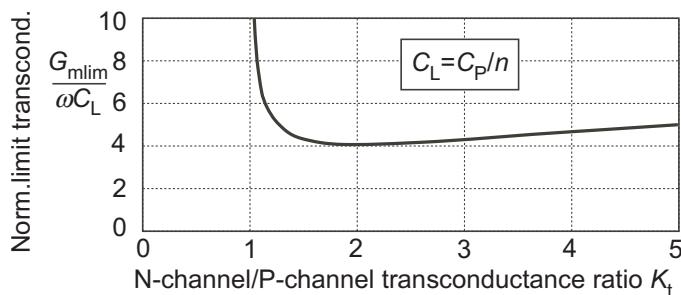
No negative resistance is possible for  $K_t \leq 1$ . The slope at  $\operatorname{Re}(Z_c = 0)$  is further worsened, as indicated by the comparison with the locus of Fig. 6.32, repeated here in dotted line.

Part (b) of the figure shows the variations of the real and imaginary parts of the circuit impedance with the transconductance, for  $K_t = 2$ . Compared to Fig. 6.20(b) for the basic circuit, the maximum of negative resistance is already reached for a small excess of transconductance  $G_m/G_{m\text{lim}}$ , and the imaginary part is strongly dependent of  $G_m$ .

Using (6.178), the limit transconductance for a negative resistance (i.e. for  $\text{Re}(Z_c) = 0$ ) is

$$G_{m\text{lim}} = \frac{2K_t}{\sqrt{K_t - 1}} \cdot \frac{\omega C_P}{n}. \quad (6.180)$$

As shown in the plot of Fig. 6.35, it has a minimum at  $K_t = 2$ . It increases rapidly below  $K_t = 1.5$  but only slowly above its minimum.



**Figure 6.35** Variation of the limit transconductance with the transconductance ratio  $K_t$ .

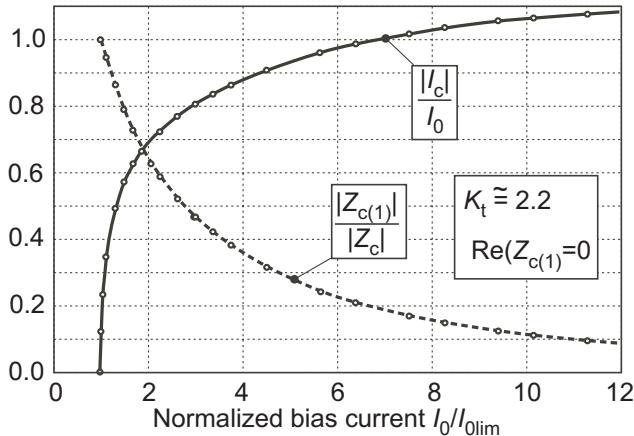
The imaginary part of the circuit impedance for  $G_m = G_{m\text{lim}}$  is obtained by introducing (6.177) and (6.180) in (6.110)

$$\text{Im}(Z_c)_{\text{lim}} = \text{Im}(Z_c)|_{\text{Re}(Z_c)=0} = \frac{K_t - 1}{\omega C_P}. \quad (6.181)$$

This can be verified in Fig. 6.34.

Nonlinear effects in the modified circuits are difficult to express analytically, since the active devices and their loads are both nonlinear. Results of a simulation of the transistors-only circuit of Fig. 6.33 for  $\text{Re}(Z_{c(1)}) = 0$  are plotted in Fig. 6.36.

As could be expected from the shape of the impedance locus,  $\text{Im}(Z_{c(1)}) = |Z_{c(1)}|$  (since  $\text{Re}(Z_{c(1)}) = 0$ ) is very dependent on the bias current: nonlinearities have a much larger effect on the frequency of oscillation than in the basic circuit (see Fig. 6.24).

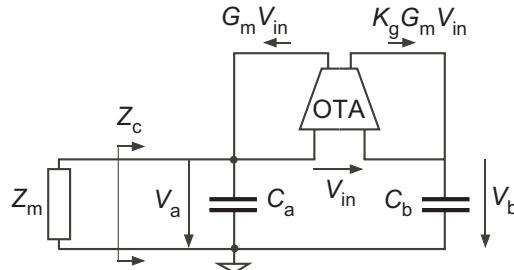


**Figure 6.36** Measurements of  $Z_{c(1)}(I_0)$  and  $|I_c|/I_0$  in a simulation of the modified circuit of Fig. 6.33 for  $\text{Re}(Z_{c(1)})=0$  with  $K_t = 2.2$ .

## 6.4 Van den Homberg Oscillator

### 6.4.1 Principle and Linear Analysis

A good example of an oscillator based on an operational transconductance amplifier (OTA) is illustrated in Fig. 6.37 [27]. The main purpose of this



**Figure 6.37** Principle of the oscillator proposed by van den Homberg.

structure is to provide a single pin oscillator (one side of the quartz grounded) with grounded capacitors only. The input  $V_{in}$  of the OTA is the difference of voltages across the two capacitors  $C_a$  (that include the electrical capacitor  $C_0$  of the resonator defined by (2.1)) and  $C_b$ . It delivers two separate output currents. The first one is proportional to  $V_{in}$  by a transconductance

$G_m$  and produces a positive feedback. The second one, with a proportional transconductance  $K_g G_m$  creates a negative feedback.

Assuming an ideal OTA and replacing the capacitances by more general impedances  $Z_a$  and  $Z_b$  including possible losses, the small-signal circuit impedance is

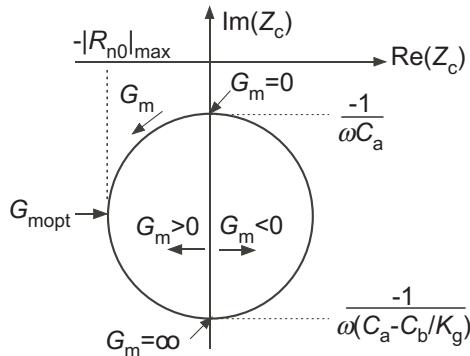
$$Z_c = \frac{Z_a + K_g G_m Z_a Z_b}{1 + G_m (K_g Z_b - Z_a)}, \quad (6.182)$$

which is again a bilinear function of the transconductance  $G_m$ . The locus of  $Z_c(G_m)$  is thus once more a circle. Without the motional impedance  $Z_m$ , the circuit must be stable, hence the real part of the poles of  $Z_c$  must be negative.

With lossless capacitors, the condition for stability becomes

$$C_b < K_g C_a, \quad (6.183)$$

meaning that the negative feedback gain  $K_g G_m / (\omega C_b)$  must be larger than the positive feedback gain  $G_m / (\omega C_a)$ . The circular locus is centered on the imaginary axis as depicted in Fig. 6.38.



**Figure 6.38** Locus of the circuit impedance for the oscillator of Fig. 6.37 with an ideal OTA and lossless capacitors.

The real part of  $Z_c$  is

$$\text{Re}(Z_c) = \frac{-G_m}{(\omega C_a)^2 + G_m^2 (K_g C_a / C_b - 1)^2}, \quad (6.184)$$

and provides a maximum value of negative resistance

$$|R_{n0}|_{\max} = \frac{1}{2\omega C_a (K_g C_a / C_b - 1)} \text{ for } G_m = G_{mopt} = \frac{\omega C_a}{K_g C_a / C_b - 1}, \quad (6.185)$$

with  $C_a \geq C_P$ .

For  $R_m \ll |R_{n0}|_{max}$  (margin factor  $K_m \gg 1$ ), the frequency pulling at the critical condition for oscillation is simply, from (4.3)

$$p_c \cong \frac{C_m}{2C_a}, \quad (6.186)$$

and the term in  $G_m^2$  in the denominator of (6.184) can be neglected. Thus, from (3.9), the critical transconductance for the lossless circuit can be approximated by

$$G_{mcrit0} \cong \omega^2 C_a^2 R_m = \frac{\omega C_a^2}{QC_m} = \frac{\omega C_m}{4Q p_c^2} \quad (6.187)$$

The locus of  $Z_c(G_m)$  resembles that for the Pierce oscillator depicted in Fig. 4.6. Here,  $C_a$  plays the role of  $C_3 + C_s$  and  $C_3$  is replaced by  $C_a - C_b/K_g$ . The latter could in principle be made as large as wanted, thereby increasing the value of  $|R_{n0}|_{max}$ . In practice, it is limited by the need to satisfy the stability condition (6.183) in the worst case of mismatch, as for the parallel resonance oscillator of Section 6.2.

Using (6.16), the maximum value of negative resistance is therefore in the range

$$\frac{1 - \varepsilon_{max}}{4\omega C_a \cdot \varepsilon_{max}} \leq |R_{n0}|_{max} \leq \infty, \quad (6.188)$$

where  $\varepsilon$  is given by (6.15) with  $nC_D/C_S$  replaced by  $K_g C_a/C_b$ .

Since  $C_a$  in this circuit includes not only the electrical capacitor  $C_0$  of the resonator, but also the overall interconnection capacitance to ground, a good matching with  $C_b$  cannot be ensured. Furthermore, since the transconductance ratio  $K_g$  must be obtained by a ratio of drain currents, it will be affected by a random error that increases when the inversion decreases. For these reasons, the practical value of  $|R_{n0}|_{max}$  is not larger than for the basic Pierce oscillator.

The comparison of (6.187) with (4.26) shows that the critical transconductance for a given amount of frequency pulling  $p_c$  is four times smaller than for the Pierce oscillator. But this does not necessarily result in a reduction of power consumption, since the OTA consumes much more current than a single transistor to produce the same transconductance.

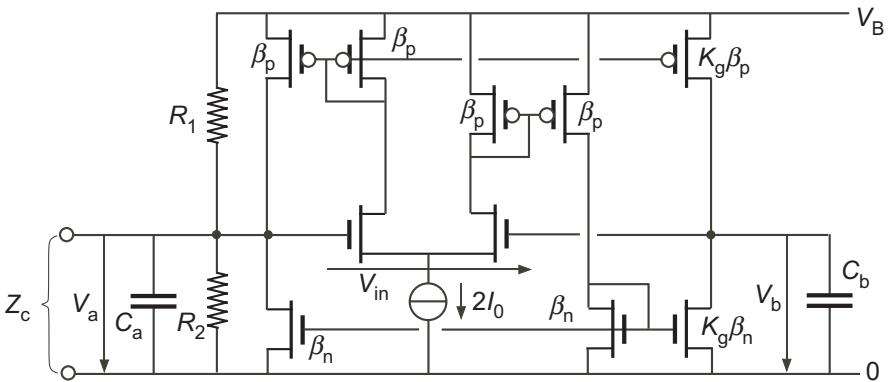
At the critical condition for oscillation, the transconductance is given by (6.187) and the voltages across the capacitors are related to the differential input voltage of the OTA by

$$V_b = -j \frac{K_g C_a}{C_b} \cdot \frac{C_a}{QC_m} V_{in} \quad \text{and} \quad V_a = V_b + V_{in}. \quad (6.189)$$

The value of  $K_g C_a / C_b$  is not much larger than unity to maximize the radius of the circular locus of Fig. 6.38. The value of  $V_b / V_{in}$  therefore depends essentially on  $QC_m / C_a = 2Qp_c$ . This value is often much larger than unity, resulting in  $|V_b| \ll |V_{in}|$  and  $|V_a| \cong |V_{in}|$ .

#### 6.4.2 Practical Implementation and Nonlinear Behavior

A full circuit implementation of the principle explained by Fig. 6.37 is shown in Fig. 6.39 [27]. The two feedback loops are implemented by adequate com-



**Figure 6.39** Circuit implementation of the oscillator of Fig. 6.37.

binations of P-channel and N-channel current mirrors. The DC bias current of each branch is  $I_0$ , except in the output stage driving  $C_b$  where it is  $K_g I_0$ . Thus, the total current is  $(4 + K_g)I_0$ , plus the current flowing through the bias resistors  $R_1$  and  $R_2$ . The ratio of these resistances is chosen for best centering of the output oscillatory signal, and their value must be sufficiently large to minimize the loss conductance  $G_a$  across  $C_a$ .

Some power could be saved by reducing the bias current in some branches. But this would increase the noise excess factor  $\gamma$  defined in Section 3.7 and the phase noise would be increased.

When the oscillation grows, the amplitude is limited by the nonlinear behavior of the input differential pair. Thus its dependency on the bias current  $I_0$  is given by (6.33) if the pair is in weak inversion, or by (6.39) if it is in strong inversion. These results are plotted in Fig. 6.6.

As for the other oscillator schemes, the bias current may be adjusted to the desired amplitude by means of a regulating loop.

## 6.5 Comparison of Oscillators

The main results obtained for the different types of oscillators are summarized in Table 6.1 for comparison.

	1	2	3	4
	Pierce	van den Homberg	parallel	series resonance
Section	4 and 5	6.4	6.2	6.3
branches	1	5	2	2
$p_c$	$\frac{C_m}{2(C_s+C_3)}$	$\frac{C_m}{2C_a}$	$\frac{C_m}{2C_D}$	$-\frac{C_m B^2}{2C_p}$
$p_{cmax}$	$< \frac{C_m}{2C_p}$	$\frac{C_m}{2C_p}$	$\frac{C_m}{2C_p}$	$\gg   -\frac{C_m}{2C_p}  $
$G_{mcrit0}$	$\frac{\omega C_m}{Q p_c^2}$	$\frac{\omega C_m}{4 Q p_c^2}$	$\frac{\omega C_m}{2 Q p_c^2}$	$\frac{2 \omega C_p}{n} \left( \frac{B^2+1}{B} + \frac{1}{2 Q  p_c } \right)$
$I_{critmin}$	$\frac{\omega C_m n U_T}{(2) Q p_c^2}$	$\frac{5 \omega C_m n U_T}{4 Q p_c^2}$	$\frac{\omega C_m n U_T}{Q p_c^2}$	$4 \omega C_p U_T \left( \frac{B^2+1}{B} + \frac{1}{2 Q  p_c } \right)$
amplitude	Fig. 4.17	Fig. 6.6	Fig. 6.6	Fig. 6.22
$\gamma_0$	$n \gamma \frac{C_1 G_{mcrit}}{C_2 G_{mcrit0}}$	-	$n \gamma \frac{G_{mcrit}}{G_{mcrit0}}$	$\frac{1+n\gamma}{n^2} (1+B^2) \frac{R_L}{R_m}$

**Table 6.1** Comparison of oscillators.

The number of branches has an impact on the total current  $I$  since a current proportional to  $I_0$  flows through each branch.

The amount of pulling  $p_c$  at the critical condition for oscillation is a measure of how much the frequency of oscillation differs from the mechanical resonant frequency of the resonator. Since  $p_c$  depends on electrical parameters that may vary with temperature and supply voltage, a large value can be expected to degrade the inherent frequency stability of the resonator, as was discussed in Section 4.3.5. The maximum possible pulling characterizes the limit of tunability of the oscillator.

The critical transconductance  $G_{mcrit}$  depends on the requirement on  $p_c$ , and on the various parameters of the resonator. The minimum current  $I_{0critmin}$  needed to obtain this transconductance is obtained in weak inversion and the minimum critical total current  $I_{critmin}$  is proportional to  $I_{0critmin}$  through the

number of branches. Somewhat larger values are needed to obtain a usable amplitude.

Calculations have shown that the phase noise excess factor  $\gamma$  does not change very much with the amplitude of oscillation. Its value  $\gamma_0$  at small amplitude is therefore used in the comparison. The effect of the noise coming from the bias current is not included.

### 6.5.1 Pierce Oscillator (1)

It is the most simple structure since the basic circuit (Fig. 4.1) requires a single active transistor. The current can be minimized by using the current-controlled CMOS implementation of Fig. 5.25, but the simple implementation with a CMOS inverter (Fig. 5.21) has many drawback, and should be avoided. The two functional capacitors  $C_1$  and  $C_2$  are grounded in the grounded source implementations (Fig. 5.1), but the resonator is not. The resonator may be grounded by using the grounded-drain implementation (Fig. 5.27), but  $C_1$  is then floating.

Oscillation is only possible if the total impedance  $Z_3 + Z_m$  between gate and drain is inductive. Therefore, according to the condition (4.16), the figure of merit  $M$  defined by (2.9) must be larger than 2. This condition should be satisfied with a large margin to maximize the frequency stability, but this margin is reduced in the grounded-drain implementation. The motional impedance  $Z_m$  is also inductive at stable oscillation, thus the pulling  $p_c$  given by (4.21) is always positive. It may be reduced by increasing  $C_s$ , the series connection of the two functional capacitors  $C_1$  and  $C_2$ . The maximum pulling is limited by  $C_p$ , the electrical capacitance  $C_0$  of the resonator augmented by unavoidable parasitic capacitors.

The critical transconductance of the lossless circuit  $G_{mcrit0}$  is related to  $p_c$  by (4.26) and is minimum for  $C_1 = C_2$ . The minimum critical total current is simply  $nU_T G_{mcrit0}$ . It may be reduced by a factor 2 by replacing the single transistor by a complementary pair.

The amplitude of oscillation depends on  $I_0/I_{0critmin}$  according to Fig. 4.17. A current  $I \geq 2.8I_{0critmin}$  is needed to obtain an amplitude  $|V_1| = 5nU_T$  at the gate.

The noise excess factor  $\gamma_0$  is minimum for  $C_1 = C_2$ . It increases with the increase of critical transconductance  $G_{mcrit}/G_{mcrit0}$  due to lossy components, but the noise associated with these components is not included.

### 6.5.2 Van den Homberg Oscillator (2)

This is the most complicated of the 4 schemes, since it requires a full double output operational transconductance amplifier (OTA), as illustrated in Fig. 6.37. Thus a minimum of 5 branches are needed with at least 5 internal nodes (Fig. 6.39). The poles related to these internal nodes should be made negligible, as was implicitly assumed in the analysis. The two functional capacitors  $C_a$  and  $C_b$  are grounded, as well as the resonator that is used as a dipole.

This circuit has no requirement on a minimum value of the figure of merit, but the condition for stability (6.183) must be fulfilled so that the negative feedback through  $C_b$  overrides the positive feedback through  $C_a$ . The circuit impedance  $Z_c$  is therefore always capacitive and thus the pulling  $p_c$  given by (6.186) always positive. It can be reduced by increasing  $C_a$ . Its maximum value  $p_{cmax}$  is obtained for  $C_a = C_p$ .

The minimum critical transconductance for a given value of  $p_c$  is close to one fourth of that of the Pierce circuit. However, the total critical current is about the same as the non-complementary implementation if the currents in the 5 branches are equal, as it should be to avoid increasing the noise.

The amplitude of oscillation is limited by the transfer function of the differential pair. Its dependency on  $I/I_{critmin}$  is plotted in Fig. 6.6. A current  $I \geq 2.5I_{critmin}$  is needed to obtain an amplitude  $|V_{in}| = 5nU_T$  at the input of the OTA. According to (6.189), the amplitude  $|V_a|$  across the resonator is always larger or equal to  $|V_{in}|$ .

The phase noise has not been evaluated for this oscillator, but its is expected to be increased by the larger number of active components.

### 6.5.3 Parallel Resonance Oscillator (3)

This is a symmetrical circuit which delivers complementary output voltages at the drain of the two transistors (Fig. 6.1(b)). It emulates a parallel resonator by using the parallel resonance of the motional impedance  $Z_m$  combined with the parallel capacitor  $C_P$ . The latter can be increased to a value  $C_D$  by an additional capacitor to reduce the pulling. This additional capacitor can be connected across the resonator, or it can be split in two grounded capacitor of double value. The sources of the transistor must be AC coupled by a capacitor  $C_S$  to avoid DC bistability. This capacitor can also be replaced by two grounded capacitors of value  $2C_S$ .

There is no condition on the maximum value of  $C_D$  (and thus on the minimum value of the figure of merit  $M_L$  defined by (6.7)). But to ensure AC stability at other frequencies than that of the resonator, the maximum value of  $C_S$  is limited by the condition (6.6). The impedance  $Z_c$  of the stable circuit is always capacitive, thus the pulling  $p_c$  given by (6.17) is always positive. Its minimum value is obtained when  $C_D$  is limited to  $C_P \geq C_0$ .

The minimum critical transconductance for the lossless circuit  $G_{mcrit0}$  is half that of the Pierce oscillator, but the minimum critical current  $I_{critmin}$  is the same, since the bias current flows in 2 branches.

As long as the impedance of the capacitance  $C_S$  is negligible compared to their source transconductance (condition (6.28) fulfilled), the active transistors operate as a differential pair. The variation of the drain to drain (or gate to gate) voltage amplitude  $|V_{in}|$  with  $I/I_{critmin}$  is shown in Fig. 6.6 for weak inversion, and for strong inversion with a given value of inversion coefficient  $IC = I_0/I_{spec}$  (thus not for a fixed value of specific current  $I_{spec}$  of the transistors).

The small-amplitude noise excess factor  $\gamma_0$  is the same as that of the Pierce oscillator with  $C_1 = C_2$ .

#### 6.5.4 Series Resonance Oscillator (4)

Whereas the first three oscillators above have comparable characteristics in spite of their different architectures, the series resonance oscillator depicted in Fig. 6.16 is very different in many aspects.

The function of the active devices of this symmetrical circuit is to change the sign of the load resistor  $R_L$  to obtain a negative resistance. Because of the capacitance  $C_P$  across the motional impedance  $Z_m$  of the resonator, a load capacitance  $C_L$  is needed to avoid parasitic oscillations. It must be sufficiently large to fulfill the condition (6.104), but not too large, since it would reduce the negative resistance. To simplify the analysis, all the derivations have been carried out with the assumption that the sufficient condition (6.103) is just fulfilled, i.e.  $C_L = C_P/n$ . The circuit impedance is always inductive ( $\text{Re}(Z_c) > 0$ ), thus the pulling  $p_c$  is always negative; the frequency of oscillation is lower than the mechanical resonance frequency of the resonator. The pulling depends on the value of the load resistor  $R_L$ . But this load resistance is neither precise nor constant in an integrated circuit. The value of  $|p_c|$  increases with  $B^2$ , and its maximum is not limited.

As expressed by (6.98) for the DC case, the transconductance  $G_m$  corresponds to a positive resistance in series with the negative resistance. It must therefore reach a limit value  $G_{mlim}$  given by (6.109) before some negative resistance is produced. This value is minimum for  $B = 1$ , that is for  $|p_c| = C_m/2C_P$ . It must be increased by a small amount  $\Delta G_m$  given by (6.119) to obtain the critical transconductance. This amount remains negligible as long as  $4Qp_c \gg 1$ .

The amplitude of oscillation is best characterized by the index of modulation of the bias current  $I_0$  by the oscillatory signal. Results based on the assumption of a perfectly sinusoidal current of amplitude  $|I_1|$  are plotted in Fig. 6.22. Just a small excess of current of about 50% is sufficient to achieve 100% current modulation. Simulations show that for higher values of bias current, the drain current tends to a square wave.

The phase noise excess factor  $\gamma_0$  is much larger than for oscillators 1 and 2 if the load resistance  $R_L$  is much larger than the motional resistance  $R_m$ . It increases rapidly for  $B > 1$ .

The performance of this oscillator (number 4) is compared with that of the three others in 4 numerical examples presented in Table 6.2.

parameter	Example a	Example b	Example c	Example d	Unit
$Q$	50000	5000	50000	500	
$R_m$	1.06	10.6	1.06	106	$\text{k}\Omega$
$M_D$	50	5	50	0.5	
$ p_c _{max(1,2,3)}$	500	500	500	500	ppm
$ p_c $	100	100	10	5000	ppm
$I_{critmin(1,2,3)}$	1.27	12.7	127	-	$\mu\text{A}$
$I_{critmin(4)}$	5.46	7.22	16.1	7.21	$\mu\text{A}$
$R_L$	30.8	30.8	9.75	218	$\text{k}\Omega$

**Table 6.2** Numerical comparison of oscillators. The frequency is 1 MHz with  $C_m = 3 \text{ fF}$ ,  $C_0 = 2 \text{ pF}$ ,  $C_P = 3 \text{ pF}$ ,  $n = 1.3$  and  $U_T = 26 \text{ mV}$ .

Example a illustrates a standard case with a high value of quality factor  $Q$  and a frequency pulling of 100 ppm. The minimum critical current for the series resonance oscillator (4) is more than four times larger than for the three others.

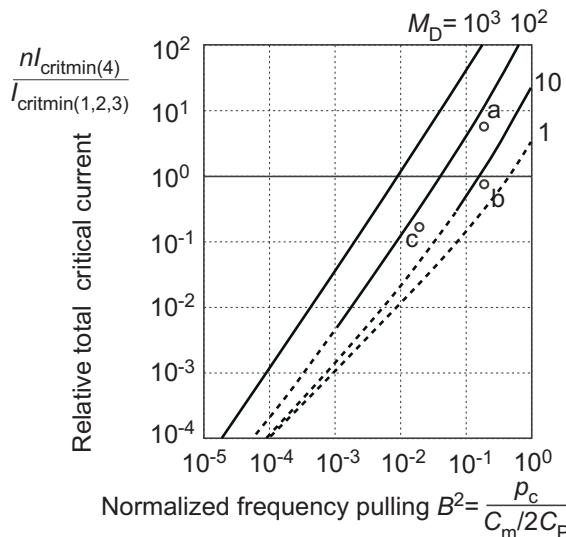
In Example b,  $Q$  is only 5000. Oscillator 4 requires less current than the others.

In Example c,  $Q$  is large but the pulling is reduced to 10 ppm. The minimum critical current is now about 8 times smaller than for the other oscillators.

Knowing that the parameter  $B$  is related to  $|p_c|$  by (6.113) (if condition (6.112) is fulfilled), the ratio of the minimum critical current for the series resonance oscillator to that of the 3 others can be expressed as

$$\frac{I_{\text{critmin}(4)}}{I_{\text{critmin}(1,2,3)}} = \frac{1}{n} (M_D B^5 + M_D B^3 + B^2), \quad (6.190)$$

where  $M_D$  is the figure of merit of the dipole resonator defined by (2.22). This ratio is plotted in Fig. 6.40. This comparison curves shows that when



**Figure 6.40** Relative total critical current of the series resonance oscillator. For the parts of the curves in interrupted line, the condition (6.112) is not fulfilled, thus  $|p_c| < C_m B^2 / 2C_P$ . Points a, b and c correspond to the first 3 examples of Table 6.2.

a very small pulling  $|p_c|$  is required (to minimize de frequency dependence on electrical parameters), the series resonance oscillator requires much less current than the three others.

In Example d, the required pulling is very large and  $Q$  is very small. This is possible with oscillator 4 with just a small increase in current. The load resistance has a large value, and can be used to tune the oscillator in a wide frequency range. The voltage drop across  $R_L/2$  is 414 mV at the critical

current, so about 600 mV for full current modulation; this is still compatible with low supply voltage.

The series resonance oscillator is thus interesting for its large tuning range capability, for minimizing the current when a very low value of pulling is required, and/or for low-*Q* resonators.

# Bibliography

1. W. G. Cady. "Method of Maintaining Electric Currents of Constant Frequency", US patent 1,472,583, filed May 28, 1921, issued Oct. 30, 1923.
2. G. W. Pierce, "Piezoelectric Crystal Resonators and Crystal Oscillators Applied to the Precise Calibration of Wavemeters", Proc. American Academy of Arts and Sciences, vol. 59, October 1923, pp. 81-106.
3. G. W. Pierce, "Electrical System", US patent 2,133,642, filed Febr. 25, 1924 , issued Oct. 18, 1938.
4. W. A. Morrison and J.W. Horton, "Precision Determination of Frequency". I.R.E. Proc. vol. 16, pp. 137154 Feb., 1928.
5. E. Vittoz, The Electronic Watch and Low-Power Circuits", IEEE Solid-State Circuits Society News, Vol. 13, No. 3, Summer 2008, pp.7-23.
6. A. Hadjimiri and T. H. Lee, "A General Theory of Phase Noise in Electrical Oscillators", IEEE J. Solid-State Circuits, vol. 33, pp. 179-194, Febr. 1998. Corrections at page 928 of the same journal (June 1998).
7. V. Uzunoglu, *Semiconductor Network Analysis and Design*, McGraw Hill, 1964, p.245.
8. M.R. Spiegel, *Complex Variables*, Schaum Publishing Co, New York, 1964.
9. F.E. Terman, *Radio Engineering HandBook*, McGraw-Hill, 1943.
10. E. Momosaki, "A Brief Review of Progress in Quartz Tuning Fork Resonators", Proceedings of the 1997 IEEE International Frequency Control Symposium, 1997, pp. 552-565, 28-30 May 1997.
11. W. P. Mason, "A New Quartz Crystal Plate, Designated the GT, Which Produces a Very Constant Frequency Over a Wide Temperature Range", Proc. IRE, vol. 28, p. 220, May 1940.

12. J. Hermann,"A Novel Miniature ZT-Cut Resonator", Proc. of the 39th Annual Symposium on Frequency Control, 1085, pp. 375-380.
13. E. Vittoz, "Quartz Oscillators for Watches", invited paper, Proc. 10th International Congress of Chronometry, pp. 131-140, Geneva, 1979.
14. E. Vittoz, M. Degrauwe and S. Bitz, "High-Performance Crystal Oscillator Circuits: Theory and Applications", IEEE J. Solid-State Circuits, vol. SC-23, pp. 774-783, June 1988.
15. H. J. Reich, *Functional Circuits and Oscillators*, Boston technical Publishers, Cambridge MS, 1965.
16. D. B. Leeson, "A Simple Model of Feedback Oscillator Noise Spectrum", Proc. IEEE, Vol. 54, pp. 329-330, Febr. 1966.
17. C. Enz, F. Krummenacher and E. Vittoz, "An Analytical MOS Transistor Model Valid in All Regions of Operation and Dedicated to Low-Voltage and Low-Current Applications", Analog Integrated Circuits and Signal Processing, Vol.8, pp. 83-114, 1995.
18. C. Enz and E. Vittoz, *Charge-Based MOS Transistor Modeling*, John Wiley and Sons, Chichester, 2006.
19. H. Oguey and S. Cserveny, "MOS Modelling at Low Current Density", Summer Course on Process and Device Modelling. ESAT-Leuven, June 1983.
20. J. K. Clapp, "An inductive-Capacitive Oscillator of Unusual Frequency Stability", Proc. IRE, vol. 36, 1948, pp. 356-358.
21. E. Vittoz and J. Fellrath, "CMOS Analog Integrated Circuits Based on Weak Inversion Operation", IEEE J. Solid-State Circuits, vol. SC-12, pp. 224-231, June 1977.
22. D. A. Aebscher, H. J. Oguey and V. R. von Kaenel, "A 2.1MHz Crystal Oscillator Time Base With a Current Consumption under 500nA", IEEE J. Solid-State Circuits, vol. 32, pp. 999-1005, July 1997.
23. J.Santos and R. Meyer, "A One-Pin Oscillator for VLSI Circuits", IEEE J. Solid-State Circuits, vol. SC-19, pp. 228-236, April 1984.
24. J. Luescher, "Oscillator Circuit Including a Quartz Crystal Operating in Parallel Resonance", US patent 3,585,527, filed oct. 27, 1969, issued June 15, 1971.
25. D. Ruffieux, "A High-Stability, Ultra-Low-Power Differential Oscillator Circuit for Demanding Radio Applications", Proc. ESSCIRC'02, pp. 85-88, 2002.
26. M. P. Forrer, "Survey of Circuitry for Watches", Proc. IEEE, vol. 60, pp.1047-1054, Sept. 1972.
27. J.A.T.M. van den Homberg, "A Universal 0.03-mm<sup>2</sup> One-Pin Crystal Oscillator in CMOS", IEEE J. Solid-State Circuits, vol. 34, pp. 956-961, July 1999.

# Index

- amplitude
  - detector, 73
  - increase of, 62, 106
  - limitation, 27, 28, 58
  - of drain voltage, 94, 184
  - of gate voltage, 58, 61, 62, 65
  - of oscillation, 5, 61, 62, 65, 94, 146, 162
  - regulation, 73, 107, 122, 162
    - stability, 116, 117
  - regulator, 108
    - curve, 110, 121, 163
    - simplified, 117
    - stability, 5
- bias current, 61, 145
  - critical, 61, 64, 108, 161
  - start-up, 109
- bilinear function, 11, 43, 167
- capacitance
  - gate oxide, 37
  - load, 48
  - motional, 8
  - parallel, 8, 14
  - parasitic, 8
- capacitive
  - attenuator, 62
  - circuit impedance, 196
  - coupling, 22, 138
  - load, 123
- transducer, 18
- channel length modulation, 39
  - voltage, 39
- channel noise excess factor, 40
- circuit impedance, 24, 43, 70, 165, 166, 191
  - for the fundamental, 24, 31, 55, 69
    - locus of, 24, 26, 56, 125
    - locus of, 43, 46, 52, 56, 134, 141, 158, 160, 162, 167, 170, 172, 187, 188, 191
    - real and imaginary parts, 167, 170, 172
- coupling
  - coefficient, 9, 18
  - electromechanical, 9
  - factor, 14, 18, 21
- critical
  - condition for oscillation, 27, 43
  - current, 108, 126, 161
    - minimum, 61, 64, 147, 194
  - supply voltage, 125, 126
  - transconductance, 44, 49, 59, 139, 143, 169, 170, 194
- current
  - bias, 65
  - specific, 37, 162
- cyclostationary noise, 33, 79, 81, 149, 151, 154, 157, 177, 179, 181
- design

- example, 89, 100, 117
- process, 84
- differential pair, 137
- distortion
  - of drain current, 174
  - of gate voltage, 57
- drain current, 36
  - forward component of, 36
  - reverse component of, 36
- duality, 30
- dynamic behavior
  - of bias, 95, 97
  - of oscillation amplitude, 97, 100
- electromechanical
  - coupling, 9
  - transducing property, 16
- electrostatic transducer, 18
- energy
  - dissipation, 34
  - exchange of, 24, 34
  - kinetic, 15
  - mechanical, 7, 15, 68, 148
  - of oscillation, 33
  - potential, 15
  - thermal, 30
- equivalent circuit
  - of series resonance oscillator, 164
    - for small signal, 164
  - of parallel resonance oscillator, 140
    - for small signal, 140
  - of Pierce oscillator, 42
    - for small signal, 42
  - of quartz resonator, 8, 10
- figure of merit, 18–20, 22, 47
  - of dipole resonator, 14
  - of loaded dipole resonator, 139
  - of resonator, 10, 14
- frequency
  - adjustment, 54
  - parallel resonance, 11–13
  - pulling, 10
  - resonant, 8, 16, 138
  - series resonance, 11–13
- stability, 69
- frequency pulling, 54, 139
  - at critical condition, 27, 44, 48, 142, 168, 171, 194
  - at stable oscillation, 26, 57
  - effect of losses on, 53
- fundamental component
  - of control voltage, 173, 174
  - of drain current, 59, 60, 63
  - of output current, 146, 147
  - of voltage, 24, 55
- impedance
  - motional, 8, 10
  - parallel, 11, 139
    - locus of, 11, 139
- impulse sensitivity function (ISF), 33, 34, 79, 81–83, 152, 153, 180, 182
- inversion
  - coefficient, 37
    - at bias current, 146
    - at critical current, 63, 174
  - strong, 37, 38
  - weak, 37, 38
- linear
  - analysis, 42, 55, 139, 144, 165, 172, 190, 193
  - approximation, 27
  - circuit, 27
    - noise, 31, 33, 150, 178
  - function, 103
  - impedance, 10
  - range of operation, 27
  - resistive element, 102
- load
  - capacitance, 48
  - resistance, 188
  - resistor, 165
- losses, 43, 163
  - effect of, 52, 54, 75, 143
  - on frequency pulling, 53
- lossless
  - capacitor, 46
  - circuit, 46, 51, 55, 84, 139

- mechanical
  - energy of oscillation, 15, 68, 148
  - power dissipation, 15, 68, 148
- MEM resonators, 18, 22
- mode
  - activity, 72
  - contour, 17
  - flexural, 16
  - fundamental, 10
  - of oscillation, 7
  - overtone, 10
  - thickness, 17
  - torsional, 17
  - unwanted, 71, 128
  - wanted, 10
- modulation index
  - of current, 173, 174, 180
  - of differential pair, 146
  - of gate voltage, 81
- MOS transistor
  - drain current, 36
  - EKV model, 36, 40, 55
  - intrinsic voltage gain, 39
  - saturation, 37
  - slope factor, 37
  - specific current, 37
  - threshold voltage, 37, 94
  - transfer function, 58
  - transfer parameter, 37
- motional
  - capacitance, 8
  - current, 9, 15
  - impedance, 8, 24, 30, 41, 68
  - locus of, 43, 141
  - inductance, 8
  - resistance, 8
- negative resistance, 41, 43, 44, 47, 52, 56, 137
  - current stable, 164
  - maximum, 47, 141, 142, 158, 160, 168, 191
  - voltage stable, 138
- noise
  - channel noise, 39
- cyclostationary, 33, 79, 81, 149, 151, 154, 157, 177, 179, 181
- excess factor, 31, 77, 78, 80, 83, 151, 152, 154, 195
- flicker, 35, 81–83, 154, 157, 181, 183
- model, 40
- of bias current, 83
- phase noise, 31, 35, 36, 77, 84, 149, 157, 177, 183
- thermal, 35
- white, 34, 35, 77–79, 81, 150, 154, 178, 180
- nonlinear
  - analysis, 55, 77, 144, 148, 172, 177
  - effects, 25, 55, 65, 69, 176, 189
  - simulation of, 56, 125, 176
  - example, 55
  - transfer function, 58, 65
- oscillation
  - amplitude, 24, 61, 62, 65, 146
  - critical condition for, 27, 43
  - energy, 15, 33
  - mode of, 8, 16
  - unwanted, 128
  - parasitic, 139, 166
  - signal extraction, 123, 185
  - stable, 25, 26, 31, 59
  - start-up of, 29
  - start-up of
    - time constant, 29, 47
- oscillator
  - applications of, 1
  - basics on, 4
  - comparison of, 194, 200
  - current-mode, 184
  - parallel resonance, 196
  - Pierce, 2, 41, 91, 93, 135, 195
  - CMOS inverter, 124, 131
  - grounded drain, 132, 135
  - grounded source, 93, 131
  - quartz, 1
  - series resonance, 197
  - single pin, 132, 190
  - symmetrical

- for parallel resonance, 137, 164
- for series resonance, 164, 189
- van den Homberg, 190, 193, 195
- parallel resonance oscillator, 137, 164, 196
- phase
  - noise, 31, 34–36, 77, 84, 149, 157, 177, 183
  - shift, 79–81, 150, 154, 180
  - stability, 5, 31, 43, 50, 138
- Pierce oscillator, 2, 41, 91, 93, 135, 195
  - CMOS inverter, 124, 131
    - current-controlled, 129, 131
    - simulation, 125
  - grounded drain, 132, 135
  - grounded source, 93, 131
- practical implementation
  - of parallel resonance oscillator, 157, 164
  - of Pierce oscillators, 93, 135
  - of series resonance oscillator, 183, 189
  - of van den Homberg oscillator, 193
- quality factor, 8, 24, 33, 44, 46, 53, 57, 70, 72, 77, 84, 89
- quartz
  - crystal, 15
  - production, 2
- quartz resonator, 7
  - cut
    - AT, 17
    - CT, 17
    - GT, 17
  - equivalent circuit, 8
  - resonant frequency of, 8
  - types of, 15
- resistor
  - elimination, 120
  - implementation, 102
- load, 165
- resonance
  - parallel, 11, 138
  - series, 11
- resonant circuit
  - parallel, 30
  - series, 8, 30
- resonator
  - dipole, 14
  - mechanical, 7
  - MEM, 18, 21, 22
  - quartz, 7
- saturation
  - drain voltage, 94
  - of MOS transistor, 37
- series resonance oscillator, 164, 189, 197
- strong inversion, 37, 63, 80, 82, 94, 146, 152
  - strict, 66, 88, 94, 146
- thermodynamic voltage, 37
- transconductance
  - amplifier, 190
  - critical, 44, 49, 52, 59, 139, 143, 169, 170, 194
  - drain transconductance, 38
  - for the fundamental frequency, 59, 67, 146
  - gate transconductance, 38
  - in saturation, 39
  - limit for negative resistance, 167, 189
  - maximum, 49
  - optimum, 43, 46, 169
  - source transconductance, 38
- van den Homberg oscillator, 190, 193, 195
- weak inversion, 37, 60, 62, 64, 72, 79, 81, 86, 89, 94, 146, 151, 155