AMD SOC Power Management: Improving Performance/Watt Using Run-time Feedback

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***Abstract* — This paper presents an analysis of four run-time power management features implemented in AMD's recent 28nM APU. These features optimize SOC performance by shifting power and frequency resources in response to workload characteristics. The Global Efficient APM (GEAPM), Core-Bound Boost (CBB) and Memory-Bound Boost (MBB) features are shown to provide a performance improvement of up to 76%, 4.3% and 12.5% respectively. The Local Efficient APM (LEAPM) feature is shown to reduce average CPU power consumption by 34% while reducing performance by less than 1%.**

***Index Terms* — Power management, SOC, workload analysis**

I. Introduction

Run-time power management has emerged as a valuable tool for improving performance and performance/Watt of SOCs. Historically, power management has been used to improve the energy efficiency of systems by reducing power consumption when the system is idle or underutilized. Common examples include clock gating, power gating and DVFS (dynamic voltage and frequency scaling). As high performance SOCs and architectures are pushed into smaller form factors, these techniques have also become critical for achieving maximum *performance*. Rather than only saving power when underutilized, power management can also take better advantage of thermal and power constraints. To provide safe, reliable operation, SOCs are designed and configured to prevent operation at power levels that cause thermal or power infrastructure violations. The problem with this approach is that a safe operating point (frequency and voltage) depends greatly on how the system is used. An application using only a single CPU core can safely operate at a much higher frequency than an application using many CPU cores at once. The concept extends to other aspects of utilization including, but not limited to: CMOS activity factor, ambient temperature, cooling solution, workload burstiness and programming model. Since the specific usage of the system cannot be known a priori, a fixed operating range must be defined that is safe for all scenarios. This can greatly reduce performance of the system when not operating in the worst-case conditions.

Run-time power management addresses this issue by accounting for and adapting to the particular operating conditions of the SOC. Rather than designing an SOC for the worst-case, frequency and voltage are adjusted on-the-fly in response to the actual power and temperature induced by the workload. Power managers of this sort have been implemented by most high performance SOC manufacturers. AMD's TurboCore® and Intel's Turbo® [1][2] features are two such examples. These features significantly raise the performance of SOCs for typical applications and operating conditions. Complex SOCs that contain diverse IP can readily deliver greater than 2X performance compared to non-power managed designs.

The primary function of power managers is to ensure the SOC operates within its infrastructure limits. As shown in Table 1, SOC infrastructure is defined in terms of temperature, current and power. The power manager raises performance of the system by increasing the frequency of the SOC whenever it is not operating beyond its infrastructure limits. While this approach maximizes utilization of the infrastructure, it does it is not necessarily maximize performance or efficiency. These aspects are provided by the four performance and efficiency optimizing features of AMD's power manager: GEAPM, CBB, MBB and LEAPM. These features track workload characteristics at run-time and choose a combination of frequencies/voltages that maximize the performance and efficiency of the SOC.

Table 1 AMD Power Manager Features

Objective	Name	Classification	Description
Temperature < Limit	Temperature Controller	Infrastructure	Limit die temperature
Current < Limit	Current Controller	Infrastructure	Limit supply current
Power < Limit	PPT	Infrastructure	Package Power Tracker
Maximize GPU Performance	GEAPM	Performance	Global Efficient APM*
Maximize CPU Performance	CBB/MBB	Performance	Core/Memory-Bound Boost
Minimize Active Power	LEAPM	Efficiency	Local Efficient APM*

*APM – Application Power Management [1]

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II. Run-Time Power Manager

To provide architectural flexibility, AMD's power manager is implemented using an on-die microcontroller. The microcontroller uses power and thermal feedback from the SOC to direct its decisions. Power feedback is provided by a digital power monitor. Using digital activity trackers on the die, the power monitor accounts for fluctuations in dynamic power caused by the workload. This approach is comparable to other published on-line power models [3][1][2]. In addition to workload variations in dynamic power, the power monitor also accounts for the effects of voltage, frequency and temperature using built-in models. To provide consistent repeatable performance, the models are calibrated for each version/model of the SOC.

A. GEAPM

The power manager contains three performance controllers: Global Efficient Application Power Management (GEAPM), Core-Bound Boost (CBB) and Memory-Bound Boost (MBB). GEAPM optimizes the balance of power between CPU and GPU within an SOC. It is *global* in the sense that it seeks to maximize the SOC-level performance rather than the individual (local) performance of either CPU or GPU. The feature works on the premise that most graphics workloads are cooperative in nature [4][5]. The net performance of the system is dictated by how well the cooperating CPU and GPU are balanced. If either is consuming an excess of the limited thermal and/or power budget, a bottleneck is introduced, thus reducing global performance. The imbalance manifests as one of the entities reaching a thermal/power limit before fully saturating other system resources. GEAPM tracks the relative performance of the cpu/gpu and shifts available power between them to maintain a balanced operating condition. Figs. 1 and 2 illustrate the impact of GEAPM through traces of graphics clock and activity level without it and with it respectively.

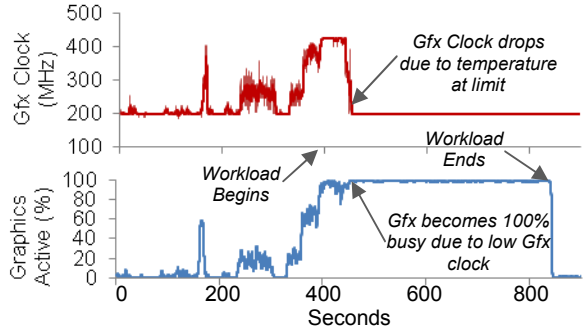

Fig. 1 Graphics Clock w/o GEAPM – 3DMark11

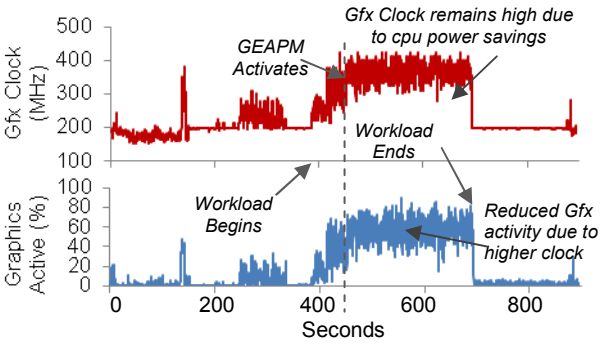

Fig. 2 Graphics Clock with GEAPM – 3DMark11

The workload begins near the 400 second mark. The power manager responds by raising graphics clock to its maximum (400MHz) since the system is not limited by temperature or power. About 40 seconds later, the GPU reaches maximum temperature, causing a frequency reduction to the minimum (200MHz). Figure 2 depicts the same workload, but with the GEAPM feature limiting CPU power when graphics activity is above a specified threshold. The reduced CPU power consumption allows the GPU to reach a higher average frequency while not starving the GPU for draw requests from the CPU.

B. CBB and MBB

The CBB and MBB features improve performance of CPU-centric workloads. Similar to GEAPM, they manage the balance between various entities in the SOC. CBB increases CPU performance by shifting power from the memory subsystem to the CPU in core-bound workloads. It takes advantage of certain workloads that have little dependence on the of the memory subsystem (DRAM). A typical example would be an application that has a working set that fits completely within the on-chip cache. Such workloads are considered "core-bound" since their performance is determined overwhelmingly by core microarchitecture and clock frequency. The MBB feature performs a similar function by detecting memory latency-sensitive workloads and shifting power to the memory controller. All of these features shift power from IPs that have less impact on performance to those with more thus providing higher performance in a constrained environment.

B. LEAPM

In some scenarios, shifting power away from an IP may be done simply to save power rather than to increase performance. LEAPM is one such feature. LEAPM works on the premise that some power management decisions can be made using only information local to the IP. A workload that is bottlenecked by something external

to the SOC such as DRAM memory accesses can be detected by tracking internal utilization of the IP[4]. Typically, the utilization of an IP drops when the IP is stalled waiting for access to external memory. When this occurs, increases to the frequency of the stalled IP do not raise the performance of the SOC. Local EAPM detects these cases and reduces the frequency of the stalled IP. This results in reduced power consumption with little to no performance loss. In some cases this approach can actually raise performance. This occurs if the reduced power of the stalled IP also reduces the temperature of the SOC. Any subsequent workloads (or phases of the original workload) that are not stalled can then achieve higher operating frequency since the SOC temperature is reduced. Since these cases are uncommon, LEAPM is classified as a power saving feature. Fig. 3 shows how the CBB, MBB and LEAPM features respond to the major CPU-centric workload types.

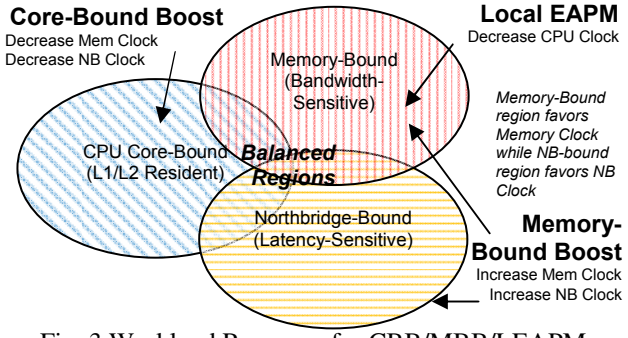

Fig. 3 Workload Response for CBB/MBB/LEAPM

III. RESULTS

This section contains measured results demonstrating the efficacy of the AMD Power Manager. The impact of GEAPM, CBB, MBB and LEAPM are considered in isolation. The benefits are quantified by comparing power and/or performance of the SOC with and without each feature. In all cases an AMD 35Watt 4-Core SOC is used. The details of the SOC are given in Table 2. The workloads chosen for each section are those most relevant for the particular feature.

Table 2 SOC and system Configuration

Model	FX7600P
CPU	4 Steam Roller 1.4-3.6GHz
Graphics SIMDs	8 Volcanic Islands 248-757MHz
Memory	8GB Dual Channel DDR3-1866
Thermal Design Power	35W
Socket	FP3 Mobile
Platform	AMD 35W Reference
Operating System	Windows 8

A. GEAPM

Table 3 presents performance results for a range of graphics-centric workloads. CPU-centric workloads are not presented since the feature is only activated for graphics workloads. The workloads have a wide range of benefit from GEAPM. The best case workloads such as those listed between Civilization 5 and Dirt Showdown have high power consumption in the gpu, yet little performance dependence on the CPU. This typically occurs for high complexity graphics applications with low frame-rates. The CPU performance demand correlates strongly with the frame rate of the application rather than the complexity of the graphics task. In these cases, GEAPM reduces the power and frequency of the CPU to maintain a balanced system. The workloads with little or no benefit have the opposite characteristic. Alien Vs Predator is largely memory-bound and hence does not benefit from increased CPU or GPU power allocation. The remaining workloads either have high frame rates or do not have enough graphics activity to engage the GEAPM feature.

Table 3 – GEAPM Uplift for Graphics Workloads

Workload	Performance
Civilization5_Mobile	76%
Crysis2_Mobile_DX11	42%
Resident Evil5_Mobile_DX11	41%
BiosShock Infinite_Low DX11	34%
Batman Arkham City_MobileDX11	23%
Dirt Showdown_Low_DX11	21%
3dMarkVantage_P_Graphics	5%
3DMark11_P_GraphicsScore	1%
Alien Vs Predator_Mobile	0%
Winzip_Lukas Corpus_OpenCLOn	0%
WinZip_Sintel_Trailer_OpenCLOn	0%

A. CBB

The performance impact of CBB is shown in Table 4. The three workloads with greater than 2% improvement represent the best case benefit for a thermally limited scenario. The SOC used in this experiment is primarily limited by CPU die temperature. CBB increases performance by reducing power consumption in the memory subsystem. This cools the CPU thus allowing it to operate at up to 5% higher frequency on average. Applying this approach to a power constrained SOC would likely improve the benefit by at least a factor of two since the CPU would receive a power increase in the exact amount of the memory subsystem power reduction. The thermally constrained cases shown here receive less than 50% of the power savings benefit due to the inefficiency of heat transfer across the SOC.

Table 4

Workload	Performance	Workload	Performance
PovRay	4.3%	WinRar	1.7%
TrueCrypt	2.4%	Cinebench-S	0.4%
Cinebench-M	2.1%	PCMarkHome	-0.2%

A. MBB

In contrast to the CBB feature, MBB shifts power from the CPU to the memory subsystem. Specifically, it is shifted to the northbridge in order to reduce memory access latency. The memory clock is left unchanged since MBB class workloads are primarily limited by latency rather than memory bandwidth. The results in Table 5 represent the performance improvement from increasing the northbridge clock by 25%. The CPU power budget decreases by about half that amount since CPU and northbridge are not strongly thermally coupled and CPU has a much larger power budget. The benefit of MBB increases with the number of threads. Memory controller congestion increases with thread count, which is alleviated by MBB. One exception is bzip2 which shows a 0.7% drop at 4-thread compared to 1-thread. This drop is not statistically significant since it is less than the ±1% run-to-run variation of the workload. The workloads shown in Table 5 are the best-case improvements within SPEC CPU 2006. The workloads not presented have a performance impact less than ±1%.

Table 5

Workload	1-Thread	4-Thread
462.libquantum	8.8%	12.5%
429.mcf	8.3%	9.6%
403.gcc	5.8%	9.2%
471.omnetpp	5.0%	5.2%
483.xalancbmk	2.3%	4.2%
473.astar	2.0%	2.1%
401.bzip2	1.7%	1.0%

A. LEAPM

For LEAPM, Table 6 presents performance and power impacts for SPEC CPU 2006 4-thread. Since the intent is to save power with a minimum impact on performance, the LEAPM feature is configured to only limit CPU frequency when the workload has less than 20% sensitivity to frequency changes. This reduces the power savings potential, but minimizes performance loss. This approach is evident in the performance results that indicate a maximum performance loss of 2.9% and an average of 0.8%. Even using such a conservative limit for performance loss, LEAPM is able to save a large portion of CPU power. On average, 34% of power is saved. The magnitude of power savings is largely dictated by the high frequencies normally achieved under the SPEC CPU 2006 workload. This workload utilizes only the CPUs and memory subsystem. No other SOC IPs, such as graphics, multimedia, audio or storage are used. As a result, the CPU is able to operate at very high frequencies and voltages. At these high frequency and voltage levels, leakage is a large component of power consumption. Even minor reductions in frequency from LEAPM greatly reduce leakage power while only mildly reducing performance.

Table 6 – LEAPM Performance and Power Impacts

Benchmark	Performance Loss	Power Savings
mcf	1.9%	64.8%
soplex	1.5%	61.8%
lbm	-0.3%	60.9%
libquantum	1.9%	56.9%
gcc	1.2%	42.0%
calculix	0.1%	4.7%
hmmer	0.5%	3.6%
povray	0.1%	3.0%
INT-Avg	1.1%	31.3%
FP-Avg	0.6%	35.4%

IV. Conclusion

This paper presents an analysis of recent power management features implemented on AMD SOCs. These features are shown to provide significant performance and performance/Watt improvements by adapting to workloads at runtime. Performance features such as GEAPM, CBB and MBB are shown to improve performance while operating within thermal and power constraints. The LEAPM feature is shown to reduce CPU power consumption with almost no loss in performance.

References

[1] A. Branover, D. Foley and M. Steinman, “AMD Fusion APU: Llano”, IEEE Micro, vol. 32, issue 2, pp 28-37, Apr. 2012.

[2] E. Rotem, A. et al., “Power Management Architecture and the 2nd Generation Intel Core Microarchitecture Formerly Codenamed SandyBridge”, IEEE Micro vol. 32, issue 2, pp 20-27, Apr. 2012.

[3] C. Isci and M. Martonosi, “Runtime Power Monitoring in High-End Processors: Methodology and Empirical Data”, 36th International Symposium on Microarchitecture, pp 93-104, Dec. 2003.

[4] I. Paul, S. Manne, M. Arora, W. L. Bircher and S. Yalamanchili. “Cooperative Boosting: Needy Versus Greedy Power Management”, IEEE/ACM International Symposium on Computer Architecture, Jun. 2013.

[5] P. Dongara, L. Bircher and J. Darilek, “Richland Client APU”, Hot Chips 25, Aug. 2013.

[6] C. Hsu and W. Feng, “Effective Dynamic Voltage Scaling Through CPU-boundedness Detection”, Lecture Notes in Computer Science, vol. 3471, Dec. 2004.