



Rev. 1.1

Data Sheet

Fastrax UC530

This document describes the electrical connectivity and functionality of the Fastrax UC530 OEM GPS Receiver.

May 3, 2012

Fastrax Ltd

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REFERENCES

Ref. #	Publisher; Reference
(1)	Fastrax; NMEA Manual for Fastrax IT500 Series GPS receivers
(2)	Fastrax; Reflow_soldering_profile.pdf

CHANGE LOG

Rev.	Notes	Date
1.0	Initial documentation, draft status	2012-03-29
1.1	Updated Reference Circuit diagrams (added option for future FORCE_ON signal; upgraded Q1) and edited chapter 7.1 accordingly	2012-05-03

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2 Overview

2.1 General

The Fastrax UC530 is an OEM GPS Antenna Module with the Mediatek MT3339 receiver. The module has ultra small form factor 9.6x14 mm, height is 1.95 mm nominal (2.25 mm max) and can be assembled with SMT reflow soldering. The Fastrax UC530 receiver provides extremely low power and very fast TTFF together with weak signal acquisition and tracking capability to meet even the most stringent performance expectations.

The UC530 provides complete signal processing from embedded antenna to host port UART and location data output is in NMEA protocol. The module requires a main and a backup power supply. The host port is configurable to UART during power up. Host data and I/O signal levels are 2.8V CMOS compatible and inputs are 3.6V tolerable.

The UC530 supports a new feature called AlwaysLocate™, which is an intelligent controller of the UC530 power saving mode. Depending on the environment and motion conditions, the module can adaptively adjust the navigation activity in order to achieve a balance in positioning accuracy, fix rate and power consumption; typical power consumption varies between 2... 8 mW.

The module is also optionally self-assisted since the EASY™ (Embedded Assist System) ephemeris extension is embedded in the software without any resources required from the host. The EASY™ data is stored on internal flash memory and allows fast TTFF typ. 3 seconds over 3 days. Also EPO™ (Extended Prediction Orbit) server generated extended ephemeris input is also supported, which allows fast TTFF 10 seconds typ. over 7/14 days.

The UC530 contains also an AIC (Active Interference Cancellation), which provides state-of-art narrow band (CW) interference and jamming elimination up to 12 CW jammers < -80dBm.

The module also supports a logging feature called LOCUS, which enables automatic logging of position data to internal flash memory. The logging capacity is >16 hrs typ. @ 15 sec storage interval.

The UC530 module supports also an external active antenna connectivity with excellent out-of-band blocking rejection and which provides also 3V antenna bias supply and automatic RF signal path switching.

This document describes the electrical connectivity and main functionality of the Fastrax UC530 OEM GPS Receiver module.

Time to First Fix, hot acq.	1 s typ. (note 1)
Supply voltage, main VDD	+3.0 ... +4.3 V
Supply voltage, backup VDD_B	+2.0 ... +4.3 V
Power consumption, Full Power	45 mW typ. @ 3.3 V (note 2)
Power consumption, AlwaysLocate™	4 mW typ. @ 3.3 V
Power consumption, Backup state	15 µW typ. @ 3.0 V
Optional External RF amplifier net gain range	+10... +30 dB
Storage temperature	-40°C...+85°C
Operating temperature	-40°C...+85°C (note 3)
Host port configuration	UART
Host port protocol	NMEA-0183 rev. 3.01
Serial data format (UART)	8 bits, no parity, 1 stop bit
Serial data speed (UART)	9600 baud (configurable 4,800... 921,600 baud)
PPS output	100 ms high pulse, rising edge +/-1 µs @ full second GPS epoch

Note 1: With nominal GPS signal levels -130dBm.

Note 2: @ 1Hz navigation, <12 GPS satellites in track, SBAS disabled, average over 24h

Note 3: Operation in the temperature range -40°C... -30°C is allowed but Time-to-First-Fix performance and tracking sensitivity may be degraded.

3 Operation

3.1 Operating Modes

After power up the UC530 module boots from the internal ROM to Navigation Mode. Modes of operation:

- Navigation Mode (Full Power)
 - Power management system modes
- Standby Mode
- Backup State/Mode
- Reset State

3.2 Full Power Mode

The module will enter Full Power (aka Navigation Mode) after first power up with factory configuration settings. Power consumption will vary depending on the amount of satellite acquisitions and number of satellites in track. This Mode is also referenced as *Full On*, *Full Power* or *Navigation Mode*.

Navigation is available and any configuration settings are valid as long as the main VDD and backup VDD_B power supplies are active. When the main VDD and backup VDD_B supply is powered off, settings are reset to factory configuration and receiver performs a cold start on next power up.

Suggestion is to keep the backup supply VDD_B active all the time in order to sustain on time, position and ephemeris in the backup RTC and RAM. The main VDD supply can be used to control the module activity, i.e. when VDD is switched off, the module operation is stopped.

Navigation fix rate can be configured by a NMEA command, see chapter 0. Note that baud rate must be set high enough or message payload low enough in order to pass through all messages pending.

3.2.1 Host port configuration

Default host port is configured to UART Port 0 by keeping GPIO9 and GPIO10 floating (not connected) during power up. UART Port1 is reserved for DGPS/RTCM protocol.

Default protocol for host communication is NMEA at 9600 baud. Details on NMEA protocol can be found in NMEA manual, ref (1). Default NMEA message output configuration: \$GPGGA, \$GPGSA, \$GPGSV, \$GPRMC and \$GPVTG rate every second. The module supports also proprietary \$PMTK input commands, see ref (1). The message payload consists of \$PMTK<cmd_id>,<data_field(s)>*<chk_sum><CR><LF>. Sample command: \$PMTK000*32<CR><LF>. For clarity <CR><LF> are not displayed in the following example messages but should be added to the payload at host.

3.3 Power Management Modes

The UC530 module supports also low power operating modes for reduced power consumption:

1. Standby Mode: In this Mode the receiver stops navigation and internal processor enters standby state; current drain at main supply VDD is reduced to 200 μ A typ. Standby Mode is entered by sending NMEA command: \$PMTK161,0*28. Host can wake up the module from Standby Mode to Full Power Mode by sending any byte via host port.
2. Backup Mode: In this mode the receiver is configured to enter autonomously to Backup State; the main power supply VDD is controlled on/off externally by a power switch that is controlled by the TIMER signal output, see reference circuit in chapter 7.1. In this mode the receiver stays in Backup state (backup supply VDD_B active) while VDD supply is switched off. Backup Mode is entered by sending NMEA command: \$PMTK225,4*1C. Host can wake up the module by switching on the VDD supply e.g. via host control signal GPS_ON signal toggle to high state ($t > 500ms$), see reference circuit diagram in chapter 7.1.

3. Periodic Mode: this mode allows autonomous power on/off with reduced fix rate to reduce average power consumption, see figure below; the main power supply VDD is controlled on/off externally by a power switch that is controlled by the TIMER signal output, see reference circuit in chapter 7.1. Periodic Mode is entered by sending the following NMEA command:
`$PMTK225,<Type>,<Run_time>,<Sleep_time>,<2nd_run_time>,<2nd_sleep_time>*<checksum><CR><LF>`,
 where **Type**=1 for Periodic Backup Mode; **Run_time** = Full Power period (ms); **Sleep_time** = Standby/Backup period (ms); **2nd_run_time** = Full Power period (ms) for extended acquisition in case GPS acquisition fails during the **Run_time**; **2nd_sleep_time** = Standby/Backup period (ms) for extended sleep in case GPS acquisition fails during the **Run_time**. Example: `$PMTK225,1,3000,12000,18000,72000*16` for periodic Mode with 3 sec Navigation and 12 sec sleep in Backup state. Acknowledge response for the command is `$PMTK001,225,3*35`. The module can exit Periodic Mode by command `$PMTK225,0*2B` sent just after the module has been wake up from previous sleep cycle.

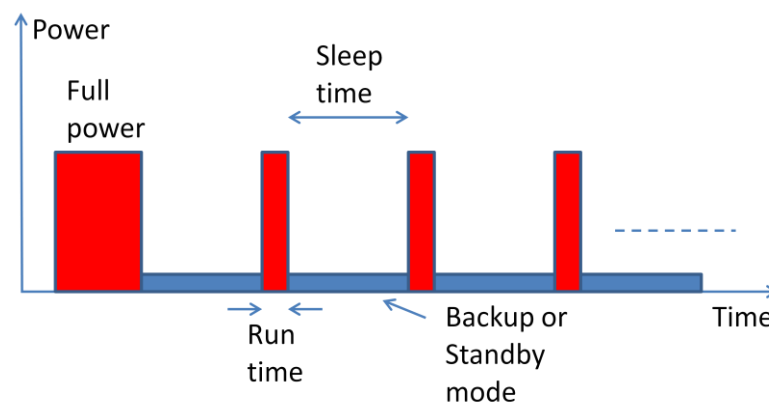


Figure 2 Periodic Mode

4. AlwaysLocate™ is an intelligent controller of the Periodic Mode; the main power supply VDD is controlled on/off externally by a power switch that is controlled by the TIMER signal output, see reference circuit in chapter 7.1. Depending on the environment and motion conditions, the module can autonomously and adaptively adjust the parameters of the Periodic Mode, e.g. on/off ratio and fix rate to achieve a balance in positioning accuracy and power consumption, see figure below. The average power drain can vary based on conditions; typical average power is 3 mW. Associated profiles are: High and Low Speed, Walking, Outdoor Static and Indoor. AlwaysLocate™ Mode is entered by sending the following NMEA command: `$PMTK225,<Mode>*<checksum><CR><LF>`, where **Mode**=9 for AlwaysLocate™ in Backup Mode. Example: `$PMTK225,9*22`. Acknowledge response for the command is `$PMTK001,225,3*35`. The module can exit AlwaysLocate™ Mode by command `$PMTK225,0*2B` sent just after the module has been wake up from previous sleep cycle.

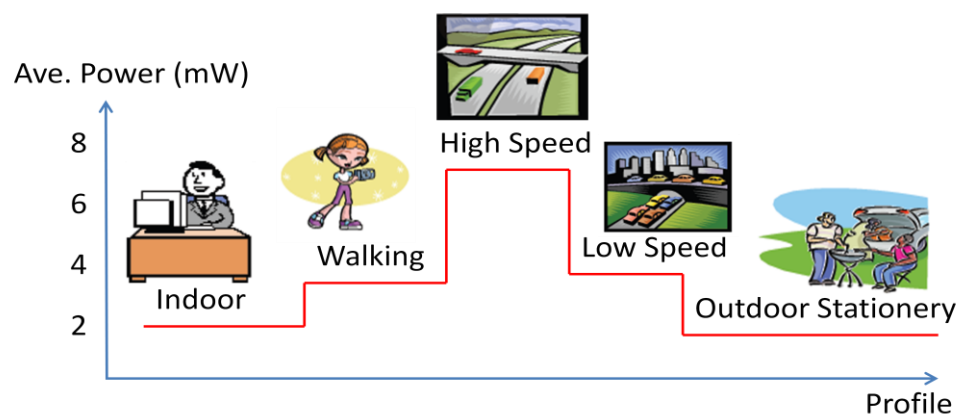


Figure 3 AlwaysLocate™ Mode

Note that when using an external VDD power switch in low power modes the host needs to enable GPS operation after initial power up by controlling GPS_ON signal (see reference circuit in chapter 7.1) to high state. The module can control the VDD power switch autonomously via TIMER signal only after the UC530 is set to Periodic, Backup or to AlwaysLocate™ mode by a NMEA command.

Note also that first fix position accuracy can be somewhat degraded in Power Management Modes when compared to Full Power operation. User can improve the position accuracy by taking the 2nd or 3rd fix after waking up.

User can exit low power Modes 3... 4 to Full Power by sending NMEA command \$PMTK,225,0*2B just after the module has woke up from previous sleep cycle.

3.4 Self-Assistance EASY™ usage

The UC530 module self-assistance uses EASY™ (Embedded Assist System) ephemeris extension, which is embedded in the software without any resources required from the host. The EASY™ data is stored on internal flash memory and allows fast TTFF typ. 3 seconds over 3 days and is enabled by default.

Allow the receiver to navigate at least for 5 minutes with good GPS satellite visibility in order to collect broadcast ephemeris and to process necessary information.

3.5 Server Assistance EPO™ usage

The UC530 module supports also input from server generated EPO™ file (Extended Prediction Orbit, i.e. ephemeris extension), which can be transferred from a FTP server and allows fast TTFF typ. 10 seconds over 7/14 days. Contact Fastrax support for details on EPO FTP server usage.

3.6 Logger LOCUS usage

The UC530 module supports embedded logger function called LOCUS and when enabled it can log position information to internal flash memory; default log interval is 15 seconds that provides typically > 16 h log capacity. The LOCUS can be enabled by NMEA command \$PMTK185,0*22. Contact Fastrax support for details on Locus usage.

3.7 DGPS usage

By default DGPS navigation mode is disabled. The host may enable DGPS/SBAS navigation mode by sending commands 'Enable Search of SBAS Satellites' \$PMTK313,1*2E followed by 'Set DGPS Data Source to SBAS' \$PMTK301,2*2E. The search for suitable SBAS satellite signal is automatic.

The host may either enable DGPS/RTCM navigation mode by sending command 'Set DGPS Data Source to RTCM' \$PMTK301,1*2D. The UART Port1 is used for RTCM message input at 9600 baud.

Note that DGPS usage is only supported at 1Hz navigation rate in Full Power mode. Note also that acquiring necessary DGPS correction parameters may take up to 1 minute prior DGPS fix status is achieved, which is indicated in the \$GPGGA message, Fix Valid Indicator. Note also that DGPS corrections do not provide corrections against multipath errors that are local; thus accuracy is not necessary improved in urban environments.

3.8 Standby Mode

Standby Mode means a low quiescent (200 µA typ. at VDD) power state where receiver operation is stopped; both the main supply VDD and the backup supply VDD_B are powered on.

The Standby Mode is entered by NMEA command \$PMTK161, see chapter 3.3. Waking up from Standby state to Full Power is controlled by host by sending any byte via host communication port.

After waking up the receiver will use all internal aiding like GPS time, Ephemeris, Last Position etc. resulting to a fastest possible TTFF in either Hot or Warm start Modes.

3.9 Backup State

Backup State means a low quiescent (5 μ A typ. at VDD_B) power state where receiver operation is stopped; only the backup supply VDD_B is powered on while the main supply VDD is switched off by host or by UC530, see also chapter 3.3. Waking up from Backup State to Full Power is controlled by host by switching on the VDD supply.

In optional Autonomous Backup Mode the UC530 module controls the VDD switching autonomously via the TIMER signal, see reference circuit in chapter 7.1 by sending NMEA command \$PMTK225,4, see chapter 3.3. The Autonomous Backup Mode is thus similar to Backup State but with autonomous control of external VDD power switch.

Note that when using an external VDD power switch in low power modes the host needs to enable GPS operation after initial power up by controlling GPS_ON signal (see reference circuit in chapter 7.1) to high state. The module can control the VDD power switch autonomously via TIMER signal only after the UC530 is set to Periodic, Backup or to AlwaysLocate™ mode by a NMEA command.

After waking up the receiver will use all internal aiding like GPS time, Ephemeris, Last Position etc. resulting to a fastest possible TTFF in either Hot or Warm start modes.

During Autonomous Backup Mode or Backup State the I/O block is powered off; thus suggestion is that host shall force it's outputs to low state or to high-Z state during Backup state to minimize small leakage currents (<10 μ A typ.) at receiver's input signals.

3.10 Reset State

Reset State stops all internal operations and it is entered internally at power up after which internal reset state is relaxed when 167 ms (typ.) has elapsed and module operations begin. The power on reset level is 2.7 +/- 0.1 V at VDD. Host can also override Reset State via RESET_N input, which is low state active. Normally external reset override is not required and RESET_N signal can be left floating (not connected).

4 Connectivity

4.1 Signal Assignments

The I/O signals are available as soldering (castellated) pads on the bottom side of the module. These pads are also used to attach the module on the motherboard. All digital I/O signal levels are 2.8V CMOS compatible (except TIMER and 32K/DR_INT that are 1.2V CMOS) and inputs are 3.6V tolerable. All unconnected I/O signals can be left unconnected when not used, unless instructed to use external pull up/down resistor.

Table 2 Signal assignment

Contact	Signal	I/O type Full Power, Standby	I/O type Backup	I/O type Reset	Signal description
1	32K/DR_INT	C1V2,B	C1V2,B	C1V2,B	- Wake up interrupt (DR_INT default), PD. <i>Can be left unconnected when not used.</i> - Optionally 32678 Hz RTC clock output
2	UI_FIX	C,B	HZ	C,B	- Fix indicator output (default). <i>Can be left unconnected when not used.</i> - GPIO6
3	TX1	C,B	HZ	C,B	UART Port1 TX data transmit. <i>Can be left unconnected when not used.</i>
4	GND	G	G	G	Ground
5	GND	G	G	G	Ground
6	RX1	C,B	HZ	C,B	UART Port1 RX data receive (RTCM), PU. <i>Can be left unconnected when not used.</i>
7	EINT1	C,B	HZ	C,B	- Standby Mode control input (not supported). <i>Can be left unconnected when not used.</i> - GPIO13
8	VDD_B	P,I	P,I	P,I	Backup power input +3.3 V nom. <i>De-couple externally with e.g. 1 uF low ESR ceramic capacitor.</i>
9	VDD	P,I	-	P,I	Power supply input +3.3 V nom. <i>De-couple externally with e.g. 4.7 uF low ESR ceramic capacitor.</i>
10	GND	G	G	G	Ground
11	GND	G	G	G	Ground
12	GND	G	G	G	Ground
13	GND	G	G	G	Ground
14	GND	G	G	G	Ground
15	GND	G	G	G	Ground
16	ANT	A,O	-	-	Embedded Antenna Output (50 ohm)
17	RF_IN	A,I	-	-	Antenna Signal Input (50 ohm)
18	GND	G	G	G	Ground
19	GND	G	G	G	Ground
20	GPIO9	C,B	HZ	C,B	<i>Reserved for future usage, leave floating.</i>
21	GND	G	G	G	Ground
22	GND	G	G	G	Ground
23	RESET_N	C,I,PU	C,I,PU	C,I,PU	External reset input, active low. <i>Can be left unconnected when not used.</i>
24	GPIO10	C,B	HZ	C,B	<i>Reserved for future usage, leave floating.</i>

Contact	Signal	I/O type Full Power, Standby	I/O type Backup	I/O type Reset	Signal description
25	TX0	C,B	HZ	C,B	UART Port0 TX data transmit (NMEA)
26	RX0	C,B	HZ	C,B	UART Port0 RX data receive (NMEA), PU. <i>Can be left unconnected when not used.</i>
27	GND	G	G	G	Ground
28	TIMER	C1V2,OD	C1V2,OD	C1V2,OD	Power control output (open drain) used to control external VDD switch. <i>When not used connect to Ground externally.</i>
29	PPS	C,B	HZ	C,B	- PPS Time Mark output signal (default) - GPIO7
30	WAKEUP	P,O	-	P,O	2.8V power output for optional control of external LNA bias switch, active high = LNA bias on. Max load current drain 2 mA. <i>Can be left unconnected when not used.</i>
31	GND	G	G	G	Ground

Note (a): Pull Up/down resistor present only shortly after power up.

Legend: A=Analogue, B=Bidirectional, C=CMOS 2.8 V, C1V2=CMOS 1.2 V, G=Ground, HZ=High Impedance, I=Input, O=Output, OD=Output Open Drain, P=Power, PU=Internal Pull Up resistor, PD=Internal Pull Down resistor. Note that with Birectional I/O the firmware has control for input vs. output I/O type depending on the firmware function.

4.2 Power supply

The Fastrax UC530 module requires two separate power supplies: VDD_B for non-volatile back up block (RTC/Backup RAM) and the VDD for digital parts and I/O. VDD can be switched off when navigation is not needed but if possible keep the backup supply VDD_B active all the time in order to keep the non-volatile RTC & RAM active for fastest possible TTFF.

Main power supply VDD current varies according to the VDD level, to the processor load, to the number of satellites in track and to the rate of satellite re-acquisition. Typical VDD peak current is 31 mA (typ.) during GPS acquisition after power up and typical average 15 mA @ VDD 3.3 V over 24 h during good sky visibility. Note that average current drain will also increase during following features:

- 15 mA average (typ.) @1 Hz navigation, <12 signals in track, good sky visibility
- +2 mA @ tracking at least 12 satellites and over (GPS and SBAS)
- +4 mA @ during first 12.5 minutes after cold and warm start due to receiving broadcast almanac data
- +2.5 mA @ 5 Hz navigation rate
- +4 mA @ 10 Hz navigation rate
- +1 mA @ Jammer Remover AIC usage

The following picture shows average current and power drain variation vs. VDD supply voltage.

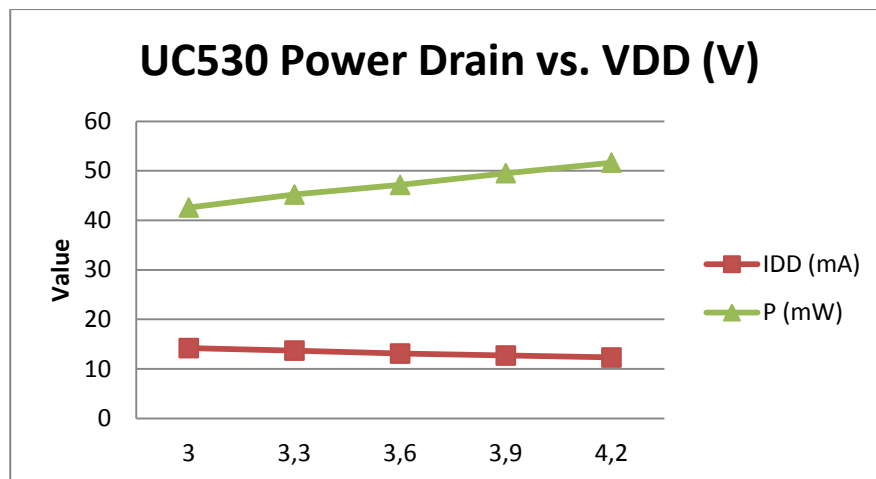


Figure 4 UC530 Power Drain (typ.) vs. VDD (V) @ 1 Hz, <12 signals

Backup supply VDD_B draws 5 μ A typ. current in Backup State. During Full Power Mode VDD_B current typically peaks up to 140 μ A and is on the average 90 μ A.

NOTE

Backup supply VDD_B has to be active whenever Main supply VDD is active.

By-pass the VDD supply input by a low ESR ceramic de-coupling capacitor (e.g. 4.7 μ F) placed nearby VDD pin to ensure low ripple voltage at VDD.

NOTE

De-couple the VDD input externally with e.g. 4.7 μ F low ESR ceramic capacitor connected to GND. The module has also internal a low ESR (\sim 0.01 ohm) by-pass capacitor at VDD supply input. Ensure that the external regulator providing VDD and VDD_B supply is compatible with low ESR load capacitors.

4.3 Host port configuration

Default host port is UART and selected by leaving GPIO 9 and 10 signals floating (not connected) after power up. Other host port configurations are not supported.

4.4 Host port UART

UART Port 0 is normally used for GPS data reports and receiver control. Serial data rates are configurable from 4,800 baud to 921,600 baud by \$PMTK251,<baud>*<checksum><CR><LF> command. Default baud rate is 115200 baud; protocol is NMEA. RX signal is pulled up internally and can be left floating (not connected) when not used.

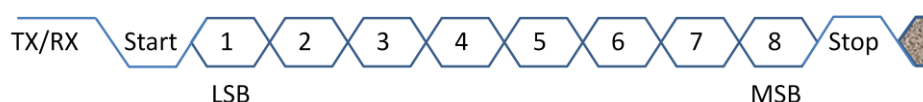


Figure 5 UART timing

Secondary UART Port 1 is configured to RTCM differential GPS data input at 9600 baud.

4.5 Reset input

The RESET_N (active low) signal provides external override of the internally generated power up/down reset. Normally external control of RESET_N is not necessary.

When RESET_N signal is used, it will force volatile RAM data loss. Note that Non-Volatile Backup RAM content is not cleared and thus fast TTFF is possible. The input has internal pull up resistor 75 kohm typ. and the signal can be left floating (not connected) if not used. Non-Volatile Backup RAM content can be cleared with NMEA command 'Factory Reset' \$PMTK104*37<CR><LF>.

4.6 Timer output

The TIMER signal provides output (Open Drain) that can be used to switch off the main VDD supply voltage by controlling autonomously an external power switch in Backup mode, see reference application circuit diagram in chapter 7.1.

When TIMER signal is used, pull it high by using an external resistor e.g. 1 Mohm. The signal is active high, i.e. VDD is active; and when pulled low by the UC530, the VDD shall be switched off.

4.7 Antenna input

The module has an embedded GPS antenna and the signal is further amplified by internal Low Noise Amplifier (LNA), which is available at ANT output. The antenna signal ANT shall be connected externally to RF_IN Antenna Input signal via a short trace between pads. The ANT signal is internally AC-coupled; max DC voltage at ANT signal is +3.6 V. Note that RF_IN signal provides DC-path to ground and thus do not apply any bias voltage to RF_IN signal; max DC voltages at RF_IN signal is 0V and thus use an external series DC-block capacitor when needed.

The RF input signal path contains first a SAW band-pass filter before LNA, which provides excellent protection against out-of-band GPS blocking caused by possible near-by wireless transmitters.

4.8 External GPS antenna connectivity

The customer may use an external active GPS antenna connected via an external RF-switch. It is suggested that the active antenna has a net gain *including cable loss* in the range from +10 dB to +30 dB. Specified sensitivity is measured with external low noise ($NF \leq 1\text{dB}$, $G \geq 15\text{dB}$) amplifier.

An active antenna requires an external antenna switch in order to select path between RF_IN input and external GPS antenna signal. For reference see e.g. the application circuit diagram in chapter 7.2 Fastrax support can also provide other antenna switch reference circuits using discrete components.

The switch shall detect external active antenna presence for switching antenna signal path to external antenna by using e.g. the active antenna bias current detection. Second option is to use a suitable RF-connector with build-in switching operation. The external antenna switch must also provide a bias supply to the external active antenna and suggestion is also to add an external short circuit and ESD protection for antenna signal.

When the module is in Standby or Backup state, the antenna switch and bias can be switched off externally by using WAKEUP signal output, see e.g. Application Circuit Diagram.

4.8.1 Jamming Remover

Jamming Remover is an embedded HW block called AIC (Active Interference Cancellation) that tracks and removes up to 12 pcs CW (Carrier Wave) type signals up to -80 dBm (total power signal levels). By default the AIC is disabled and usage requires an NMEA command \$PMTK286,1*23<CR><LF> to enable.

Jamming Remover can be used for solving EMI problems in the customer's system and it is effective against e.g. narrow band clock harmonics. When enabled, Jammer Remover will increase current drain by about 1 mA and

impact on GPS performance is low at modest jamming levels; however at high jammer levels -90... -80 dBm the RF signal sampling (ADC) starts to get saturated after which GPS signal levels start to reduce.

Note that Jamming Remover is not effective against wide band noise (e.g. from host CPU memory bus), which cannot be separated from thermal noise floor. Wide band Jamming signal increases effective noise floor and eventually reduces GPS signal levels.

4.9 PPS output

The PPS output signal provides pulse-per-second output pulse signal for timing purposes. Pulse length (high state) is 100 ms and it has 1us accuracy synchronized at rising edge to full UTC second with nominal GPS signal levels. The PPS will output PPS after a few seconds from first fix after the fix epoch is synchronized to full second.

The PPS output is valid when navigation is valid and will also continue 'freewheel' after valid fix is lost by a certain navigation DR timeout, typ. 10 seconds. User can also enable NMEA \$GPZDA message that is sent right after the PPS pulse just sent.

4.10 Wakeup output

The WAKEUP output voltage provides indication to host that the module is active. Polarity is active high = module active.

WAKEUP output is intended to drive only CMOS inputs; do not load WAKEUP signal with current exceeding 2mA. Only loads with steady state current drain is allowed (i.e. loads with ripple currents are prohibited).

NOTE

Do not load WAKEUP output with current exceeding 2mA. Only loads with steady state current drain is allowed, i.e. loads with ripple currents are prohibited.

4.11 Interrupt input EINT1

The default EINT1 function is Standby mode control but the function is not supported; leave signal floating (not connected).

4.12 UI_FIX signal

The default UI_FIX function is valid fix indicator output. Without a valid fix the signal is at low state; during valid fix condition the signal outputs 1 s pulses every 2 seconds.

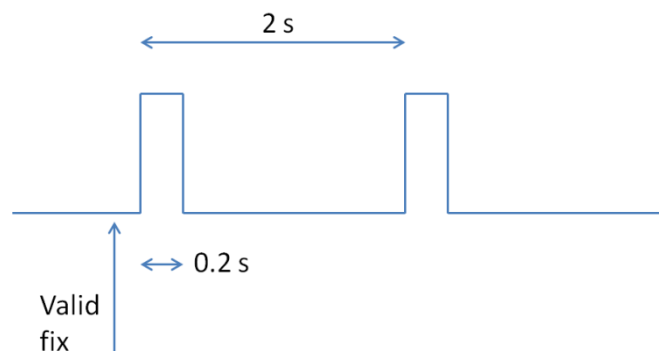


Figure 6 UI_FIX valid fix indicator timing

4.13 32K/DR_INT signal

The default 32K/DR_INT function is wake up interrupting input. The module is able to wake up from Standby and Backup modes to Full Power mode when the signal is toggled by low-high-low state with >10 ms pulse length. While in the DR_INT function the input is pulled low with an internal pull down resistor and the input can be left floating (not connected).

Optionally the signal can be configured to 32768 Hz RTC clock signal output with a custom firmware. The 32K/DR_INT signal has CMOS 1.2V logic levels and when input, the signal is +3.6V tolerable.

4.14 Mechanical Dimensions

Module size is square 9.6 mm (width), 14.0 mm (length) and 1.95 mm (height, 2.25 mm max). General tolerance is ± 0.3 mm. Note pin 1 polarity mark on the corner on the shield.

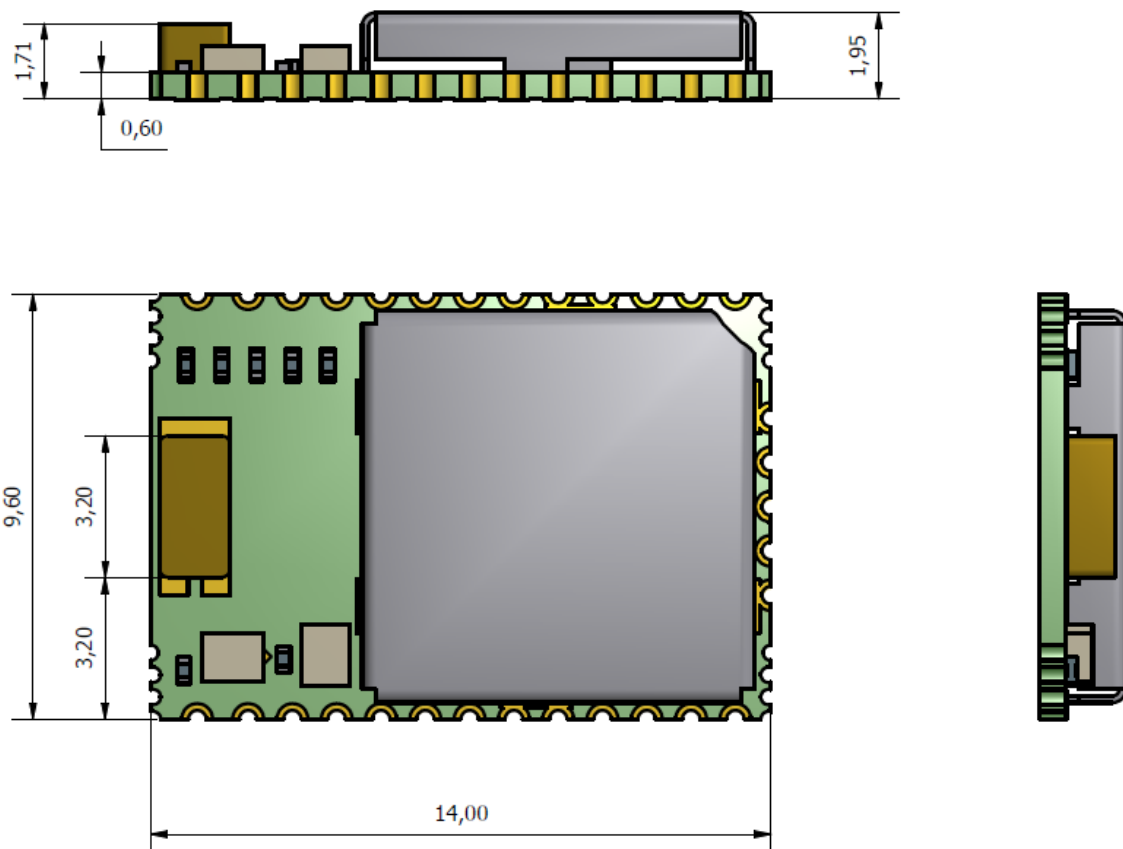


Figure 7 Mechanical Dimensions

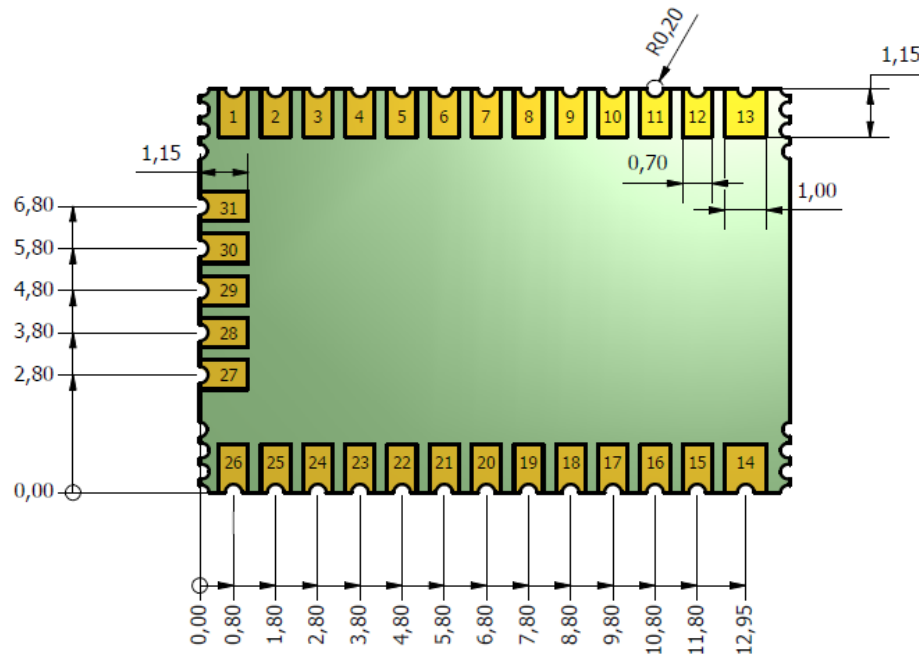


Figure 8 Pin numbering and dimensions, bottom view

4.15 Suggested pad layout

Suggested paste mask openings equal to pad layout. Note the keepout (void area) 4.8x7.2mm for copper & trace & components for all layers under the embedded antenna.

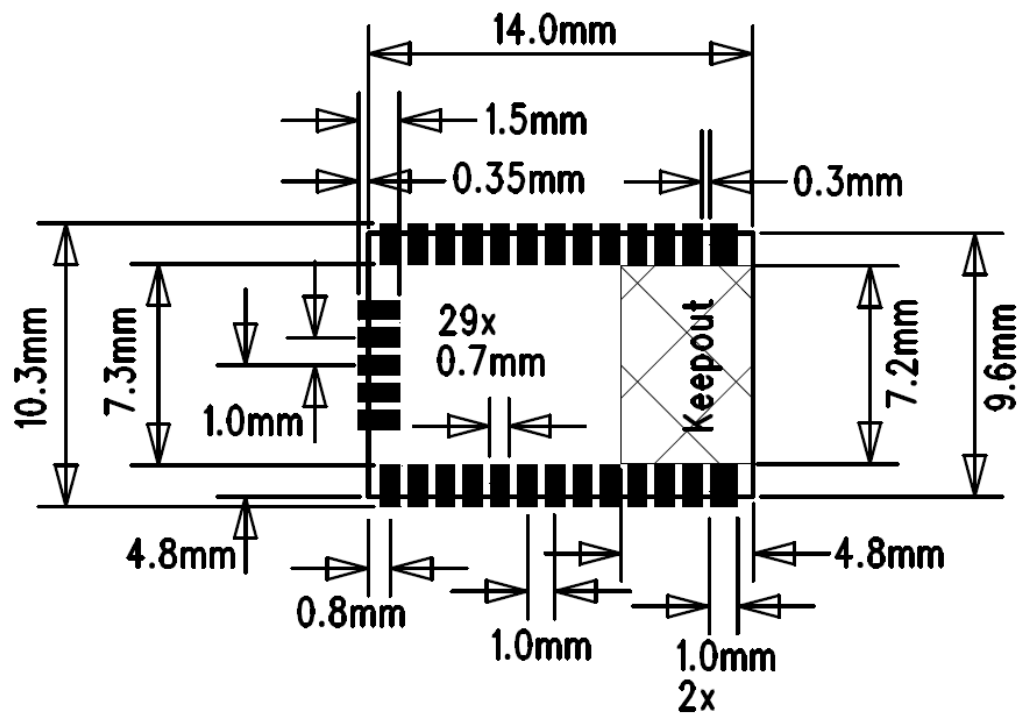


Figure 9 Suggested pad layout and occupied area, top view

5 Electrical Specifications

5.1 Absolute Maximum Ratings

Stressing the device beyond the Absolute Maximum Ratings may cause permanent damage. Operation beyond the DC Electrical Specifications is not recommended and extended exposure beyond the Recommended Operating Conditions can affect device reliability.

Table 3 Absolute Maximum Ratings

Symbol	Parameter	Min	Max	Unit
T_{AMB}	Operating and storage temperature	-40	+85	°C
P_{DIS}	Power dissipation	-	200	mW
VDD	Supply voltage input	-0.3	+4.3	V
VDD_B	Supply voltage input, Backup	-0.3	+4.3	V
V_{ANT}	DC Voltage at ANT output signal	-0.5	+3.6	V
V_{RF_IN}	DC Voltage at RF_IN input signal	-	0	V
$V_{IO}(ESD)$	I/O ESD voltage	-1000	+1000	V
P_{RF}	RF_IN input power (in band 1575 +/- 10 MHz)	-	-40	dBm
P_{RF}	RF_IN input power (out of band <1460 MHz or >1710 MHz)	-	+15	dBm

NOTE

Note that module is Electrostatic Sensitive Device (ESD).



5.2 DC Electrical specifications

Operating conditions are $T_{AMB} = +25^{\circ}\text{C}$, VDD = +3.3 V and VDD_B = +3.0 V unless stated otherwise; tracking less than 12 satellites, navigation at 1 Hz.

Table 4 DC Electrical characteristics

Symbol	Parameter	Min	Typ	Max	Unit
T_{AMB}	Operating temperature (note 1)	-40	+25	+85	°C
VDD	Supply voltage input	+3.0	+3.3	+4.3	V
VDD_B	Supply voltage input, Backup	+2.0	+3.0	+4.3	V
$I_{VDD}(\text{peak})$	Supply current, peak acq.		25		mA
$I_{VDD}(\text{ave})$	Supply current average, tracking		13.6		mA
$I_{VDD_B}(\text{peak})$	Supply current Backup, peak		140		μA
$I_{VDD_B}(\text{ave})$	Supply current Backup, average		90		μA
I_{VDD_B}	Supply current, Backup state		5		μA
$I_{I(LEAK)}$	Leakage current, Digital Input	-10		+10	μA
V_{OL}	Low level output voltage, I_{OL} 8 mA	-0.3		+0.4	V
V_{OH}	High level output voltage, I_{OH} 8 mA	+2.4	+2.8	+3.1	V
V_{IL}	Low level input voltage	-0.3		+0.8	V
V_{IH}	High level input voltage	+2.0		+3.6	V
R_{PU}	Internal Pull Up resistor	40	75	190	kohm

R _{PD}	Internal Pull Down resistor	40	75	190	kohm
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Note 1: Operation in the temperature range -40°C... -30°C is allowed but Time-to-First-Fix performance and tracking sensitivity may be degraded.

Table 5 DC Electrical characteristics, 1.2 V CMOS domain (TIMER & 32K/DR_INT)

Symbol	Parameter	Min	Typ	Max	Unit
V _{OL}	Low level output voltage, I _{OL} 0.9 mA			+0.42	V
V _{OH}	High level output voltage, I _{OH} 0.9 mA	+0.78			V
V _{IL}	Low level input voltage	-0.3		+0.54	V
V _{IH}	High level input voltage	+0.66		+3.6	V
R _{PU}	Internal Pull Up resistor	130		560	kohm
R _{PD}	Internal Pull Down resistor	130		560	kohm

5.3 AC Electrical characteristics

Operating conditions are T_{AMB} = +25°C and VDD = +1.8 V unless stated otherwise.

Table 6 AC Electrical characteristics

Symbol	Parameter	Min	Typ	Max	Unit
t _{PPS}	PPS cycle time		1		s
t _{PPS,H}	PPS, high state pulse length		100		ms
Δt _{PPS}	PPS accuracy, rising edge (note 1)	-1		+1	μs
f _{RTC}	RTC output (32K/DR_INT) frequency (note 2)		32768		Hz

Note 1: with nominal GPS signal levels -130dBm.

Note 2: when enabled by I/O configuration.

6 Manufacturing

6.1 Assembly and Soldering

The UC530 module is intended for SMT assembly and soldering in a Pb-free reflow process on the top side of the PCB. Suggested solder paste stencil height is 150µm minimum to ensure sufficient solder volume. If required paste mask pad openings can be increased to ensure proper soldering and solder wetting over pads.

Use pre-heating at 150... 180°C for 60... 120 sec. Suggested peak reflow temperature is 235... 245°C (for SnAg3.0Cu0.5 alloy). Absolute max reflow temperature is 260°C. For details see Fastrax document 'Soldering Profile' ref (7).

Note that module is Electrostatic Sensitive Device (ESD).

NOTE

Note that module is Electrostatic Sensitive Device (ESD).



Avoid also ultrasonic exposure due to internal crystal and SAW components.

The UC530 module meets the requirements of Directive 2002/95/EC of the European Parliament and of the Council on the Restriction of Hazardous Substance (RoHS). For details contact Fastrax support.

6.2 Moisture sensitivity

UC530 module is moisture sensitive at MSL 3 (see the standard IPC/JEDEC J-STD-020C). The module must be stored in the original moisture barrier bag or if the bag is opened, the module must be repacked or stored in a dry cabin (according to the standard IPC/JEDEC J-STD-033B). Factory floor life in humid conditions is 1 week for MSL 3.

Moisture barrier bag self life is 1 year; thus it is suggested to assemble modules prior self life expiration. If the moisture barrier bag self life is exceeded, the modules must be baked prior usage; contact Fastrax support for details.

6.3 Marking

Module marking includes type code, batch code and serial number.

Type code is e.g. **UC530rbbbb** (may vary), where

- **UC530** is module type code for UC530
- **r** is incremental firmware revision (e.g. **C**, may vary)
- **bbbb** is BOM (Bill-of-Materials) revision code (e.g. **4288**, may vary)

Batch code is e.g. **120208** (may vary), where

- **1** is factory code
- **2** is last digit of the year (e.g. 20**12**)
- **02** is month (e.g. February)

- **08** is incremental number of the production batch during the month

Serial number is unique for each module having 10 digits including tester code, last two digits of the year, Julian date code and incremental number.

6.4 Tape and reel

Reel is packed in 500 pcs per reel.

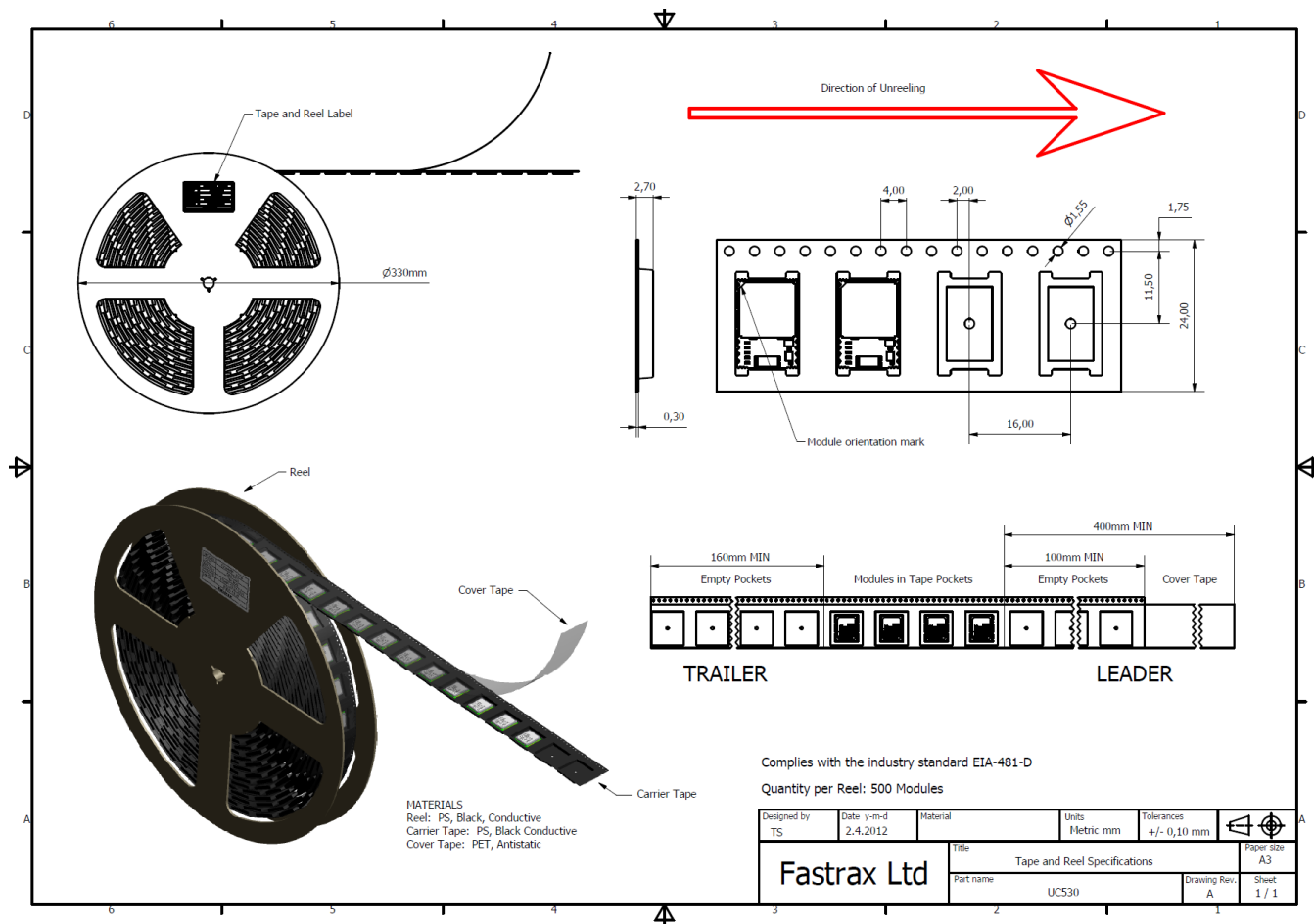


Figure 10 Tape and reel specification

6.5 Environmental Specification

The UC530 module shall be qualified for environmental stresses with the following test series:

Table 7 Environmental tests

Test	Condition	Standard
Temperature Cycle	Test: +85°C (20min) / -40°C (20min), Ramp Slope: 10°C/min, Test Cycles: 300 Cycles	JESD22A104
High Temperature Storage	Temperature +85°C , Test Time: 1,000hr	JESD22A103C
Temperature Humidity Test	Temperature +85°C , 85% R.H., Test Time: 1,000hr	JESD22A101

Vibration Test	10G, 10... 1,000Hz, 1 Octave/min (amplitude 1.0mm max @ <70Hz)	JESD22B103
Shock Test	100G pulse, duration 2ms, 5 Shock 2 directions 3 Axis = 30 Shocks	JESD22B110

7 Reference design

The idea of the reference design is to give a guideline for the applications using the OEM GPS module. In itself it is not a finished product, but an example that performs correctly.

In the following two chapters the reader is exposed to design rules that he should follow, when designing the GPS receiver in to the application. By following the rules one end up having an optimal design with no unexpected behavior caused by the PCB layout itself. In fact these guidelines are quite general in nature, and can be utilized in any PCB design related to RF techniques or to high speed logic.

7.1 Reference circuit diagram

The following picture describes a minimum connectivity for a typical autonomous navigation application. It consists of the UC530 module, which is powered by the main VDD supply (+3.3 V typ.) and backup supply VDD_B (+3.0V typ) powered by battery BT1. The external by-pass capacitor C1 and C2 is used to de-couple the supply inputs placed close to the pin.

Suggestion is to keep the backup supply VDD_B active all the time and host may use the VDD supply to control module activity between Full Power and Backup operation modes. When needed the VDD can be connected directly to a LiPo battery but in this case the backup battery BT1 must be charged from a separate 3V supply.

Embedded Antenna Signal (ANT) must be routed to RF-input (RF_IN) via a short trace between pads 16 and 17.

The host port is configured to UART by keeping GPIO 9 & 10 floating. Serial port TX output is connected to host UART input. RX input connection to host UART output is required when sending commands to UC530. UART signals are decoupled with series resistors R1 and R2 in order to minimize risk for internal EMI.

For optional Backup/Periodic modes of operation the external power switch U1 shall be assembled while omitting by-pass resistor R9 (OR). The U1 power switch shall be controlled autonomously by the TIMER signal from UC530. After the UC530 has been controlled to Autonomous Backup Mode or to Periodic Mode via an NMEA message, the module can control VDD activity autonomously via TIMER signal that has control on the VDD power switch U1. Host can wake up the module by toggling the GPS_ON control signal to high state (e.g. pulse > 0.5 s), which enables the power switch U1 by via diode D2. Resistor R7 (0 ohm) adds an option for future upgrade with FORCE_ON signal in case external power switch can be omitted.

Optional connectivity to host includes PPS, UI_FIX, 32K/DR_INT signals. UART Port 1 RX1 signal can be used optionally as input for RTCM differential GPS messages.

Note that all I/O signal levels are CMOS 2.8V compatible (excluding TIMER and 32K/DR_INT signals that have 1.2 V CMOS domain) and inputs are 3.6 V tolerable.

Some I/O signals have series resistors 47... 220 ohm, which are intended for RF-decoupling purposes to improve rejection to internally generated EMI that may leak to embedded GPS antenna.

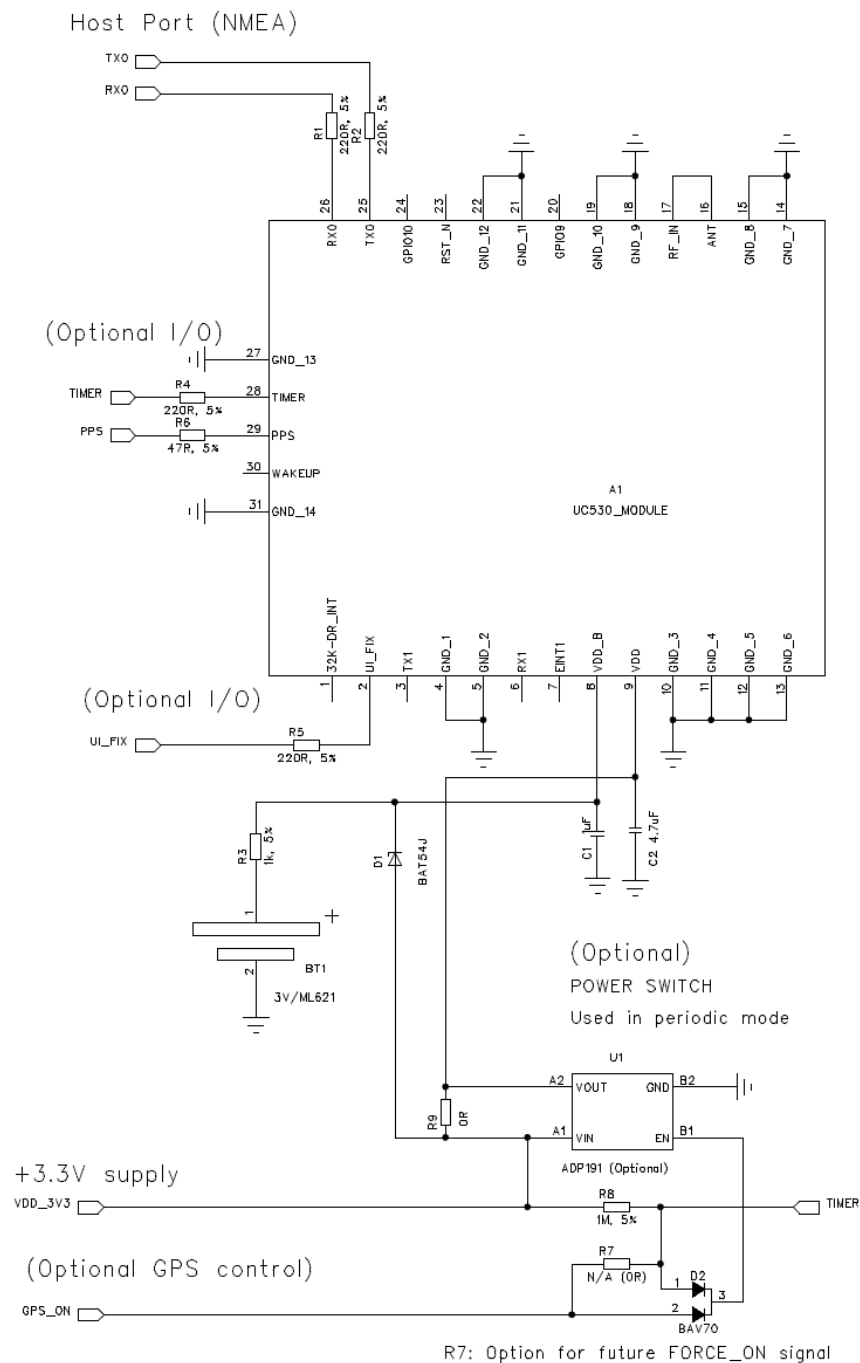


Figure 11 Reference circuit diagram, minimum connectivity

7.2 Reference circuit diagram, external antenna connectivity

The following reference circuit adds external GPS antenna connectivity by using a RF-conductor (e.g. MCX) + Switch combo (e.g. Aliner 31-301AA), which detects the external antenna by the presence of the mating connector plugged and then switching RF signal path from external antenna at J1 to RF_IN.

The TVS diode D1 (e.g. Infineon ESD0P2RF) provides optional protection against static discharge (ESD) at J1. The transistor Q1 provides antenna bias switch function to switch bias voltage off during Standby and Backup modes

and which is controlled by the WAKEUP signal. The Q1 provides also short circuit protection and limits bias current to 50... 60 mA typ.

WAKEUP signal can be used to drive external antenna bias ANT_BIAS (+3.3 V typ.) voltage switch (Q1) during Full Power/Standby/Backup Modes. L1 and C5 provide RF decoupling at VDD_ANT supply.

Keep RF signal traces to J1 short in order to minimize losses and keep transmission line impedance at 50 ohm, see next chapter.

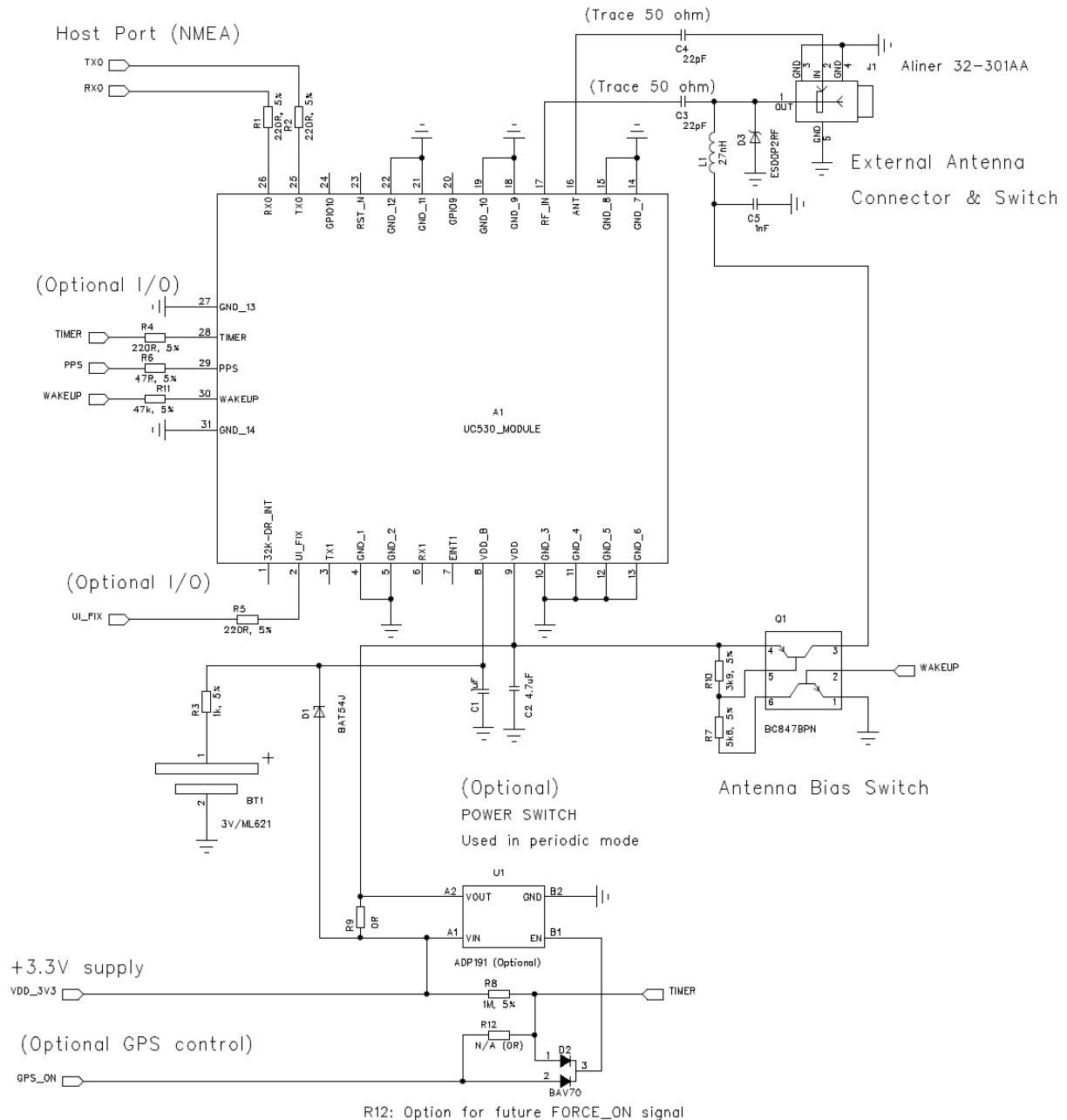


Figure 12 Reference circuit diagram, external antenna connectivity

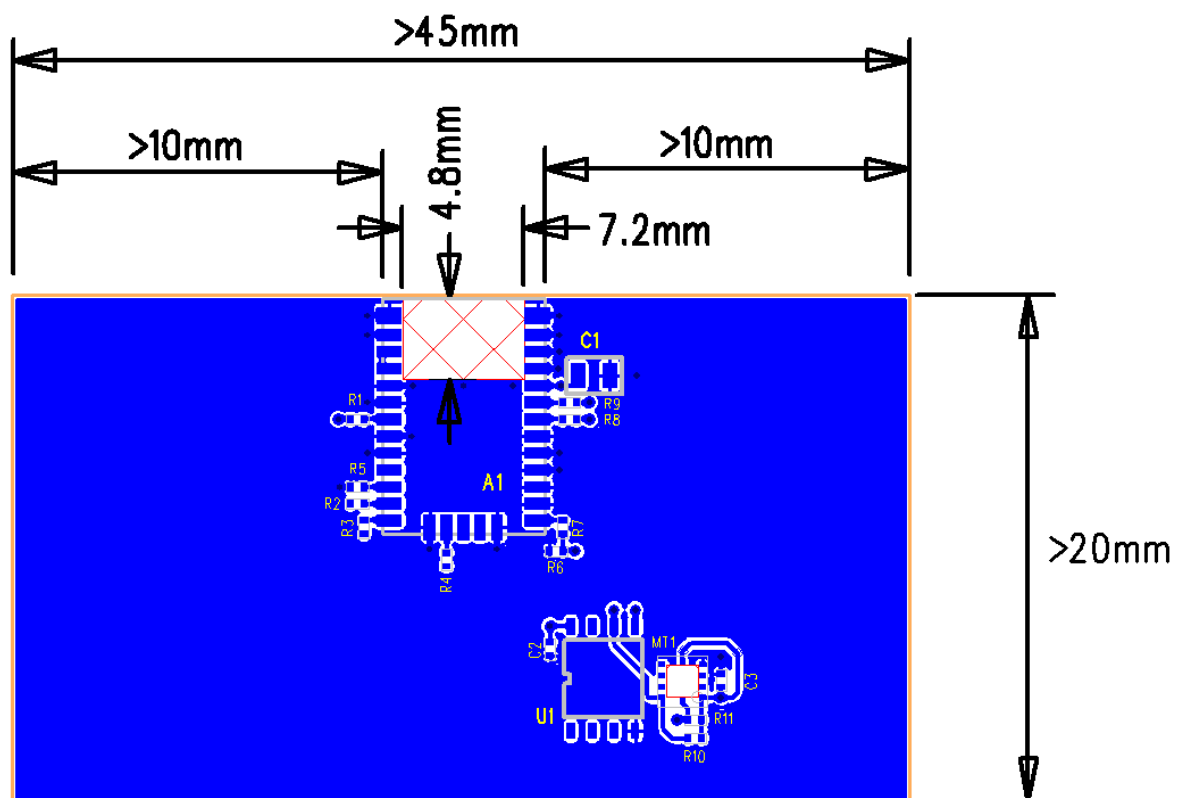
7.3 PCB layout suggestion

The suggested 4-layer PCB build up is presented in the following table.

Table 8 Suggested PCB build up

Layer	Description
1	Components + Ground plane (opening under UC530 antenna)
2	Signals and RF trace (opening under UC530 antenna)
3	Ground and power planes, signals (opening under UC530 antenna)
4	Ground plane, also short traces allowed (opening under UC530 antenna)

The UC530 module is intended to be assembled at the top edge of the mother board. The embedded antenna operation relies on the ground plane on the mother board; optimum size is 80x40mm but larger or smaller ground plane can be used. Suggested minimum ground plane size is 45x20mm. Optimum placement is at the center of the top edge but offset placement is allowed by keeping at least 10mm distance to nearest ground plane edge.

**Figure 13 Mother board ground plane and UC530 placement**

Note keepout 4.8x7.2mm under the embedded antenna. Follow also GND via hole suggestive locations.

Routing signals directly under the module should be avoided. This area should be dedicated to keep-out to both traces and assigned to ground plane (copper plane), except for via holes, which can be placed close to the pad under the module. If possible, the amount of VIA holes underneath the module should be minimized.

Note that the embedded GPS antenna requires a small ground plane clearance and void area (keep out 4.8x7.2mm) for copper plane & trace for all layers under the antenna. Placement of other components is not allowed under the keep out on opposite side.

For a multi-layer PCB the inner layers below the UC530 is suggested to be dedicated signal traces and copper plane for the rest of the area. It is always better to route very long signal traces in the inner layers of the PCB. In this way the trace can be easily shielded with ground areas from above and below.

The serial resistors at the I/O should be placed as close to the UC530 module as possible. In this way the risk for the EMI leakage is minimized. For the same reason by-pass supply capacitors should be connected very close to the module with short traces to IO contacts and to the ground plane. Place a GND via hole as close as possible to the capacitor.

Connect the GND soldering pads of the UC530 to ground plane with short traces (thermals) to via holes, which are connected to the ground plane. Use preferably one via hole for each GND pad.

A RF signal is suggested to be routed clearly away from other signals between two ground planes as a Stripline Transmission Line; this minimizes the possibility of interference and coupling. The proper width for the 50 ohm transmission line impedance depends on the dielectric material of the substrate, width of the signal trace and the height (separation) of the two ground planes. With FR-4 material the width of the trace shall be about 30% of the ground plane height. E.g. 0.4mm ground plane height results to 0.15mm trace width with FR-4 substrate.

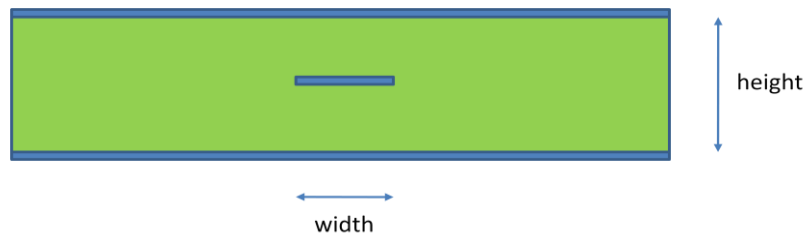


Figure 14 Stripline transmission line

Any board space free of signal traces should be covered with copper areas connected to ground net; in this way a solid RF ground plane is achieved throughout the circuit board. Several via holes should be used to connect the ground areas between different layers.

Additionally, it is important that the PCB build-up is symmetrical on both sides of the PCB core. This can be achieved by choosing identical copper content on each layers, and adding copper areas to route-free areas. If the circuit board is heavily asymmetric, the board may bend (wrap) during the PCB manufacturing or reflow soldering. Bending and wrapping may cause soldering failures and reduce end product reliability.

The AC530 Application Board layout described in next chapter can be also used as layout reference implementation.

7.3.1 Other electronics on mother board

Signal traces on top and bottom layers should have minimum length. Route signals mainly at inner layers below the top or bottom ground plane. In this way, a solid RF ground is achieved throughout the circuit board on top and bottom sides. Several via holes should be used to connect the ground areas between different layers.

Areas with dense component placing and dense routing requirements should be covered with a metal shield, which should be connected to ground plane with multiple GND via holes. Small ground plane openings for SMT components (length few mm, like LED or push buttons) in the ground plane are OK without a shield.

Dense areas having multiple via holes may open the ground plane for wide areas, thus blind and buried via holes are suggested to be used when changing layers for internal signals and power planes.

Use a power plane layer dedicated solely for power nets. Use wide trace width or even copper plane areas to achieve low impedance for power nets. Dedicate at least one layer as ground planes on adjacent layer above or below power plane layer in order to maximize capacitance to ground plane.

7.3.2 Avoiding EMI

Any GPS receiver is vulnerable to external spurious EMI signals since GPS signals are very weak below thermal noise floor. Any man made noise or spurious signals picked up by the nearby GPS antenna increases the noise floor and reduces GPS signal levels. Carrier Wave (CW) type spurious signals like clock harmonics on GPS band may also cause cross correlation products that may interfere with GPS signal tracking and cause position offsets.

The embedded GPS antenna may pick up local EMI signals and thus it is essential for good GPS performance that the following measures against EMI are properly implemented:

- High speed electronics like host CPU & memory bus are enclosed in a 'Faraday shield'. The electrical enclosure is formed by the ground planes on PCB + metal shield over components. Route signals at inner layers as discussed previously. Use preferably a power plane(s) layer for supply nets.
- Any signal that is routed outside the Faraday shield is protected against EMI noise on 1575MHz with a serial RF filter like
 - a serial resistor (> 330ohm, suitable for I/O with low current)
 - with a dedicated EMI filter (or ferrite bead) suitable for higher current
 - with suitable by-pass capacitor e.g. 18pF (low impedance due to series resonance at 1575MHz).

The following picture gives a suggestion for e.g. a 6-layer PCB build up, which forms a Faraday shield together with ground planes on PCB and with the shield over high speed electronics. Buried and blind via holes are used to keep EMI signal inside ground planes. I/O signals that are routed outside the Faraday enclosure are filtered with a suitable EMI filter. Power plane layer is used for supply nets with low impedance traces/planes.

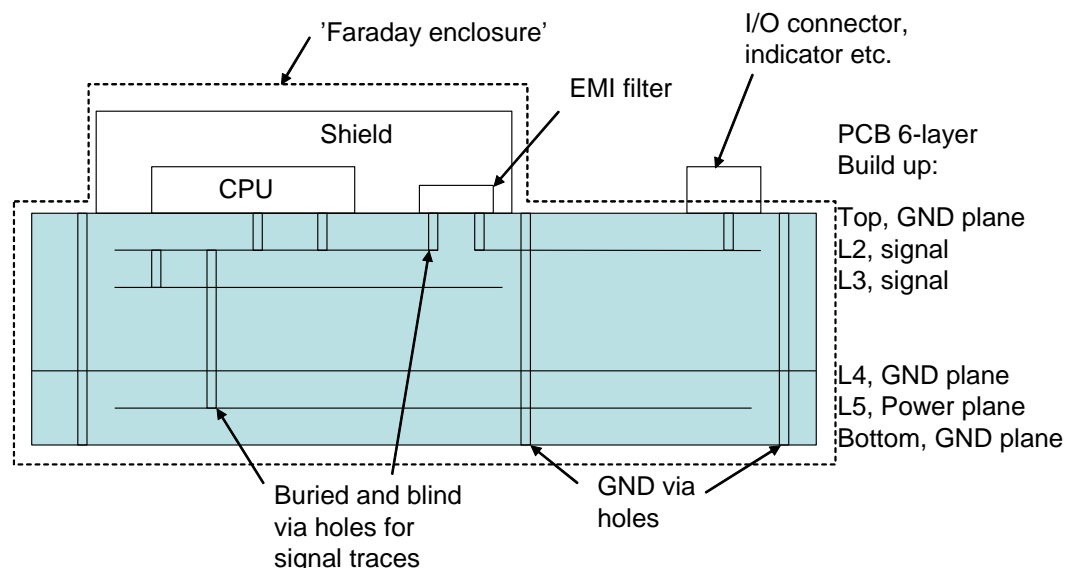


Figure 15 Avoiding EMI with Faraday enclosure

7.4 Embedded antenna operation

The embedded GPS antenna provides optimal radiation efficiency 80% typ. with 80x40mm ground plane. The antenna provides linear polarization with peak gain 1.1dBi and radiation pattern optimized for portable devices. The antenna is insensitive to surroundings and has high tolerance against frequency shifts. However on small ground plane widths the antenna gain and radiation efficiency reduces, e.g. the AC530 application board having

53mm width reduces signal levels by 2dB when compared to full 80x40mm ground plane dimensions. Radiation pattern of the embedded GPS antenna is shown in the picture below (on 80x40mm ground plane).

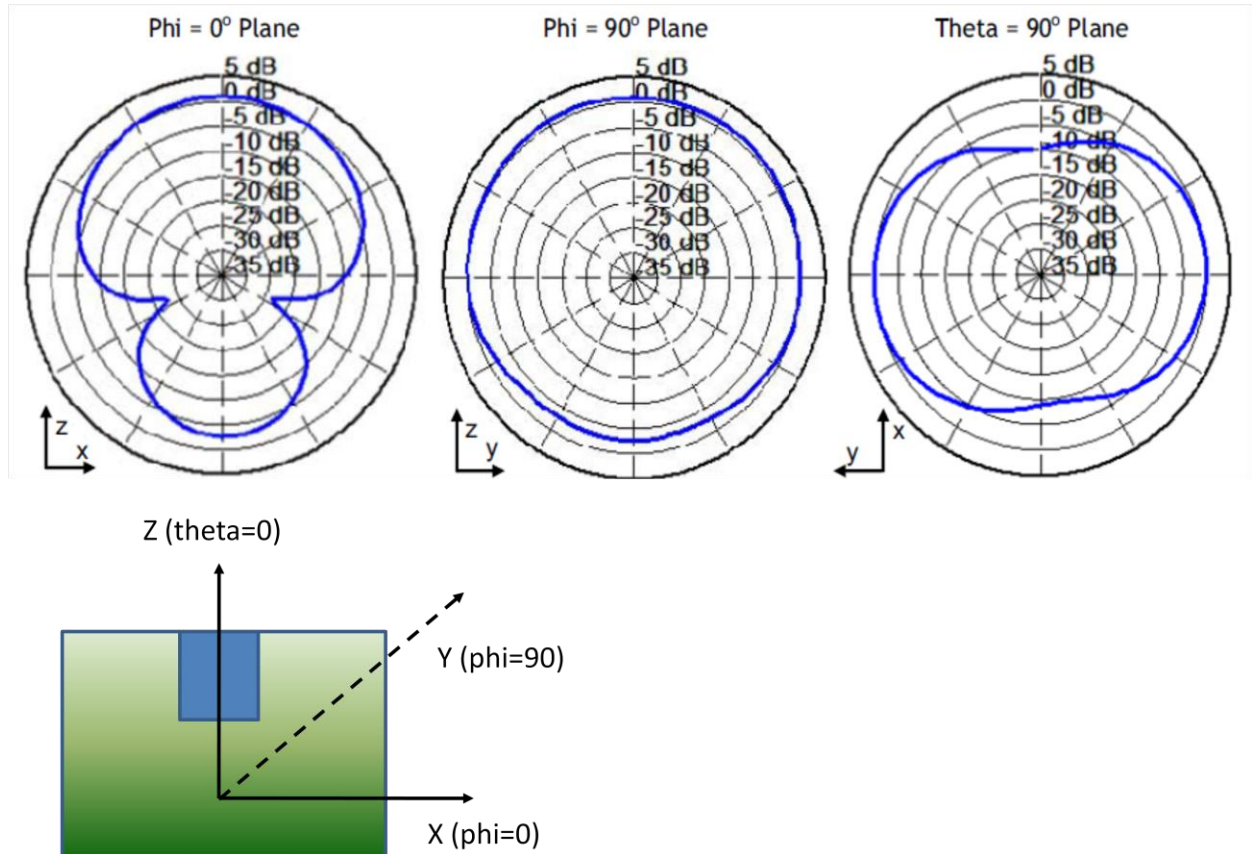


Figure 16 Radiation pattern of the embedded antenna, 80x40mm ground plane

Avoid placement of the module at a corner of the mother board. This will reduce radiation efficiency and cause frequency shifts. Optimal placement is at center of top edge; keep at least 10mm distance to nearest ground plane corner.

Placement of tall nearby components ($h > 3\text{mm}$) should keep minimum $d = 6\text{mm}$ distance to the embedded antenna. Also any adjacent conductive metal plane should have $d = 6\text{mm}$ distance to the top edge of the module. Enclosure or plastic cover should have minimum $d = 1.5\text{mm}$ distance to the antenna.

Placement near human body (or any biological tissue) is accepted by keeping minimum $d = 10\text{mm}$ distance between mother board and the body. With smaller distances to the body, the radiation efficiency of the antenna will start to reduce due to signal losses in biological tissue. E.g. $d = 5\text{mm}$ to biological tissue will reduce GPS signal levels by about 6dB. Note also that the body will act also as a reflector and thus radiation pattern will point perpendicular to the body.

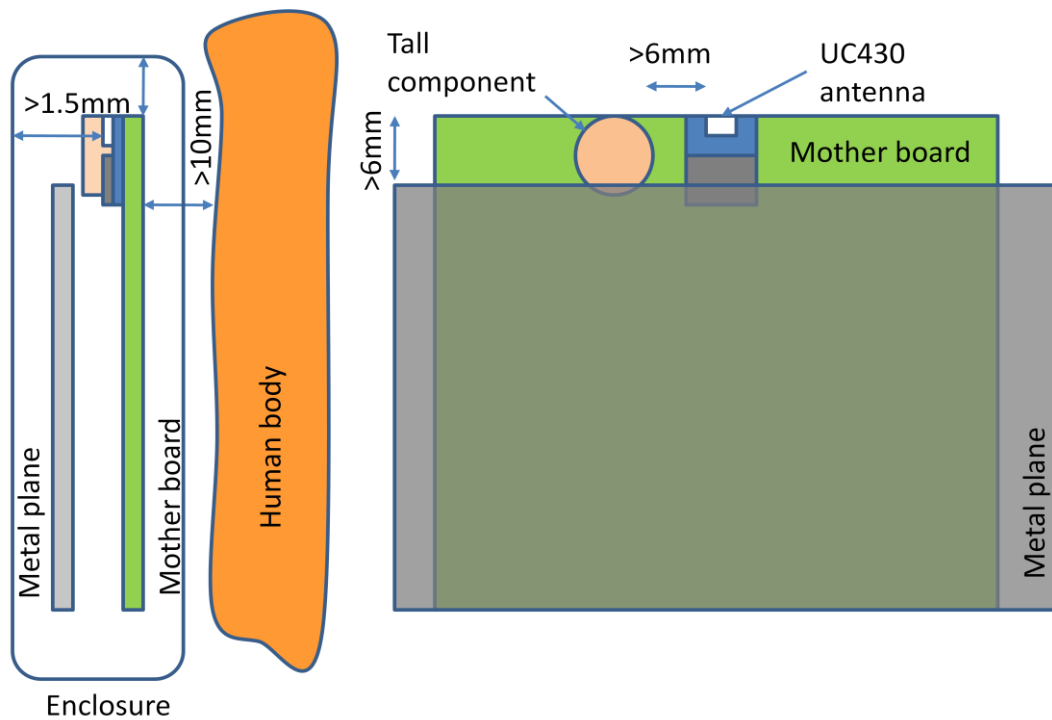


Figure 17 Placement of UC530 relative to surroundings

8 AC530 Application board for UC530

The Fastrax Application Board AC530 provides the UC530 connectivity to the Fastrax Evaluation Kit or to other evaluation purposes. It provides a single PCB board equipped with the UC530 module, MCX antenna connector, Antenna Bias +3.3 V switch, VDD Power Switch, switch for GPS_ON control and 2x20 pin Card Terminal connector.

Default host port configuration is set to UART by switch S4... S6 'ON' and S7 & S8 'OFF'. S3 should be 'ON' for first power up; for successive power up and for low power modes the S3 shall be switched to 'OFF'.

8.1 Board Terminal I/O-connector

The following signals are available at the 40-pin Card Terminal I/O connector J2. The same pin numbering applies also to the Fastrax Evaluation Kit pin header J4. Note that UART Port 0 maps to serial Port 0 at the Fastrax Evaluation Kit. I/O signal levels are CMOS 3.3V compatible unless stated otherwise.

Table 9 Board Terminal signals

Pin	Signal	I/O	Alternative name	GPIO	Interface to Fastrax Evaluation Kit
1	TX1	O	-		UART Port 1 async. output
2	GND	-	-		Ground
3	RX1	I	-		UART Port 1 async. input (RTCM)
4	GND	-	-		Ground
5	TX0	O	-		UART Port 0 async. output (NMEA)
6	GND	-	-		Ground
7	RX0	I	-		UART Port 0 async. input (NMEA)
8	GND	-	-		Ground
9	VDD_3V3	I	-		Power supply input +3.3V
10	GND	-	-		Ground
11	PPS	O	-		1PPS signal output
12	GND	-	-		Ground
13	RESET_N	I	-		Active low async. system reset
14	-	-	-		Not connected
15	-	-	-		Not connected
16	-	I	-		Not connected
17	GND	-	-		Ground
18	-	-	-		Not connected
19	-	-	-		Not connected
20	-	-	-		Not connected
21	GND	-	-		Ground
22	-	-	-		Not connected
23	-	-	-		Not connected
24	-	-	-		Not connected
25	GND	-	-		Ground
26	UI_FIX	O	-		UI indicator B output
27	-	-	-		UART CTS signal
28	-	-	-		Not connected
29	-	-	-		UART RTS signal
30	WAKEUP	O	-		UI indicator A output
31	GND	-	-		Ground
32	-	-	-		Not connected
33	GND	-	-		Ground
34	-	I	-		Not connected
35	GND	-	-		Ground

Pin	Signal	I/O	Alternative GPIO name	Interface to Fastrax Evaluation Kit
36	EINT1	I	-	EINT1 (Standby) control input
37	GND	-	-	Ground
38	32K/DR_INT	I/O	-	Default: DR_INT wakeup control input
39	GND	-	-	Ground
40	GPS_ON_N	I	-	Inverted GPS_ON control input, pulled up to VDD_3V3

8.2 Bill of materials

REF	TECHNICALDESCRIPTION	VALUE
A1	UC530 MODULE	UC530
BT1	PANASONIC ML621/F9D, 3V 5mAh	3V/ML621
C1	Capacitor chip, 1uF 6.3V +20% X5R 0402	1uF
C2	Capacitor chip, 22pF 50V 5% NP0 0402	22pF
C3	Capacitor chip, 1nF 50V 10% X7R 0402	1nF
C4	Capacitor chip, 22pF 50V 5% NP0 0402	22pF
C7	4,7uF 6,3V X5R 0805 +20%	4u7F
C11	4,7uF 6,3V X5R 0805 +20%	4u7F
C12	Capacitor chip, 1uF 6.3V +20% X5R 0402	1uF
D1	Diode 40V 225mA, BAT54J	BAT54J
D2	Diode 40V 225mA, BAT54J	BAT54J
D3	Diode 40V 225mA, BAT54J	BAT54J
D4	LED Red	TLSU1008
D5	LED Red	TLSU1008
J1	Aliner Industries Inc, MCX connector with switch	Aliner 32-301AA
J2	EDGE MOUNT SOCKET STRIP 40 PINS	2x20 edge
J3	2x5 pin-header, straight, 2.54mm	2x5P2.54
J4	1x2 pin-header, straight, pitch 2.54mm	1x2P2.54
J5	1x2 pin-header, straight, pitch 2.54mm	1x2P2.54
L1	Coil chip, 27nH 0402C +5%, 300mA, Q>60 @ 1.7GHz	27nH
PCB1	Application board for UC530 rev A	PCB/AC530A00
Q1	BC847B	BC847B
R1	Resistor chip, 1k 5% 0402 63mW	1k, 5%
R2	Resistor chip, 47R 0402 63mW 5%	47R, 5%
R3	Resistor chip, 47R 0402 63mW 5%	47R, 5%
R4	Resistor chip, 220R 5% 0402 63mW	220R, 5%
R5	Resistor chip, 47R 0402 63mW 5%	47R, 5%
R6	Resistor chip, 220R 5% 0402 63mW	220R, 5%
R7	Resistor chip, 220R 5% 0402 63mW	220R, 5%
R8	Resistor chip, 1M 5% 0402 63mW	1M, 5%
R9	Resistor chip, 470R 5% 0402 63mW	470R, 5%
R10	Resistor chip, 220R 5% 0402 63mW	220R, 5%
R11	Resistor chip, 220R 5% 0402 63mW	220R, 5%
R12	Resistor chip, 220R 5% 0402 63mW	220R, 5%
R13	Resistor chip, 220R 5% 0402 63mW	220R, 5%

R14	Resistor chip, 220R 5% 0402 63mW	220R, 5%
R15	Resistor chip, 470R 5% 0402 63mW	470R, 5%
R16	Resistor chip, 10k 5% 0402 63mW	N/A
R17	Resistor chip, 10k 5% 0402 63mW	10k, 5%
R18	Resistor chip, 220R 5% 0402 63mW	220R, 5%
R19	Resistor chip, 3.9k 5% 0402 63mW	3k9, 5%
R20	Resistor chip, 5k6 5% 0402 63mW	5k6, 5%
R21	Resistor chip, 220R 5% 0402 63mW	220R, 5%
R22	Resistor chip, 47k 5% 0402 63mW	47k, 5%
R26	Resistor chip, 10k 5% 0402 63mW	10k, 5%
R27	Resistor chip, 10k 5% 0402 63mW	10k, 5%
S1	Jumper, Pitch, 2.54mm, Red colour	J4/P1-P2
S2	Label 13x16mm iTrax03s	STICKER13x16
S3	Switch, on-off	SW JMP 2P54
S4	Switch, on-off	SW JMP 2P54
S5	Switch, on-off	SW JMP 2P54
S6	Switch, on-off	SW JMP 2P54
S7	Switch, on-off	SW JMP 2P54
S8	Switch, on-off	SW JMP 2P54
S9	Jumper, Pitch, 2.54mm, Red colour	J5/P1-P2
U1	POWER SWITCH 0.1 ohm	ADP191
U2	Logic buffer	NC7SZ125
U3	Logic buffer	NC7SZ125
U4	Schmit-Trigger inverter	NC7SZ14M5X

HOST PATH (Port 0)		HOST STRAP		PATH & I/O LEVEL		
PORT	S4	S5	S6	S7	S8	
UART	ON	ON	ON	OFF	OFF	J2 (DEFAULT)
I2C	OFF	OFF	OFF	ON	ON	J3 (support TBD)

The schematic also includes a table at the bottom right listing the pin connections for the HOST PATH (Port 0), HOST STRAP, and PATH & I/O LEVEL. The table is as follows:

HOST PATH (Port 0)		HOST STRAP		PATH & I/O LEVEL		
PORT	S4	S5	S6	S7	S8	
UART	ON	ON	ON	OFF	OFF	J2 (DEFAULT)
I2C	OFF	OFF	OFF	ON	ON	J3 (support TBD)

Figure 18 AC530 Circuit diagram

8.4 AC530 layout and assembly

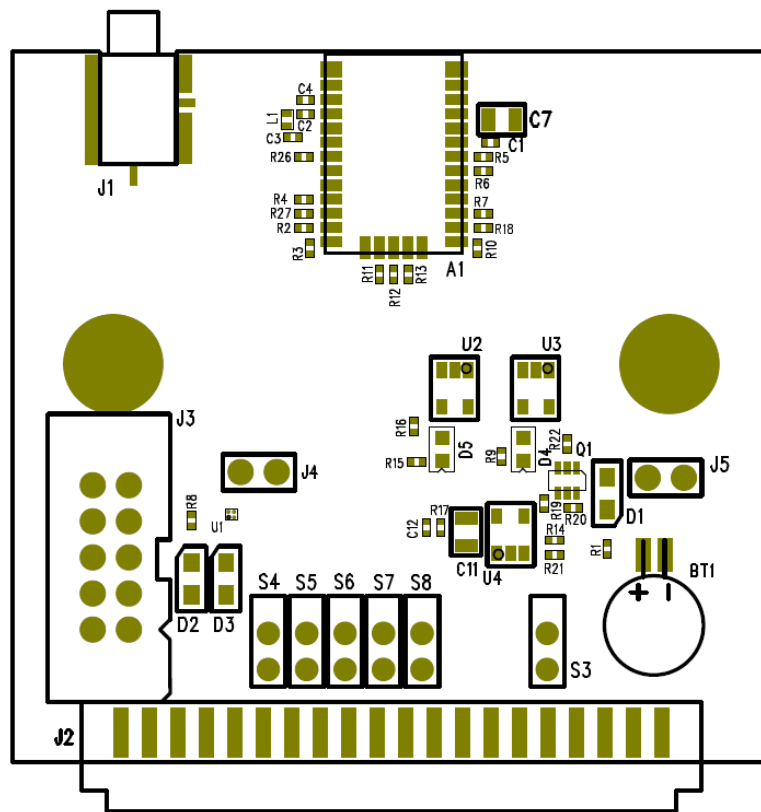


Figure 19 Assembly drawing, top side

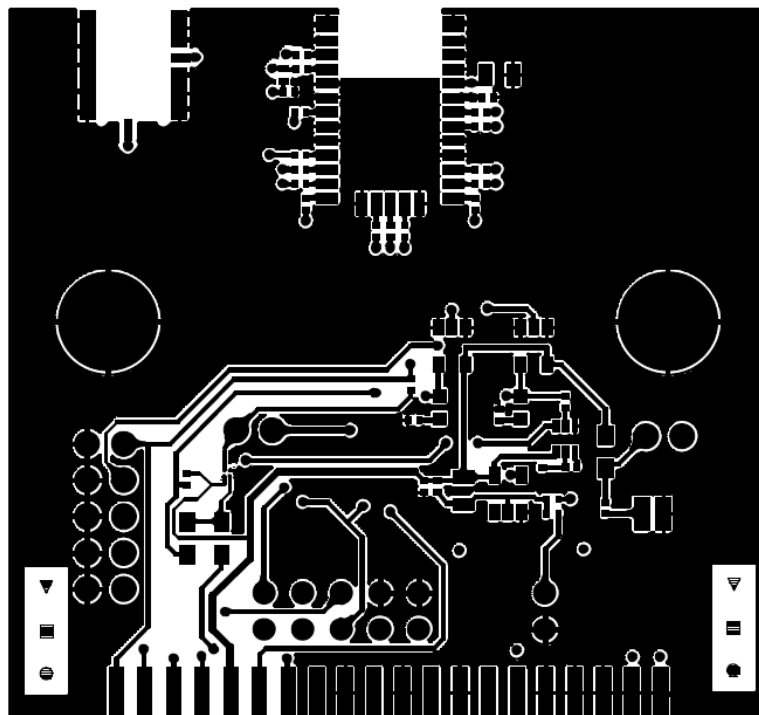


Figure 20 Layer 1, (top)

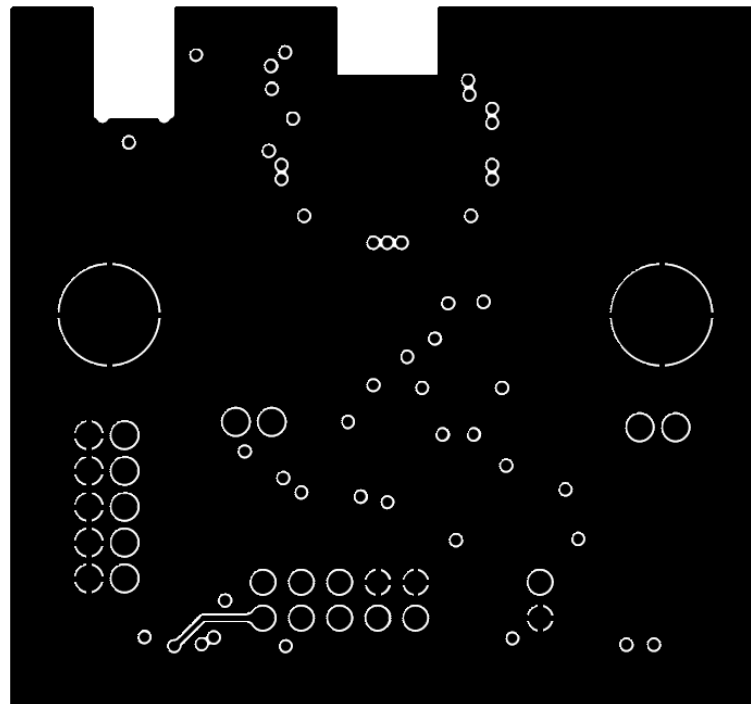


Figure 21 Layer 2

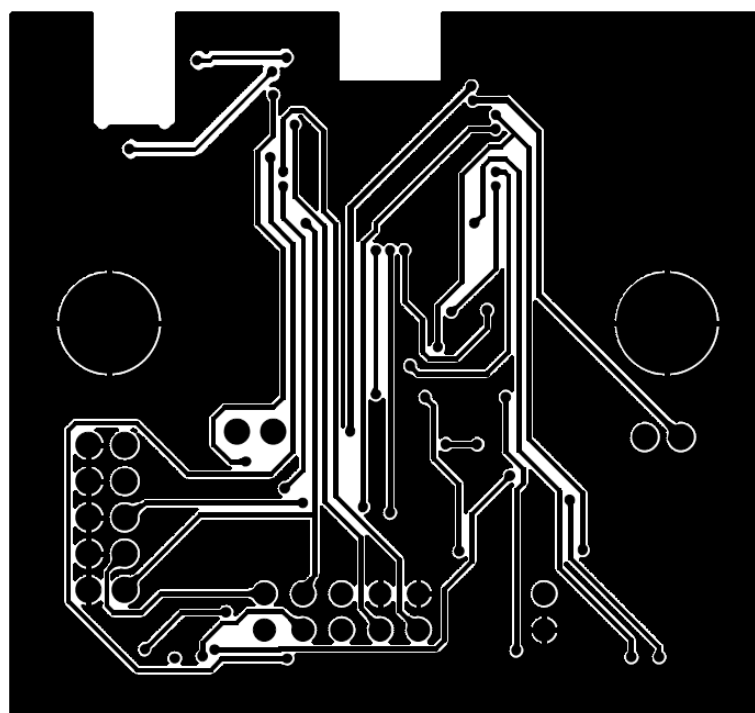


Figure 22 Layer 3

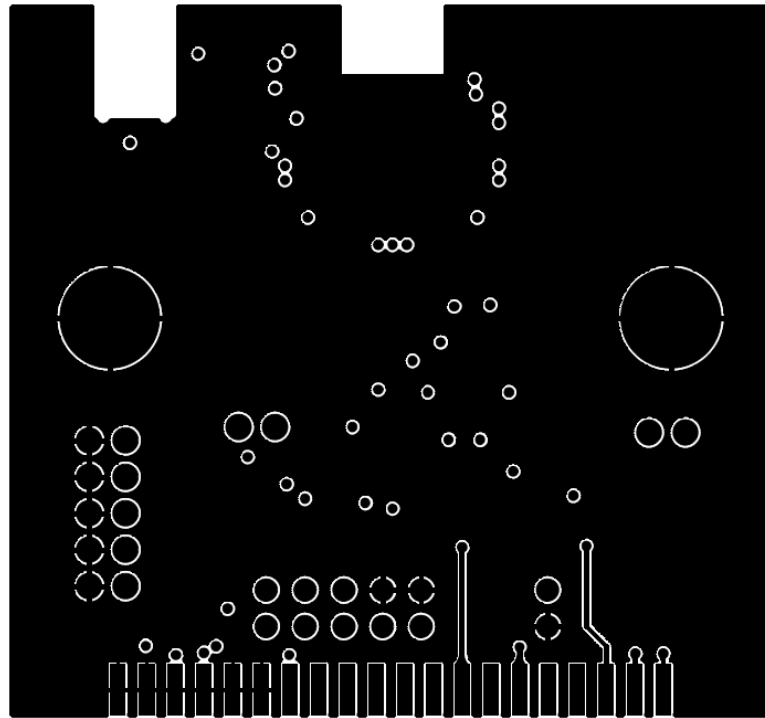


Figure 23 Layer 4 (bottom)

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