#### ADERA.

# Pin Information for the Cyclone™ II EP2C5 Device

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1      1 C3      T144      Q208      in Q208        2      2 F4      In Q208      in Q208        4      4 C2      In Q208      In Q208        5      DC2      In Q208      In Q208        6      E5      In Q208      In Q208      In Q208        6      E6      In Q208      In Q210      In Q208        6      B      In Q208      In Q210      In Q210        7      13 F3      In Q210      In Q210      In Q210        8      14 E1      In Q210      In Q210      In Q210        10      In Q210      In Q210      In Q210      In Q210        11      17 G1      In Q210      In Q210      In Q210      In Q210        11      17 G1      In Q210      I	Bank	VREFB	Pin Name /	Optional Function(s) Configuration	Configuration 1	-144 Q2	08 F256	'144 Q208 F256 DQS for x8/x9 in	DQS for x8/x9 in	DQS for x16/x18	DQS for x8/x9 in	DQS for x16/x18
WREFINIO (O      ASDO      ASDO      1 C3      C      C      C      C      C      C      C      C      C      C      C      C      C      C      C      C      C      C      C      C      C      C      C      C      C      C      C      C      C      C      C      C      C      C      C      C      C      C      C      C      C      C      C      C      C      C      C      C      C      C      C      C      C      C      C      C      C      C      C      C      C      C      C      C      C      C      C      C      C      C      C      C      C      C      C      C      C      C      C      C      C      C      C      C      C      C      C      C      C      C      C      C      C      C      C      C      C      C      C      C      C      C	Number	Group	Function		Function			T144	Q208		F256	in Q208
VREFBIND   O   LVOS90   LVOS	B1			ASDO	ASDO	1	1 C3					
VREFENNO   O LVDSSA   2   2   1   1   1   1   1   1   1   1	B1	VREFB1N0	OI	nCSO	nCSO	2						
WREEBIND (OC LYDSSP)      CLKUSR      4 G22      PODIO      CD0280      CD010      D0010	B1	VREFB1N0	OI	LVDS9p	CRC_ERROR	3	3 C1					
WREFBINO (ONDORSING)      LVDSSP      5 PS      7      CEC	B1	VREFB1N0		LVDS9n	CLKUSR	4	4 C2					
WREEBIND (OC)      LVDS6n      6 E6      P      COLUG      COLUGE      COLUGE </td <td>B1</td> <td>VREFB1N0</td> <td>OI</td> <td>LVDS8p</td> <td></td> <td></td> <td></td> <td></td> <td></td> <td></td> <td></td> <td></td>	B1	VREFB1N0	OI	LVDS8p								
WREEBIND (NCC)OTAL      UNDSTAD      6      6      6      6      6      6      6      6      6      6      6      6      6      6      6      6      6      6      6      6      6      6      6      6      6      6      6      6      6      6      6      6      6      6      6      6      6      6      6      6      6      6      6      6      6      6      6      6      6      6      6      6      6      6      6      6      6      6      6      6      6      6      6      6      6      6      6      6      6      6      6      6      6      6      6      6      6      6      6      6      6      6      6      6      6      6      6      6      6      6      6      6      6      6      6      6      6      6      6      6      6      6      6      6 <td>B1</td> <td>VREFB1N0</td> <td>OI</td> <td>LVDS8n</td> <td></td> <td></td> <td></td> <td></td> <td></td> <td></td> <td>DQ0L0</td> <td>DQ1L0</td>	B1	VREFB1N0	OI	LVDS8n							DQ0L0	DQ1L0
VREFBIND   O	B1	VREFB1N0	VCCI01			2	7					
WRETERINO GND	B1	VREFB1N0		LVDS7p					DQ1L0		DQ0L1	DQ1L1
VREFBIND   O LVDS7n   VREFBIND   O LVDS6p   O LVDS6p	B1					9	6					
WREFBIND      (O)      LVDS6p      11 D3      D0112      D0112      D0013        WREFBIND      (O)      LVDS6n      7 13 P3      7 13 P3      7 13 P3      7 10 P3	B1	VREFB1N0	OI	LVDS7n			10 E4		DQ1L1		DQ0L2	DQ1L2
VREFBIND   O VREFBIND   VREFBIND   VREFBIND   VREFBIND   VCCIO1   VCDS5p   VREFBIND   VCCIO1   VCCIO1   VREFBIND   VCCIO1   V	B1	VREFB1N0		LVDS6p					DQ1L2		DQ0L3	DQ1L3
VREFB1ND   O   VRE	B1	VREFB1N0	OI	LVDS6n			12 D4		DQ1L3		DQ0L4	DQ1L4
WREFBIND (ACCIOT)      LVDSSP      8      1 E I DPCLKO/DQSOL	B1	VREFB1N0	OI	VREFB1N0		7	13 F3					
WREFB1ND      IO      LVDSSp      8      14 E1      DPCLKNDQS0L      <	B1	VREFB1N0	VCCI01									
VREFB1ND      IO      LVDSSn      15 EZ      P      DOULS      D	B1	VREFB1N0		LVDS5p		8		DPCLK0/DQS0L	DPCLK0/DQS0L	DPCLK0/DQS0L	DPCLK0/DQS0L	DPCLK0/DQS0L
VREFB1ND      TDO      10      16      C2      PREFB1ND      TMS      11      17 G1      PREFB1ND      TMS      11      17 G1      PREFB1ND      TCK      12      18 F2      PREFB1ND      TCK      12      18 F2      PREFB1ND      TCK      14      20 F1      PREFB1ND      TCK      TCK      14      20 F1      PREFB1ND      TCK      TCK <td>B1</td> <td>VREFB1N0</td> <td>OI</td> <td>LVDS5n</td> <td></td> <td>6</td> <td>15 E2</td> <td></td> <td></td> <td></td> <td>DQ0L5</td> <td>DQ1L5</td>	B1	VREFB1N0	OI	LVDS5n		6	15 E2				DQ0L5	DQ1L5
VREFB1ND      TMS      T	B1	VREFB1N0	TDO		TDO	10	16 G2					
VREFB1ND      TCK      12      18 F2      PM      PM        VREFB1ND      TDI      13      19 H5      PM      PM        VREFB1ND      DATAO      DATAO      14      20 F1      PM      PM        VREFB1ND      DCEK      DCLK      15      21 H4      PM      PM      PM        VREFB1ND      CLKO      LVDSCLKOp/input(1)      17      23 H2      PM      PM      PM        VREFB1ND      CLK1      LVDSCLKOp/input(1)      18      24 H1      PM      PM      PM        VREFB1ND      CLK1      LVDSCLK1p/input(1)      20      26 J5      PM      PM      PM        VREFB1NI      CLK3      LVDSCLK1p/input(1)      22      28 J1      PM      PM      PM        VREFB1NI      CLK3      LVDSCLK1p/input(1)      22      28 J1      PM      PM      PM        VREFB1NI      CLK3      LVDSGLK1n/input(1)      23      29      PM      PM      PM        VREFB1NI      CLK3      LVDS4p      LVDS3p      LVDS3p      PM <td>B1</td> <td>VREFB1N0</td> <td>TMS</td> <td></td> <td>TMS</td> <td>11</td> <td></td> <td></td> <td></td> <td></td> <td></td> <td></td>	B1	VREFB1N0	TMS		TMS	11						
VREFBIND      TDI      TDI      13      19      H5      PM	B1	VREFB1N0	TCK		TCK	12						
VREFBIND      DATAO      DATAO      14      20 F1      AB	B1	VREFB1N0	TDI		TDI	13	19 H5					
VREFBIND      DCLK      DCLK      15      21 H4      PREFBIND      CLK      LVDSCLKOp/input(1)      17      23 H2      PREFBIND      CLKO      LVDSCLKOp/input(1)      18      24 H1      PREFBIND      CLK      LVDSCLKOp/input(1)      18      24 H1      PREFBIND      CLK      LVDSCLKTop/input(1)      18      24 H1      PREFBIND      CLK	B1	VREFB1N0		DATA0	DATA0	14	20 F1					
VREFB1ND      CLKD      LVDSCLKOp/input(1)      17      23 H2      PREFB1ND      CLKD      LVDSCLKOp/input(1)      18      24 H1      PREFB1ND      CLKD      LVDSCLKOp/input(1)      18      24 H1      PREFB1ND      CLKD      LVDSCLK1p/input(1)      18      24 H1      PREFB1ND      CONFIG      LVDSCLK1p/input(1)      20      26 J5      PREFB1ND      PREFB1ND      CLK3      LVDSCLK1p/input(1)      21      27 J2      PREFB1ND      PREFB1ND      CLK3      LVDSCLK1p/input(1)      22      28 J1      PREFB1ND	B1			DCLK	DCLK	15	21 H4					
VREFB1ND      CLKD      LVDSCLKOp/input(1)      17      23 Hz      A      A      A      A      A      A      A      A      A      A      A      A      A      A      A      A      A      A      A      A      A      A      A      A      A      A      A      A      A      A      A      A      A      A      A      A      A      A      A      A      A      A      A      A      A      A      A      A      A      A      A      A      A      A      A      A      A      A      A      A      A      A      A      A      A      A      A      A      A      A      A      A      A      A      A      A      A      A      A      A      A      A      A      A      A      A      A      A      A      A      A      A      A      A      A      A      A      A      A      A	B1	VREFB1N0	nCE		nCE	16	22 G5					
VREFB1ND      CLK1      LVDSCLKOn/input(1)      18      24 H1      4      4      4      4      4      4      4      4      4      4      4      4      4      4      4      4      4      4      4      4      4      4      4      4      4      4      4      4      4      4      4      4      4      4      4      4      4      4      4      4      4      4      4      4      4      4      4      4      4      4      4      4      4      4      4      4      4      4      4      4      4      4      4      4      4      4      4      4      4      4      4      4      4      4      4      4      4      4      4      4      4      4      4      4      4      4      4      4      4      4      4      4      4      4      4      4      4      4      4      4	B1	VREFB1N0	CLK0	LVDSCLK0p/input(1)		17	23 H2					
VREFB1N0      GND      nCONFIG      20      26 J5      Consist of the con	B1	VREFB1N0	CLK1	LVDSCLK0n/input(1)		18	24 H1					
VREFB1ND      Inconfig      20      26 J5      Amount      Amount </td <td>B1</td> <td>VREFB1N0</td> <td>GND</td> <td></td> <td></td> <td>19</td> <td>25</td> <td></td> <td></td> <td></td> <td></td> <td></td>	B1	VREFB1N0	GND			19	25					
VREFB1N1      CLK2      LVDSCLK1p/input(1)      21      27 J2      28 J1      CREFB1N1      CLK3      LVDSCLK1n/input(1)      22      28 J1      CREFB1N1      CLK3      LVDSAph      23      29      DPCLK1/DQS1L      DPCLK1/DQS1L<	B1				nCONFIG	20	26 J5					
VREFB1N1      CLK3      LVDSCLK1n/input(1)      22      28 J1      Amount	B1		CLK2	LVDSCLK1p/input(1)		21	27 J2					
VREFB1N1 IO      LVDS4h      24      30 k2      DPCLK1/DQS1L      DPCLK1/	B1		CLK3	LVDSCLK1n/input(1)		22	28 J1					
VREFB1N1      IO      LVDS4p      24      30 k2      DPCLK1/DQS1L	B1	VREFB1N1	VCCI01			23	29					
VREFB1N1 IO      LVDS3h      26      32 K4      DQ1L4      DQ1L4        VREFB1N1 IO      LVDS3h      27      33 K5      DQ1L4      DM0L        VREFB1N1 IO      LVDS2p      35 L1      DQ1L6      DQ1L0	B1	VREFB1N1		LVDS4p		24	30 K2	DPCLK1/DQS1L	DPCLK1/DQS1L	DPCLK1/DQS1L	DPCLK1/DQS1L	DPCLK1/DQS1L
VREFB1N1 IO      LVDS3p      26      32 K4      DQ1L4      DQ1L4      DQ1L5        VREFB1N1 IO      LVDS2p      34 M1      DQ1L5      DM0L        VREFB1N1 IO      LVDS2p      35 L1      DQ1L6      DQ1L0	B1	П		LVDS4n		25	31 K1	_			DQ0L6	DQ1L6
VREFB1N1 IO      LVDS2p      27      33 K5      DQ1L4      DM0L        VREFB1N1 IO      LVDS2p      35 L1      DQ1L6      DQ1L0	B1 \rangle	VREFB1N1	0	LVDS3p		56	32 K4				DQ0L7	DQ1L7
VREFB1N1 IO      LVDS2p      34 M1      DQ1L5      DM0L        VREFB1N1 IO      LVDS2p      35 L1      DQ1L6      DQ1L0	B1	VREFBINI	Q	LVDS3n		77	33 K5	7	DQ1L4			DQ1L8
VREFB1N1 IO LVDS2p 35 L1 DQ1L6 DQ1L0	B1						34 M1		DQ1L5		DMOL	DM1L0/BWS#1L0
	B1	VREFB1N1	OI	LVDS2p			35 L1		DQ1L6		DQ1L0	DQ1L9

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Jaca	VPEER	Din Name /	Optional Function(s) Configuration		T11/1	3202 5056	T144 0208 E256 DOS for x8/x9 in	DOS for v8/v0 in	DOC for v16/v18	DOS for v8/v9 in	DOS for v16/v18
Number	Group	Function				<u> </u>	T144	Q208	in Q208	F256	in Q208
B1	VREFB1N1	OI	LVDS2n			36 L2				DQ1L1	DQ1L10
B1	VREFB1N1	OI	VREFB1N1		28	37 J4					
B1	VREFB1N1	OI				M2				DQ1L2	DQ1L11
B1	VREFB1N1	GND				38					
B1	VREFB1N1	OI				39 M3		DQ1L7		DQ1L3	DQ1L12
B1	VREFB1N1	OI	LVDS1p			40 N1		DQ1L8		DQ1L4	DQ1L13
B1	VREFB1N1	01	LVDS1n			41 N2		DM1L/BWS#1L		DQ1L5	DQ1L14
B1	VREFB1N1 VCCIO1	VCCI01			29	42					
B1	VREFB1N1	01				43 L3				DQ1L6	DQ1L15
B1	VREFB1N1	OI	LVDS0p			44 P1				DQ1L7	DQ1L16
B1	VREFB1N1	OI	LVDS0n			45 P2				DQ1L8	DQ1L17
B1	VREFB1N1	OI			30	46 P3				DM1L/BWS#1L	DM1L1/BWS#1L1
B1	VREFB1N1	OI	PLL1_OUTp		31	47 L4					
B1	VREFB1N1	OI	PLL1_OUTn		32	48 M4					
B1		GND			33	49					
B1	VREFB1N1	GND_PLL1			34	20 L5					
B1	VREFB1N1	VCCD_PLL1			35	51 L6					
B1	VREFB1N1	GND_PLL1			36	52 N5					
B4	VREFB4N1	VCCA_PLL1			37	53 M5					
B4	VREFB4N1	GNDA_PLL1			38	54 M6					
B4		GND			39	22					
B4	VREFB4N1	OI	LVDS58n	DEV_OE	40	56 R3					
B4	VREFB4N1	OI	LVDS58p		41	57 T3	DM1B/BWS#1B	DM1B/BWS#1B	DM1B1/BWS#1B1	DM1B/BWS#1B	DM1B1/BWS#1B1
B4	VREFB4N1	OI	LVDS57p		42	58 P5	DQ1B8	DQ1B8	DQ1B17	DQ1B8	DQ1B17
B4	VREFB4N1	OI	LVDS57n		43	59 P4	DQ1B7	DQ1B7	DQ1B16	DQ1B7	DQ1B16
B4	VREFB4N1	OI	LVDS56p		44	60 T4	DQ1B6	DQ1B6	DQ1B15	DQ1B6	DQ1B15
B4	VREFB4N1	OI	LVDS56n		45	61 R4	DQ1B5	DQ1B5	DQ1B14	DQ1B5	DQ1B14
B4	VREFB4N1	VCCIO4			46	62					
B4	VREFB4N1	01	LVDS55p		47	63 T5	DPCLK2/DQS1B	DPCLK2/DQS1B	DPCLK2/DQS1B	DPCLK2/DQS1B	DPCLK2/DQS1B
B4	VREFB4N1 GND	GND									
B4	VREFB4N1 IO	OI	LVDS55n		48	64 R5				DQ1B4	DQ1B13
B4	VREFB4N1 VCCIO4	VCCI04									
B4	VREFB4N1	GND									
B4		GND			49	65					
B4	VREFB4N1	0				16 T6				DQ1B3	DQ1B12
B4	VREFB4N1 VCCINT	VCCINT			20	99					

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Bank Number	VREFB Group	Pin Name / Function	Optional Function(s) Configuration	Configuration Function	1144	2208 F256		DQS for x8/x9 in Q208	DQS for x16/x18 in Q208	DQS tor x8/x9 in F256	DQS for x16/x18 in Q208
B4	VREFB4N1	OI	VREFB4N1		51	67 N8					
B4	VREFB4N1	OI	LVDS54p		52	21 89 L	DQ1B4	DQ1B4	DQ1B13	DQ1B2	DQ1B11
B4	VREFB4N1	OI	LVDS54n			69 R7		DQ1B3	DQ1B12	DQ1B1	DQ1B10
B4	VREFB4N1	OI	LVDS60p			۲٦					
B4	VREFB4N1	OI	LVDS60n			8T					
B4	VREFB4N1	OI	LVDS53p		23	70 T8	DQ1B3	DQ1B2	DQ1B11	DQ1B0	DQ1B9
B4	VREFB4N1	VCCIO4			54	71					
B4	VREFB4N1	<u>o</u>	LVDS53n		22	72 R8	DQ1B2	DQ1B1	DQ1B10		DM1B0/BWS#1B0
B4	VREFB4N1	GND			99	73					
B4	VREFB4N1 IO	<u>o</u>	LVDS52p		22	74 T9	DQ1B1	DQ1B0	DQ1B9		
B4	VREFB4N1	OI	LVDS52n		28	75 R9	DQ1B0				
B4	VREFB4N0	<u>o</u>	LVDS59p			6N					
B4	VREFB4N0	OI	LVDS59n			N10					
B4	VREFB4N0	VCCIO4									
B4	VREFB4N0	OI	LVDS51p		29	76 T11					
B4	VREFB4N0	GND									
B4	VREFB4N0	OI	LVDS51n		09	77 R11				DM0B	DQ1B8
B4	VREFB4N0	GND			61	78					
B4	VREFB4N0	VCCINT			62	62					
B4	VREFB4N0	OI				80 P11					
B4	VREFB4N0 IO	OI	LVDS50p			81 L9					
B4	VREFB4N0	OI	LVDS50n			82 L10					
B4	VREFB4N0	VCCIO4				83					
B4	VREFB4N0	OI	LVDS49p			84 R10		DM0B	DM1B0/BWS#1B0		
B4	VREFB4N0	GND				85					
B4	VREFB4N0	OI	LVDS49n			86 T10			DQ1B8	DQ0B7	DQ1B7
B4	VREFB4N0	OI	LVDS48p			87 K11		DQ0B7	DQ1B7		
B4	VREFB4N0	OI	LVDS48n			88 K10		DQ0B6	DQ1B6		
B4	VREFB4N0	Q	VREFB4N0		63	89 N11					
B4	VREFB4N0	OI	LVDS47p			90 P12		DQ0B5	DQ1B5	DQ0B6	DQ1B6
B4	VREFB4N0 VCCIO4	VCCIO4				91					
B4	VREFB4N0 10	OI	LVDS47n			92 P13		DQ0B4	DQ1B4	DQ0B5	DQ1B5
B4	VREFB4N0	GND				63					
B4	VREFB4N0	OI	LVDS46p		4	94 T12	DPCLK4/DQS0B	DPCLK4/DQS0B	DPCLK4/DQS0B	DPCLK4/DQS0B	DPCLK4/DQS0B
B4	VREFB4N0	<u>o</u>	LVDS46n		65	95 R12				DQ0B4	DQ1B4
B4	VREFB4N0	<u>o</u>				96 L12		DQ0B3	DQ1B3		

### **然自信系**。

Bank	VREFB Pin Name /	Optional Function(s) Configuration	Comignianon		)	Ox 0 001 . 001x				
Number	Group Function		Function			T144	Q208	in Q208	F256	in Q208
B4	VREFB4N0 IO	LVDS45p			97 T13	3	DQ0B2	DQ1B2	DQ0B3	DQ1B3
B4	VREFB4N0 VCCIO4			99	86					
B4	VREFB4N0 IO	LVDS45n		67	99 R13	13	DQ0B1	DQ1B1	DQ0B2	DQ1B2
B4	VREFB4N0 GND			89	100					
B4	VREFB4N0 IO	LVDS44p		69	101 T14	4	DQ0B0	DQ1B0	DQ0B1	DQ1B1
B4	VREFB4N0 IO	LVDS44n		20	102 R14	4			DQ0B0	DQ1B0
B4	VREFB4N0 IO	LVDS43p		71	103 M11	11				
B4	VREFB4N0 IO	LVDS43n		72	104 L11	1				
B3	VREFB3N1 IO	LVDS42n		73	105 N12	12 DM1R/BWS#1R				
B3	VREFB3N1 IO	LVDS42p		74	106 M12	12 DQ1R8	DM1R/BWS#1R	DM1R1/BWS#1R1		
B3	VREFB3N1 IO	LVDS41n	INIT_DONE	22	107 N13	13				
B3	VREFB3N1 IO	LVDS41p	nCEO	92	108 N14	4				
B3	VREFB3N1 IO				P14	4				
B3	VREFB3N1 VCCIO3			22	109					
B3	VREFB3N1 IO	LVDS40n			110 P15	2	DQ1R8	DQ1R17	DM1R/BWS#1R	DM1R1/BWS#1R1
B3	VREFB3N1 GND			78	111					
B3	VREFB3N1 IO	LVDS40p			112 P16	9	DQ1R7	DQ1R16	DQ1R8	DQ1R17
B3	VREFB3N1 IO	LVDS39n			113 N15	15	DQ1R6	DQ1R15	DQ1R7	DQ1R16
B3	VREFB3N1 IO	LVDS39p			114 N16	9	DQ1R5	DQ1R14	DQ1R6	DQ1R15
B3	VREFB3N1 IO	LVDS38n			115 M15	15	DQ1R4	DQ1R13	DQ1R5	DQ1R14
B3	VREFB3N1 IO	LVDS38p			116 M16	91	DQ1R3	DQ1R12	DQ1R4	DQ1R13
B3	VREFB3N1 IO	VREFB3N1		79	117 M14	14				
B3	VREFB3N1 IO				118 L14	4	DQ1R2	DQ1R11		
B3	VREFB3N1 IO	LVDS37n		80	119 L1	15			DQ1R3	DQ1R12
B3	VREFB3N1 IO	LVDS37p		81	120 L1	L16			DQ1R2	DQ1R11
B3			nSTATUS	82	121 M13	13				
B3					122					
B3	VREFB3N1 CONF_DONE		CONF_DONE	83	123 L13	3				
B3	VREFB3N1 GND				124					
B3	VREFB3N1 MSEL1		MSEL1	84	125 K12	2				
B3	VREFB3N1 MSEL0		MSEL0	82	126 J13					
B3		LVDS36n		86	127 K16		DQ1R1	DQ1R10	DQ1R1	DQ1R10
B3		LVDS36p		87	128 K15	5 DPCLK6/DQS1R	DPCLK6/DQS1R	DPCLK6/DQS1R	DPCLK6/DQS1R	DPCLK6/DQS1R
B3		LVDSCLK3n/input(1)		88	129 J16	9				
B3		LVDSCLK3p/input(1)		89	130 J15	5				
B3	VRFFR3NO CLK5	1 V/OC/1 V25/15/11/11								



Bank	VREFB	Pin Name /	Optional Function(s) Configuration	Configuration	T144	3208 F.	T144 Q208 F256 DQS for x8/x9 in	DQS for x8/x9 in	DQS for x16/x18	DQS for x8/x9 in	DQS for x16/x18
Number	Group	Function	•	Function			T144	Q208		F256	in Q208
B3	<b>VREFB3N0</b>	CLK4	LVDSCLK2p/input(1)		91	132 H					
B3	<b>VREFB3N0</b>	OI	LVDS35n		85	133 H12		DQ1R0	DQ1R9	DQ1R0	DQ1R9
B3	<b>VREFB3N0</b>	OI	LVDS35p		93	134 J1	J12 DPCLK7/DQS0R	DPCLK7/DQS0R	DPCLK7/DQS0R	DPCLK7/DQS0R	DPCLK7/DQS0R
B3	<b>VREFB3N0</b>	OI	LVDS34n		6	135 G	G16 DQ1R5	DMOR	DM1R0/BWS#1R0	DMOR	DM1R0/BWS#1R0
B3	<b>VREFB3N0</b>	VCCIO3			<del>2</del> 6	136					
B3	VREFB3N0	<u>O</u>	LVDS34p		96	137 G	G15 DQ1R4		DQ1R8		DQ1R8
B3	VREFB3N0 IO	<u>o</u>	LVDS33n		26	138 F15	15 DQ1R3	DQ0R7	DQ1R7	DQ0R7	DQ1R7
B3	VREFB3N0 IO	OI	LVDS33p			139 F16	16	DQ0R6	DQ1R6	DQ0R6	DQ1R6
B3	VREFB3N0 GND	GND			86	140					
B3	VREFB3N0 IO	OI	LVDS32n			141 J11	11	DQ0R5	DQ1R5	DQ0R5	DQ1R5
B3	<b>VREFB3N0</b>	OI	LVDS32p			142 H11	11	DQ0R4	DQ1R4	DQ0R4	DQ1R4
B3	<b>VREFB3N0</b>	OI	LVDS31n			143 G12	12	DQ0R3	DQ1R3	DQ0R3	DQ1R3
B3	<b>VREFB3N0</b>	OI	LVDS31p			144 G13	13	DQ0R2	DQ1R2	DQ0R2	DQ1R2
B3	<b>VREFB3N0</b>	OI	VREFB3N0		66	145 H13	13				
B3	<b>VREFB3N0</b>	OI	LVDS30n		100	146 D15	15 DQ1R2	DQ0R1	DQ1R1	DQ0R1	DQ1R1
B3	<b>VREFB3N0</b>	OI	LVDS30p		101	147 D	D16 DQ1R1	DQ0R0	DQ1R0	DQ0R0	DQ1R0
B3	VREFB3N0	VCCIO3			102	148					
B3	<b>VREFB3N0</b>	OI				Е	E16				
B3	VREFB3N0 IO	OI	LVDS29n			149 C14	14				
B3	VREFB3N0 IO	<u>O</u>	LVDS29p			150 D13	13				
B3	VREFB3N0 IO	OI	PLL2_OUTp		103	151 E14	14 DQ1R0				
B3	VREFB3N0 IO	OI	PLL2_OUTn		104	152 D14	14				
B3	VREFB3N0 GND	GND			105	153					
B3	<b>VREFB3N0</b>	GND_PLL2			106	154 F12	12				
B3	<b>VREFB3N0</b>	VCCD_PLL2			107	155 F11	11				
B3	<b>VREFB3N0</b>	GND_PLL2			108	156 D12	12				
B2	VREFB2N0	VCCA_PLL2			109	157 E	E12				
B2	VREFB2N0	GNDA_PLL2			110		E11				
B2	VREFB2N0	GND			111	159					
B2	VREFB2N0 IO	O	LVDS28n		112	160 B14	14				
B2	VREFB2N0 IO	OI	LVDS28p		113	161 A14	14	DQ0T0	DQ1T0	DQ0T0	DQ1T0
B2	VREFB2N0 IO	OI	LVDS27n		114	162 C13	13	DQ0T1	DQ1T1	DQ0T1	DQ1T1
B2	VREFB2N0 10	OI	LVDS27p		115	163 C12	12	DQ0T2	DQ1T2	DQ0T2	DQ1T2
B2	VREFB2N0	0	LVDS26n			164 B13	13	DQ0T3	DQ1T3	DQ0T3	DQ1T3
B2	VREFB2N0	<u>O</u>	LVDS26p			165 A13	13	DQ0T4	DQ1T4	DQ0T4	DQ1T4
B2	VREFB2N0 VCCIO2	VCCI02			116	166					

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Function      Function      Function      Function      T144      Q208        OND      LVDS26n      117      167      11      167      11      167      11      167      11      167      167      167      167      167      167      167      167      167      167      167      167      167      167      167      167      167      167      167      167      167      167      167      167      167      167      167      167      167      167      167      167      167      167      167      167      167      167      167      167      167      167      167      167      167      167      167      167      167      167      167      167      167      167      167      167      167      167      167      167      167      167      167      167      167      167      167      167      167      167      167      167      167      167      167      167      167      167	VREFB Pin N	Pin Name / Optional Function(s) Configuration	Configuration	T144 Q2	08 F256	T144 Q208 F256 DQS for x8/x9 in	DQS for x8/x9 in	DQS for x16/x18	DQS for x8/x9 in	DQS for x16/x18
WREEBAND (OND)      LVDSZBA      117 167      167        WREEBAND (OND)      LVDSZBA      118 168 B12      PPCLK8DOSOT        WREEBAND (OND)      LVDSZBA      119 169 A12      DPCLK8DOSOT        WREEBAND (OND)      LVDSZBA      120 170 C11      DPCLK8DOSOT        WREEBAND (SCO)      LVDSZBA      121 171 G10      DOOT6        WREEBAND (SCO)      LVDSZBA      122 173 G11      DOOT6        WREEBAND (SCO)      LVDSZBA      122 173 G11      DOOT6        WREEBAND (SCO)      LVDSZBA      176 B10      DOOT6        WREEBAND (SCO)      LVDSZBA      178 B10      DOOT6        WREEBAND (SCO)      LVDSZBA      172 B10      DOT7        WREEBAND (SCO)      LVDSZBA      122 B16      DOT7        WREEBAND (SCO)      LVDSZBA      122 B16      DOT7        WREEBAND (SCO)      LVDSZBA      122 B178      DOT7        WR		tion	Function			T144	Q208	in Q208	F256	in Q208
WREFERENO (AND)      LVDSZBA      117      167        VREFERENO (OC)      LVDSZBA      119      168 B12      DPCLK8/DOSOT        VREFERENO (OC)      LVDSZBA      119      168 B12      DPCLK8/DOSOT        VREFERENO (OC)      LVDSZBA      120      177 G10      DOOTS        VREFERENO (CC)O2      LVDSZBA      121      177 G10      DOOTS        VREFERENO (CC)O2      LVDSZBA      178 G11      DOOTS        VREFERENO (CC)O2      LVDSZBA      178 G10      DOOTT        VREFERENO (CC)O2      LVDSZBA      178 G10      DOOTT        VREFERENO (CC)O2      LVDSZBA      122 G19      DOTT        VREFERENO (CC)O2      LVDSZBA					B11					
WREFERIND      IO      LVDS26h      118      168 B12      PCLK8DQS0T      DPCLK8DQS0T        WREFBZNO IO      LVDS26h      119      169 A12      IPCLK8DQS0T      DPCLK8DQS0T        WREFBZNO IO      LVDS24h      120      170 C11      DQ0T6      DQ0T6        WREFBZNO IO      LVDS24h      122      173 G11      DQ0T6      DQ0T6        WREFBZNO IO      LVDS23h      172 B10      DQ0T6      DQ0T6      DQ0T6        WREFBZNO IO      LVDS23h      173 B10      DQ0T7      DQ0T7      DQ0T7        WREFBZNO IO      LVDS22h      173 B10      DQ0T7      DQ0T7      DQ0T7        WREFBZNO IO      LVDS22h      172 B10      DQ0T7      DQ0T7      DQ0T7        WREFBZNO IO      LVDS22h      122 B18      F9      DQ0T7      DQ0T7        WREFBZNO IO      LVDS22h      122 B18      TR      DQ0T7      DQ0T7        WREFBZNO IO      LVDS20h      LVDS20h      128 B2      DQ0T7      DQ0T7        WREFBZNO IO      LVDS20h      LVDS20h      LVDS20h      LVDS20h      DQ0T7      DQ0T7<					191					
WREFBZNO IO      LVDS25P      119 169 A12      IPOCLK8DOSOT      DPCLK8DOSOT        VREFBZNO IO      VREFBZNO IO      VREFBZNO IO      VREFBZNO IO      DO075        VREFBZNO IO      LVDS24P      121 171 G10      DO076        VREFBZNO IO      LVDS23P      122 173 G11      DO076        VREFBZNO IO      LVDS23P      172 B10      DO076        VREFBZNO IO      LVDS23P      172 B10      DO077        VREFBZNO IO      LVDS23P      172 B10      DO077        VREFBZNO IO      LVDS23P      172 B10      DO077        VREFBZNO IO      LVDS22P      172 B10      DO077        VREFBZNO IO      LVDS22P      122 177      PF0        VREFBZNO IO      LVDS22P      122 B10      DO077        VREFBZNO IO      LVDS22P      126 B10      DO170        VREFBZNO IO      LVDS22P      126 B10      DO170        VREFBZNO IO      LVDS20P      126 B20      DO170        VREFBZNO IO      LVDS20P      127 B1      B2        VREFBZNI IO      LVDS20P      128 B2      DO171        VREFBZNI		LVDS25n			168 B12				DQ0T5	DQ1T5
WREFBZNO (ODDORS)      VREFBZNO (ODDORS)		LVDS25p			169 A12	DPCLK8/DQS0T	DPCLK8/DQS0T	DPCLK8/DQS0T	DPCLK8/DQS0T	DPCLK8/DQS0T
WREFBEND IO      POOTF        VREFBEND GND      LVDS23h      12      173 G11      DOOTF      DOOTF        VREFBEND GND      LVDS23h      174 B10      DOOTT      DOOTT        VREFBEND GND      LVDS22h      175 B10      DOOTT        VREFBEND GND      LVDS22h      178 A10      DOOTT        VREFBEND GND      LVDS22h      173 A7      DOOTT        VREFBEND GND      LVDS22h      173 A7      DOOTT        VREFBEND GND      LVDS21h      124 A7      P        VREFBEND GND      LVDS21h      126 A7      DOTT        VREFBEND GND      LVDS20h      182 B9      DOTT        VREFBEND GND      LVDS30h      182 B9      DOTT        VREFBEND GND      LVDS30h      122 BB B9      DOTT					A11					
WREFBAND IO      LVDS24n      121      171 G10      DO0T6        WREFBAND (CCOQ)      LVDS24p      12      173 G11      DO0T6        WREFBAND (GND      LVDS23n      174      DO0T6      DO0T6        WREFBAND (IO      LVDS23p      175 B10      DO0T7        WREFBAND (IO      LVDS22p      175 A10      DO0T7        WREFBAND (IO      LVDS22p      173 A7      DO0T7        WREFBAND (IO      LVDS22p      172 A10      DO0T7        WREFBAND (IO      LVDS21p      124 A10      DO0T7        WREFBAND (IO      LVDS21p      12      178 B10      DO0T0        WREFBAND (IO      LVDS21p      12      178 B10      DO0T0        WREFBAND (IO      LVDS21p      12      120 B0      DO0T0        WREFBAND (IO      LVDS20p      12      127 B10      DO0T0        WREFBAND (IO      LVDS20p      12      182 B9      DO0T0        WREFBAND (IO      LVDS30p      12      182 B9      DO0T0        WREFBAND (IO      LVDS30p      13      186 B7      DO0T1		VREFB2N0			170 C11					
WREFBAND (ACCIOS)      LVDS24p      122      173 G11      DQ0T6        VREFBAND (SND)      LVDS23n      175 B10      DQ0T7        VREFBAND (SND)      LVDS22p      175 B10      DQ0T7        VREFBAND (SND)      LVDS22p      177 F10      DQ0T7        VREFBAND (SND)      LVDS22p      177 F10      DQ0T7        VREFBAND (SND)      LVDS22p      178 F10      DQ0T7        VREFBAND (SND)      LVDS21n      123 177 F10      DQ0T0        VREFBAND (SND)      LVDS21n      123 178 F10      DQ0T0        VREFBAND (SND)      LVDS21n      125 179 D11 DQ0T0      DM0T        VREFBAND (SND)      LVDS22p      126 89      DM0T        VREFBAND (SND)      LVDS20n      127 (183)      DM0T        VREFBAND (SOD)      LVDS20n      127 (183)      DM0T        VREFBAND (SOD)      LVDS20n      127 (183)      DM0T        VREFBAND (SOD)      LVDS19p      128 184      DM0T        VREFBAND (SOD)      LVDS19p      128 184      DM0T        VREFBAND (SOD)      LVDS18p      131 130      DM0T	VREFB2N0 IQ	LVDS24n			171 G10		DQ0T5	DQ1T5		
WREFBAND      IO      LVDS24p      122      173      Color      DO0TO        VREFBAND      IO      LVDS23n      176      A10      DO0T7        VREFBAND      IO      LVDS23n      176      A10      DO0T7        VREFBAND      IO      LVDS22p      173      A77      A78      A10        VREFBAND      IO      LVDS22p      124      178      A17	VREFB2N0 VCCI	03		Ú	172					
WRERBAND GND      LVDS23n      175 B10      DOUT7        VREFBZND IO      LVDS22n      175 B10      DOUT7        VREFBZND IO      LVDS22n      175 B10      DOUT7        VREFBZND GND      LVDS22p      123 177      F9      DOUT7        VREFBZND IO      LVDS22p      124 178      DOUT0      DOUT7        VREFBZND IO      LVDS21n      124 178      DOUT0      DOUT0        VREFBZND IO      LVDS21p      125 179 D11 DOUT0      DOUT0      DOUT0        VREFBZND IO      LVDS20p      126 180 D01 DOUT1      DOUT0      DOUT0        VREFBZND IO      LVDS20p      127 183 B9      DOUT0      DOUT0        VREFBZNI IO      LVDS20p      128 184 B9      DOUT0      DOUT0        VREFBZNI IO      LVDS19p      128 184 B9      DOUT0      DOUT0        VREFBZNI IO      LVDS19p      180 D0      DOUT1      DOUT1        VREFBZNI IO      LVDS18p      180 D0      DOUT1      DOUT1        VREFBZNI IO      LVDS18p      181 B7      DOUT1      DOUT1        VREFBZNI IO      LVDS17p      <	VREFB2N0 IO	LVDS24p			173 G11		DQ0T6	DQ1T6	DQ0T6	DQ1T6
WREFBZNO IO      LVDS23h      176 B10      D0077        VREFBZNO IO      LVDS22h      176 A10      D0077        VREFBZNO IO      LVDS22h      123 177      F0        VREFBZNO IO      LVDS22p      124 178      P0        VREFBZNO IO      LVDS21h      124 178      D010        VREFBZNO IO      LVDS21h      125 179 D11      D010        VREFBZNO IO      LVDS21h      125 179 D11      D0171        VREFBZNO IO      LVDS20h      181 A9      D0171        VREFBZNO IO      LVDS20h      182 B9      D0170        VREFBZNI IO      LVDS19h      127 (83)      D0172      D0110        VREFBZNI IO      LVDS19h      186 B7      D0112      D0112        VREFBZNI IO      LVDS19h      187 A      D0112      D0113        VREFBZNI IO      LVDS18h      188 B7      D0112        VREFBZNI IO      LVDS18h      188 B7      D0112        VREFBZNI IO      LVDS18h      188 B7      D0112        VREFBZNI IO      LVDS18h      189 B7      D0112        VREFBZNI IO      <	VREFB2N0 GND			-	174					
WREFBZNO IO      LVDS23P      176 A10        VREFBZNO IO      LVDS2ZD      123        VREFBZNO IO      LVDS2ZP      124        VREFBZNO IO      LVDS2ZP      124        VREFBZNO IO      LVDS2ZD      124        VREFBZNO IO      LVDS2ZD      126        VREFBZNO IO      LVDS2ZD      127        VREFBZNO IO      LVDS2ZD      128        VREFBZNI IO      LVDS2ZD      127        VREFBZNI IO      LVDS2ZD      128        VREFBZNI IO      LVDS1BD      138        VREFBZNI IO      LVDS1BD      138        VREFBZNI IO      LVDS1BD      138        VREFBZNI IO      LVDS1BD      131        VREFBZNI IO      LVDS1BD      132        VREFBZNI IO      LVDS1BD      132        VREFBZNI IO      LVDS1D      134        VREFBZNI IO      LVDS1D	VREFB2N0 IO	LVDS23n		-	175 B10		DQ0T7	DQ1T7	DQ0T7	DQ1T7
WREFBZNO GND      LVDS22h      123      177      F9        VREFBZNO GND      LVDS22p      123      177      F9        VREFBZNO VCCINT      LVDS21h      124      178      P        VREFBZNO GND      LVDS21h      125      179      DMOT      DMOT        VREFBZNO GND      LVDS21h      125      179      DMOT      DMOT        VREFBZNO GND      LVDS20h      126      180      DMOT      DMOT        VREFBZNO GND      LVDS20h      127      181      DMOT      DMOT        VREFBZNO GND      LVDS20h      128      184      DMOT      DMOT        VREFBZNI GND      LVDS19h      128      184      DMOT      DMOT        VREFBZNI GND      LVDS18h      188      DMOT      DMOT      DMOT        VREFBZNI IO      LVDS18h      188      DMOT      DMOT      DMOT      DMOT        VREFBZNI IO      LVDS18h      132      182      DMOT		LVDS23p		-	176 A10			DQ1T8		DQ1T8
VREFBZNO GND      LVDS22p      123      177      F9      CONTRACT CONTRAC		LVDS22n			F10					
WREFBZNO IO      LVDS22p      F9      F9        VREFBZNO VCCINT      124      178      P        VREFBZNO IO VCCIOZ      128      179      D        VREFBZNO IO VCCIOZ      120      LVDS21h      D      D        VREFBZNO IO VCCIOZ      120      LVDS20h      126      180      DO      D        VREFBZNO IO VCCIOZ      120      LVDS20h      126      180      DO      D      D        VREFBZNO IO VCCIOZ      120      LVDS20h      126      180      DO      D      D      D      D      D      D      D      D      D      D      D      D      D      D      D      D      D      D      D      D      D      D      D      D      D      D      D      D      D      D      D      D      D      D      D      D      D      D      D      D      D      D      D      D      D      D      D      D      D      D      D      D      D      D					122					
VREFBZN0 (VCCINT)      124 178      178      (Coloration)	_	LVDS22p			F9					
VREFEZNO (NCCIO2      VREFEZNO (SND      LVDS21n      125      179      D11      DQ1T0      DM0T        VREFEZNO (SND      LVDS21n      126      180      D10      DQ1T1      DQ1T1        VREFEZNO (SOCIOZ)      LVDS20n      126      181      A9      DQ1T1      DQ1T0        VREFEZNO (SCIOZ)      LVDS20p      127      182      B9      DQ1T2      DQ1T0        VREFEZNI (SND      LVDS19n      128      184      DQ1T2      DQ1T0        VREFEZNI (SND      LVDS19n      188      B7      DQ1T1        VREFEZNI (SND      LVDS18n      188      B7      DQ1T2        VREFEZNI (O      LVDS18n      189      DQ1T2      DQ1T2        VREFEZNI (O      LVDS18n      189      DQ1T2      DQ1T4        VREFEZNI (O      LVDS18n      189      DQ1T4      DQ1T4        VREFEZNI (O      LVDS18n      131      190      DQ1T4        VREFEZNI (O      LVDS17p      132      186      DQ1T4      DQ1T4        VREFEZNI (O      LVDS17p      LYB-R      DQ1T4	VREFB2N0 VCCI	TA			178					
VREFBZNO      GND      LVDS21n      125      179      D11      D01T0      DM0T        VREFBZNO      IO      LVDS21p      126      180      D10      D01T1      DM0T        VREFBZNO      IO      LVDS20p      128      181 A9      M0T      M0T        VREFBZNI      GND      LVDS20p      128      182 B9      M0T      M0T        VREFBZNI      GND      LVDS20p      128      184 B      M0T      M0T        VREFBZNI      GND      LVDS19p      187 A7      M0T      M0T      M0T        VREFBZNI      IO      LVDS18p      188 B7      M0T      M0T        VREFBZNI      IO      LVDS18p      189 F7      M0T      M0T        VREFBZNI      IO      LVDS18p      191 F8      M0T      M0T        VREFBZNI      IO      LVDS18p      134 B6      M0T      M0T        VREFBZNI      IO      LVDS17p      134 B6      M0T      M0T        VREFBZNI      IO      LVDS17p      M0T      M0T      M0T      M0	VREFB2N0 VCCI	02								
VREFBZN0 IO      LVDS21n      125      179 D11      DQ1T0      DM0T        VREFBZN0 IO      LVDS20n      181 A9      181 A	VREFB2N0 GND									
VREFBZNO      IO      LVDS21p      126      180      Dto      Dto <th< td=""><td>VREFB2N0 IO</td><td>LVDS21n</td><td></td><td></td><td>179 D11</td><td>DQ1T0</td><td>DM0T</td><td>DM1T0/BWS#1T0</td><td>DMOT</td><td>DM1T0/BWS#1T0</td></th<>	VREFB2N0 IO	LVDS21n			179 D11	DQ1T0	DM0T	DM1T0/BWS#1T0	DMOT	DM1T0/BWS#1T0
VREFBZN0 IO      LVDS20n      181 A9        VREFBZN1 VCCIO2      LVDS20p      127 (183)        VREFBZN1 GND      LVDS19n      128 184        VREFBZN1 GND      LVDS19n      130 186        VREFBZN1 IO      LVDS19n      188 B7        VREFBZN1 IO      LVDS18n      181 A7        VREFBZN1 IO      LVDS18n      181 F8        VREFBZN1 IO      LVDS18n      191 F8        VREFBZN1 IO      LVDS18p      191 F8        VREFBZN1 IO      LVDS18p      191 F8        VREFBZN1 IO      LVDS17n      132 192 D8        VREFBZN1 IO      LVDS17n      133 193 B6      DQ1174        VREFBZN1 IO      LVDS17n      134 195 A5      DQ1174        VREFBZN1 IO      LVDS17p      134 195 A6      DQ1174        VREFBZN1 IO      LVDS17p      136 A6      DQ1174	VREFB2N0 IO	LVDS21p			180 D10					
VREFBZN1      LVDS20p      LVDS20p      127      (183)      Medical Procession of the Proce	VREFB2N0 IO	LVDS20n		1	181 A9					
VREFBZN1 (CCIO2)      127 (183)      128 (184)      128 (184)      128 (184)      128 (184)      128 (184)      128 (184)      128 (184)      128 (184)      128 (184)      128 (184)      128 (184)      128 (184)      128 (184)      128 (184)      128 (184)      128 (184)      128 (184)      128 (184)      128 (184)      128 (184)      128 (184)      128 (184)      128 (184)      128 (184)      128 (184)      128 (184)      128 (184)      128 (184)      128 (184)      128 (184)      128 (184)      128 (184)      128 (184)      128 (184)      128 (184)      128 (184)      128 (184)      128 (184)      128 (184)      128 (184)      128 (184)      128 (184)      128 (184)      128 (184)      128 (184)      128 (184)      128 (184)      128 (184)      128 (184)      128 (184)      128 (184)      128 (184)      128 (184)      128 (184)      128 (184)      128 (184)      128 (184)      128 (184)      128 (184)      128 (184)      128 (184)      128 (184)      128 (184)      128 (184)      128 (184)      128 (184)      128 (184)      128 (184)      128 (184)      128 (184)      128 (184)      128 (184)      128 (184)		LVDS20p		,	182 B9					
VREFB2N1 GND      LVDS19n      129      185      AR      DQ1T2      DQ1T0      I        VREFB2N1 GND      LVDS19n      130      186      DQ1T2      DQ1T0      I        VREFB2N1 IO      LVDS19n      188      DQ1T1      I        VREFB2N1 IO      LVDS18n      188      DQ1T2      I        VREFB2N1 IO      LVDS18n      DQ1T2      I        VREFB2N1 IO      LVDS18p      191      DQ1T3      I        VREFB2N1 IO      LVDS17n      132      192      DB      DA1T3      I        VREFB2N1 IO      LVDS17n      133      193      BG      DQ1T4      I        VREFB2N1 IO      LVDS17p      134      195      DQ1T4      DQ1T5      I        VREFB2N1 IO      LVDS17p      136      DQ1T4      DQ1T5      I        VREFB2N1 IO      LVDS17p      196      DQ1T4      DQ1T5      I	~	02)		)	(83)					
VREFB2N1 IO      LVDS19n      130      185 A8      DQ1T2      DQ1T0      I        VREFB2N1 IO      LVDS19n      187 A7      DQ1T1      DQ1T1      I        VREFB2N1 IO      LVDS18n      189 F7      DQ1T2      I        VREFB2N1 IO      LVDS18p      131 190      DQ1T2      I        VREFB2N1 IO      LVDS18p      191 F8      DQ1T3      I        VREFB2N1 IO      LVDS17p      132 192 D8      DQ1T3      I        VREFB2N1 IO      LVDS17p      133 193 B6      DQ1T3      I        VREFB2N1 IO      LVDS17p      134 195 A6      DQ1T4      I        VREFB2N1 IO      LVDS17p      134 195 A6      DQ1T4      DQ1T5      I        VREFB2N1 IO      LVDS17p      196      DQ1T5      I					184					
VREFB2N1 GND      LVDS19n      130      186      DQ1T1        VREFB2N1 IO      LVDS19n      187 A7      DQ1T1      I        VREFB2N1 IO      LVDS18n      189 F7      DQ1T2      I        VREFB2N1 IO      LVDS18p      131      190      DQ1T3      I        VREFB2N1 IO      LVDS17p      132      192 D8      DQ1T3      I        VREFB2N1 IO      LVDS17p      133      193 B6      DQ1T3      I        VREFB2N1 IO      LVDS17p      134      195 A6      DQ1T4      I        VREFB2N1 IO      LVDS17p      134      195 A6      DQ1T4      I        VREFB2N1 IO      LVDS17p      136      DQ1T4      DQ1T5      I					185 A8	DQ1T2	DQ1T0	DQ1T9		
VREFB2N1 IO      LVDS19n      187 A7      DQ1T1      I        VREFB2N1 IO      LVDS18n      189 F7      DQ1T2      I        VREFB2N1 VCINT      LVDS18n      131 190      DQ1T2      I        VREFB2N1 VCINT      LVDS18p      191 F8      DQ1T3      I        VREFB2N1 IO      LVDS17n      132 192 D8      DQ1T3      I        VREFB2N1 IO      LVDS17n      133 193 B6      DQ1T3      I        VREFB2N1 IO      LVDS17p      134 195 A6      DQ1T4      DQ1T5      I        VREFB2N1 IO      LVDS17p      136 A6      DQ1T4      DQ1T5      I					186					
VREFB2N1 IO      LVDS18p      188 B7      DQ1T1      I        VREFB2N1 IO      LVDS18n      139 F7      DQ1T2      I        VREFB2N1 VCINT      LVDS18p      191 F8      DQ1T3      I        VREFB2N1 IO      LVDS18p      132 192 D8      DQ1T3      I        VREFB2N1 IO      LVDS17n      133 193 B6      DQ1T3      I        VREFB2N1 IO      LVDS17p      134 195 A6      DQ1T4      I        VREFB2N1 IO      LVDS17p      134 195 A6      DQ1T4      DQ1T5      I        VREFB2N1 IO      LVDS17p      196      DQ1T5      I		LVDS19n		,-	187 A7				DQ1T0	DQ1T9
VREFB2N1 IO      LVDS18n      131 190      DQ1T2      I        VREFB2N1 VCCINT      LVDS18p      191 F8      DQ1T3      I        VREFB2N1 IO      LVDS18p      132 192 D8      DQ1T3      I        VREFB2N1 IO      LVDS17n      133 193 B6      DQ1T3      I        VREFB2N1 IO      LVDS17p      134 195 A6      DQ1T4      I        VREFB2N1 IO      LVDS17p      134 195 A6      DQ1T4      I	VREFB2N1 IO	LVDS19p		,-	188 B7		DQ1T1	DQ1T10	DQ1T1	DQ1T10
VREFB2N1      VCCINT      LVDS18p      191 F8      DQ1T3      DQ1T3      DQ1T3      DQ1T3      DQ1T3      DQ1T4      DQ1T4      DQ1T4      DQ1T4      DQ1T4      DQ1T5	VREFB2N1 IO	LVDS18n		1	189 F7		DQ1T2	DQ1T11	DQ1T2	DQ1T11
VREFBZN1 IO      LVDS18p      191 F8      DQ1T3      I        VREFBZN1 IO      VREFBZN1 IO      LVDS17n      133 193 B6      DQ1T3      DQ1T4      I        VREFBZN1 IO      LVDS17p      134 195 A6      DQ1T4      I        VREFBZN1 IO      LVDS17p      134 195 A6      DQ1T4      I        VREFBZN1 IO      LVDS17p      196      DQ1T5      I	VREFB2N1 VCCI	_			190					
VREFBZN1      IO      VREFBZN1      IO      LVDS17n      132      192      D8      DQ1T4      I        VREFBZN1      IO      LVDS17n      133      193      B6      DQ1T3      DQ1T4      I        VREFBZN1      IO      LVDS17p      134      195      A6      DQ1T5      I        VREFBZN1      GND      LVDS17p      196      DQ1T5      I		LVDS18p		1	191 F8		DQ1T3	DQ1T12	DQ1T3	DQ1T12
VREFB2N1 IO      LVDS17n      133      193 B6      DQ1T3      DQ1T4      I        VREFB2NK VCCIO2 VREFB2N1 IO      LVDS17p      134      195 A6      DQ1T4      DQ1T5      I        VREFB2N1 GND      LVDS17p      196      LVDS17p		VREFB2N1			192 D8					
VREFB2N (VCCIO2)      LVDS17p      134 195 A6      DQ1T4      DQ1T5        VREFB2N1 GND      196      196      196					193 B6	DQ1T3	DQ1T4	DQ1T13	DQ1T4	DQ1T13
VREFB2N1 IO      LVDS17p      134 195 A6      DQ1T4      DQ1T5        VRFFB2N1 GND      196      196      196      196      196      196      196      196      196      196      196      196      196      196      196      196      196      196      196      196      196      196      196      196      196      196      196      196      196      196      196      196      196      196      196      196      196      196      196      196      196      196      196      196      196      196      196      196      196      196      196      196      196      196      196      196      196      196      196      196      196      196      196      196      196      196      196      196      196      196      196      196      196      196      196      196      196      196      196      196      196      196      196      196      196      196      196      196 <t< td=""><td></td><td><math>\wedge</math></td><td></td><td><math>\mathcal{L}</math></td><td>194</td><td></td><td></td><td></td><td></td><td></td></t<>		$\wedge$		$\mathcal{L}$	194					
VREEB2N1 GND		LVDS17p			195 A6	DQ1T4	DQ1T5	DQ1T14	DQ1T5	DQ1T14
	VREFB2N1 GND			_	196					

REAL MANABEL GROUP   Function      Function      Function      Function      Function      Fase      in        REAL MEREDARI   COLUMNISTION   LVDS16h      LVDS16h      1005 (6)      1005 (6)      1005 (6)      1005 (6)      1005 (6)      1005 (6)      1005 (6)      1005 (6)      1005 (6)      1005 (6)      1005 (6)      1005 (6)      1005 (6)      1005 (6)      1005 (6)      1005 (6)      1005 (6)      1005 (6)      1005 (6)      1005 (6)      1005 (6)      1005 (6)      1005 (6)      1005 (6)      1005 (6)      1005 (6)      1005 (6)      1005 (6)      1005 (6)      1005 (6)      1005 (6)      1005 (6)      1005 (6)      1005 (6)      1005 (6)      1005 (6)      1005 (6)      1005 (6)      1005 (6)      1005 (6)      1005 (6)      1005 (6)      1005 (6)      1005 (6)      1005 (6)      1005 (6)      1005 (6)      1005 (6)      1005 (6)      1005 (6)      1005 (6)      1005 (6)      1005 (6)      1005 (6)      1005 (6)      1005 (6)      1005 (6)      1005 (6)      1005 (6)      1005 (6)      1005 (6)      1005 (6)      1005 (6)      1005 (6)      1005 (6)      1005 (6)      1005 (6)	Bank	VREFB	Pin Name /	Optional Function(s) Configuration T	Configuration	T144 C	208 F25	144 Q208 F256 DQS for x8/x9 in	DQS for x8/x9 in	DQS for x16/x18	DQS for x8/x9 in	DQS for x16/x18
VMERERAH   O	Number	Group	Function		Function			T144	Q208	in Q208	F256	in Q208
WREFERM IO VREFERM IO	B2	VREFB2N1	OI	LVDS16n			99					
WREFERMI (O.D.)      LVDS16n      197 D6      198 C6      197 D6      198 C6      <	B2	VREFB2N1		LVDS16p			C3					
WREFERM I OCCOL      LVDS14h      CG      CA      CA <td>B2</td> <td>VREFB2N1</td> <td></td> <td>LVDS15n</td> <td></td> <td></td> <td></td> <td></td> <td></td> <td></td> <td></td> <td></td>	B2	VREFB2N1		LVDS15n								
WREFERNI   O   LVDS14p   198   C6   C6   C6   C7   C7   C7   C7   C7	B2	VREFB2N1	VCCI02									
WREFERM I ON VORTHORM      LVDS14P      155      199 BG DATE      C4      CA	B2	VREFB2N1	OI	LVDS15p			198 C6					
WREFBANI IO      LVDS14h      CG	B2	VREFB2N1	GND									
WREFBRAH IO      LVDS14p      135      19 65      DOTT5      DOTT6      DOTT6      DOTT6      DOTT6      DOTT6      DOTT7	B2	VREFB2N1	OI	LVDS14n			C5					
WREFERM IO VREFERM IO VREFERM COLOZ VREFERM IO VREFERM IO VREFER	B2	VREFB2N1	OI	LVDS14p			C4					
WREFERAN IO VREFERAN IO VRCIOI VREFERAN IO VRCIOI VREFERAN IO VRCIOI VREFERAN IO VRCIOI VREFERAN IO VRCIOI VRCIOI VREFERAN IO VRCIOI VRCIOI VREFERAN IO VRCIOI VRCIOI VRCIOI VREFERAN IO VRCIOI VRCIOI VRCIOI VRCIOI VRCIOI VRCIOI VRCIOI VRCIOI VRCIOI VRCIOI VRCIOI VRCIOI VRCIOI VRCIOI VRCIOI VRCIOI VRCIOI VRCIOI VRCIOI VRCIOI VRCIOI VRCIOI VRCIOI VRCIOI VRCIOI VRCIOI VRCIOI VRCIOI VRCIOI VRCIOI VRCIOI VRCIOI VRCIOI VRCIOI VRCIOI VRCIOI VRCIOI VRCIOI VRCIOI VRCIOI VRCIOI VRCIOI VRCIOI VRCIOI VRCIOI VRCIOI VRCIOI VRCIOI VRCIOI VRCIOI VRCIOI VRCIOI VRCIOI VRCIOI VRCIOI VRCIOI VRCIOI VRCIOI VRCIOI VRCIOI VRCIOI VRCIOI VRCIOI VRCIOI VRCIOI VRCIOI VRCIOI VRCIOI VRCIOI VRCIOI VRCIOI VRCIOI VRCIOI VRCIOI VRCIOI VRCIOI VRCIOI VRCIOI VRCIOI VRCIOI VRCIOI VRCIOI VRCIOI VRCIOI VRCIOI VRCIOI VRCIOI VRCIOI VRCIOI VRCIOI VRCIOI VRCIOI VRCIOI VRCIOI VRCIOI VRCIOI VRCIOI VRCIOI VRCIOI VRCIOI VRCIOI VRCIOI VRCIOI VRCIOI VRCIOI VRCIOI VRCIOI VRCIOI VRCIOI VRCIOI VRCIOI VRCIOI VRCIOI VRCIOI VRCIOI VRCIOI VRCIOI VRCIOI VRCIOI VRCIOI VRCIOI VRCIOI VRCIOI VRCIOI VRCIOI VRCIOI VRCIOI VRCIOI VRCIOI VRCIOI VRCIOI VRCIOI VRCIOI VRCIOI VRCIOI VRCIOI VRCIOI VRCIOI VRCIOI VRCIOI VRCIOI VRCIOI VRCIOI VRCIOI VRCIOI VRCIOI VRCIOI VRCIOI VRCIOI VRCIOI VRCIOI VRCIOI VRCIOI VRCIOI VRCIOI VRCIOI VRCIOI VRCIOI VRCIOI VRCIOI VRCIOI VRCIOI VRCIOI VRCIOI VRCIOI VRCIOI VRCIOI VRCIOI VRCIOI VRCIOI VRCIOI VRCIOI VRCIOI VRCIOI VRCIOI VRCIOI VRCIOI VRCIOI VRCIOI VRCIOI VRCIOI VRCIOI VRCIOI VRCIOI VRCIOI VRCIOI VRCIOI VRCIOI VRCIOI VRCIOI VRCIOI VRCIOI VRCIOI VRCIOI VRCIOI VRCIOI VRCIOI VRCIOI VRCIOI VRCIOI VRCIOI VRCIOI VRCIOI VRCIOI VRCIOI VRCIOI VRCIOI VRCIOI VRCIOI VRCIOI VRCIOI VRCIOI VRCIOI VRCIOI VRCI	B2	VREFB2N1	OI	LVDS13n		135	199 B5	DQ1T5			DQ1T6	DQ1T15
WREFERAM      IOO      LVDS12n      137      201 B4      DOTTO      DOTTO      DOTTO        VREFERAN      VCCIOLA      LVDS12p      138      2024      DOTTO      DOTTO      DOTTO        VREFERAN I OLITORISTO      LVDS11p      DEV CLR      142      204      DOTTO      DOTTO      DOTTO        VREFERAN I OLITORISTO      LVDS11p      DEV CLR      142      206 BA      DOTTO      DOTTO      DOTTO        VREFERAN I OLITORISTO      LVDS10p      LVDS10p      HA      206 BA      DOTTO      DOTTO      DOTTO        VREFERAN I OLITORISTO      LVDS10p      HA      206 BA      DATTEWS#1T      DATTEWS#1T      DATTEWS#1T      DATTEWS#1T        VRCINT      VCCINT      HA      206 BA      ACCINT      HA      ACCINT      ACCINT <t< td=""><td>B2</td><td>VREFB2N1</td><td>OI</td><td>LVDS13p</td><td></td><td>136</td><td>200 A5</td><td>DPCLK10/DQS1T</td><td>DPCLK10/DQS1T</td><td>DPCLK10/DQS1T</td><td>DPCLK10/DQS1T</td><td>DPCLK10/DQS1T</td></t<>	B2	VREFB2N1	OI	LVDS13p		136	200 A5	DPCLK10/DQS1T	DPCLK10/DQS1T	DPCLK10/DQS1T	DPCLK10/DQS1T	DPCLK10/DQS1T
WREFBANG      VOCIO2      138      Co202      138      Co203      14      DO117      DO1176      DO1176      DO1176      DO1176      DO1176      DO1176      DO1176      DO1177	B2	VREFB2N1		LVDS12n		137	201 B4	DQ1T6	DQ1T6	DQ1T15	DQ1T7	DQ1T16
WREFBANI IO      LVDS12p      139      203 A4      DO117      DO1176      DO1176      DO1178      DO1176      DO1178      DO1178      DO1177      DO1176      DO1178      DO1177      DO117	B2	VREFB2N	VCCI02			138	(202)					
WREFBANT GND      LVDS11p      140      204      DQ1T8      DQ1T8      DQ1T7      DMT/BWS#TT        VREFBANT GO      LVDS10p      LVDS10p      LVDS10p      142      205 R6      DM1T/BWS#TT      DM1T/BWS#TT      DM1T/BWS#TT        VREFBANT GO      LVDS10p      143      207 R6      DM1T/BWS#TT      DM1T/BWS#TT      DM1T/BWS#TT        VREFBANT GO      LVDS10p      144      208 R6      DM1T/BWS#TT      DM1T/BWS#TT      DM1T/BWS#TT        VRCOINT      VCCINT      HT0      HT0<	B2	VREFB2N1		LVDS12p		139	203 A4	DQ1T7	DQ1T7	DQ1T16	DQ1T8	DQ1T17
WREFBANI IO      LVDS11p      141      205 A3      DQ1T8      DQ1T8      DQ1T17      DM1T/BWS#1T        VREFBANI IO      LVDS10p      142      206 E3      DM1T/BWS#1T      DM1T/BWS#1T      DM1T/BWS#1T        VREFBANI IO      LVDS10p      144      208 F6      DM1T/BWS#1T      DM1T/BWS#1T      DM1T/BWS#1T        VREFBANI IO      LVDS10p      144      208 F6      DM1T/BWS#1T      DM1T/BWS#1T      DM1T/BWS#1T        VCCINT      VCCINT      HT      HT      M1      M1      M1      M1        VCCINT      VCCINT      KCINT      KG      KG      KG      KG      KG        VCCIO1      VCCIO1      KG      KG      KG      KG      KG      KG        VCCIO4      VCCIO4      KG      M1      KG      KG      KG      KG        VCCIO4      VCCIO4      KG      KG      KG      KG      KG      KG        VCCIO4      VCCIO4      KG      KG      KG      KG      KG      KG        VCCIO4      VCCIO4      KG <t< td=""><td>B2</td><td>VREFB2N1</td><td></td><td></td><td></td><td>140</td><td>204</td><td></td><td></td><td></td><td></td><td></td></t<>	B2	VREFB2N1				140	204					
VREFEADM IO      LVDS11n      DEV_CLRn      142      206      B3      DM1T/BWS#1T      DM1T/BWS#1T        VREFEAN IO      LVDS10n      LVDS10n      143      207 E6      DM1T/BWS#1T      DM1T/BWS#1T        VCCINT      CCINT      CCINT      H10      H10      DM1T/BWS#1T      DM1T/BWS#1T        VCCINT      CCINT	B2	VREFB2N1	OI	LVDS11p		141	205 A3	DQ1T8	DQ1T8	DQ1T17	DM1T/BWS#1T	DM1T1/BWS#1T1
VREFEZN1   O      LVDS10p      143      207 E6      DM1T/BWS#1T      DM1T/BWS#1T        VREFEZN1   O      LVDS10n      144      208 F6      M17      DM1T/BWS#1T      DM1T/BWS#1T        VCCINT      VCCINT      H7      H7      M10      M10 <td>B2</td> <td>VREFB2N1</td> <td>OI</td> <td>LVDS11n</td> <td>DEV_CLRn</td> <td>142</td> <td>206 B3</td> <td></td> <td></td> <td></td> <td></td> <td></td>	B2	VREFB2N1	OI	LVDS11n	DEV_CLRn	142	206 B3					
VREFBZN1      IO      LVDS10n      144      208        MOCGINT	B2	VREFB2N1	OI	LVDS10p		143	207 E6	DM1T/BWS#1T	DM1T/BWS#1T	DM1T1/BWS#1T1		
	B2	VREFB2N1	OI	LVDS10n		144	208 F6					
			VCCINT				69					
			VCCINT				H7					
			VCCINT				H10					
			VCCINT				J7					
			VCCI01				B1					
			VCCI01				G3					
			VCCI01				K3					
			VCCI01				꼰					
			VCCIO4				M7					
			VCCIO4				M10					
			VCCIO4				P7					
			VCCIO4				P10					
			VCCIO4				T2					
			VCCIO4				T15					
			VCCIO3				B16					
			VCCIO3				G14					
			VCCIO3				K14					
			VCCIO3				R16					

#### **MDTERM**

Bank \	VREFB	Pin Name /	Optional Function(s) Configuration	Configuration	T144 Q208	F256 DQ	T144 Q208 F256 DQS for x8/x9 in	DQS for x8/x9 in	DQS for x16/x18	DQS for x8/x9 in	DQS for x16/x18
Number	Group	Function		Function		T144			in Q208	F256	in Q208
		VCCI02				A2					
		VCCI02				A15					
		VCCI02				C7					
		VCCI02				C10					
		VCCI02				E7					
		VCCI02				E10					
		GND				89					
		GND				완					
		GND				6 H					
		GND				18					
		GND				A1					
		GND				A16					
		GND				B2					
		GND				B15					
		GND				80					
		GND				60					
		GND				E8					
		GND				E9					
		GND				H3					
		GND				H14					
		GND				J3					
		GND				114					
		GND				M8					
		GND				6W					
		GND				P8					
		GND				Ь9					
		GND				R2					
		GND				R15					
		GND				T1					
		GND				T16					
		GND				66					
		GND				K9					
		NC				B8					
		NC				C15					
		NC				C16					
		NC				D1					

### ADERA.

1															1								
DQS for x8/x9 in DQS for x16/x18	in Q208																						
DQS for x8/x9 in	F256																						
DQS for x16/x18	in Q208																						
T144 Q208 F256 DQS for x8/x9 in DQS for x8/x9 in DQS for x16/x18	Q208																						
DQS for x8/x9 in	T144																						
-256	•	D2	D7	60	E13	E15	F5	F13	F14	G4	9Н	J6	110	9X	K7	K8	K13	N3	N4	9N	ZN	P6	R6
208 F		_	]	]	E	E	F	_	_	)	_	,	,	_	_	1	1	7	7	_	_	F	F
144 G																							
Optional Function(s) Configuration																							
/ 6	Function	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC
VREFB	Group																						
Bank	Number																						

<sup>(1)</sup> If the dedicated CLK pins are not used to feed the global clock networks, they can be used as general-purpose input pins to feed core logic.

They do not have support for an I/O register.

### AD BRANG.

# Pin Information for the Cyclone™ II EP2C5 Device Final version 1.5

Pin Name	Pin Type (1st, 2nd, & 3rd Function)	Pin Description
		Supply and Reference Pins
VCCINT	Power	These are internal logic array voltage supply pins. VCCINT also supplies power to the input buffers used for the LVPECL, LVDS, HSTL and SSTL I/O standards. All VCCINT pins must be connected to 1.2 V.
VCCIO[18]	Power	These are I/O supply voltage pins for banks 1 through 8. Each bank can support a different voltage level. VCCIO supplies power to the output buffers for all I/O standards. VCCIO also supplies power to the input buffers used for the LVTTL, LVCMOS, 1.5 V, 1.8 V, 2.5 V, 3.3-V PCI, and 3.3-V PCI-X I/O
GND	Ground	Device ground pins. All GND pins should be connected to the board GND plane.
VREFB[1.4]N[01]	0/1	Input reference voltage for each I/O bank. If a bank is used for a voltage-referenced I/O standard, then these pins are used as the voltage-reference pins for that bank. All of the VREF pins within a bank are shorted together. VREF pins can be used as user I/O pins with slightly higher pin capacitance if the bank it resides does not use voltage-reference I/O standards. If VREF pins are not used, designers should connect them to either VCC or GND.
VCCA_PLL[14]	Power	Analog power for PLLs[14]. The designer must connect these pins to 1.2 V, even if the PLL is not used.
VCCD_PLL[14]	Power	Digital power for PLLs[14]. The designer must connect these pins to 1.2 V, even if the PLL is not used. Designer is advised to keep isolated from other VCC for better jitter performance.
GNDA_PLL[14]	Ground	Analog ground for PLLs[14]. The designer can connect this pin to the GND plane on the board.
GND_PLL[14]	Ground	Ground for PLLs[14]. The designer can connect this pin to the GND plane on the board.
NC	No Connect	No connect pins should not be connected on the board. They should be left floating.
	De	Dedicated Configuration/JTAG Pins
DCLK	Input (PS) Output (AS)	Dedicated configuration clock pin. In PS configuration, DCLK is used to clock configuration data from an external source into the Cyclone II device. In AS mode, DCLK is an output from the Cyclone II device that provides timing for the configuration interface. DCLK should not be left floating. Designer should drive it high or low, whichever is more convenient on the board.
DATA0	Input	Dedicated configuration data input pin. In serial configuration modes, bit-wide configuration data is received through this pin. In AS mode, DATA0 has an internal pull-up resistor that is always active.

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### **風口信記**

# Pin Information for the Cyclone™ II EP2C5 Device Final version 1.5

Pin Name	Pin Type (1st, 2nd, & 3rd Function)	Pin Description
MSEL[01]	Input	Configuration input pins that set the Cyclone II device configuration scheme. These pins must be hardwired to VCCPD or GND. The designer should connect MSEL[01] to 00 for AS, 10 for PS, 01 for Fast AS and 00 for JTAG-based Configuration.
nCE	Input	Dedicated active-low chip enable. When nCE is low, the device is enabled. When nCE is high, the device is disabled. In multi-device configuration, nCE of the first device is tied low while its nCEO pin drives the nCE of the next device in the chain. In single device configuration, nCE is tied low.
nCONFIG	Input	Dedicated configuration control input. Pulling this pin low during user-mode will cause the FPGA to lose its configuration data, enter a reset state & tri-state all I/O pins. Returning this pin to a logic high level will initiate reconfiguration. If the configuration scheme uses an enhanced configuration device or EPC2, nCONFIG can be tied directly to the configuration device's nINIT_CONF pin. If JTAG configuration is used, nCONFIG can be tied to VCC.
CONF_DONE	Bidirectional (open-drain)	This is a dedicated configuration status pin. As a status output, the CONF_DONE pin drives low before and during configuration. Once all configuration data is received without error and the initialization cycle starts, CONF_DONE is released. As a status input, CONF_DONE goes high after all data is received. Then the device initializes and enters user mode. It is not available as a user I/O pin. CONF_DONE should be pulled high by an external 10-k Ω pull-up resistor.
nCEO	Output	Output that drives low when device configuration is complete. During multi-device configuration, this pin feeds a subsequent device's nCE pin and must be pulled high to Vccio by an external $10k$ $\Omega$ pull-up resistor. During single device configuration and for the last device in multi-device configuration, this pin can be used as an user $I/O$ after configuration.
nSTATUS	Bidirectional (open-drain)	This is a dedicated configuration status pin. The FPGA drives nSTATUS low immediately after power-up and releases it after POR time. As a status output, the nSTATUS is pulled low if an error occurs during configuration. As a status input, the device enters an error state when nSTATUS is driven low by an external source during configuration or initialization. It is not available as a user I/O pin. nSTATUS should be pulled high by an external 10-k Ω pull-up resistor.
TCK	Input	Dedicated JTAG input pin. The JTAG circuitry can be disabled by connecting TCK to GND.
TMS	Input	Dedicated JTAG input pin. The JTAG circuitry can be disabled by connecting TMS to VCC.
TDI	Input	Dedicated JTAG input pin. The JTAG circuitry can be disabled by connecting TDI to VCC.
TDO	Output	Dedicated JTAG output pin. The JTAG circuitry can be disabled by leaving TDO unconnected.
		Clock and PLL Pins

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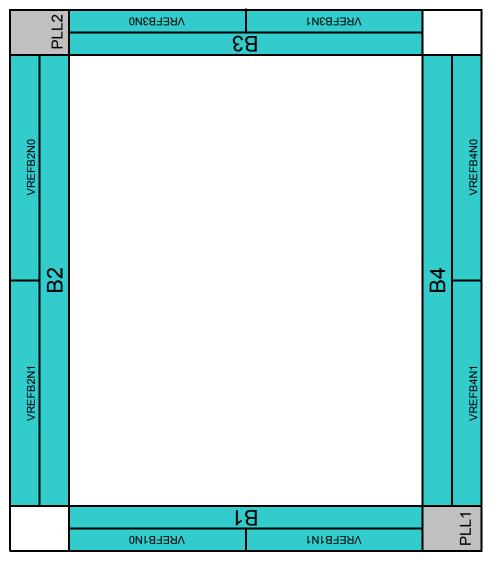
Pin Name	Pin Iype (1st, 2nd, & 3rd Function)	Pin Description
CLK[0.2,4,6,8,10,12,14], LVDSCLK[07]p	Clock, Input	Dedicated global clock input pins that can also be used for the positive terminal inputs for differential global clock input or user input pins.
CI KH 3579111315] I VDSCI KIO Zin	Clock Input	Dedicated global clock input pins that can also be used for the negative terminal inputs for differential clock input or user input pins
PLL[14]_OUTp	I/O, Output	Optional positive terminal for external clock outputs from PLL [14].
PLL[14]_OUTn	I/O, Output	Optional negative terminal for external clock outputs from PLL[14].
	Option	Optional/Dual-Purpose Configuration Pins
		Output control signal from the Cyclone II FPGA to the nCS pin of the serial configuration
		device in AS mode that enables the configuration device by driving it low. In AS mode, the
nCSO	Output	nCSO has internal weak pull-up resistor, which is always active.
		Output control signal from the Cyclone II FPGA to the serial configuration device in AS mode
ASDO	Output	which is always active.
acada Sas	+110 O/1	Active high signal that indicates that the error detection circuit has detected errors in the configuration SDAM bits. This pin is optional and is used when the CDC error detection circuit is enabled.
ראט באטא	I/O, Output	SKAM DIS. This pin is optional and is used when the CRC error detection circuit is enabled.
	I/O (when option off),	Optional chip-wide reset pin that allows you to override all clears on all device registers. When this pin is driven low, all registers are cleared; when this pin is driven high, all registers behave as programmed. The DEV_CLRn pin does not affect JTAG boundary-scan or programming operations. This pin is enabled
DEV_CLRn	Input (when option on)	by turning on the Enable device-wide reset (DEV_CLRn) option in the Quartus II software.
DEV_OE	I/O (when option off), Input (when option on)	Optional pin that allows you to override all tri-states on the device. When this pin is driven low, all I/O pins are tri-stated; when this pin is driven high, all I/O pins behave as defined in the design. This pin is enabled by turning on the Enable device-wide output enable (DEV_OE) option in the Quartus II software.
INIT_DONE	I/O, Output (open-drain)	This is a dual-purpose status pin and can be used as an I/O pin when not enabled as INIT_DONE. When enabled, a transition from low to high at the pin indicates when the device has entered user mode. If the INIT_DONE output is enabled, the INIT_DONE pin cannot be used as a user I/O pin after configuration. This pin is enabled by turning on the Enable INIT_DONE output option in the Quartus II software.
		Optional user-supplied clock input. Synchronizes the initialization of one or more devices. If this pin is not enabled for use as a user-supplied configuration clock, it can be used as a user I/O pin. This pin is enabled by turning on the Enable user-supplied start-up clock (CLKUSR) option in the Quartus II
CLKUSR	I/O, Input	software.
	Dual-Purpose L	Dual-Purpose Differential & External Memory Interface Pins

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	Pin Type (1st, 2nd, &	
Pin Name	3rd Function)	Pin Description
		Dual-purpose differential transmitter/receiver channels 0 to 59. These channels can be used for
		transmitting/receiving LVDS compatible signals. Pins with a "p" suffix carry the positive signal for the
		differential channel. Pins with an "n" suffix carry the negative signal for the differential channel. If not
LVDS[0-59][p,n]	I/O, TX/RX channel	used for differential signaling, these pins are available as user I/O pins.
		Dual-purpose DPCLK/DQS pins can connect to the global clock network for high-fanout control signals
		such as clocks, asynchronous clears, presets and clock enables. It can also be used as optional data
		strobe signal for use in external memory interfacing. These pins drive to dedicated DQS phase shift
DPCLK[0,1,2,4,6,7,8,10]/		circuitry, which allows fine tune of the phase shift for input clocks or strobes to properly align clock
DQS[[0,1]L,[1,0]B,[1,0]R,[0,1]T]	I/O, DPCLK/DQS	edges needed to capture data.
DQ1[B,R,T][017]	I/O, DQ	Optional data signal for use in external memory interfacing in the x16 or x18 modes.
DQ[0[B,R,T],1[B,L,R,T]][08]	I/O, DQ	Optional data signal for use in external memory interfacing in the x8 or x9 modes.
		Optional data mask pins for x16/x18 modes are required when writing to DDR SDRAM and DDR2
		SDRAM devices. A low signal indicates that the write is valid. If the DM signal is high, the memory
DM1[B,R,T][0,1]	I/O, DM	masks the DQ signals. Each group of DQ & DQS signals requires a DM pin.
		Optional data mask pins for x8/x9 modes are required when writing to DDR SDRAM and DDR2 SDRAM
		devices. A low signal indicates that the write is valid. If the DM signal is high, the memory masks the
DM[0[B,R,T],1[B,L,R,T]]	I/O, DM	DQ signals. Each group of DQ & DQS signals requires a DM pin.





- This is a top view of the silicon die.
  This is a pictoral representation only to get an idea of placement on the device. Refer to the pin list and the Quartus II software for exact locations.

AUTERA		Pin Information for the Cyclone™ II EP2C5 Device Final version 1.5
Version Number	Date	Changes Made
1.0	10/6/2004	Initial revision
1.1	1/18/2005	Added F256 package
1.2	2/24/2005	Modified Pin Definitions for DATA0 pin
1.3	5/3/2005	Added CRC_ERROR pin in Pin List and Pin Definition
		Changed pin name from GNDD_PLL and GNDG_PLL to GND_PLL
		Finalize
1.4	6/2/2005	Modified Pin Type column in Pin Definitions for VREFB[18]N[01] pins
1.5	2002/82/2	Modified LVDS naming in Pin List:
		LVDS12p/n to LVDS22p/n
		LVDS22p/n to LVDS21p/n
		LVDS21p/n to LVDS20p/n
		LVDS20p/n to LVDS19p/n
		LVDS19p/n to LVDS18p/n
		LVDS18p/n to LVDS17p/n
		LVDS11p/n to LVDS16p/n
		LVDS17p/n to LVDS15p/n
		LVDS10p/n to LVDS14p/n
		LVDS16p/n to LVDS13p/n
		LVDS15p/n to LVDS12p/n
		LVDS14p/n to LVDS11p/n
		LVDS13p/n to LVDS10p/n