```
0515  00                ;
  16  BC  PHI   RC      ;RC - Indexes bit pattern
  17  F8  LDI           ;Load RD
  18  04                ;With address
  19  BD  PHI   RD      ;Of CHIP-8 storage array
  1A  F8  LDI           ;     "      "       "
  1B  E3                ;     "      "       "
  1C  AD  PLO   RD      ;     "      "       "
  1D  9C  GHI   RC      ;Get address of bit pattern
  1E  5D  STR   RD      ;Store second address digit in array
  1F  1D  INC   RD      ;RD+1
0520  8C  GLO   RC      ;Second half of address
  21  F6  SHR           ;Shift right for third address digit
  22  F6  SHR           ;  "     "          "      "       "
  23  F6  SHR           ;  "     "          "      "       "
  24  F6  SHR           ;  "     "          "      "       "
  25  5D  STR   RD      ;Store in array
  26  1D  INC   RD      ;RD+1
  27  8C  GLO   RC      ;Second half of address - fourth address digit
  28  5D  STR   RD      ;Store in array (MSB's ignored by CHIP-8)
  29  1D  INC   RD      ;RD+1
  2A  9C  GHI   RC      ;Save RC for other machine language subroutines
  2B  5D  STR   RD      ; at 04E2 - 04E3
  2C  1D  INC   RD      ; "   "   "   "       "      "         "
  2D  8C  GLO   RC      ; "   "   "   "       "      "         "
  2E  5D  STR   RD      ; "   "   "   "       "      "         "
  2F  F8  LDI           ;Address bit pattern storage
0530  DA                ;
  31  AD  PLO   RD      ;RD=04DA
  32  F8  LDI           ;Load Utility
  33  04                ;Register with
  34  AF  PLO   RF      ;Loop count
  35  0C  LDN   RC      ;Get Bit pattern @ RC
  36  FA  ANI           ;And "AND" it with
  37  F0                ;F0 for MSB's
  38  5D  STR   RD      ;Store at RD for CHIP-8 DXYN instruction
  39  1D  INC   RD      ;RD+1 - next storage slot
  3A  4C  LDA   RC      ;Same bit pattern - advance pointer
  3B  FE  SHL           ;Shift left for LSB's
  3C  FE  SHL           ;  "     "        "
  3D  FE  SHL           ;  "     "        "
  3E  FE  SHL           ;  "     "        "
  3F  5D  STR   RD      ;Store @ RD for DXYN instruction
0540  1D  INC   RD      ;RD+1 - next storage slot
  41  2F  DEC   RF      ;Loop count (-1)
  42  8F  GLO   RF      ;Test if done
  43  3A  BNE           ;Branch if ≠ 00
  44  35                ;Loop until done to 0535
  45  12  INC   R2      ;Reset Stack Pointer
  46  D4  SEP   R4      ;Return control to CHIP-8
```