RadioGaGa

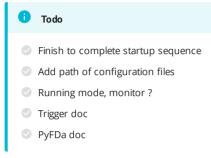
Radio Gammas Gerbe Atmosphériques

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1. Welcome to RadioGaGa documentation

Link: svn/NenuFar/trunk/receivers/RadioGAGA/doc/



This documentation uses mkdocs (documentation: mkdocs-material-docs) To avoid to install all dependencies needed, a dockerfile is set in the doc directory. You need to have docker installed on your machine.

You can download it here

For ubuntu :

sudo apt-get install \
apt-transport-https \
ca-certificates \
curl \
gnupg \
Isb-release

curl -fsSL https://download.docker.com/linux/ubuntu/gpg | sudo gpg -dearmor -o /usr/share/keyrings/docker-archive-keyring.gpg

sudo apt-get update
sudo apt-get install docker-ce docker-ce-cli containerd.io

echo \
"deb [arch=amd64 signed-by=/usr/share/keyrings/docker-archive-keyring.gpg] https://download.docker.com/linux/ubuntu \
\$(lsb_release -cs) stable" | sudo tee /etc/apt/sources.list.d/docker.list > /dev/null

sudo apt-get update
sudo apt-get update
sudo apt-get update
sudo apt-get update

1.0.1 Run Docker commands without sudo

1. ADD THE DOCKER GROUP IF IT DOESN'T ALREADY EXIST

sudo groupadd docker

2. ADD THE CONNECTED USER \$USER TO THE DOCKER GROUP

Optionally change the username to match your preferred user.

sudo gpasswd -a \$USER docker



Important

Log out and log back in so that your group membership is re-evaluated.

3. RESTART THE DOCKER DAEMON

sudo service docker restart

If you are on Ubuntu 14.04-15.10, use docker.io instead:

sudo service docker.io restart

1.1 Commands

- ./build_docker.sh Build the docker image
- ./changelog.sh Update docs/changelog.md
- ./doc-build Build the doc and generate the PDF.
- ./doc-serve Start the live-reloading docs server. You can access it here : http://localhost:8000/

2. Firmware

2.1 Signal Processing

2.1.1 IPD Module

Introduction

This page will confirm the fonctionnement of the IPD module. We will see what it expexted in simulation. And confirm the fonctionnement with signaltap in the FPGA

Presentation

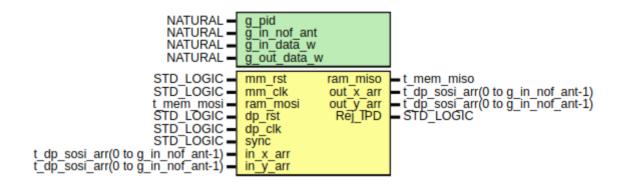


Figure 1: IPD entity

The figure 1 shows ports of the module. The input data bus is directly connected to the output of ADC. Input data bus is size of 8x14 bits and same in output. This module is a delay line, it allows to to correct time travel of signal above the instrument. To do this the module allows to set a delay from 0 to 255 sample on each channel. Those delay are configurable in the register interface The module has the address offset of 16#1340000#.

 $16\#1340000\# = c_processing_address_offset + c_radiogaga_address_offset + c_IPD_address_offset + c_radiogaga_address_offset + c_IPD_address_offset + c_radiogaga_address_offset + c_radiogagaa_address_offset + c_radiogagaa_address_offset + c_radioga$

| Name | Address | Read | Write | Width | Comment |
|----------------------|---------|------|-------|-------|----------------------------------|
| c_ipd_delay_x_offset | 16#00# | х | х | 4 | Add delay to antennas on X polar |
| c_ipd_delay_y_offset | 16#10# | × | Х | 4 | Add delay to antennas on X polar |

Simulation

SHIFT TEST

IPD has 2 writable registers, *delay_x* and *delay_y*. So we can apply delay to both polarisations of each antenna. Each delay can be set on the range [0:255]. In simulation, I set delay incrementally by 25, like this we can see a shift of 25 sample on each channels. For this I wrote in the following registers:

X polar 16#1340000# = 0 16#1340001# = 25 16#1340002# = 50 16#1340003# = 75

Y polar

16#1340010# = 100

16#1340011# = 125

16#1340012# = 150

16#1340013# = 175



Figure 2 : Delays configuration

For simulation I sent the same pulse on each channels as we can see on in_y_arr(0).

First of all, we can see a shift between <code>in_y_arr(0)</code> and <code>out_x_arr(0)</code>. The delay of it was set to 0 but there is a shift of 15 ns. This is due by signal latching in VHDL. This delay is equivalent as 3 clock shots. This delay is not really important because it is applied on each <code>OUT</code> channel, so if we mesure shift between them, it will be correct.

Now we can see on the figure 3 a shift of 125 ns between the out_x_arr(0) and out_x_arr(1).

25 = 125/5ns. Our shift is correct.

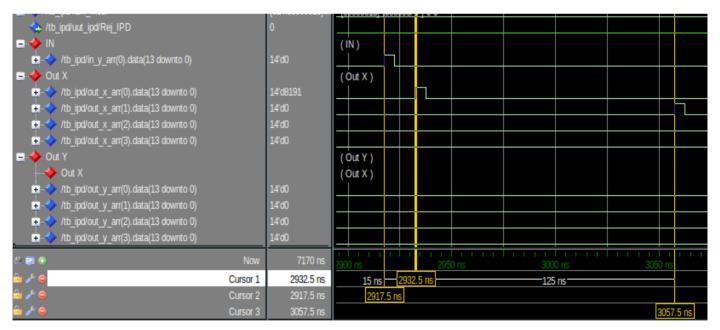


Figure 3 : Delays measurements

An other example on the figure 4 between the first channel $in_x_arr(0)$ with delay set at 0 and the last sample $in_y_arr(3)$ with delay set at 175 = 875/5ns



Figure 4 : Delays measurements 2

REJ_IPD TEST

When delays are set by the register interface, signals can be unstable during the max length of the delay-line. So after reset or reconfiguration the signal Rej_IPD is pulled high. Such as the out signal is invalid during this period.

- At the beginning of the simulation Rej_IPD is pulled high because the FPGA start up
- On the first yellow marker, delays are set by interface register, Rej_IPD is pulled high again during 1280 = 256 135ns
- On the third yellow marker we can see an another writing configuration by register interface.

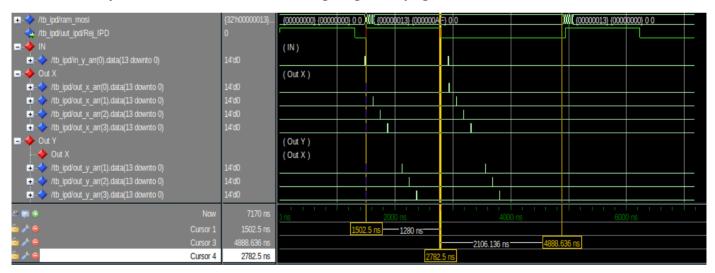


Figure 5 : Rej_IPD measurement

Signal TAP

SHIFT TEST

To test the FPGA in real condition, I set a signal tap with some interesting signal. On input of the card. I set a pulse sent every milliseconds.

On the figure 6 we can see a test with delay set to 0 and the figure 7 incrementally by 25 such as in simulation

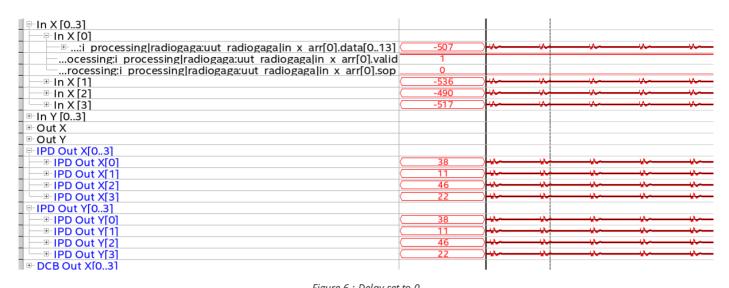


Figure 6: Delay set to 0

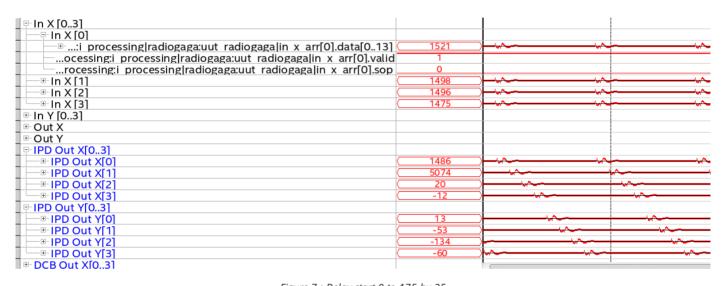


Figure 7 : Delay start 0 to 175 by 25

REJ_IPD TEST

To test it, i just put a trigger on Rej_IPD, reconfigure the delays and we see the signal is pulled HIGH during 255 sample.

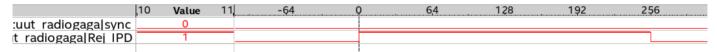


Figure 8: REJ_IPD test

2.1.2 DCB

Introduction

This document will present and confirm the fonctionnement of DCB module. We will see what it expected in simulation. And confirm the fonctionnement with Signal Tap in the FPGA

Presentation

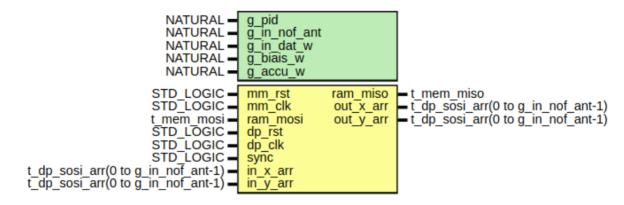


Figure 1 : DCB entity

The figure 1 show the port of the module. The input is directly connected to the output of IPD module. Input data bus is size of 8x14 bits and 8x16 bits in output. The goal of this module is to add biais in order to delete DC offset from the ADC. To do this the module allow to estimate the average of the input. To read average and configure biais the register interface is set like below.

The module has the address offset of |16#1350000#.

16#1350000# = c_processing_address_offset + c_radiogaga_address_offset + c_DCB_address_offset

| Name | Address | Read | Write | Width | Comment |
|--------------------------|---------|------|-------|-------|----------------------------|
| c_DCB_biais_x_offset | 16#00# | x | × | 4 | Delete DC offset on ADC |
| c_DCB_biais_y_offset | 16#10# | X | X | 4 | Delete DC offset on ADC |
| c_DCB_accu_x_low_offset | 16#20# | X | | 4 | Lower bits of accumulator |
| c_DCB_accu_y_low_offset | 16#30# | X | | 4 | Lower bits of accumulator |
| c_DCB_accu_x_high_offset | 16#40# | X | | 4 | Higher bits of accumulator |
| c_DCB_accu_y_high_offset | 16#50# | x | | 4 | Higher bits of accumulator |

Simulation

BIAIS ADD

DCB has 2 writable registers, biais_x and biais_y. Those biais has a width of 16 bit, 14 for integer part and 2 for decimal part. If we apply a biais of 10, these are :

 $(1010)_2 = (10)_{10}$

```
(1010 + 00)_2 = (40)_{10}
```

So we can apply biais to both polarization of each antenna. In simulation, I set biais incrementally by 100, like this we can see + 100 on each channels.

To set biais we have to write in following registers:

```
# X polar

16#1350000# = 0

16#1350001# = 400

16#1350002# = 800

16#1350003# = 1200

# Y polar

16#1350010# = 1600

16#1350011# = 2000

16#1350012# = 2400
```

16#1350013# = 2800



Figure 2 : Biais configuration

The value are multiply by 4 caused by 2 bit added for the decimal part.

So now we apply a signal of 10 on all the input :

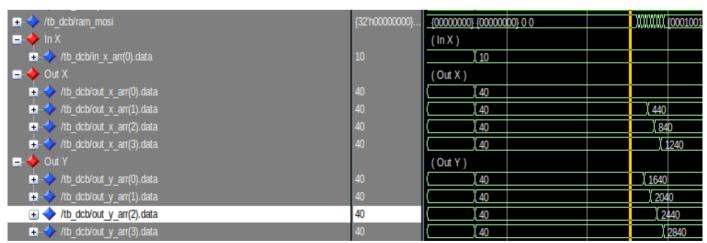


Figure 3 : Biais test

AVERAGE ESTIMATION

To set biais we need to estimate the average of the input. To calcul it, the FPGA accumulate the input during 200M of sample (1 sec). Is difficult to divide in vhdl, so the module return the accumulation not normalized. The division by 200M will be done by the soft on server.

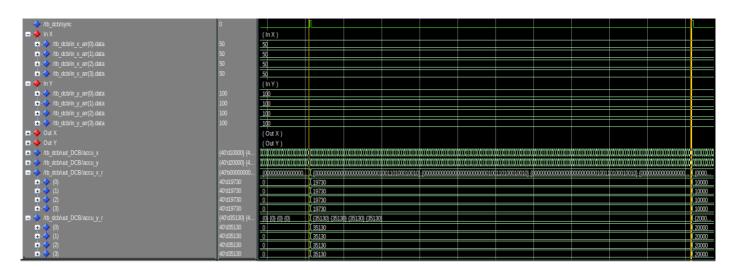


Figure 4 : Average test

On the figure 4 we can see the signal accumulate on a period of 1 μ s (1 sec in reality). On the right bottom corner, the accumulation is latched on a rising edge of sync and we can see the value of the accumulation during 1 μ s. So on the X input it gives :

In FPGA

n_sample = 1 000ns/5ns n_sample = 200 accu_x_r = 50 * 200 accu_x_r = 10 000 In soft moyenne = 10 000 / 200

moyenne = 10 000 / 200 moyenne = 50

Signal TAP

BIAIS ADD

To verify the fonctionnement of this module on the FPGA, the input of the card are still open. To estimate the average on each input I realized a little python program to parse the signal TAP data. With and without biais configuration it gives:

| (base) berthet@nanptb: | /STP\$ python3 STP2csv.py | (base) berthet@nanptb:~ | /STP\$ python3 STP2csv.py |
|-----------------------------------|----------------------------|-------------------------|----------------------------|
| Connection successfully | | Connection successfully | |
| sys:1: DtypeWarning: Co | olumns (474,575) have mixe | sys:1: DtypeWarning: Co | lumns (300) have mixed typ |
| 0 | 1024.000000 | 0 | 1024.000000 |
| <pre>dcb:i_dcb out_x_arr[0]</pre> | 26.246950 | dcb:i_dcb out_x_arr[0] | 0.373353 |
| dcb:i_dcb out_x_arr[1] | -74.867740 | dcb:i_dcb out_x_arr[1] | 0.239141 |
| dcb:i_dcb out_x_arr[2] | 52.896047 | dcb:i_dcb out_x_arr[2] | |
| dcb:i_dcb out_x_arr[3] | -55.080527 | dcb:i_dcb out_x_arr[3] | -0.578819 |
| dcb:i_dcb out_y_arr[0] | 285.052221 | dcb:i_dcb out_y_arr[0] | 1.583699 |
| dcb:i_dcb out_y_arr[1] | 173.497316 | dcb:i_dcb out_y_arr[1] | 1.823328 |
| dcb:i_dcb out_y_arr[2] | 77.969741 | dcb:i_dcb out_y_arr[2] | 0.626159 |
| dcb:i_dcb out_y_arr[3] | 290.619815 | dcb:i_dcb out_y_arr[3] | 1.387994 |
| in_x_arr[0] | 6.559785 | in_x_arr[0] | 5.845290 |
| in_x_arr[1] | -18.718399 | in_x_arr[1] | -18.437775 |
| in_x_arr[2] | 13.225476 | in_x_arr[2] | 13.526110 |
| in_x_arr[3] | -13.772572 | in_x_arr[3] | -13.639336 |
| in_y_arr[0] | 71.264031 | in_y_arr[0] | 71.147877 |
| in_y_arr[1] | 43.374817 | in_y_arr[1] | 43.456808 |
| in_y_arr[2] | 19.491459 | in_y_arr[2] | 19.408004 |
| in_y_arr[3] | 72.657394 | in_y_arr[3] | 73.345046 |

Without biais

With biais

Figure 5: Average estimation

On the left of figure 5 we can see the average on 1024 sample on each input. DCB out is just the input with 2 bit added for decimal part. On the right of the figure 5 we can see when we applied biais on each entry. To this we apply $-26.2 (4 \times 6.55)$ on in_x_arr[0] +74.9 on in_x_arr[1] etc. Values are nears to zero, what is expected.

5.2. Average Estimation

Now to read accumulation from the FPGA it was a bit complicated. The value is accumulate in a 40 bits word. But the register interface accept only until 32 bits word. So i cut the word in 2 part; low_acc(32 lower bits) and high_acc(8 higher bits). In the soft those value are stock in two variable uint64_t. The MSB is duplicated on the whole word to keep the sign. Then the hig_acc part is shifted by 32 bits. Finally the 2 parts are added to be divided by 200M.

```
-- SPECIAL
  20 : read average_x
  21 : read average_y
  22 : biais_x_auto
  23 : biais_y_auto
 -1 : Exit
 21
R 0x01360030 = 4f4425bb
R 0x01360050 = 00000003
Hexa: 34f4425bb
Dec : 71.07
R 0x01360031 = 01211956
R 0x01360051 = 00000002
Hexa: 201211956
Dec : 43.04
R 0x01360032 = e2fb0dec
R 0x01360052 = 00000000
Hexa : e2fb0dec
Dec : 19.04
R 0x01360033 = 6a5b7df6
R 0x01360053 = 00000003
Hexa: 36a5b7df6
Dec : 73.35
```

Figure 6 : Read average

For Example on the figure 6 we can see the DC offset on the Y polarisation. That's correspond with the figure 5.

2.1.3 Presum

Introduction

This page will confirm the fonctionnement of the presum module. We will see what it expected in simulation. And confirm the fonctionnement with signaltap in the FPGA

Presentation

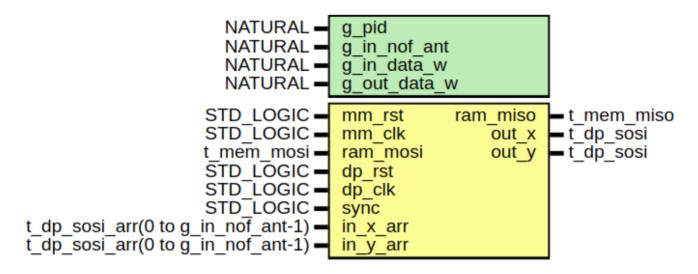


Figure 1: Presum entity

The figure 1 shows ports of the module. The input is directly connected to the output of DCB. Input data bus is size of 8x16 bits and 2x18 bits in output. This module will just add all antennas on both polarization. In register interface it's allow to disable one or more antenna. The register interface is set like below. The module has the address offset of 16#1360000#.

16#1360000# = c_processing_address_offset + c_radiogaga_address_offset + c_presum_address_offset

| Name | Address | Read | Write | Width | Comment |
|---------------------------|---------|------|-------|-------|--------------------------------|
| c_presum_ant_sel_x_offset | 16#00# | × | х | 4 | Disable antennas on x polar |
| c_presum_ant_sel_y_offset | 16#10# | х | х | 4 | Disable antennas on Y polar |

Simulation

ENABLE/DISABLE ANTENNAS

The register ant_sel_x and ant_sel_y are initialized to "1" in the FPGA. Like this all inputs are enable. To disable we have to write "0" to the antenna which we want want to disable.

For exemple to disable the 2nd and 4th antenna of the X polarization we have to write in the register interface like below:

X polar

16#1360000# = 1

16#1360001# = 0

16#1360002# = 1

16#1360003# = 0

SUMMATION

Now the FPGA check for each antenna if ant_sel is '0' or '1' and if is '1' datas of the inputs are added, else the input is replaced by zero.

On the figure 2, at the beginning of simulation, all antennas are set to "1" so the output is equal to sum of 4 antennas for each polarization. Then the 2nd and the 4th antenna are disable for X and Y polar respectively.

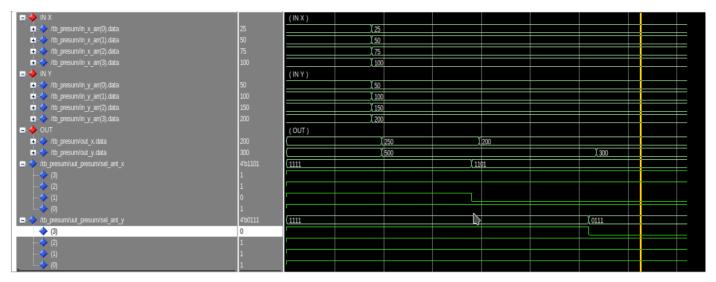


Figure 2 : Summation test

Signal TAP

ENABLE/DISABLE ANTENNAS

On the figure 3 we can read and write in both register. For this test we can see I disable the 2nd and the 4th antenna for the X polar. And for the 1st and 2nd antenna are disable.

```
What do you want to do ?
//////// presum ////////
-- READ
0 : sel_ant_x
1 : sel_ant_y
-- WRITE
10 : sel_ant_x
11 : sel_ant_ y
-1 : Exit
10 1 0 1 0
W 0x01360000 = 0x000000001
W 0x01360002 = 0x000000001
W 0x01360003 = 0x00000000
11 0 0 1 1
W 0x01360010 = 0x00000000
W 0x01360011 = 0x00000000
W 0x01360012 = 0x00000001
W 0x01360013 = 0x00000001
-1
```

Figure 3 : Disable antennas in test soft

SUMMATION

To verify the good fonctionnement of it, we will use the same python program like we used to test DCB. It export data from signal TAP and we can read the average of each polar in different modules.

```
STP: bash - Konsole
Connection succesfully stablished ...
0 1024.000000
dcb:i dcb|out x arr[0]
                                  21.546120
dcb:i_dcb|out_x_arr[1]
                                -77.196681
dcb:i_dcb|out_x_arr[2]
dcb:i_dcb|out_x_arr[3]
                                 55.951196
                                -51.336262
dcb:i_dcb|out_y_arr[0]
dcb:i_dcb|out_y_arr[1]
dcb:i_dcb|out_y_arr[2]
                                171.121523
                                 76.919473
dcb:i_dcb|out_y_arr[3]
                                294.163006
                                   5.361640
in_x_arr[0]
in_x_arr[1]
                                -19.327965
in_x_arr[2]
                                 14.030747
in_x_arr[3]
                                 71.879941
in_y_arr[1]
                                 42.867252
                                 19.274280
in_y_arr[2]
in_y_arr[3]
ipd:i_ipd|out_x_arr[0]
                                  73.581259
                                  5.384578
ipd:i_ipd|out_x_arr[1]
                                -19.302099
ipd:i_ipd|out_x_arr[2]
                                 13.986823
ipd:i_ipd|out_x_arr[3]
                                -12.834553
                                 71.856515
ipd:i_ipd|out_y_arr[0]
ipd:i_ipd|out_y_arr[1]
ipd:i_ipd|out_y_arr[2]
                                 19.229868
                                  73.541240
ipd:i_ipd|out_y_arr[3]
                              41822.127867
out_y
                              62766.221571
presum:i_presum|out_x
                                  77.571498
presum:i_presum|out_y
                                371.291362
                                   0.000000
sample
dtype: float64
(base) berthet@nanptb:~/STP$
```

Figure 4: Verify the output of presum

On the figure 4 we can see the sum on highlight lines. presum_out is equal to the sum of DCB_out_x_arr[n] on each polar.

So if we take the exemple beside for X polar :

 $presum \mid out_x = dcb \mid out_x_arr[0] + dcb \mid out_x_arr[2] \ presum \mid out_x = 21.5 + 56 \ presum \mid out_x = 77.5$

And for the Y polar:

 $presum \mid out_y = dcb \mid out_x_arr[2] + dcb \mid out_x_arr[3] \ presum \mid out_y = 76.9 + 294.2 \ presum \mid out_y = 371.1 \ pre$

2.1.4 Filter

Introduction

This page will confirm the fonctionnement of the filter module. We will see what it expected in simulation. And confirm the fonctionnement with signaltap in the FPGA

Presentation

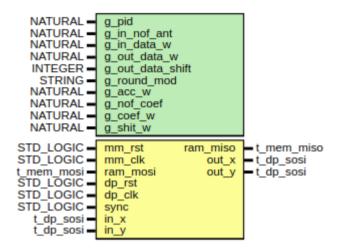


Figure 1: Filter entiry

The figure 1 shows ports of the module. The input data bus is directly connected to the output of presum. Input data bus is size of 2x18 bits and 2x18 bits in output. This module is a numeric filter. It takes 128 coef and use FIR implementation to filter the signal. It possible to shift the output of the signal to decrease the gain of the filter.

The module has the address offset of 16#1370000#.

 $16\#1370000\# = c_processing_address_offset + c_radiogaga_address_offset + c_filter_address_offset + c_radiogaga_address_offset + c_filter_address_offset + c_filter_address_o$

| Name | Address | Read | Write | Width | Comment |
|-----------------------|---------|------|-------|-------|------------------------------|
| c_filter_coef_offset | 16#00# | Х | × | 128 | Coefficient of the filter |
| c_filter_shift_offset | 16#FF# | х | X | 1 | Shift to apply on the output |

This module has 2 architectures, **normal** and **transposed**. Difference between both are explained here. Today, is the transposed structure that is used, it allows to use DSP blocks in FPGA, explained here.

This module have important generic port to determine the good fonctionnement.

- g_round_mod : This allow to choose the rounding mode for the output. Today only truncate is available.
- g_nof_coef : Determine the number of coefficient for the implementation. 128 is sufficient for our application.
- g_out_data_shift: For the normal architecture only, the shift is not configurable in the register interface so it's declared here.

$$^{\circ}$$
 g_acc_w : 18 + 18 + $\frac{\log(128)}{\log(2)}$ = 44

- g_coef_w : Coefficients are defined on 16 bits.
- g_shift_w : The shift value is defined on 6 bits.

Simulation

RAMP COEFFICIENTS

First of all before to test is the filter make the job, we can set coefs from 0 to 128 by 1. To do this we have to write to the following addresses:

```
16#137000# = 1
16#1370001# = 2
16#1370002# = 3
...
16#13700126# = 127
16#13700127# = 128
```

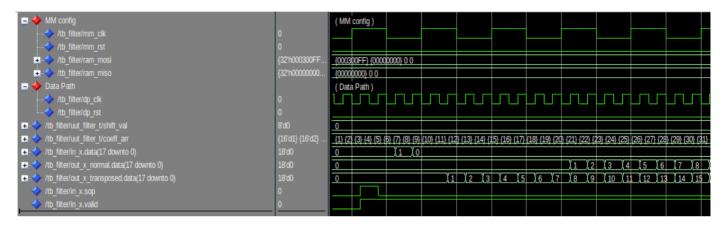


Figure 2 : Coefficient from 0 to 128

On the figure 2 we can see a pulse of **1** is sent on in_x.data during only one sample. We have 2 outputs because I instantiate both architecture, normal and transposed. So we can see our pulse multiplied by each coefficient until the 128th.



We can notice the transposed implementation generates less retard than the normal structure.

SHIFT TEST

To compensate the gain involved by the filter. An adjustable shift is implemented. It allow to shift to the right the signal. For exemple:

```
mysignal <= 80 -(0b1010000)
mysignal <= shift_right(mysignal, 2)
- mysignal = 20 (0b10100)
```

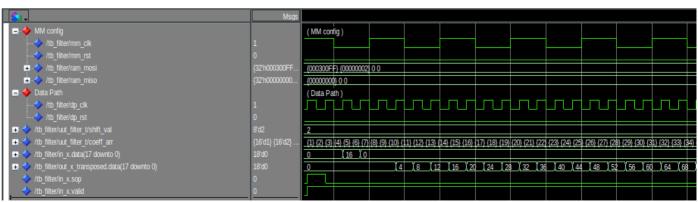


Figure 3: Shift test

On the figure 3 the pule is now of **16** and the shift of **2**. And we can see on the output the signal is always multiplied by the ramp coefficients but now is divided by $2^2 = 4$

Signal TAP

TEST OF A 36MHZ REJECTOR

To verify the fonctionnement of the filter I directly test it in the FPGA. For it I just generated a sinusoidal with a GBF.

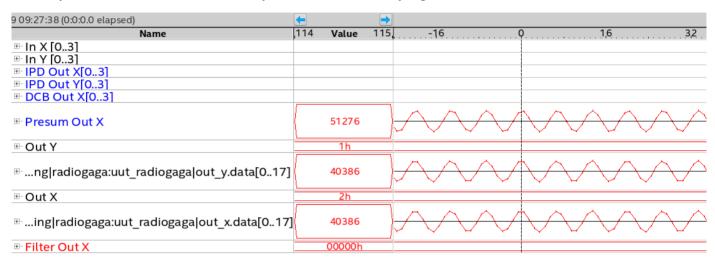
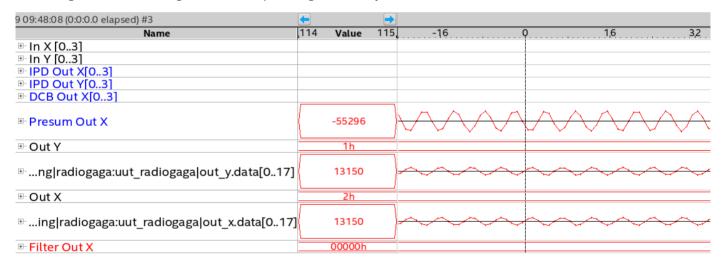


Figure 4: Signal of 30MHz

On the figure 4 we can see a signal of 30MHz, it pass trough without any attenuation.



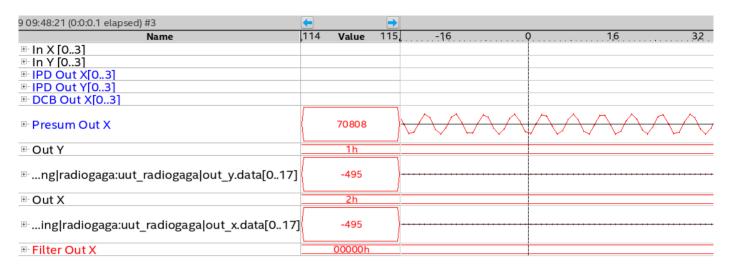


Figure 5 : Signal of 35MHz and 36MHz

Now on the figure 5 we can see the signal is a bit attenuated at 35MHz and completely at 36MHz. We can also see the spectrum of the output. There is a big reject of 50dB at 36M.

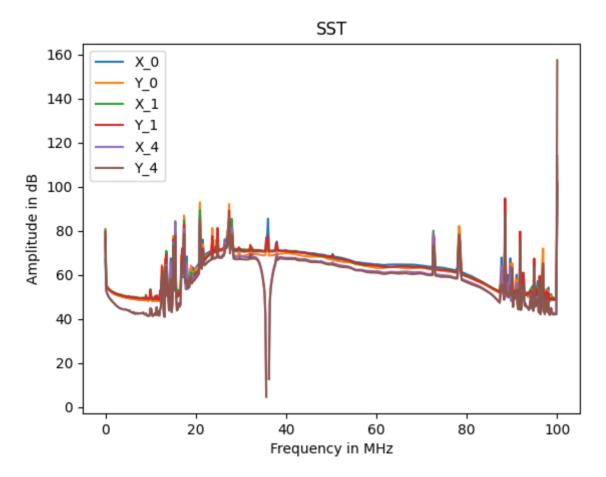


Figure 6 : SST of filter output



The filter module is instantiate 3 times, so we can apply 3 different filters on the signal. We just have to reconfigure the coefficient in the register interface. To generate coefficient, we used pyFDA explained here: PyFDA doc

2 2 UDP Sender

2.2.1 Introduction

This document will present and confirm the fonctionnement of UDP_sender module. We will see what it expected in simulation. And confirm the fonctionnement with Signal Tap in the FPGA.

2.2.2 Presentation

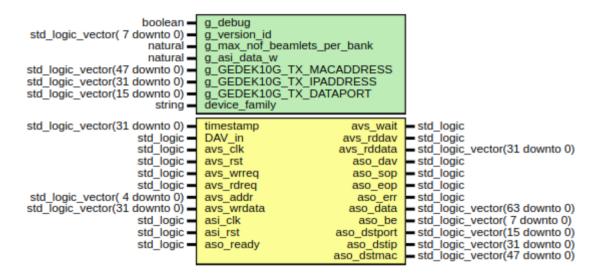


Figure 1: UDP_sender entity

This has to sent an UDP frame on the network when a cosmic gerbe is detected. The frame will be transmitted by a 10G link. For this on the figure 1 we can see different ports (yellow) of the module.

In the generic interface (green) we can set the default IP configuration of the destination server.

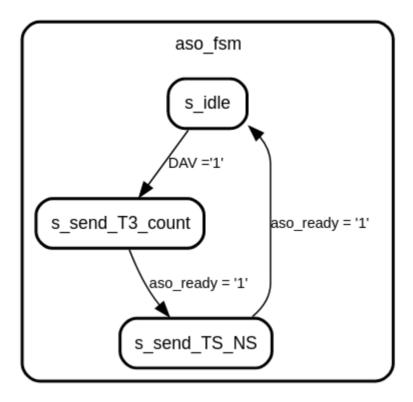


Figure 2 : State machine

On the figure 2 we can see the state machine of the module. By default the module is in **idle** mode. It is waiting a **DAV** from the trigger module.

When a DAV is sent, the module will put 2 packets of 64 bits in the frame :

-- First packet --

!T3!: Header of the frame. 4 ASCII character, so 32 bits width.

count: Number of the frame since the boot of the card.

-- Second packet --

timestamp: Is the timestamp when the trig happened

nanosecond: Is the nanosecond in the timestamp when the trig happened for more accuracy.

So now one the figure 3 we can see reception of a frame with netcat.

```
() tbb — Konsole

[tberthet@nenufarb0 ~]$ printf '0x%x\n' $(date +%s)
0x60bf3f18

[tberthet@nenufarb0 ~]$ nc -ul 1242 | xxd
00000000: 2154 3321 0a00 0000 1f3f bf60 be12 180d !T3!...?.`...
0000010: 2154 3321 0b00 0000 1f3f bf60 bc38 6235 !T3!...?.`.8b5
0000020: 2154 3321 0c00 0000 203f bf60 f2c1 ae1a !T3!...?.`...
```

Figure 3: Reception of a frame with netcat

The module has the address 16#980000#. Below they are the different address of the register interface.

| Name | Address | Read | Write | Width | Comment |
|--------------------------------|---------|------|-------|-------|--|
| c_UDP_sender_version_id_offset | 16#00# | Х | | 1 | Version _ id of the framer |
| c_UDP_sender_lo_32_mac_offset | 16#01# | Х | Х | 1 | Lower 32 bits of the mac address |
| c_UDP_sender_hi_16_mac_offset | 16#02# | Х | х | 1 | Higher 32 bits of the mac address |
| c_UDP_sender_ip_offset | 16#03# | Х | Х | 1 | Ip address |
| c_UDP_sender_port_offset | 16#04# | Х | Х | 1 | Port |
| c_UDP_sender_manual_dav_offset | 16#05# | | Х | 1 | Allow to send a frame manually (for test) |
| c_UDP_sender_delay_ns_offset | 16#06# | X | × | 1 | Time in number of sample to delete the traitement time |

2.2.3 Simulation

To simulate this module, we have just have to up DAV during one sample and watch the frame on the 10G bus.

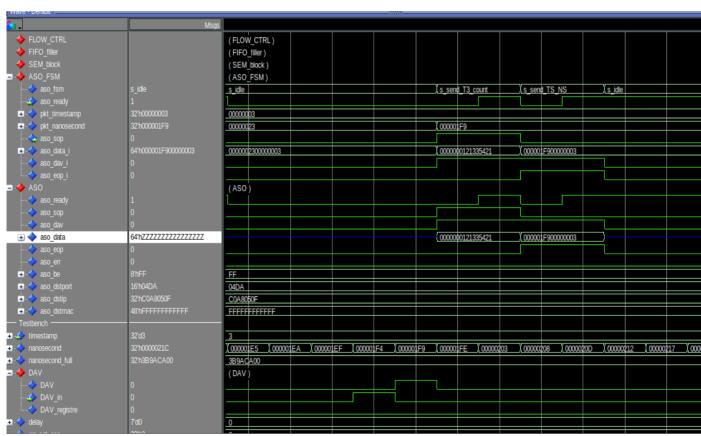


Figure 4: Test bench of UDP_sender without delay

Here we can see the nanosecond during the pulse is **1F9** and we can see it in the frame on aso_data.

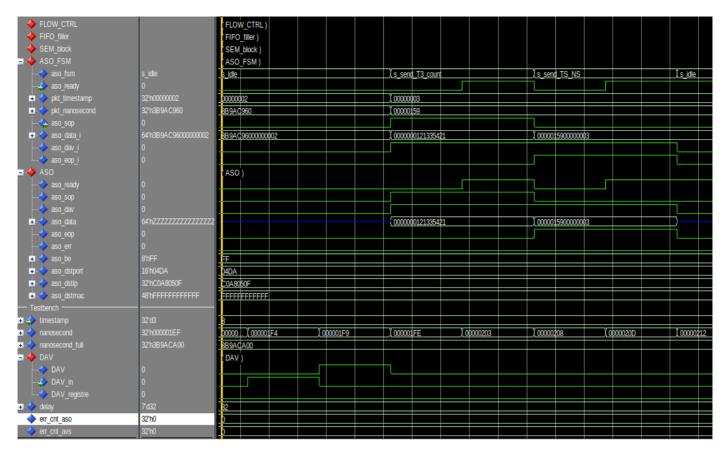


Figure 5: Test bench of UDP sender with delay

Now the DAV is always at **1F9** but in the frame we see **159**. Because we want to delay of 32 sample. 0x1F9 - 32 * 5 = 0x159

2.2.4 Signal TAP

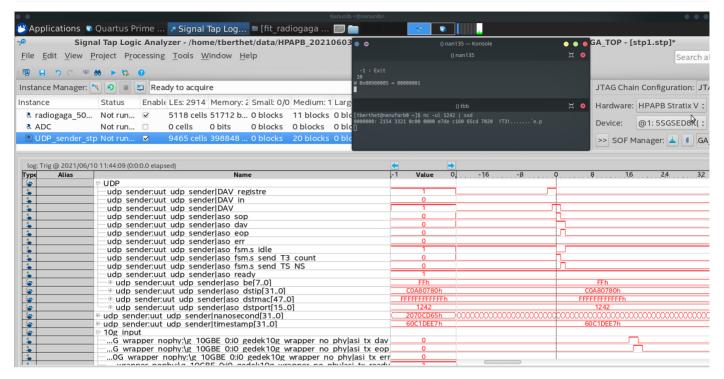


Figure 6 : Signal TAP of UDP sender

In the register interface of UDP sender is possible to send a DAV manually. Is very useful to test if the 10G configuration is working well. So on the figure 6 we see in the terminal we write '1' in at the address 16#980005#. So after this the frame is built and put on the 10G interface. By inverting the bytes 2 by 2 we can read timestamp and nanosecond correctly.

2.3 Trigger / decision

Trigger and decision module are the core of the RadioGaGa firmware. It's here that the detection processing appear. Trigger will processing datas to detect or not detect something. And the decision module will instantiate 3 triggers modules, each retarded of a determined time in fact to have 3 windows of detection. A detection is valid when there is a detection only in the middle window (Figure 1). We will saw it in detail below.

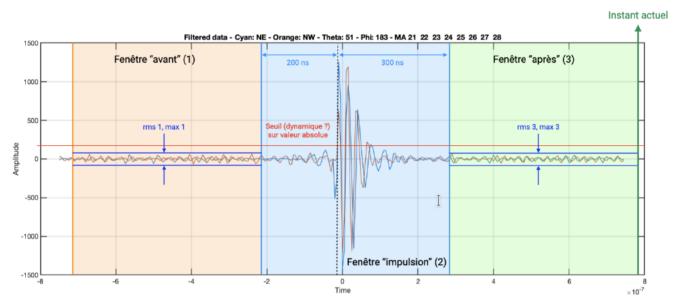


Figure 1 : Valid detection

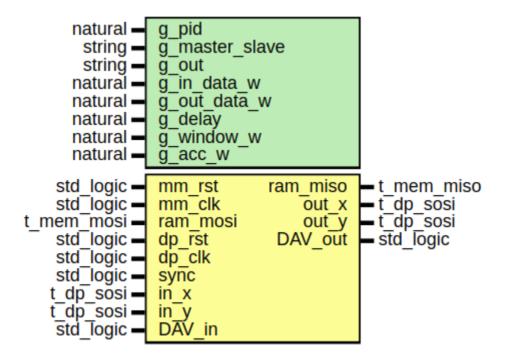


Figure 2: Trigger entity

On the figure 1 we can see ports of the modules. The input data bus is connected to the output of the last filter.

2.3.1 Principe of the detection

3. Software

3.1 Configuration files for RadioGaga

3.1.1 Presentation of files

This page will describe how configuration files works for RadioGaGa.

There are 2 types of files:

startup_configuration_board_X.conf

Contains all command to configure radiogaga module at the startup of the service. This files should load stable commands to enable the same startup each times.



Warning

Need to generate one file by board

This include:

- Load filter coefficients and configure shift.
- Apply a value of K and a shift for the trigger, not so low for prevent too much detection.
- Configure the register in SumX, '0' for the last board, '1' for others.
- UDP_sender :
 - enable or not to send frames to TBB
 - set the delay time on TS to delete the traitment time.
 - Configure IP, mac address and port of TBB

recursive_configuration_board_X.conf

Those files allow to reconfigure specifics registers at each new pointing .



Warning

Need to generate one file by board

This include:

- Change coefficients and shift of filters.
- Set a new value to K and shift for the trigger.
- Allow to disable some MR in presum if there are some parasites or something else.

3.1.2 How to generate those files

To generate those files there is python script which take .yaml files to set

```
config_startup.yaml
# Input file to generate startup configurations files. board:
- 0:
       filter:
             - path: 22M_rej.conf
         - shift: 15
- 2:
            - path: 36M_rej.conf
         - shift: 15
- 3:
            - path: 22M_73M_band.conf
- shift: 15
      trigger:
- k: 200
etc.
       config_recursive.yaml
# Input file to generate recursive configurations files. board:
   - 0:
      filter:
- 1:
             - path: 22M_rej.conf
         - shift: 15
- 2:
             - path: 36M_rej.conf
         - shift: 15
             - path: 22M_73M_band.conf
- shift: 15
      trigger:
- k: 400
```

Then just need to run the appropriate python script

```
startup

python gen_startup_conf_file.py

recursive

python gen_recursive_conf_file.py
```

After running scripts. Configurations files are generated, they have the same format than HPAPB_ADC.conf

```
startup_configuration_board_0.conf

TODO
```

3.2 Startup sequence

This chapter will present step by step the configuration needed at the startup of the HPAPB board.

The firmware RadioGaGa is based on LANewBa, so there is a lot of similitude between both.

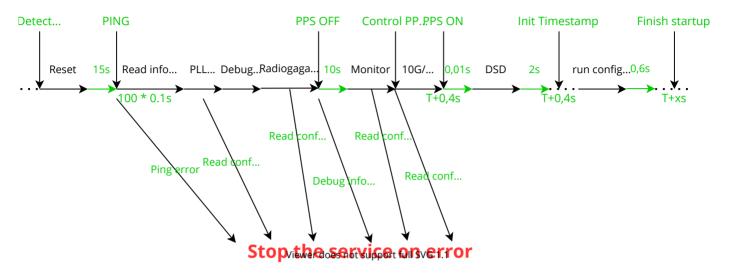


Figure 1 : Timeline of the startup

Ping

First of all when tartup is detected we need to ping the board on the 1G interface.

1G configuration:

• GEDEK_IP_ADDRESS: 192.168.6.128 + number_of_the_card

• GEDEK_MACADDRESS: 00:07:ed:a8:06:80

• GEDEK_UDP_AVM_PORT: 2271
• GEDEK_UDP_TXPORT: 1271

Read status

Read constant of the board (version of the firmware, temperature etc.) Sames addresses than LANewBa.

TODO

ADC and PLL configuration

There is exactly same on LANewBa, we need to run the file: svn/NenuFar/trunk/recepteur_LANewBa/trunk/firmware/HPAPB/soft/HPAPB_LMK.conf

Config RadioGaGa modules

To configure RadioGaGa modules, we need to run the startup_configuration_board_X.conf for each board. For more information read this page: Software/Configuration files

Monitor

Run the configuration file svn://MonitorPath

DSD

Write '1' in the register c_DSD_control_offset

W 010300F0 1

END of startup configuration

3.3 Running mode

3.3.1 Monitor

When the board is booted correctly, it needed to read in some registers for safety of the board. For this we read in registers of monitor modules.

To this it's exactly the same than LANewBa.

TODO

3.3.2 SumX

SumX uses fifo, we need to monitor if those fifo are not full or empty. To this we should to read at the address c_sumX_debug_fifo_offset

R 0x009c0401 = 0

This is a 7 bits words

```
debug_fifo[6] = sop_misalign
debug_fifo[5] = tx_dcifo_wrful
debug_fifo[4] = tx_dcifo_vrful
debug_fifo[3] = rx_dcfifo_wrful
debug_fifo[2] = rx_dcfifo_vrful
debug_fifo[7] = resync_scfifo_wrful
debug_fifo[7] = resync_scfifo_wrful
debug_fifo[7] = resync_scfifo_wrful
```

It should be always at "0" else on error occurred, we can know which fifo is wrong by decoding the word.

3.3.3 Recursive configuration

As it's explained here: Software/Configuration files we need the possibility to reconfigure some modules in the FPGA. To this it's needed to reload the recursive_configuration_board_X.conf at each new pointing.

4. Divers

4.1 PyFDA

This page explains how to generate coefficients for filter module.

To do it we use pyFDA, it's a open source python program. To dowload it:

pip install pyfda

5. Changelog

```
r9826 | berthet | 2021-06-18 18:58:08 +0200 (ven. 18 juin 2021) | 1 ligne
 Update software section
r9825 | berthet | 2021-06-18 18:52:14 +0200 (ven. 18 juin 2021) | 1 ligne
 Add todo list plugin
r9824 | berthet | 2021-06-18 18:51:55 +0200 (ven. 18 juin 2021) | 1 ligne
 remove sudo in script, add procedure to add docker to user group in Index.md
r9823 | berthet | 2021-06-18 18:49:48 +0200 (ven. 18 juin 2021) | 1 ligne
 modify dockerfile, use a very lighter version of python
r9817 | viou | 2021-06-17 14:04:57 +0200 (jeu. 17 juin 2021) | 1 ligne
 Move changelog at the end of the doc and include all doc files (incl. scripts) in changelog
r9816 | viou | 2021-06-17 13:41:08 +0200 (jeu. 17 juin 2021) | 1 ligne
 boot -> startup
r9815 | berthet | 2021-06-17 10:01:27 +0200 (jeu. 17 juin 2021) | 1 ligne
 doc - Update generation scripts
r9814 | berthet | 2021-06-17 09:46:07 +0200 (jeu. 17 juin 2021) | 1 ligne
 doc - Add pdf
r9813 | berthet | 2021-06-17 09:30:37 +0200 (jeu. 17 juin 2021) | 1 ligne
 doc - Move css and is in assets dir
r9812 | berthet | 2021-06-17 09:23:51 +0200 (jeu. 17 juin 2021) | 1 ligne
 doc - Add subdirectory to better structure the doc dir.
r9803 | berthet | 2021-06-14 18:00:37 +0200 (lun. 14 juin 2021) | 1 ligne
 Update svn keywords in .yml
r9802 | berthet | 2021-06-14 17:59:19 +0200 (lun. 14 juin 2021) | 1 ligne
 Add pdf directory with first pdf
r9801 | berthet | 2021-06-14 17:26:02 +0200 (lun. 14 juin 2021) | 1 ligne
 New doc, generated with mkdoc.
```

r9800 | berthet | 2021-06-14 16:33:12 +0200 (lun. 14 juin 2021) | 1 ligne

Remove old doc using makefile with pandoc

r9758 | berthet | 2021-06-02 12:12:56 +0200 (mer. 02 juin 2021) | 1 ligne

Add documentation of IPD,DCB,Presum, Demande_ALSE_sumX

r9757 | berthet | 2021-06-02 12:08:11 +0200 (mer. 02 juin 2021) | 2 lignes

DOCUMENTAION Update makefile, add some configurations files (template, script to install dependencies,font)

r9640 | berthet | 2021-04-08 14:31:21 +0200 (jeu. 08 avril 2021) | 1 ligne

Add directory RadioGAGA in receivers. This include docs and symbolic link to firmware and soft.