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Revisions

Rev	Description	Date	Approved
XA	Initial Release	APR-13-2016	O. Romero
A	Prototype Production	APR-14-2016	O. Romero
AX1	Development	AUG-16-2016	O. Romero
B	2nd Release	SEP-02-2016	O. Romero
B1	Update BOM	DEC-16-2016	O. Romero

S32K144EVB-Q100

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ICAP Classification: CP: IUO: PUBI: X

Designer: Osvaldo Romero	Drawing Title: S32K144EVB-Q100	
Drawn by: Osvaldo Romero	Page Title: TITLE PAGE	
Approved: APPROVER	Size: C	Document Number: SCH-29248 PDF: SPF-29248 — Rev: B1
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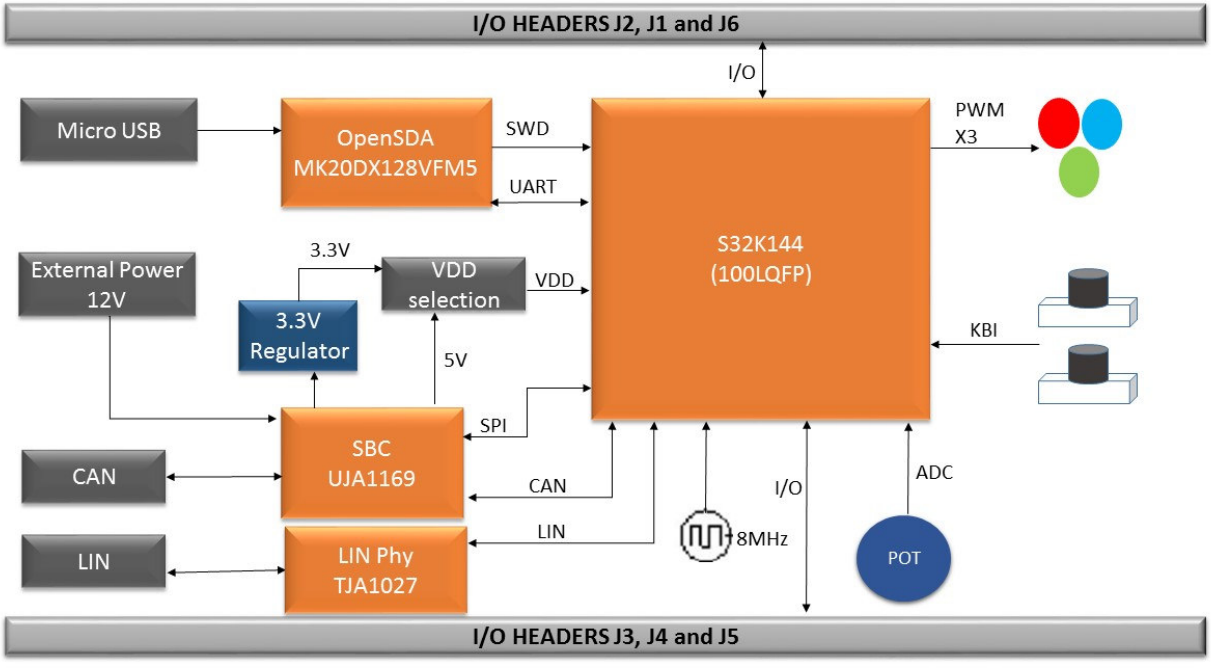
1. Unless Otherwise Specified:
   All resistors are in ohms, 1% and 5 %
   All capacitors are in uF, 10% , 20 % and 5%
   All voltages are DC
   All polarized capacitors are aluminum electrolytic

2. Interrupted lines coded with the same letter or letter combinations are electrically connected.

3. Device type number is for reference only. The number varies with the manufacturer.

4. Special signal usage:
   _B Denotes - Active-Low Signal
   <> or [] Denotes - Vectored Signals

5. Interpret diagram in accordance with American National Standards Institute specifications, current revision, with the exception of logic block symbology.



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Drawing Title: **S32K144EVB-Q100**

Page Title: **Notes and Block Diagram**

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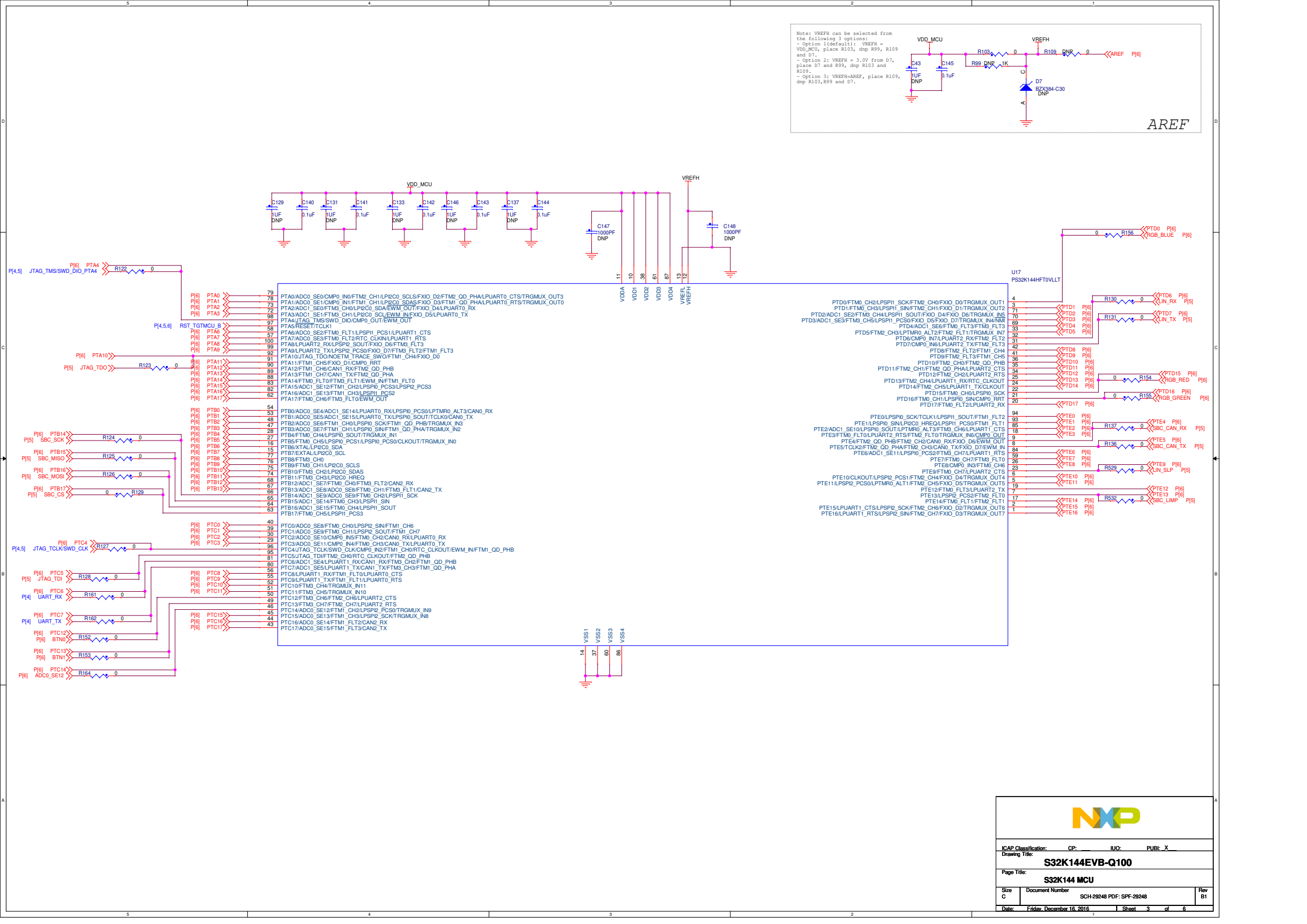
Note: VREFH can be selected from the following 3 options:
- Option 1(default): VREFH = VDD_MCU, place R103, dnp R99, R109 and D7.
- Option 2: VREFH = 3.0V from D7, place D7 and R99, dnp R103 and R109.
- Option 3: VREFH=AREF, place R109, dnp R103,R99 and D7.
VDD_MCU
VREFH
C43 1UF DNP
C145 0.1uF
R103 0
R99 DNP 1K
R109 DNP 0
AREF P[6]
D7 RZX384-C30 DNP
AREF
C129 1UF DNP
C140 0.1uF
C131 1UF DNP
C141 0.1uF
C133 1UF DNP
C142 0.1uF
C146 1UF DNP
C143 0.1uF
C137 1UF DNP
C144 0.1uF
C147 1000PF DNP
C148 1000PF DNP
VDDA VDD1 VDD2 VDD3 VDD4 VREFL VREFH
VSS1 VSS2 VSS3 VSS4
U17
PS32K144HFT0VLLT
PTA0/ADC0_SE0/CMP0_IN0/FTM2_CH1/LPI2C0_SCLS/FXIO_D2/FTM2_QD_PHA/LPUART0_CTS/TRGMUX_OUT3
PTA1/ADC0_SE1/CMP0_IN1/FTM1_CH1/LPI2C0_SDAS/FXIO_D3/FTM1_QD_PHA/LPUART0_RTS/TRGMUX_OUT0
PTA2/ADC1_SE0/FTM3_CH0/LPI2C0_SDA/EWM_OUT/FXIO_D4/LPUART0_RX
PTA3/ADC1_SE1/FTM3_CH1/LPI2C0_SCL/EWM_IN/FXIO_D5/LPUART0_TX
PTA4/JTAG_TMS/SWD_DIO/CMP0_OUT/EWM_OUT
PTA5/RESET/TCLK1
PTA6/ADC0_SE2/FTM0_FLT1/LPSPI1_PCS1/LPUART1_CTS
PTA7/ADC0_SE3/FTM0_FLT2/RTC_CLKIN/LPUART1_RTS
PTA8/LPUART2_RX/LPSPI2_SOUT/FXIO_D6/FTM3_FLT3
PTA9/LPUART2_TX/LPSPI2_PCS0/FXIO_D7/FTM3_FLT2/FTM1_FLT3
PTA10/JTAG_TDO/NOETM_TRACE_SWO/FTM1_CH4/FXIO_D0
PTA11/FTM1_CH5/FXIO_D1/CMP0_RRT
PTA12/FTM1_CH6/CAN1_RX/FTM2_QD_PHB
PTA13/FTM1_CH7/CAN1_TX/FTM2_QD_PHA
PTA14/FTM0_FLT0/FTM3_FLT1/EWM_IN/FTM1_FLT0
PTA15/ADC1_SE12/FTM1_CH2/LPSPI0_PCS3/LPSPI2_PCS3
PTA16/ADC1_SE13/FTM1_CH3/LPSPI1_PCS2
PTA17/FTM0_CH6/FTM3_FLT0/EWM_OUT
PTB0/ADC0_SE4/ADC1_SE14/LPUART0_RX/LPSPI0_PCS0/LPTMR0_ALT3/CAN0_RX
PTB1/ADC0_SE5/ADC1_SE15/LPUART0_TX/LPSPI0_SOUT/TCLK0/CAN0_TX
PTB2/ADC0_SE6/FTM1_CH0/LPSPI0_SCK/FTM1_QD_PHB/TRGMUX_IN3
PTB3/ADC0_SE7/FTM1_CH1/LPSPI0_SIN/FTM1_QD_PHA/TRGMUX_IN2
PTB4/FTM0_CH4/LPSPI0_SOUT/TRGMUX_IN1
PTB5/FTM0_CH5/LPSPI0_PCS1/LPSPI0_PCS0/CLKOUT/TRGMUX_IN0
PTB6/XTAL/LPI2C0_SDA
PTB7/EXTAL/LPI2C0_SCL
PTB8/FTM3_CH0
PTB9/FTM3_CH1/LPI2C0_SCLS
PTB10/FTM3_CH2/LPI2C0_SDAS
PTB11/FTM3_CH3/LPI2C0_HREQ
PTB12/ADC1_SE7/FTM0_CH0/FTM3_FLT2/CAN2_RX
PTB13/ADC1_SE8/ADC0_SE8/FTM0_CH1/FTM3_FLT1/CAN2_TX
PTB14/ADC1_SE9/ADC0_SE9/FTM0_CH2/LPSPI1_SCK
PTB15/ADC1_SE14/FTM0_CH3/LPSPI1_SIN
PTB16/ADC1_SE15/FTM0_CH4/LPSPI1_SOUT
PTB17/FTM0_CH5/LPSPI1_PCS3
PTC0/ADC0_SE8/FTM0_CH0/LPSPI2_SIN/FTM1_CH6
PTC1/ADC0_SE9/FTM0_CH1/LPSPI2_SOUT/FTM1_CH7
PTC2/ADC0_SE10/CMP0_IN5/FTM0_CH2/CAN0_RX/LPUART0_RX
PTC3/ADC0_SE11/CMP0_IN4/FTM0_CH3/CAN0_TX/LPUART0_TX
PTC4/JTAG_TCLK/SWD_CLK/CMP0_IN2/FTM1_CH0/RTC_CLKOUT/EWM_IN/FTM1_QD_PHB
PTC5/JTAG_TDI/FTM2_CH0/RTC_CLKOUT/FTM2_QD_PHB
PTC6/ADC1_SE4/LPUART1_RX/CAN1_RX/FTM3_CH2/FTM1_QD_PHB
PTC7/ADC1_SE5/LPUART1_TX/CAN1_TX/FTM3_CH3/FTM1_QD_PHA
PTC8/LPUART1_RX/FTM1_FLT0/LPUART0_CTS
PTC9/LPUART1_TX/FTM1_FLT1/LPUART0_RTS
PTC10/FTM3_CH4/TRGMUX_IN11
PTC11/FTM3_CH5/TRGMUX_IN10
PTC12/FTM3_CH6/FTM2_CH6/LPUART2_CTS
PTC13/FTM3_CH7/FTM2_CH7/LPUART2_RTS
PTC14/ADC0_SE12/FTM1_CH2/LPSPI2_PCS0/TRGMUX_IN9
PTC15/ADC0_SE13/FTM1_CH3/LPSPI2_SCK/TRGMUX_IN8
PTC16/ADC0_SE14/FTM1_FLT2/CAN2_RX
PTC17/ADC0_SE15/FTM1_FLT3/CAN2_TX
PTD0/FTM0_CH2/LPSPI1_SCK/FTM2_CH0/FXIO_D0/TRGMUX_OUT1
PTD1/FTM0_CH3/LPSPI1_SIN/FTM2_CH1/FXIO_D1/TRGMUX_OUT2
PTD2/ADC1_SE2/FTM3_CH4/LPSPI1_SOUT/FXIO_D4/FXIO_D6/TRGMUX_IN5
PTD3/ADC1_SE3/FTM3_CH5/LPSPI1_PCS0/FXIO_D5/FXIO_D7/TRGMUX_IN4/NMI
PTD4/ADC1_SE6/FTM0_FLT3/FTM3_FLT3
PTD5/FTM2_CH3/LPTMR0_ALT2/FTM2_FLT1/TRGMUX_IN7
PTD6/CMP0_IN7/LPUART2_RX/FTM2_FLT2
PTD7/CMP0_IN6/LPUART2_TX/FTM2_FLT3
PTD8/FTM2_FLT2/FTM1_CH4
PTD9/FTM2_FLT3/FTM1_CH5
PTD10/FTM2_CH0/FTM2_QD_PHB
PTD11/FTM2_CH1/FTM2_QD_PHA/LPUART2_CTS
PTD12/FTM2_CH2/LPUART2_RTS
PTD13/FTM2_CH4/LPUART1_RX/RTC_CLKOUT
PTD14/FTM2_CH5/LPUART1_TX/CLKOUT
PTD15/FTM0_CH0/LPSPI0_SCK
PTD16/FTM0_CH1/LPSPI0_SIN/CMP0_RRT
PTD17/FTM0_FLT2/LPUART2_RX
PTE0/LPSPI0_SCK/TCLK1/LPSPI1_SOUT/FTM1_FLT2
PTE1/LPSPI0_SIN/LPI2C0_HREQ/LPSPI1_PCS0/FTM1_FLT1
PTE2/ADC1_SE10/LPSPI0_SOUT/LPTMR0_ALT3/FTM3_CH6/LPUART1_CTS
PTE3/FTM0_FLT0/LPUART2_RTS/FTM2_FLT0/TRGMUX_IN6/CMP0_OUT
PTE4/FTM2_QD_PHB/FTM2_CH2/CAN0_RX/FXIO_D6/EWM_OUT
PTE5/TCLK2/FTM2_QD_PHA/FTM2_CH3/CAN0_TX/FXIO_D7/EWM_IN
PTE6/ADC1_SE11/LPSPI0_PCS2/FTM3_CH7/LPUART1_RTS
PTE7/FTM0_CH7/FTM3_FLT0
PTE8/CMP0_IN3/FTM0_CH6
PTE9/FTM0_CH7/LPUART2_CTS
PTE10/CLKOUT/LPSPI2_PCS1/FTM2_CH4/FXIO_D4/TRGMUX_OUT4
PTE11/LPSPI2_PCS0/LPTMR0_ALT1/FTM2_CH5/FXIO_D5/TRGMUX_OUT5
PTE12/FTM0_FLT3/LPUART2_TX
PTE13/LPSPI2_PCS2/FTM2_FLT0
PTE14/FTM0_FLT1/FTM2_FLT1
PTE15/LPUART1_CTS/LPSPI2_SCK/FTM2_CH6/FXIO_D2/TRGMUX_OUT6
PTE16/LPUART1_RTS/LPSPI2_SIN/FTM2_CH7/FXIO_D3/TRGMUX_OUT7
JTAG_TMS/SWD_DIO_PTA4
JTAG_TDO
RST_TGTMCU_B
SBC_SCK
SBC_MISO
SBC_MOSI
SBC_CS
JTAG_TCLK/SWD_CLK
JTAG_TDI
UART_RX
UART_TX
BTN0
BTN1
ADC0_SE12
RGB_BLUE
LIN_RX
LIN_TX
RGB_RED
RGB_GREEN
SBC_CAN_RX
SBC_CAN_TX
LIN_SLP
SBC_LIMP
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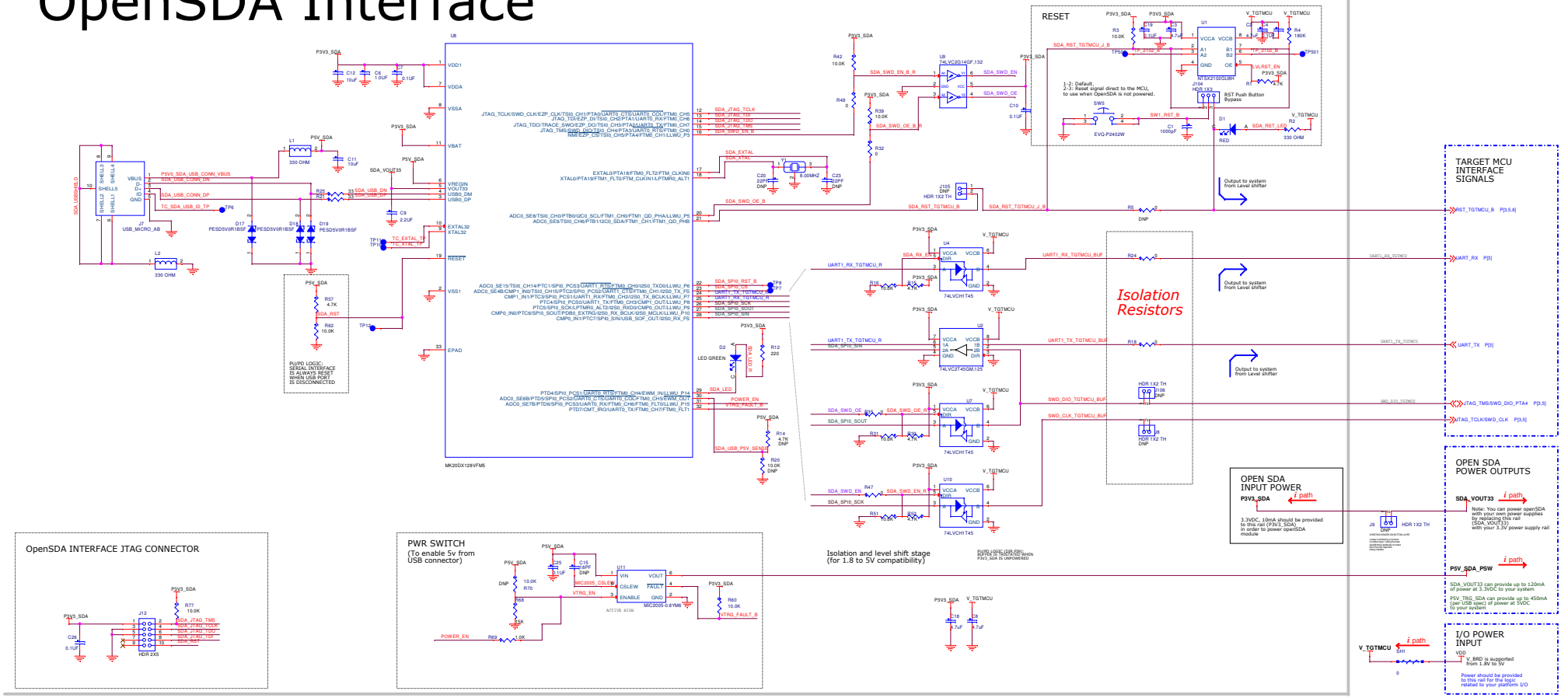
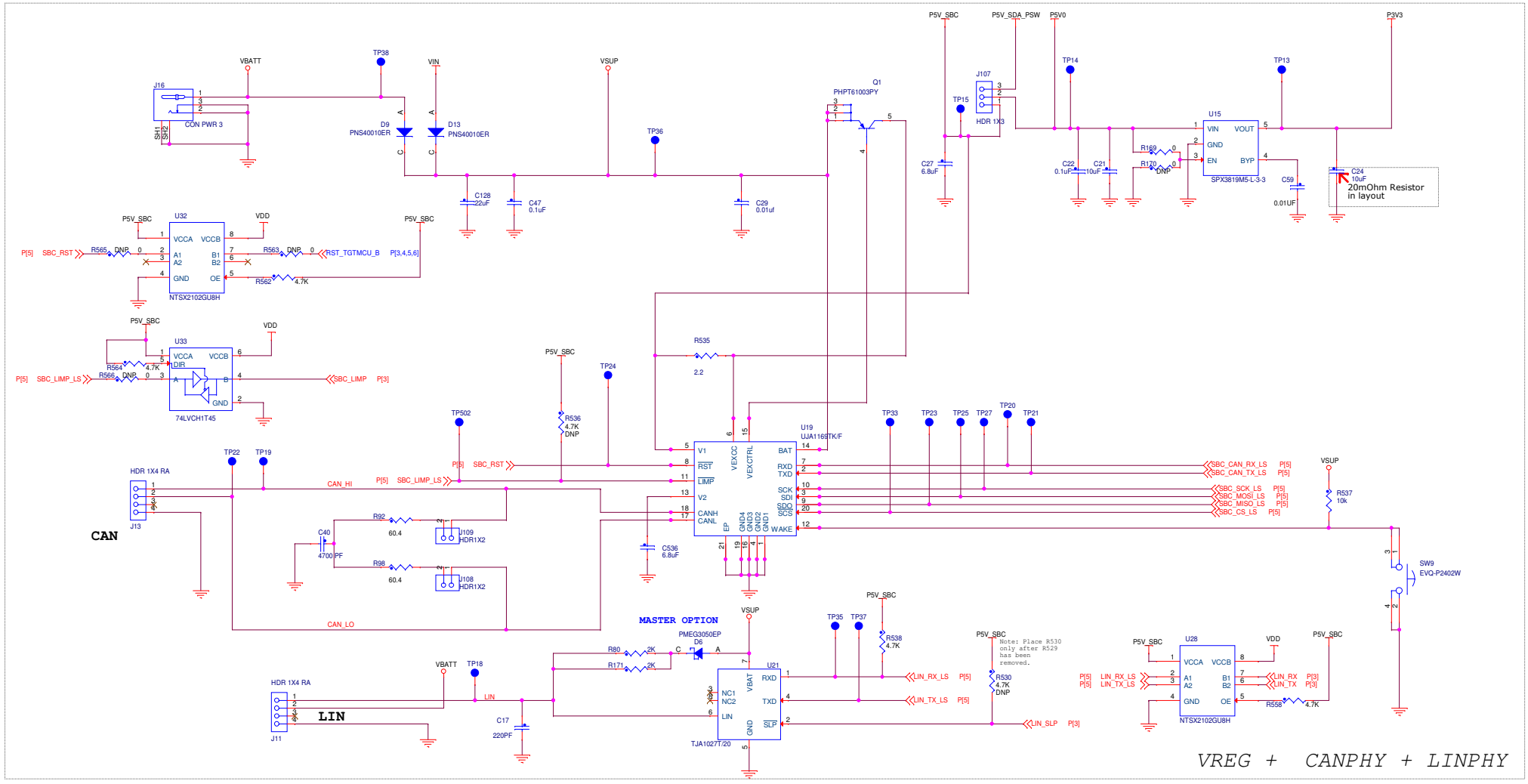
OpenSDA Interface





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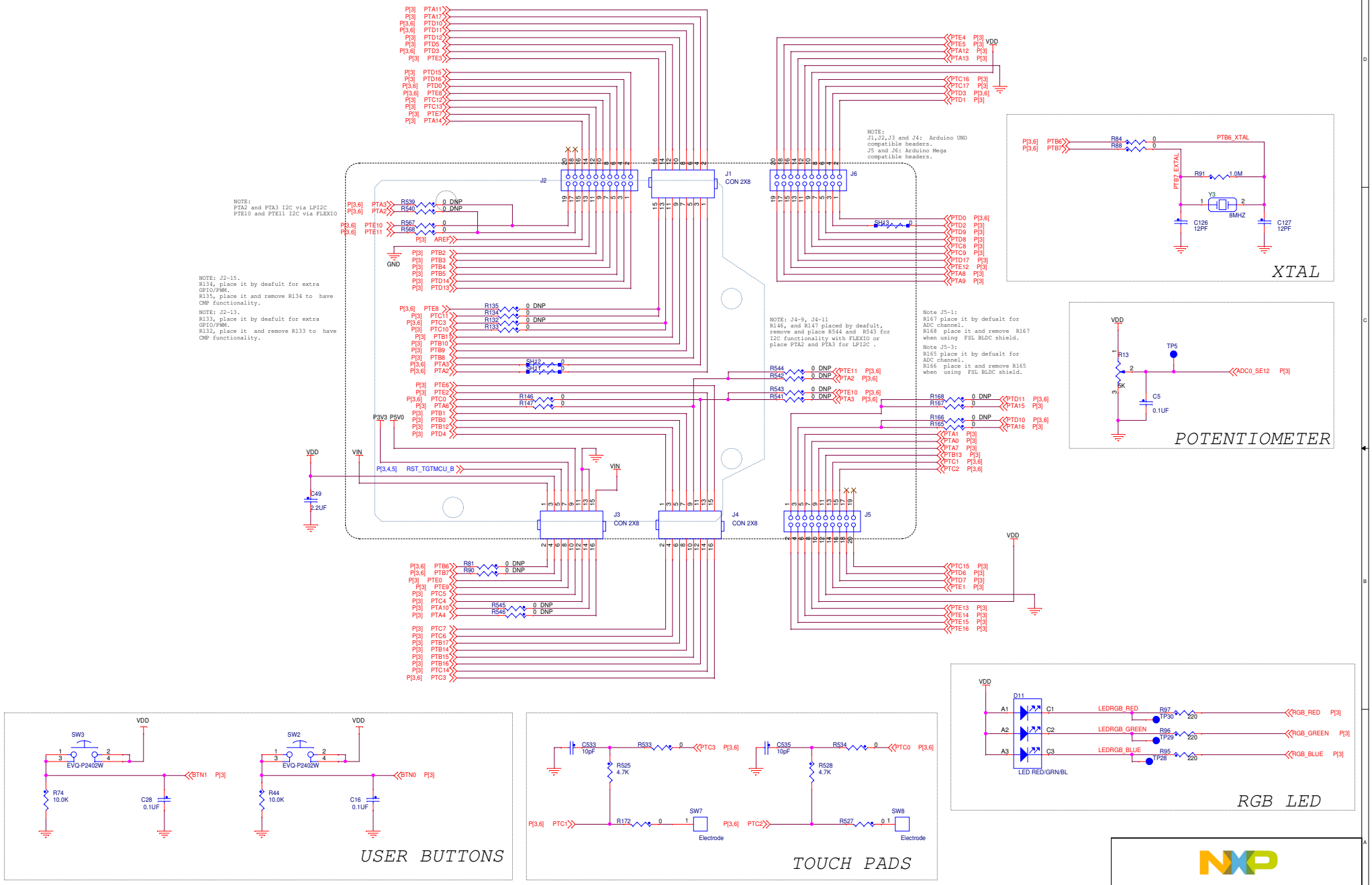

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