Lab 02 - Vivado

My repository

My git - Tomáš Křička, 223283

Constanst tables

Multiplexor connection

Port	Connected to	FPGA pin	Pin
a_i[0]	SW [0]	J15	IO_L24N_T3_RS0_15
a_i[1]	SW [1]	L16	IO_L3N_T0_DQS_EMCCLK_14
b_i[0]	SW [2]	M13	IO_L6N_T0_D08_VREF_14
b_i[1]	SW [3]	R15	IO_L13N_T2_MRCC_14
c_i[0]	SW [4]	R17	IO_L12N_T1_MRCC_14
c_i[1]	SW [5]	T18	IO_L7N_T1_D10_14
d_i[0]	SW [6]	U18	IO_L17N_T2_A13_D29_14
d_i[1]	SW [7]	R13	IO_L5N_T0_D07_14
sel_i[0]	SW [14]	U11	IO_L19N_T3_A09_D25_VREF_14
sel_i[1]	SW [15]	V10	IO_L21P_T3_DQS_14
f_o[0]	LED [0]	H17	IO_L18P_T2_A24_15
f_o[1]	LED [1]	K15	IO_L24P_T3_RS1_15

Nexys A7 - 50T, connection table

Switch	FPGA package pin	FPGA pin
SW[0]	J15	IO_L24N_T3_RS0_15
SW[1]	L16	IO_L3N_T0_DQS_EMCCLK_14
SW[2]	M13	IO_L6N_T0_D08_VREF_14
SW[3]	R15	IO_L13N_T2_MRCC_14
SW[4]	R17	IO_L12N_T1_MRCC_14
SW[5]	T18	IO_L7N_T1_D10_14

Switch	FPGA package pin	FPGA pin
SW[6]	U18	IO_L17N_T2_A13_D29_14
SW[7]	R13	IO_L5N_T0_D07_14
SW[8]	T8	IO_L24N_T3_34
SW[9]	U8	IO_25_34
SW[10]	R16	IO_L15P_T2_DQS_RDWR_B_14
SW[11]	T13	IO_L23P_T3_A03_D19_14
SW[12]	H6	IO_L24P_T3_35
SW[13]	U12	IO_L20P_T3_A08_D24_14
SW[14]	U11	IO_L19N_T3_A09_D25_VREF_14
SW[15]	V10	IO_L21P_T3_DQS_14

LED	FPGA package pin	FPGA pin
LED[0]	H17	IO_L18P_T2_A24_15
LED[1]	K15	IO_L24P_T3_RS1_15
LED[2]	J13	IO_L17N_T2_A25_15
LED[3]	N14	IO_L8P_T1_D11_14
LED[4]	R18	IO_L7P_T1_D09_14
LED[5]	V17	IO_L18N_T2_A11_D27_14
LED[6]	U17	IO_L17P_T2_A14_D30_14
LED[7]	U16	IO_L18P_T2_A12_D28_14
LED[8]	V16	IO_L16N_T2_A15_D31_14
LED[9]	T15	IO_L14N_T2_SRCC_14
LED[10]	U14	IO_L22P_T3_A05_D21_14
LED[11]	T16	IO_L15N_T2_DQS_DOUT_CSO_B_14
LED[12]	V15	IO_L16P_T2_CSI_B_14
LED[13]	V14	IO_L22N_T3_A04_D20_14
LED[14]	V12	IO_L20N_T3_A07_D23_14
LED[15]	V11	IO_L21N_T3_DQS_A06_D22_14

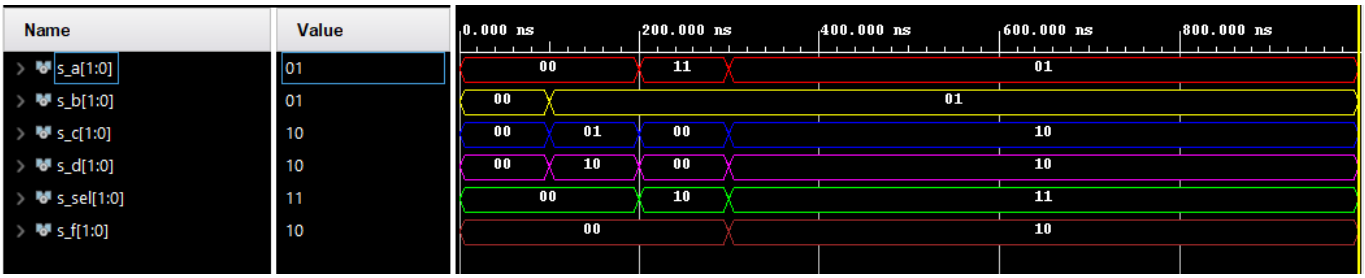
Architecture

```
architecture Behavioral of mux_2bit_4to1 is
begin

    f_o <= a_i when (sel_i = "00") else
           b_i when (sel_i = "01") else
           c_i when (sel_i = "10") else
           d_i;


    -- WRITE "GREATER" AND "EQUALS" ASSIGNMENTS HERE


end architecture Behavioral;
```

Stimulus

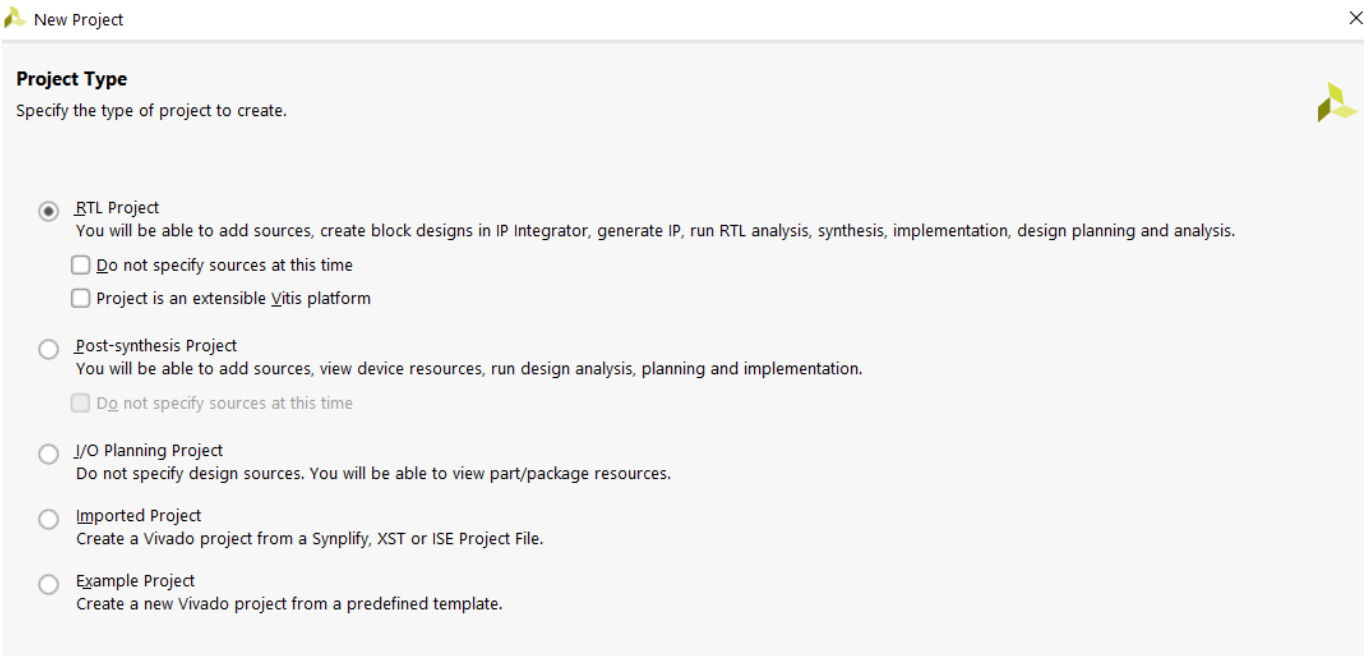
```
    p_stimulus : process
    begin
        -- Report a note at the begining of stimulus process
        report "Stimulus process started" severity note;

        s_d <= "00"; s_c <= "00"; s_b <= "00"; s_a <= "00";
        s_sel <= "00"; wait for 100 ns;

        s_d <= "10"; s_c <= "01"; s_b <= "01"; s_a <= "00";
        s_sel <= "00"; wait for 100 ns;

        s_d <= "00"; s_c <= "00"; s_b <= "01"; s_a <= "11";
        s_sel <= "10"; wait for 100 ns;

        s_d <= "10"; s_c <= "10"; s_b <= "01"; s_a <= "01";
        s_sel <= "11"; wait for 100 ns;


        -- WRITE OTHER TESTS HERE


        -- Report a note at the end of stimulus process
        report "Stimulus process finished" severity note;
        wait;
    end process p_stimulus;
```

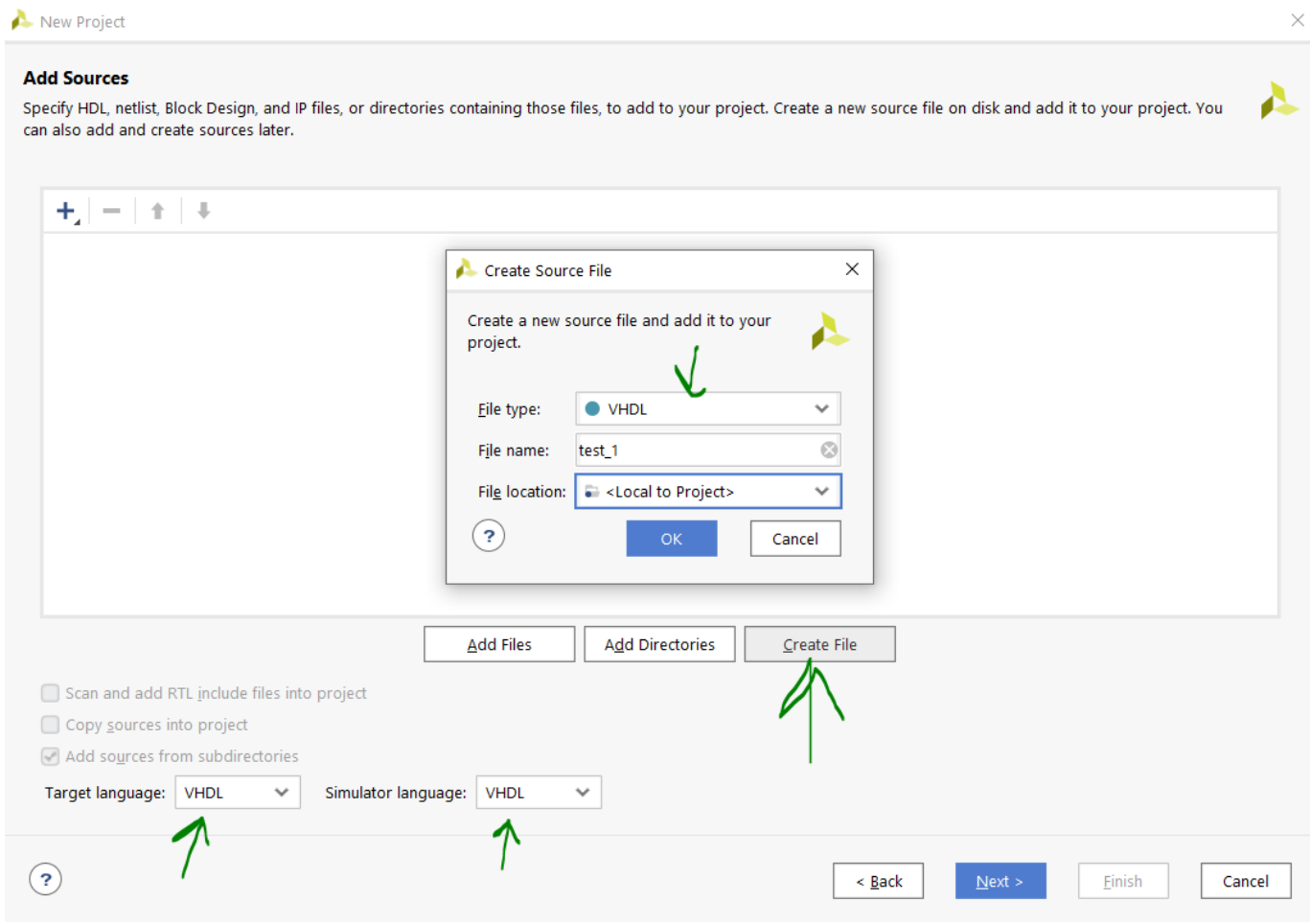
Waveforms

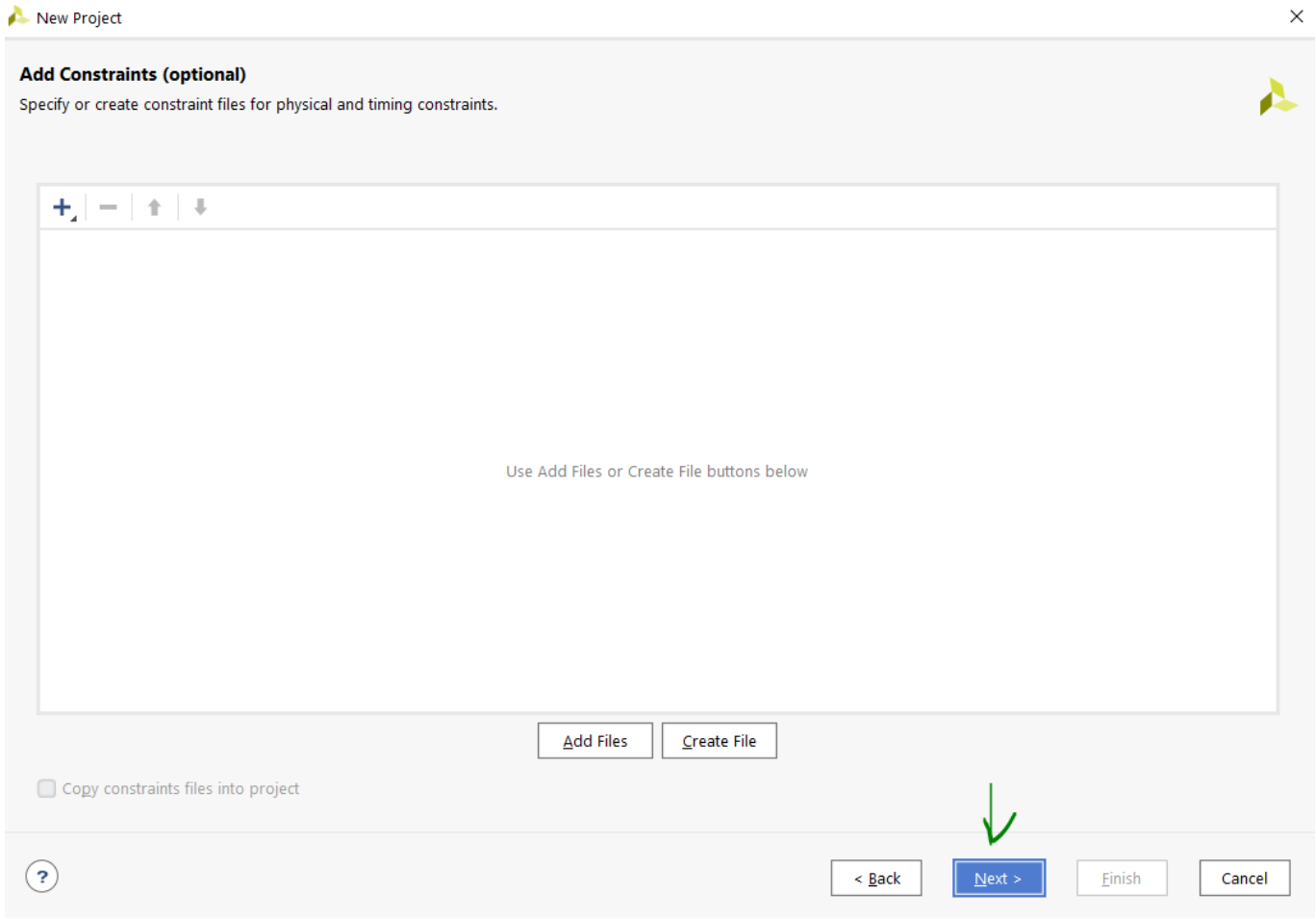


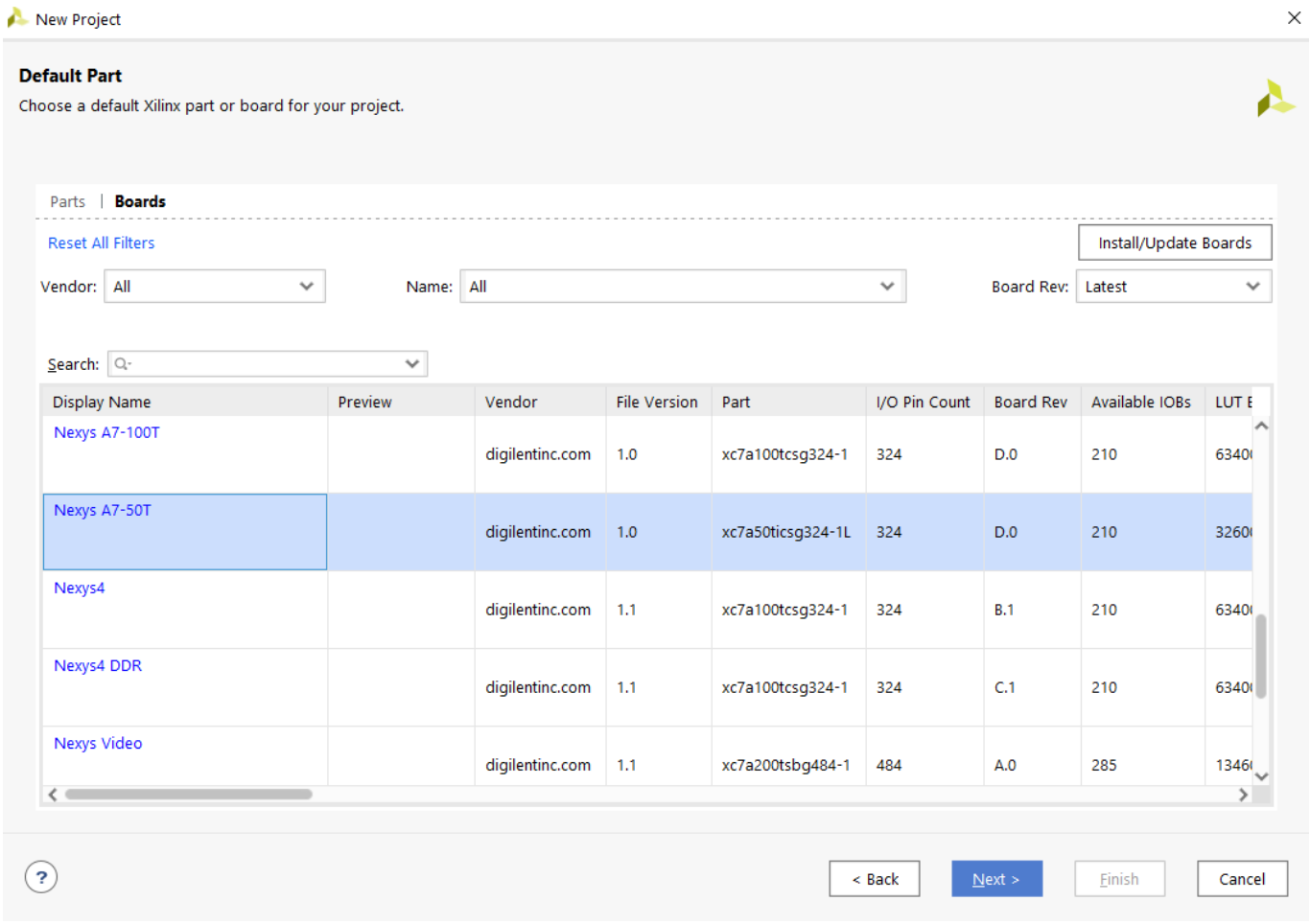
Vivado tutotial

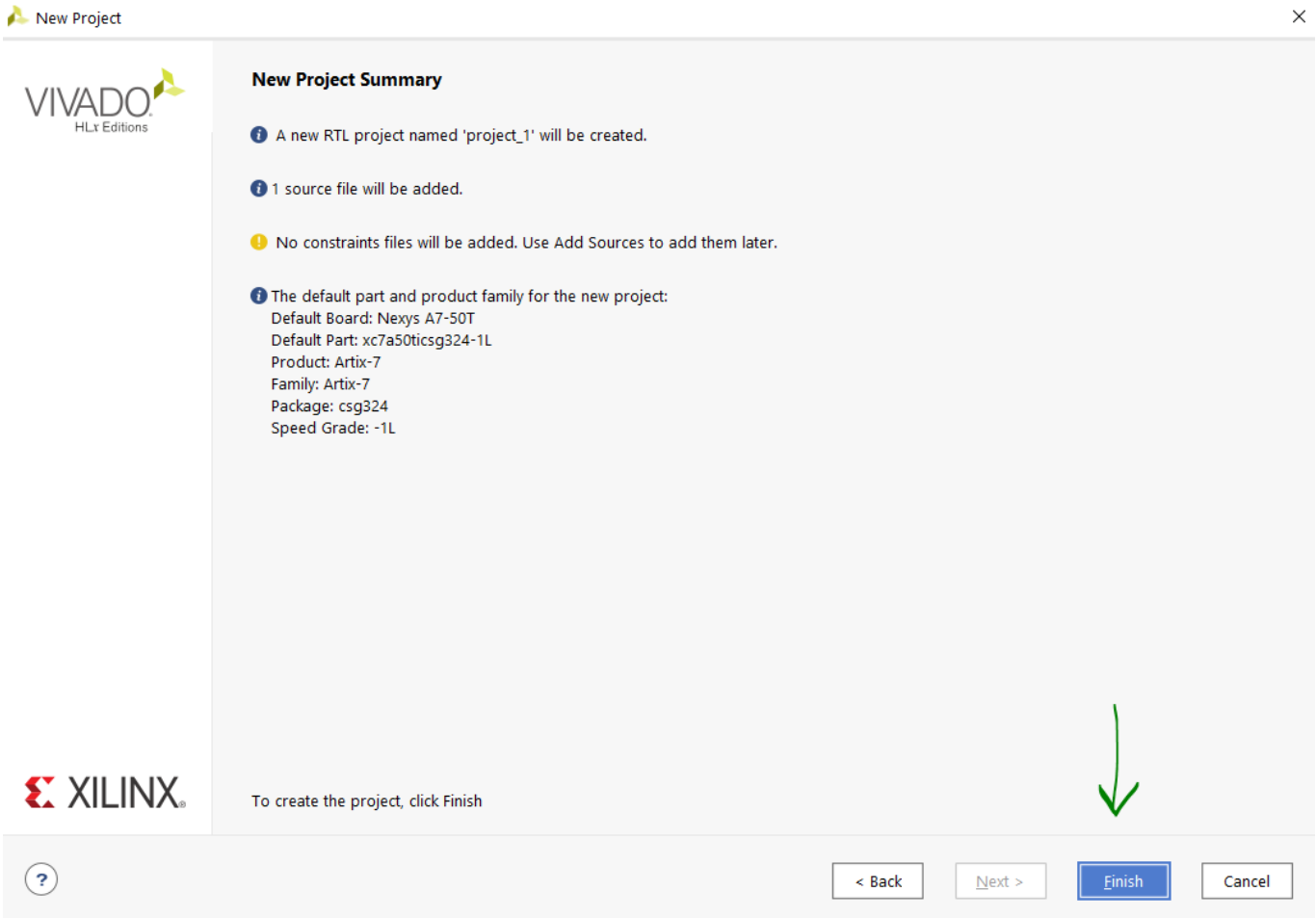
1. Create project and design

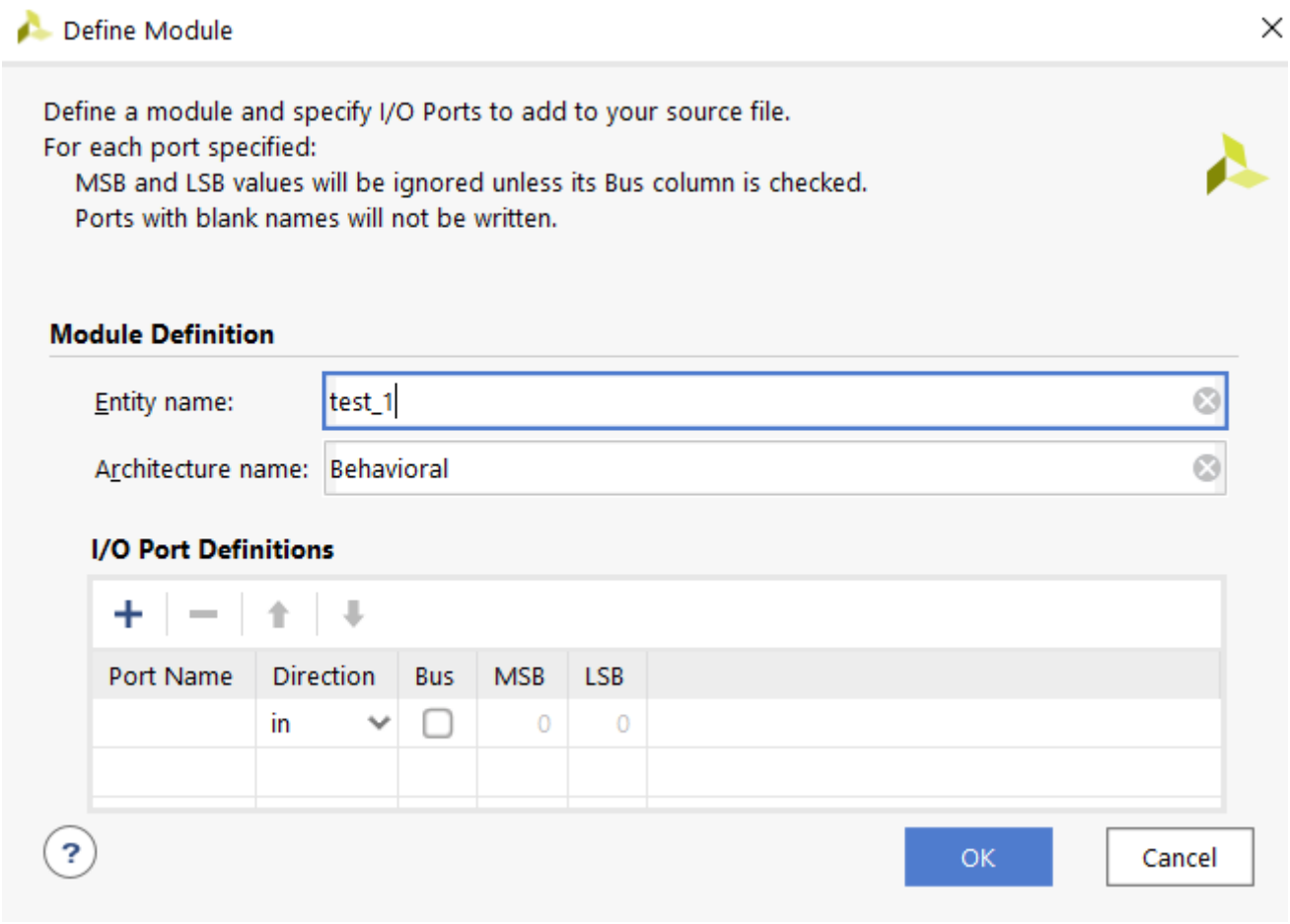


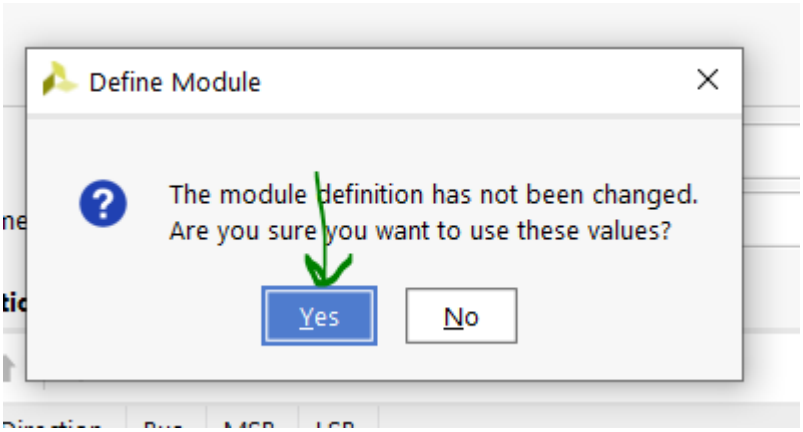

New Project
Add Sources
Specify HDL, netlist, Block Design, and IP files, or directories containing those files, to add to your project. Create a new source file on disk and add it to your project. You can also add and create sources later.
Create Source File
Create a new source file and add it to your project.
File type: VHDL
File name: test_1
File location: <Local to Project>
OK
Cancel
Add Files
Add Directories
Create File
Scan and add RTL include files into project
Copy sources into project
Add sources from subdirectories
Target language: VHDL
Simulator language: VHDL
< Back
Next >
Finish
Cancel


New Project
Add Constraints (optional)
Specify or create constraint files for physical and timing constraints.
Use Add Files or Create File buttons below
Add Files
Create File
Copy constraints files into project
< Back
Next >
Finish
Cancel

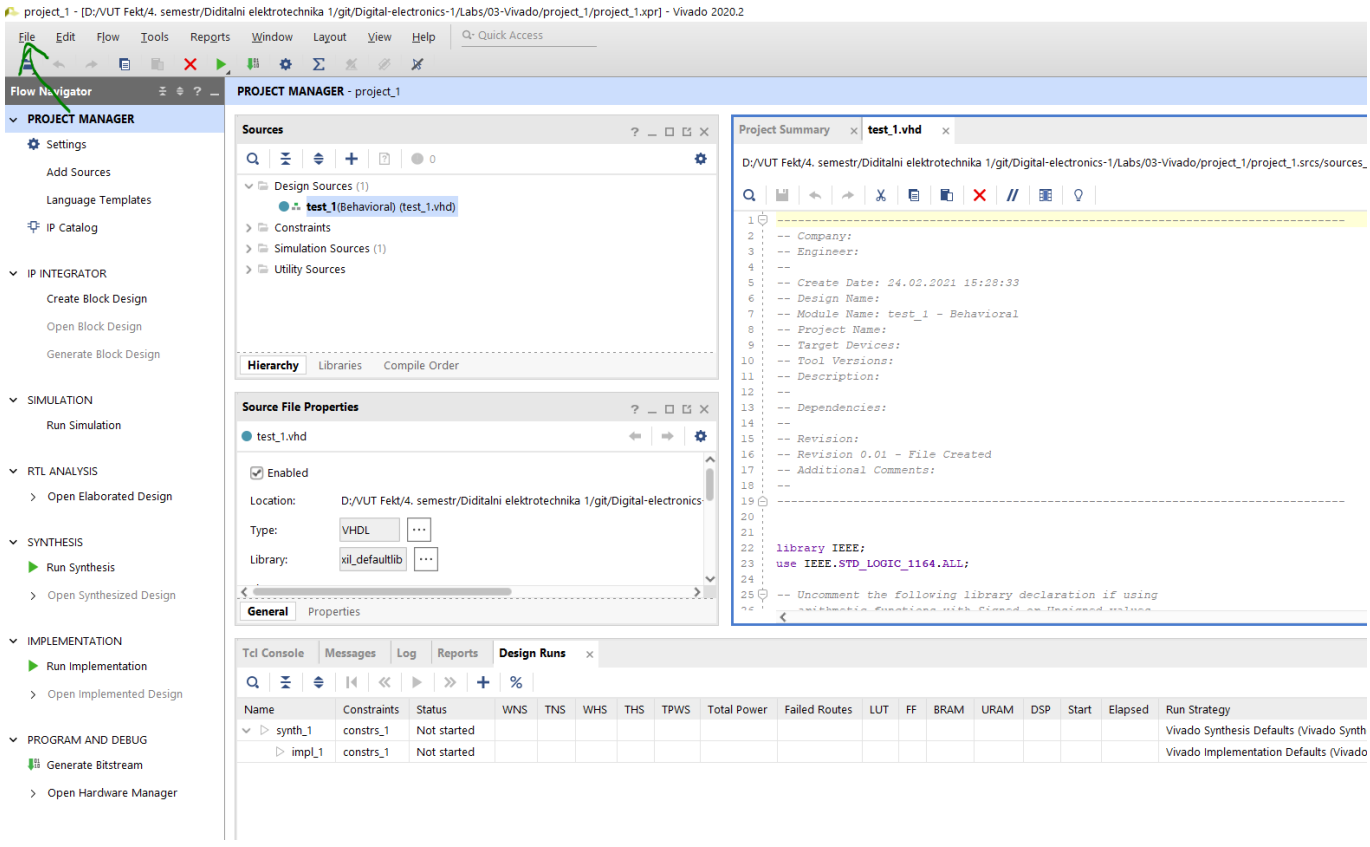

New Project
Default Part
Choose a default Xilinx part or board for your project.
Parts | Boards
Reset All Filters
Install/Update Boards
Vendor: All
Name: All
Board Rev: Latest
Search:
Display Name | Preview | Vendor | File Version | Part | I/O Pin Count | Board Rev | Available IOBs | LUT E
Nexys A7-100T | digilentinc.com | 1.0 | xc7a100tcsg324-1 | 324 | D.0 | 210 | 6340
Nexys A7-50T | digilentinc.com | 1.0 | xc7a50ticsg324-1L | 324 | D.0 | 210 | 3260
Nexys4 | digilentinc.com | 1.1 | xc7a100tcsg324-1 | 324 | B.1 | 210 | 6340
Nexys4 DDR | digilentinc.com | 1.1 | xc7a100tcsg324-1 | 324 | C.1 | 210 | 6340
Nexys Video | digilentinc.com | 1.1 | xc7a200tsbg484-1 | 484 | A.0 | 285 | 1346
< Back
Next >
Finish
Cancel

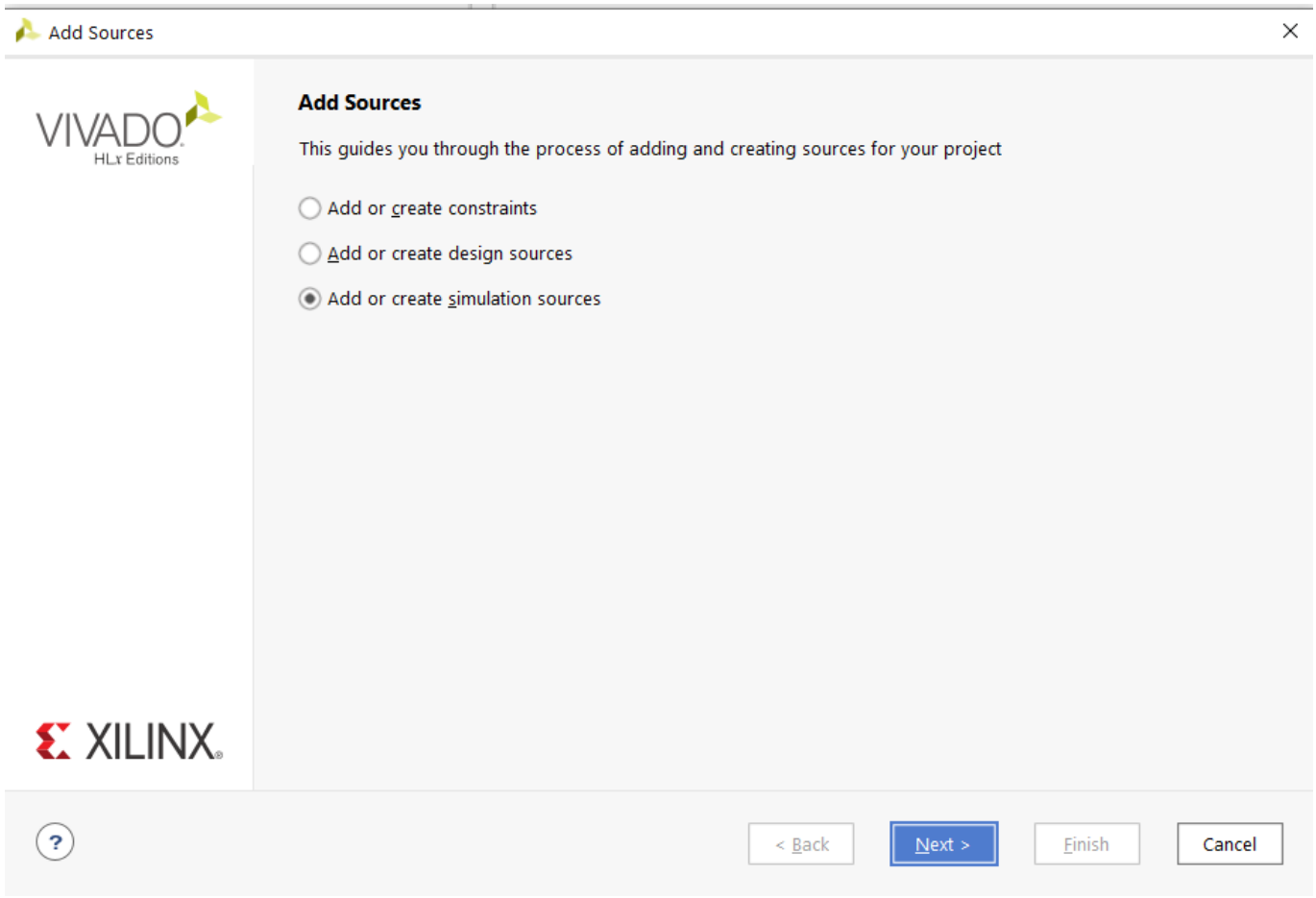

New Project
VIVADO HLx Editions
New Project Summary
A new RTL project named 'project_1' will be created.
1 source file will be added.
No constraints files will be added. Use Add Sources to add them later.
The default part and product family for the new project:
Default Board: Nexys A7-50T
Default Part: xc7a50ticsg324-1L
Product: Artix-7
Family: Artix-7
Package: csg324
Speed Grade: -1L
XILINX
To create the project, click Finish
< Back
Next >
Finish
Cancel

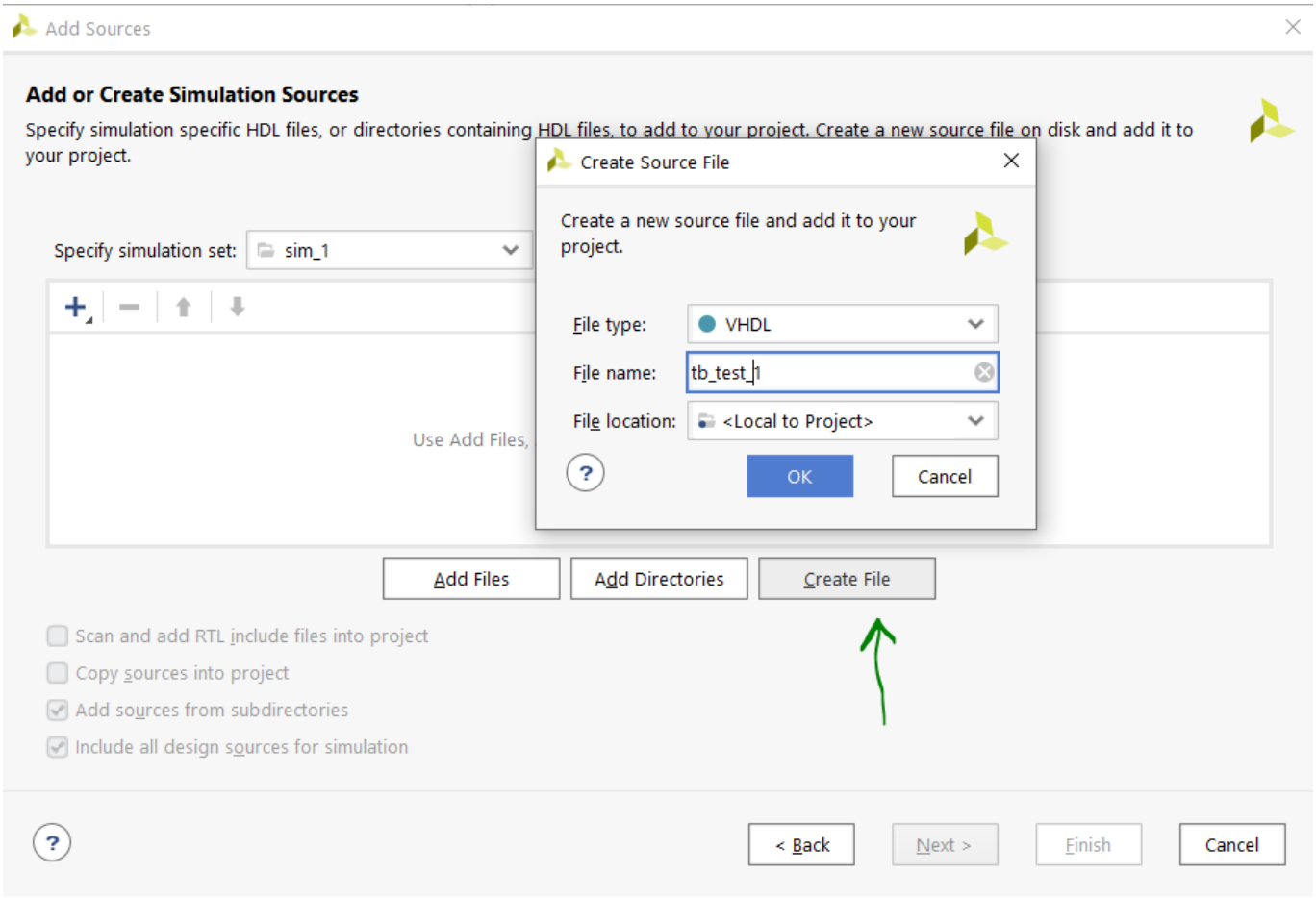


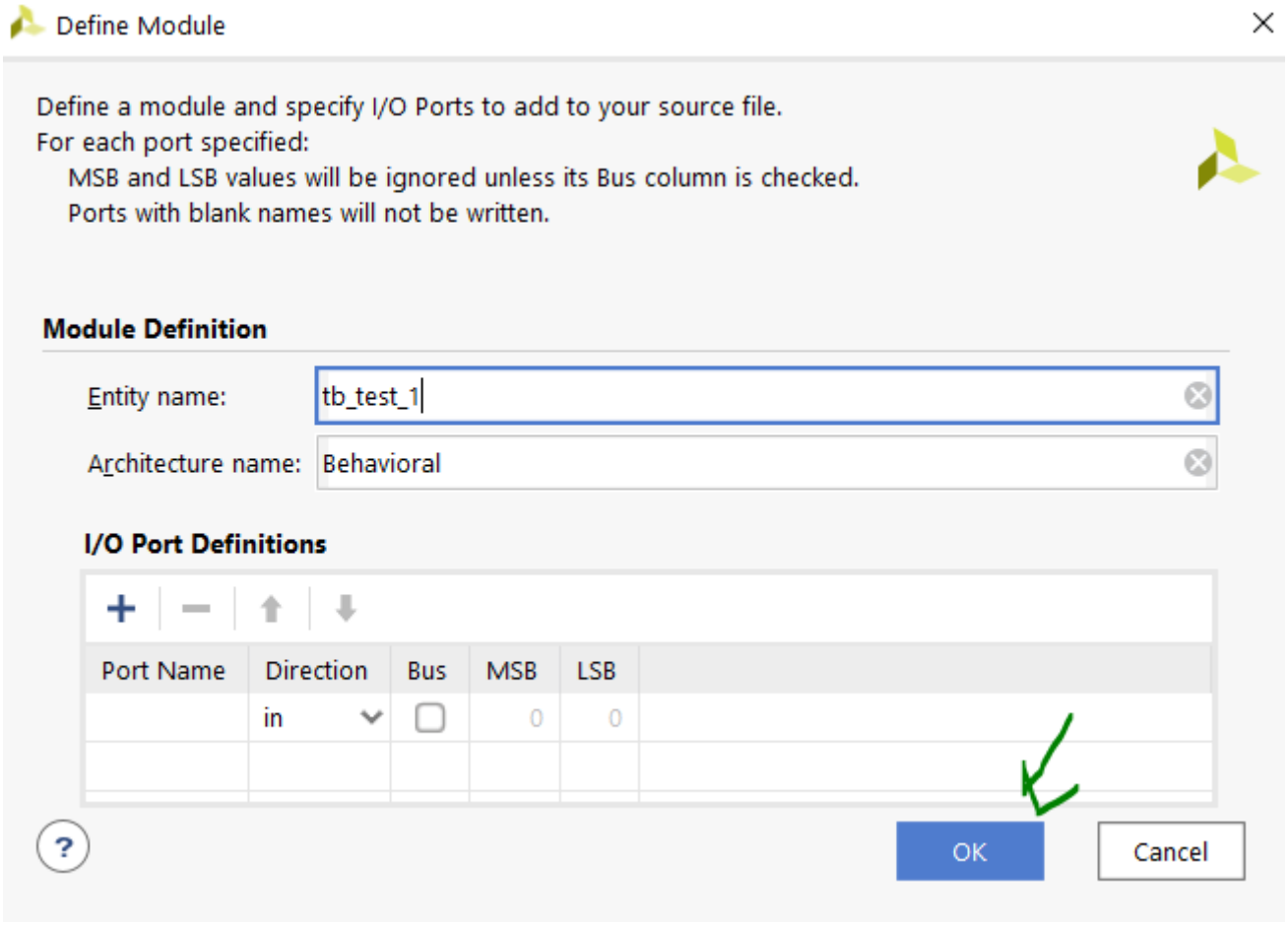


2. Create testbench

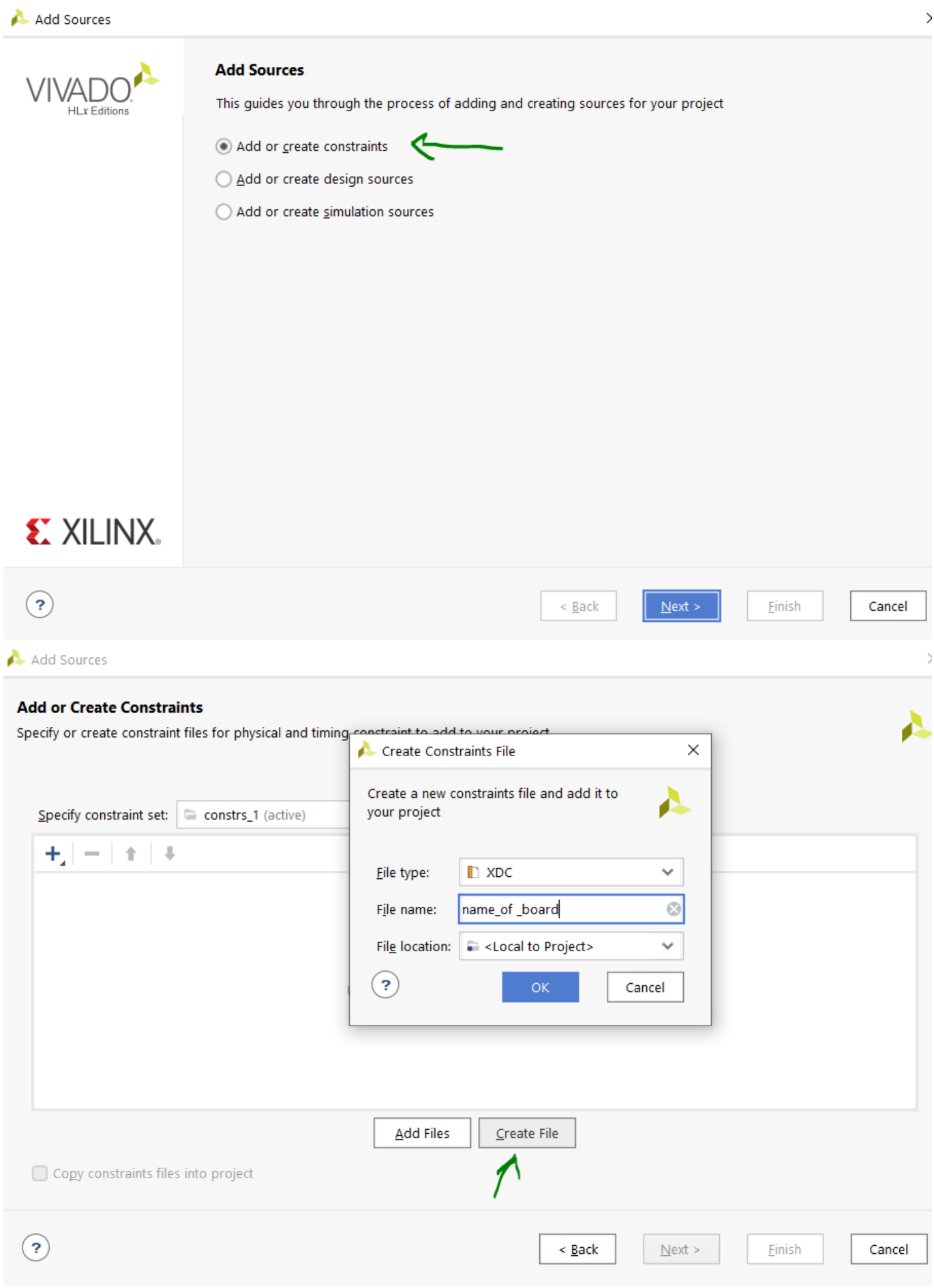

project_1 - [D:/VUT Fekt/4. semestr/Diditalni elektrotechnika 1/git/Digital-electronics-1/Labs/03-Vivado/project_1/project_1.xpr] - Vivado 2020.2
File Edit Flow Tools Reports Window Layout View Help
Quick Access
Flow Navigator
PROJECT MANAGER
Settings
Add Sources
Language Templates
IP Catalog
IP INTEGRATOR
Create Block Design
Open Block Design
Generate Block Design
SIMULATION
Run Simulation
RTL ANALYSIS
Open Elaborated Design
SYNTHESIS
Run Synthesis
Open Synthesized Design
IMPLEMENTATION
Run Implementation
Open Implemented Design
PROGRAM AND DEBUG
Generate Bitstream
Open Hardware Manager
PROJECT MANAGER - project_1
Sources
Design Sources (1)
test_1(Behavioral) (test_1.vhd)
Constraints
Simulation Sources (1)
Utility Sources
Hierarchy Libraries Compile Order
Source File Properties
test_1.vhd
Enabled
Location: D:/VUT Fekt/4. semestr/Diditalni elektrotechnika 1/git/Digital-electronics-
Type: VHDL
Library: xil_defaultlib
General Properties
Project Summary
test_1.vhd
D:/VUT Fekt/4. semestr/Diditalni elektrotechnika 1/git/Digital-electronics-1/Labs/03-Vivado/project_1/project_1.srcs/sources_
-- Company:
-- Engineer:
-- Create Date: 24.02.2021 15:28:33
-- Design Name:
-- Module Name: test_1 - Behavioral
-- Project Name:
-- Target Devices:
-- Tool Versions:
-- Description:
-- Dependencies:
-- Revision:
-- Revision 0.01 - File Created
-- Additional Comments:
library IEEE;
use IEEE.STD_LOGIC_1164.ALL;
-- Uncomment the following library declaration if using
Tcl Console Messages Log Reports Design Runs
Name Constraints Status WNS TNS WHS THS TPWS Total Power Failed Routes LUT FF BRAM URAM DSP Start Elapsed Run Strategy
synth_1 constrs_1 Not started Vivado Synthesis Defaults (Vivado Synth
impl_1 constrs_1 Not started Vivado Implementation Defaults (Vivado


Add Sources
VIVADO HLx Editions
Add Sources
This guides you through the process of adding and creating sources for your project
Add or create constraints
Add or create design sources
Add or create simulation sources
XILINX
< Back
Next >
Finish
Cancel

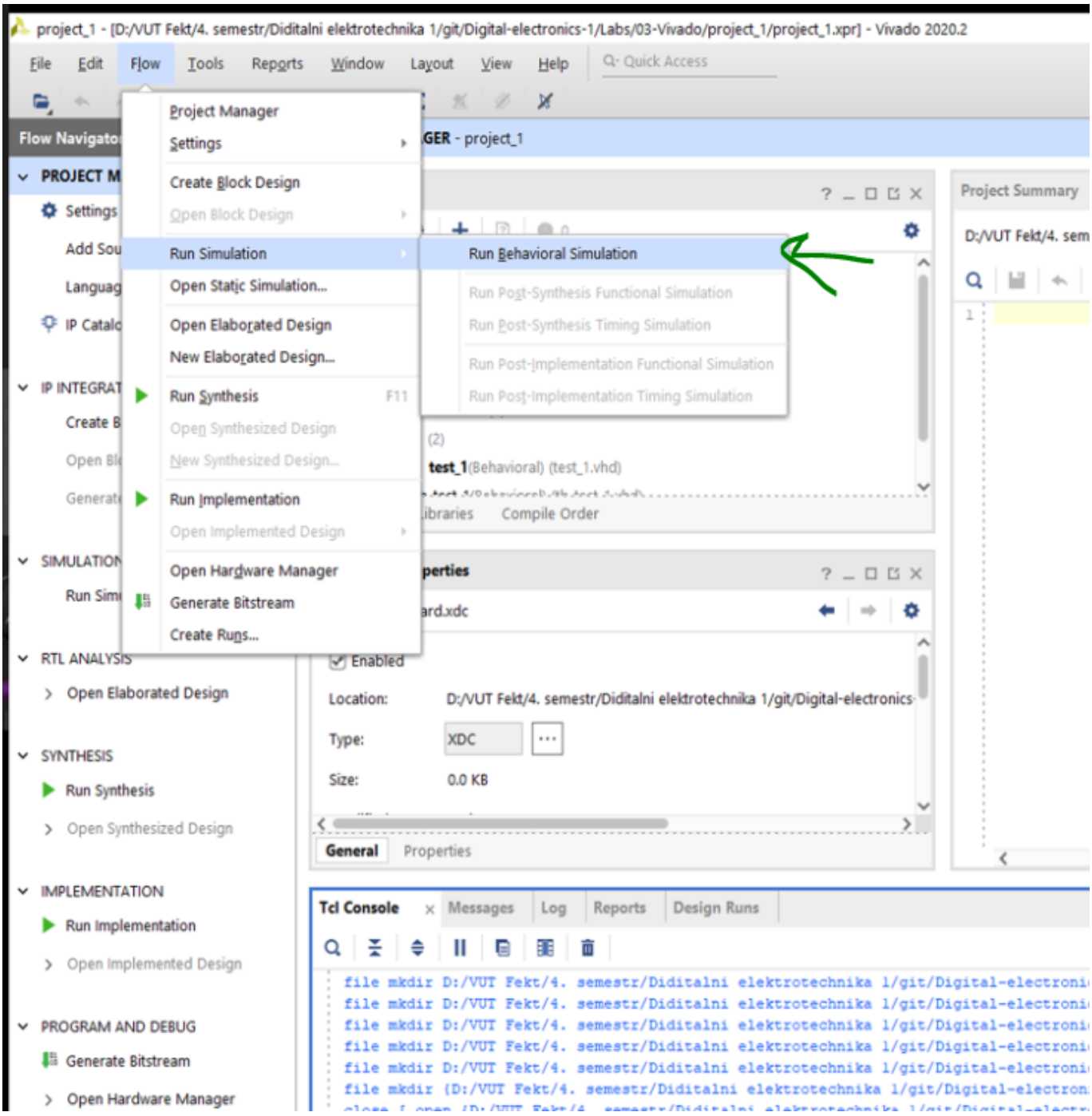




3. Create Constants



4. Run simulation


project_1 - [D:/VUT Fekt/4. semestr/Diditalni elektrotechnika 1/git/Digital-electronics-1/Labs/03-Vivado/project_1/project_1.xpr] - Vivado 2020.2
File Edit Flow Tools Reports Window Layout View Help
Quick Access
Project Manager
Settings
Create Block Design
Open Block Design
Run Simulation
Open Static Simulation...
Open Elaborated Design
New Elaborated Design...
Run Synthesis F11
Open Synthesized Design
New Synthesized Design...
Run Implementation
Open Implemented Design
Open Hardware Manager
Generate Bitstream
Create Runs...
Run Behavioral Simulation
Run Post-Synthesis Functional Simulation
Run Post-Synthesis Timing Simulation
Run Post-Implementation Functional Simulation
Run Post-Implementation Timing Simulation
Flow Navigator
PROJECT MANAGER - project_1
Project Summary
D:/VUT Fekt/4. sem
test_1(Behavioral) (test_1.vhd)
Libraries Compile Order
Properties
Enabled
Location: D:/VUT Fekt/4. semestr/Diditalni elektrotechnika 1/git/Digital-electronics
Type: XDC
Size: 0.0 KB
General Properties
SIMULATION
Run Simulation
RTL ANALYSIS
Open Elaborated Design
SYNTHESIS
Run Synthesis
Open Synthesized Design
IMPLEMENTATION
Run Implementation
Open Implemented Design
PROGRAM AND DEBUG
Generate Bitstream
Open Hardware Manager
Tcl Console
Messages
Log
Reports
Design Runs
file mkdir D:/VUT Fekt/4. semestr/Diditalni elektrotechnika 1/git/Digital-electroni
file mkdir D:/VUT Fekt/4. semestr/Diditalni elektrotechnika 1/git/Digital-electroni
file mkdir D:/VUT Fekt/4. semestr/Diditalni elektrotechnika 1/git/Digital-electroni
file mkdir D:/VUT Fekt/4. semestr/Diditalni elektrotechnika 1/git/Digital-electroni
file mkdir D:/VUT Fekt/4. semestr/Diditalni elektrotechnika 1/git/Digital-electroni
file mkdir {D:/VUT Fekt/4. semestr/Diditalni elektrotechnika 1/git/Digital-electron