Advance Information

AMD 80C287

80-Bit CMOS Numeric Processor

Advanced Micro Devices

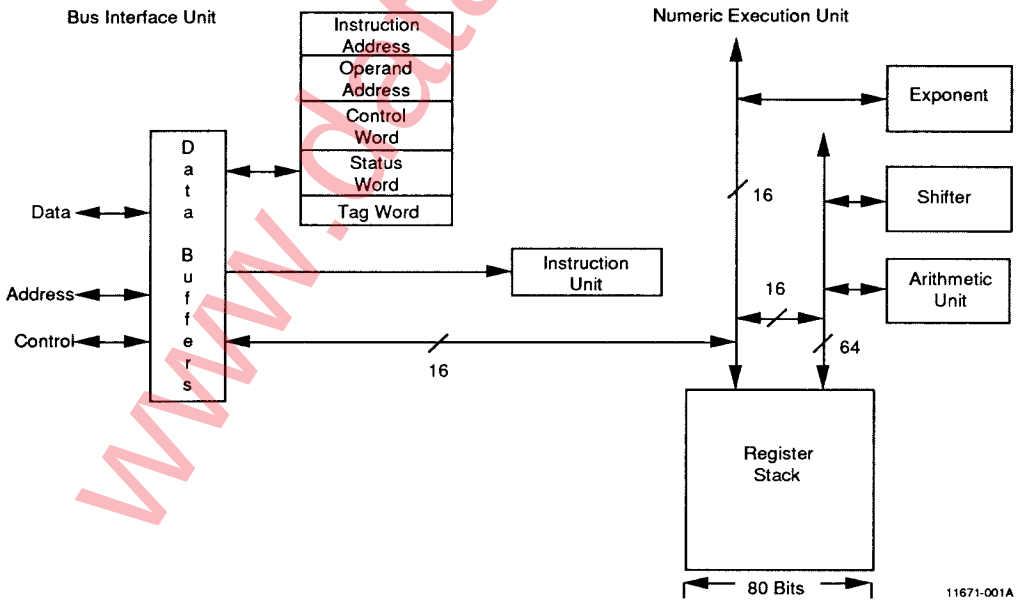
DISTINCTIVE CHARACTERISTICS

- **Pin compatible and functionally equivalent to the Intel 80287**
- **High-performance CMOS process yields 10-MHz, 12-MHz, and 16-MHz speed grades**
- **Available in space-saving 44-pin PLCC as well as 40-pin DIP**
- **80-bit numeric accelerator for 80C286 and 80286-based systems**
- **Compatible with IEEE floating-point standard 754**
- **Static CMOS design does not require a minimum clock rate, resulting in significantly lower power dissipation**
- **Performs single-, double-, and extended-precision floating-point, as well as word, short, and long integer and 18-digit BCD conversions**
- **Adds trigonometric, logarithmic, exponential, and arithmetic instructions to the 80C286 instruction set**

GENERAL DESCRIPTION

The 80C287 is implemented in AMD's advanced static CMOS process that allows for significantly higher speeds at a much lower power dissipation than traditional NMOS versions or standard CMOS. Functionally equivalent to the Intel 80287, the 80C287 is a high-performance arithmetic processor that expands the 80C286 instruction set with floating-point instructions including transcendentals, and integer and BCD conversions. The floating-point operations comply with the IEEE Standard 754. The device is available in 8-, 10-, 12-, and 16-MHz speed grades and is provided in 44-pin PLCC and 40-pin DIP packages. When coupled with the 80C286, the 80C287 provides a complete solution for high-performance numeric processing applications.

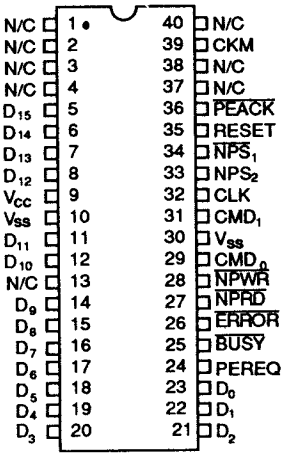
BLOCK DIAGRAM



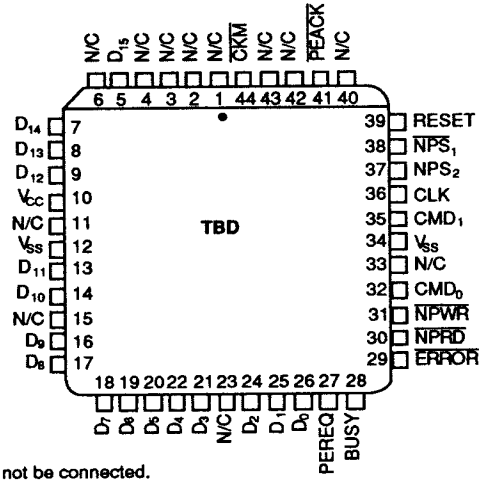
Publication # 11671 Rev. B Amendment /0
Issue Date: June 1989

CONNECTION DIAGRAM

DIP



PLCC



Note: N/C pins should not be connected.
Pin 1 is marked for orientation.

11671-002A

PIN DESCRIPTION

$\overline{BUSY}$ $\overline{Busy\ Status}$ (Output; Active Low)

A LOW level indicates that the 80C287 is currently executing a command.

CKM Clock Mode Signal (Input)

When CKM is HIGH, the CLK is used directly. When CKM is LOW, CLK is divided by three. This input must be either HIGH or LOW 20 CLK cycles before RESET goes LOW.

CLK Clock (Input)

Provides timing for 80C287 operations.

CMD_1, CMD_0 Command Lines (Input)

CMD_1 and CMD_0, along with select inputs, allow the CPU to direct the 80C287 operations. These inputs are timed relative to the read and write strobes.

D_{15}–D_0 Data (Input/Output)

Bidirectional data bus. These inputs are timed relative to the read and write strobes.

$\overline{ERROR}$ $\overline{Error\ Status}$ (Output; Active Low)

Reflects the error summary status bit of the status word. A LOW level indicates that an unmasked exception condition exists.

$\overline{NPRD}$ $\overline{Numeric\ Processor\ Read}$ (Input; Active Low)

A LOW level enables transfer of data from the 80C287. This input may be asynchronous to the 80C287 clock.

$\overline{NPS_1}$, NPS_2 Numeric Processor Selects (Input)

Indicates the CPU is transferring data to and from the 80C287. Asserting both signals ($\overline{NPS_1}$ LOW and NPS_2 HIGH) enables the 80C287 to transfer floating-point data or instructions. No data transfers involving the 80C287 will occur unless the 80C287 is selected via $\overline{NPS_1}$ and NPS_2. These inputs are timed relative to the read and write strobes.

$\overline{NPWR}$ Numeric Processor Write (Input; Active Low)

A LOW level enables transfer of data from the 80C287. This input may be asynchronous to the 80C287 clock.

$\overline{PEACK}$ Processor Extension Acknowledge (Input; Active Low)

A LOW level indicates that the request signal (PEREQ) has been recognized. $\overline{PEACK}$ causes the request (PEREQ) to be withdrawn when no more transfers are required. $\overline{PEACK}$ may be asynchronous to the 80C287 clock.

PEREQ Processor Extension Request (Output)

A HIGH level indicates that the 80C287 is ready to transfer data. PEREQ will be disabled upon assertion of $\overline{PEACK}$ or upon actual data transfer, whichever occurs first, when no more transfers are required.

RESET System Reset (Input)

Reset causes the 80C287 to immediately terminate its present activity and enter a dormant state. Reset must be HIGH for more than four CLK cycles. For proper initialization the HIGH-LOW transition must occur no sooner than 50 µs after V_{CC} and CLK meet their DC and AC specifications.

V_{CC} +5 V Supply (Input)

V_{SS} System Ground (Input)

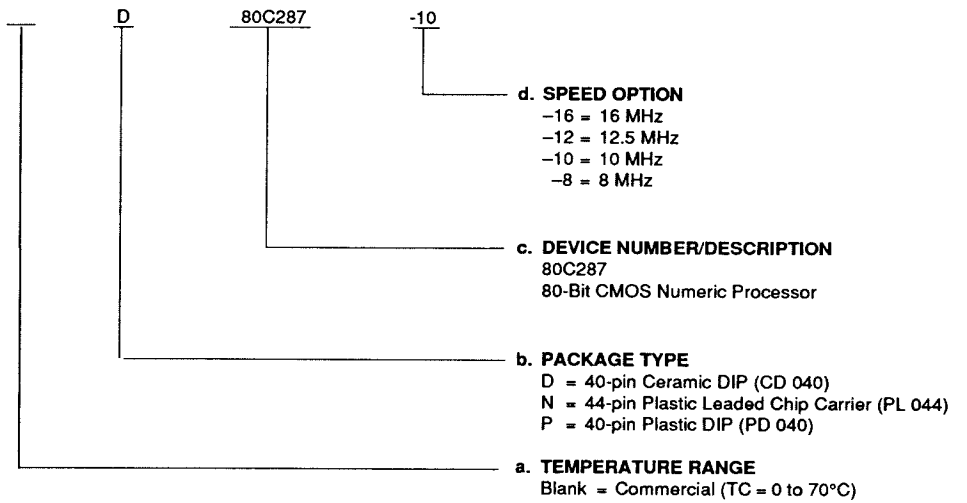
Both pins must be connected to ground.

ORDERING INFORMATION

Commodity Products

AMD products are available in several packages and operating ranges. The order number (Valid Combination) is formed by a combination of:

a. Temperature Range
b. Package Type
c. Device Number
d. Speed Option (if applicable)
e. Optional Processing



Valid Combination	
D, N, P	80C287–16
	80C287–12
	80C287–10
	80C287–8

Valid Combination

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations and to check on newly released valid combinations.

SIMPLIFIED FUNCTIONAL DESCRIPTION

The 80C287 is internally divided into two basic processing units; the numeric execution unit, and the bus interface unit as shown in the block diagram. The numeric execution unit performs numeric instructions. The bus interface unit receives and decodes instructions, executes processor control instructions, and requests operands transfers to and from memory. The 80C286 may execute non-numeric instruction concurrently with numeric instruction executed on the 80C287. Synchronization and error recognition occurs when the next numeric instruction is decoded by the 80C286.

The Numeric Execution Unit

The numeric execution data path is 80 bits wide. All operands are converted to the internal 80-bit format before use. These instructions include arithmetic, transcendental, constant, and data transfer instructions.

The Bus Interface Unit

The bus interface unit decodes the ESC instruction executed by the 80C286. The signal $\overline{BUSY}$ is activated for 80C286/80C287 synchronization and the signal $\overline{ERROR}$ is activated for error detection. $\overline{BUSY}$ is activated when an instruction is transferred and deactivated when the instruction completes. $\overline{ERROR}$ will be asserted if an error has occurred when $\overline{BUSY}$ is deactivated.

The signals PEREQ, $\overline{PEACK}$, $\overline{NPRD}$, $\overline{NPWR}$, $\overline{NPS_1}$, CMD_0, CMD_1, and NPS_2 control data transfers between the 80C287 and the 80C286. The 80C286 performs the actual data transfer with memory.

The Register Stack

The register stack contains eight 80-bit data registers, organized as a push down stack. Operations are performed on the stack top, between the stack top and another register, or between the stack top and memory.

System Configuration with 80C286

A simplified block diagram of the 80C287 interface to a 80C286 CPU is shown in Figure 1. The 80C287 can operate concurrently with the host CPU. The signals PEREQ, $\overline{PEACK}$, $\overline{BUSY}$, $\overline{NPRD}$, $\overline{NPWR}$, CMD_0, and CMD_1 allow the 80C287 to receive instructions and data from the 80C286. Detection of errors are indicated to the CPU by asserting the signal $\overline{ERROR}$. The address decode logic, bus control and timing logic is shown in this implementation using AMD PAL® devices but may also be accomplished using standard chip sets.

The 80C287 operates either directly from the CPU clock or with a dedicated clock. The 80C287 functions at two-thirds the frequency of the 80C286 when operating with the CPU clock (i.e., for a 16-MHz 80C286, the 32-MHz clock is divided down to 10.6 MHz).

1

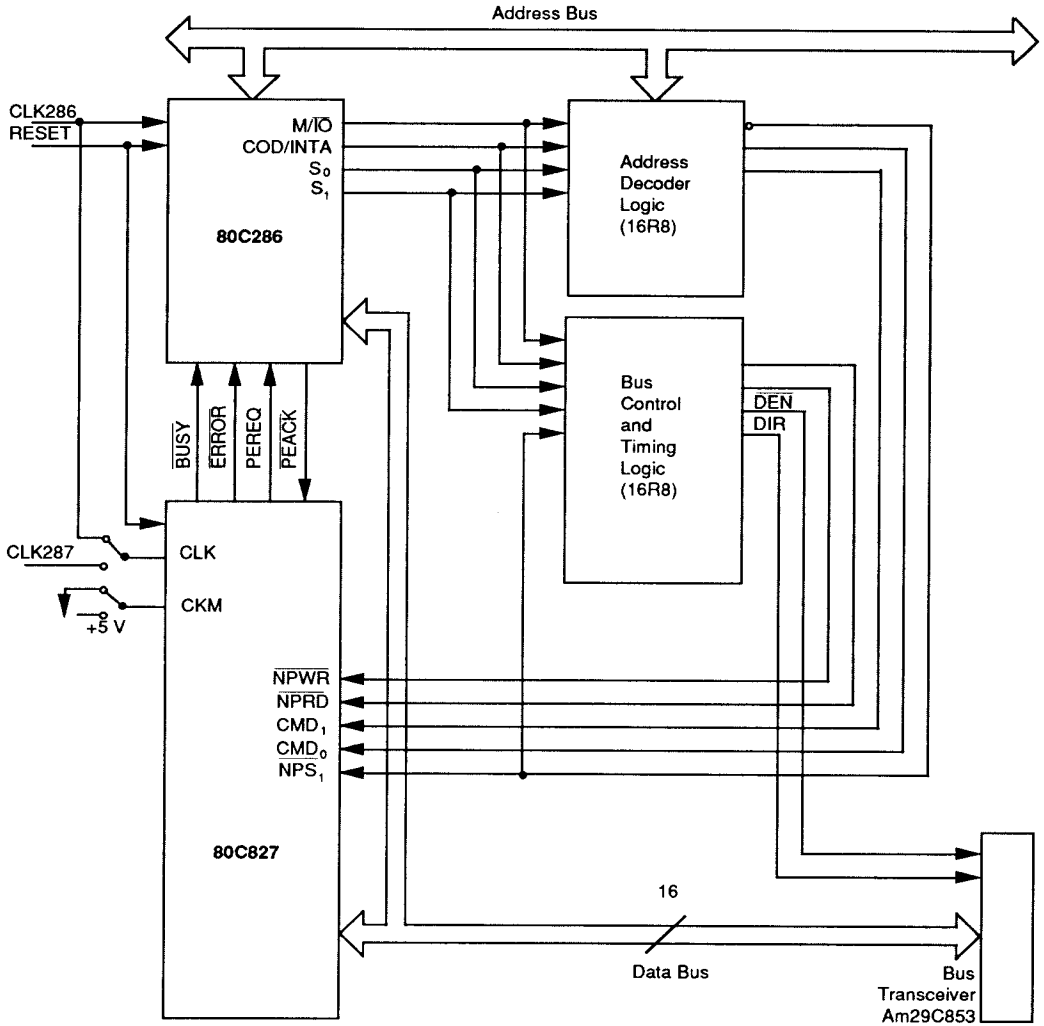


Figure 1. 80C286/80C287 Simplified System Configuration

11671-003A

ABSOLUTE MAXIMUM RATINGS

Storage Temperature ..... –65 to +150° C
Ambient Temperature Under Bias ..... –55 to +125° C
Supply Voltage to Ground Potential
Continuous ..... –1.0 to +7.0 V
DC Voltage Applied to Outputs
for HIGH Output State ..... –0.3 V to + V_{CC} +0.3 V
DC Input Voltage ..... –0.3 to V_{CC} +0.3 V
DC Output Current, into LOW Outputs ..... 30 mA
DC Input Current ..... –10 to +10 mA
Power Dissipation (max.) ..... 1.5 W

Stresses above those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may affect devices reliability.

OPERATING RANGES

Commercial (C) Devices
Temperature, Ambient (T_A) ..... 0 to +70°C
(also meets 0 to 100°C Case Temperature (T_C) for laptop requirements)
Supply Voltage (V_{CC}) ..... +4.75 to +5.25 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

DC CHARACTERISTICS over operating range unless otherwise specified (for APL Products, Group A, Subgroups 1, 2, 3 are tested unless otherwise noted)

Parameter Symbol	Parameter Description	Test Conditions		Min.	Max.	Unit
V_{OH}	Output HIGH Voltage	V_{CC} = Min. V_{IN} = V_{IL} or V_{IH}	I_{OH} = -0.4 mA	2.4		V
V_{OL}	Output LOW Voltage	V_{CC} = Min. V_{IN} = V_{IL} or V_{IH}	I_{OL} = 3 mA		0.45	
V_{IH}	Guaranteed Input Logical HIGH Voltage (see note below)			2.0	V_{CC} +0.5	V
V_{IL}	Guaranteed Input Logical LOW Voltage (see note below)			–0.5	0.8	V
V_{IHC}	Clock Input HIGH Voltage CKM = 1 CKM = 0			2.0 3.8	V_{CC} +1.0 V_{CC} +1.0	V V
V_{ILC}	Clock Input Low Voltage CKM = 1 CKM = 0			 –0.5 –0.5	 0.8 0.6	 V V
I_{LI}	Input Leakage Current	0 V ≤ V_{IN} ≤ V_{CC}			±10	µA
I_{OZH}	Off-State (HIGH Impedance) Output Current	V_{CC} = Max., V_O = 2.4 V			10	µA
I_{OZL}	Off-State (HIGH Impedance) Output Current	V_{CC} = Max., V_O = 0.45 V			–10	µA
I_{CCD}	Power Supply Current, Operating	V_{CC} = Max. Outputs Unloaded		10 mA/MHz		
I_{CCS}	Power Supply Current, Static	V_{CC} = Max., V_{IN} – V_{CC} or GND, I_O = OµA		5 mA		

Note: These input levels provide zero-noise immunity and should only be statically tested in a noise-free environment (not functionally tested).

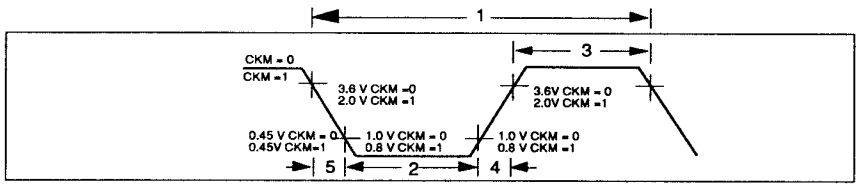
SWITCHING CHARACTERISTICS over COMMERCIAL operating range

No.	Parameter Description	Test Conditions	80C287-8 Min.	80C287-8 Max.	Unit
1	Clock Period				
	CLM = 1		125		ns
	CLM = 0		50		ns
2	Clock LOW Time				
	CLM = 1		68		ns
	CLM = 0		15		ns
3	Clock HIGH Time				
	CLM = 1		43		ns
	CLM = 0		20		ns
4	Clock Rise Time			10	ns
5	Clock Fall Time			10	ns
6	Data Setup to $\overline{\text{NPWR}}$ Inactive		75		ns
7	Data Hold from $\overline{\text{NPWR}}$ Inactive		18		ns
8	$\overline{\text{NPWR}}$, $\overline{\text{NPRD}}$ Active Time		90		ns
9	Command Valid Setup Time		0		ns
10	PEREQ Active to $\overline{\text{NPRD}}$ Active		130		ns
11	$\overline{\text{PEACK}}$ Active Time		85		ns
12	$\overline{\text{PEACK}}$ Inactive Time		250		ns
13	$\overline{\text{PEACK}}$ Inactive to $\overline{\text{NPRD}}$, $\overline{\text{NPWR}}$ Inactive		40		ns
14	$\overline{\text{NPRD}}$, $\overline{\text{NPWR}}$ Inactive to $\overline{\text{PEACK}}$ Active		–30		ns
15	Command Valid Hold Time		30		ns
16	$\overline{\text{PEACK}}$ Active Setup to $\overline{\text{NPRD}}$, $\overline{\text{NPWR}}$		40		ns
17	$\overline{\text{NPRD}}$, $\overline{\text{NPWR}}$ to CLK Setup		70		ns
18	$\overline{\text{NPRD}}$, $\overline{\text{NPWR}}$ CLK Hold		45		ns
19	$\overline{\text{RESET}}$ to CLK Setup		20		ns
20	$\overline{\text{RESET}}$ from CLK Hold		20		ns
21	$\overline{\text{NPRD}}$ Inactive to Data Float			35	ns
22	$\overline{\text{NPRD}}$ Active to Data Valid			60	ns
23	$\overline{\text{ERROR}}$ Active to $\overline{\text{BUSY}}$ Inactive		100		ns
24	$\overline{\text{NPWR}}$, Active to $\overline{\text{BUSY}}$ Active			100	ns
25	$\overline{\text{PEACK}}$ Active to $\overline{\text{PEREQ}}$ Inactive			127	ns
26	$\overline{\text{NPRD}}$, $\overline{\text{NPWR}}$ Active to $\overline{\text{PEREQ}}$ Inactive			100	ns
27	Command Inactive Time				
	Write to Write				ns
	Read to Read				ns
	Write to Read				ns
	Read to Write				ns
28	Data Hold from Time $\overline{\text{NPRD}}$ Inactive				ns

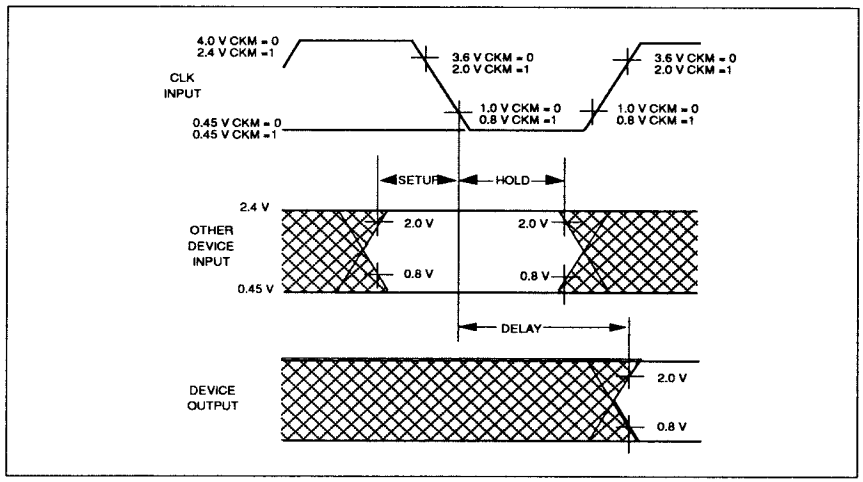
SWITCHING CHARACTERISTICS over COMMERCIAL operating range (continued)

No.	Parameter Description	Test Conditions	80C287-10		80C287-12		80C287-16		Unit
			Min.	Max.	Min.	Max.	Min.	Max.	
1	Clock Period								
	CLM = 1		100		80		62.5		ns
	CLM = 0		40		35		30		ns
2	Clock LOW Time								
	CLM = 1		62		50		37		ns
	CLM = 0		18		13		8		ns
3	Clock HIGH Time								
	CLM = 1		28		22		17		ns
	CLM = 0		18		13		12		ns
4	Clock Rise Time			10		8		4	ns
5	Clock Fall Time			10		8		4	ns
6	Data Setup to $\overline{\text{NPWR}}$ Inactive		75		75		60		ns
7	Data Hold from $\overline{\text{NPWR}}$ Inactive		18		15		10		ns
8	$\overline{\text{NPWR}}$, $\overline{\text{NPRD}}$ Active Time		90		70		50		ns
9	Command Valid Setup Time		0		0		0		ns
10	$\overline{\text{PEREQ}}$ Active to $\overline{\text{NPRD}}$ Active		100		80		62		ns
11	$\overline{\text{PEACK}}$ Active Time		60		50		36		ns
12	$\overline{\text{PEACK}}$ Inactive Time		200		160		125		ns
13	$\overline{\text{PEACK}}$ Inactive to $\overline{\text{NPRD}}$, $\overline{\text{NPWR}}$ Inactive		40		32		25		ns
14	$\overline{\text{NPRD}}$, $\overline{\text{NPWR}}$ Inactive to $\overline{\text{PEACK}}$ Active		–30		–30		–30		ns
15	Command Valid Hold Time		22		18		15		ns
16	$\overline{\text{PEACK}}$ Active Setup to $\overline{\text{NPRD}}$, $\overline{\text{NPWR}}$		40		30		30		ns
17	$\overline{\text{NPRD}}$, $\overline{\text{NPWR}}$ to CLK Setup		53		40		30		ns
18	$\overline{\text{NPRD}}$, $\overline{\text{NPWR}}$ CLK Hold		37		29		22		ns
19	$\overline{\text{RESET}}$ to CLK Setup		20		20		20		ns
20	$\overline{\text{RESET}}$ from CLK Hold		20		20		20		ns
21	$\overline{\text{NPRD}}$ Inactive to Data Float			21		17		13	ns
22	$\overline{\text{NPRD}}$ Active to Data Valid			60		50		40	ns
23	$\overline{\text{ERROR}}$ Active to $\overline{\text{BUSY}}$ Inactive		100		100		100		ns
24	NPWR, Active to $\overline{\text{BUSY}}$ Active			100		80		60	ns
25	$\overline{\text{PEACK}}$ Active to $\overline{\text{PEREQ}}$ Inactive			100		80		60	ns
26	$\overline{\text{NPRD}}$, $\overline{\text{NPWR}}$ Active to $\overline{\text{PEREQ}}$ Inactive			100		80		60	ns
27	Command Inactive Time								
	Write to Write		75		60		50		ns
	Read to Read		75		60		50		ns
	Write to Read		75		60		50		ns
	Read to Write		75		60		50		ns
28	Data Hold from Time $\overline{\text{NPRD}}$ Inactive		3		1		1		ns

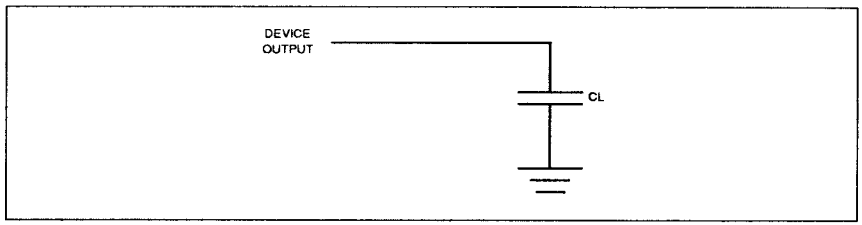
SWITCHING WAVEFORMS



AC Drive and Measurement Points—CLK Input

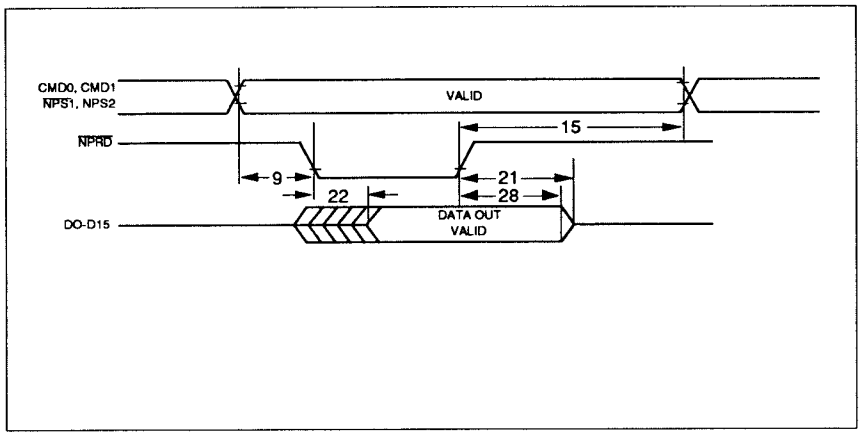


AC Setup, Hold and Delay Time Measurement—General

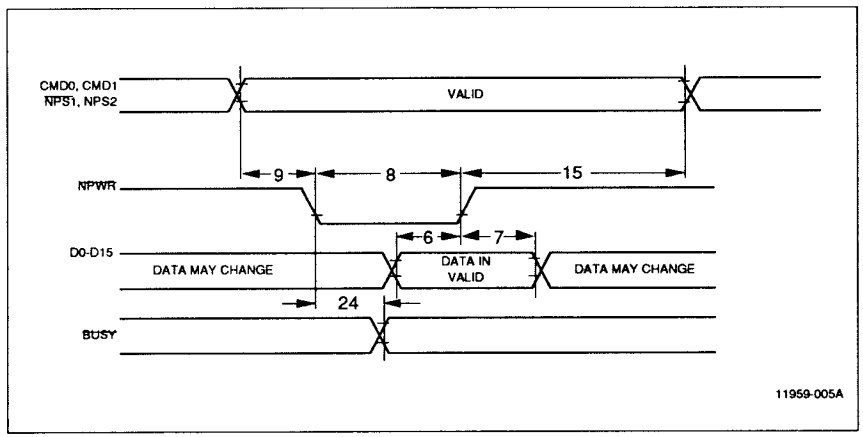


AC Test Loading on Outputs

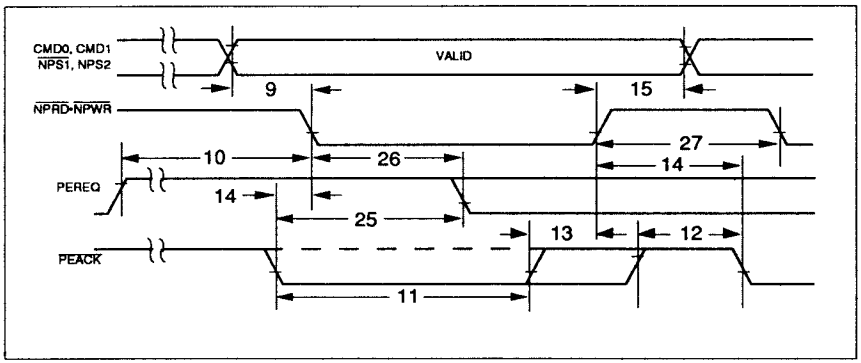
11959-004



Read Timing From 80C287

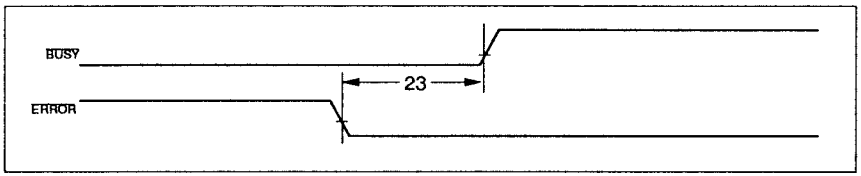


Write Timing From 80C287

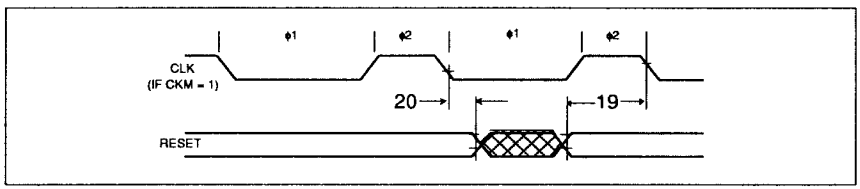


Data Channel Timing (Initiated by 80C287)

11959-006A



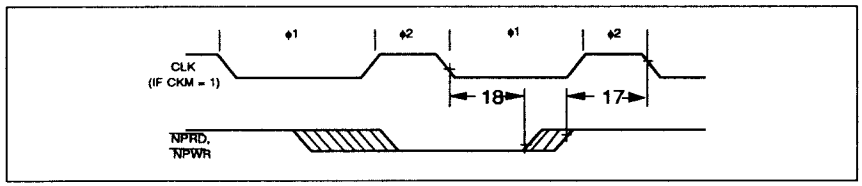
Error Output Timing



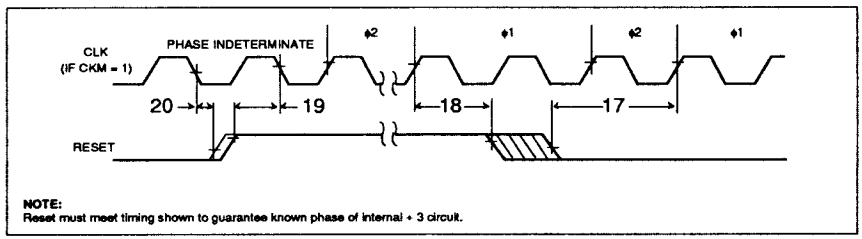
11959-007A

Clk, Reset Timing (Ckm = 1)

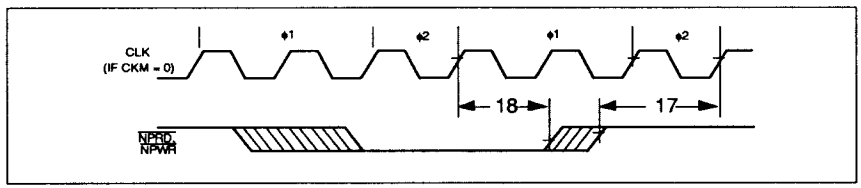
NOTE:
Reset, NPWR, NPRD are inputs asynchronous to CLK. Timing requirements above are given for testing purposes only, to assure recognition at a specific CLK edge.



CLK, $\overline{\text{NPRD}}$, $\overline{\text{NPWR}}$ Timing (CKM = 1)



CLK, RESET Timing (CKM = 0)



CLK, $\overline{\text{NPRD}}$, $\overline{\text{NPWR}}$ Timing (CKM = 0)

11959-008A